Component Modeling for an Integrated Digital Pixel

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Abstract

Future portable imaging products can benefit from the integration of a detector, analog-to-digital converter, digital processing, and data storage within a single chip. One approach combines these components into a processing element that can be tiled into a focal plane processor (FPP) array. Silicon area tradeoffs among the detector, analog interface, processing, and storage can influence system performance. This paper presents a technique that combines area models for each component of the tiled cell to evaluate system implementation alternatives for a 650mm^2 FPP array with Quad-CIF (176 x 144) resolution. A pixel design tool enables comparisons of architectural design choices such as fill factor and data storage. Reducing data storage can increase fill factor. However, this sacrifices versatility in the application suite. Future work includes the development of performance models of each component based upon its physical implementation in silicon.

1 INTRODUCTION

Today's society has placed a huge emphasis on multimedia processing devices for both work-related and recreational tasks to provide users with bundled information of video, audio, and text. In addition, these devices must accommodate a mobile society by encapsulating functionality within portable products. Inexpensive imaging chips are being incorporated into a wide range of devices such as video and still cameras, laptops, portable data assistants (PDAs), and even children's toys. One technique is the use of smart pixels [1] to create an embedded imaging system. A processing element (PE) tile is replicated to form a focal plane array imager with integrated analog to digital conversion and SIMD processing. This moves the computation closer to the data acquisition to reduce the storage requirements of the system. Data parallel processing on the focal plane offers superior performance and efficiency for early image processing applications such as convolution and median filtering [2, 3].

However, digitizing and processing a pixel at the detection site presents new design challenges [4-6]. The most significant issue is silicon area allocation, since in single-level VLSI, the detector, the analog-to-digital converter, the digital processing core, and the memory compete for silicon area in a small replicated tile. The wide range of design techniques and metrics for these components leads to a complicated design problem. Steady advances in semiconductor technology [7] and detector design [8] support increasingly complex systems, but offer a moving target to design efforts. Each component retains minimal area for feasibility with the remaining area allocated among the components to improve overall performance. This requires an effective measure of merit relating silicon area to performance for each functional component.

2 DIGITAL PIXEL COMPONENTS

A programmable digital pixel [9], integrates the functionality of data acquisition, analog-to-digital conversion, image processing, and memory into a single processing element (PE). Photodetection gathers the light intensity for the selected image. Oversampling delta-sigma techniques perform the conversion to the digital domain. Arithmetic and logical functions form the basis of the processing core. Data storage provides the resources for the calculated intermediate and final values of a given image application. This tile element is replicated to form a focal plane array imager with integrated analog-to-digital conversion and SIMD processing. The design challenge of the digital pixel is the allocation of limited resources while delivering high performance and high efficiency, since in single-level VLSI, the detector, analog-to-digital converter (ADC), digital processing, and storage compete for silicon area.

3 RESEARCH STATUS

The development of a pixel design tool provides a common context for component area models within an integrated pixel processing array. The development of area models for the components is described in [3]. The technology feature size is 120nm. The digital architecture uses a 12-bit datapath. The pixel design tool has been implemented to correlate data storage to fill factor for a target system. The pixel to processing element (PPE) ratio is 1:1 for the device. Using the area for a single PE, the maximum resolution is calculated for a fixed chip area. The design is bounded within a total area equal to

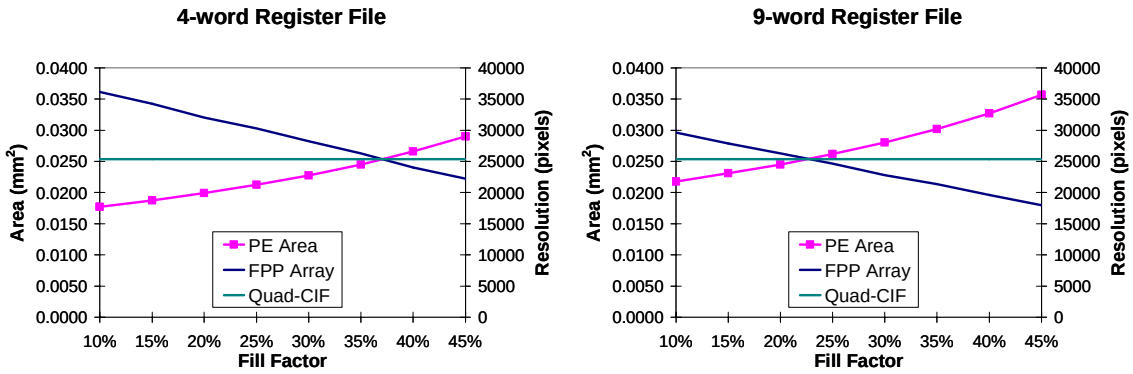

Figure 1: Maximum fill factor for Focal Plane Processor array implementations

650mm^2. The desired system resolution is grayscale (8-bit) Quad-CIF (176 pixels x 144 pixels).

Reducing data storage sacrifices application functionality for improved detector capability. The fill factor can be increased from approximately 23% to approximately 38% by reallocating the silicon area for 5 register words to the photodiode (Figure 1). However, with a 9-word register file, convolution, inside edge detection, and median filtering can be executed on the FPP array. Only convolution can be executed with a 4-word register file [3]. To further quantify the tradeoff, a performance model of the photodiode based upon its physical implementation in silicon will be developed to show the performance gain from the increased fill factor.

4 SUMMARY

A system-on-a-chip, created by a tiled monolithic array of digital pixels, can utilize the anticipated technological improvements in fabrication. However, the limited silicon resources require fundamental tradeoffs among the functional areas within the digital pixel. This paper presents a technique that combines physical models for each element of the tiled cell to investigate the impact of various resource allocations among digital pixel components. It is apparent that silicon resource tradeoffs affect the performance of each functional component. However, no formal analysis exists to quantify the relationships among functional elements based upon silicon resource allocation. The research addresses the issue of what is reasonable to include in a digital pixel tile and explores the design space to identify regions of feasibility that provide good functionality. Architectural choices can be made through quantitative comparisons of silicon area allocation using the pixel design tool.

5 REFERENCES

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