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Comprehensive Evaluation on Efficiency and Thermal Loading of Associated Si and SiC based PV Inverter Applications

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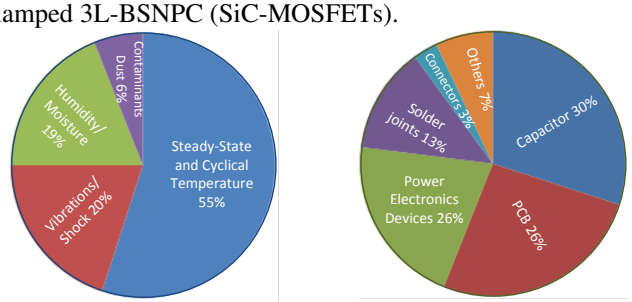
Abstract*—This paper deals with the design, control, efficiency and thermal cycling estimation of associated Si and SiC based three-phase PV-inverters. A novel Electro-Thermal Model able to consider the thermal coupling within the Transistor and Diode integrated on the same package is proposed. For each topology, three different cases study are simulated, according to the heatsink repartition: one-leg heatsink, shared heatsink and individual heatsink. Based on the model, it has been determined the minimum required heatsink thermal impedance in order not to overpass the device physically thermal limitations. Finally, simulation results are analyzed in order to decide which topology has a higher efficiency and a better thermal loading distribution within the devices.** ***Keywords—PV-inverter; Efficiency; thermal loading distribution;

I. INTRODUCTION

Nowadays, the power devices requirements include higher blocking voltages, higher switching frequency, higher efficiency, higher power density and higher reliability. In order to achieve this goal, the development of high power devices based on Wide Band-Gap (WBG) semiconductors like silicon carbide (SiC) and gallium nitride (GaN) are interesting. These WBG devices have superior electrical properties and are likely candidates to replace Si in some applications [1],[2]. It is worth to mention that according to their rated power (available on the market today), the main applications that can be covered by this field are PV-inverters, adjustable speed drives, small pumps and automotive. Moreover, PV-inverters companies already started to produce converters based on these devices (ex: SMA with STP 20000TLHE-10, REFUsol with 020K-SCI) [3][4].

The converter availability in PV-systems application is the most important aspect which depends on the component reliability, efficiency and its maintenance [5]. Therefore, highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs [6],[7]. From Fig. 1(a) [8] can be seen the main source of stressors distribution which involves failure, where temperature is the most important matter. Due to these causes the failure rate sharing of the main components used in a power converter design has the distribution according to Fig. 1(b) [9]. It is worth to mention that semiconductor devices, capacitors and PCBs are the most prone to failure within the converter components. Therefore, the maximum electrical ratings and the thermal limitations of the semiconductor devices plays a key role in the robustness design and reliability of power electronics converters [10]. Moreover, the producers should guarantee that under all mentioned operating conditions, the case and junction temperature T_j of all devices do not exceed their designed physical limits, otherwise it may involve failures of the product [11]. This problem has a higher/an interesting impact for the new generation of power converters, which are based on WBG-devices, due to their superior Electro-Thermal properties which involves a higher temperature operating point compared to the Si-based devices [2]. Therefore, it is important to perform a thermal loading analysis of the converter in order to determine if the devices are performing within maximum allowed physical limits, especially in the worst case scenario.

This paper deals with a comparison of associated Si and SiC based PV-converters in terms of efficiency and thermal loading distribution. The study is performed by considering the following three-phase grid connected PV-inverter topologies: three-level diode neutral point clamped 3L-DNPC (Si-IGBTs) and three-level bipolar-switch neutral point clamped 3L-BSNPC (SiC-MOSFETs).



(a)Source of stress distribution [8] (b)Failure cause distribution [9]

Fig. 1. Stress causes and failure distribution in power electronic systems

II. SYSTEM DESIGN DESCRIPTION

Power electronics is the key technology in order to enable the photovoltaic (PV) system to be connected to the grid. There are many converter configurations in this field. Our study focus on two of the most efficient three-phase PV-inverter topologies which are used nowadays in industry 3L-DNPC and 3L-BSNPC [4]. The proposed PV-system, depicted in Fig. 2, consists of a 3L-D/BS NPC inverter connected to the

three phase grid through a passive LCL-filter (in order to mitigate the switching frequency harmonics).

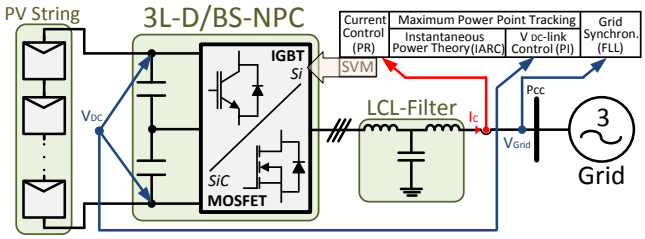


Fig. 2. Grid connected PV-inverter

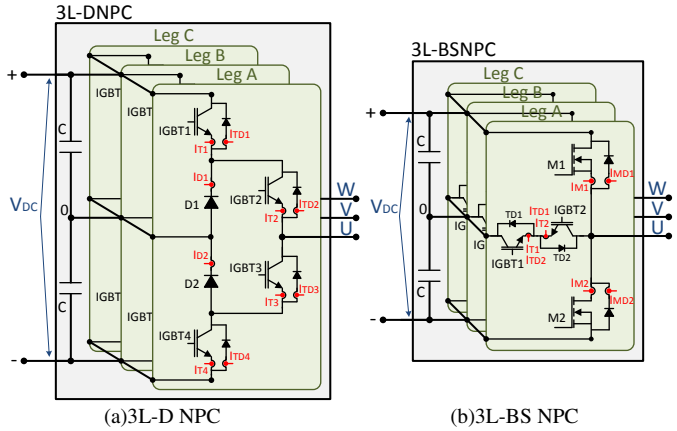
A. PV-inverter design

The design of a 12 kVA grid connected converter will be performed according with the power rating parameters and topologies of PV-inverters produced by Danfoss (3L-D NPC) and SMA (3L-BS NPC).[3]

According to Table I, the DC-link voltage is 1 kV and the nominal output current is 18 A (RMS). The chosen devices for 3L-D NPC topology (Fig. 3(a)) have to fulfill the following requirements: withstand at least half of the V_{DC} (500 V), conduct the rated current and it should be able to operate in the higher switching frequency range. Therefore Si devices are suitable for this topology. The chosen devices are Si IGBTs from Infineon which can withstand the required demands. As an alternative , the 3L-BS NPC topology requires devices able to withstand full V_{DC} ,therefore SiC MOSFETs from CREE are used for switches M1 and M2 (Fig. 3(b)). The connection to the middle-point 0 requires two switches so the voltage stress is shared between them. Moreover by considering the converter costs, the IGBTs from Infineon are suitable for this case.

TABLE I. CONVERTER DESIGN RAITINGS

3L-D/BS NPC PV-inverter Power Ratings			
Rated power	S=12 kVA		
Conv. Output phase voltage (RMS)	V_N = 230 V (RMS) (325 V peak)		
Max. Output current (RMS)	I_{max} = 18 A (RMS) (25 A peak)		
Max. DC-link Voltage	$V_{DC\text{-}max}$ = 1000 V		
Switching Frequency	F_{sw} = 48 kHz		
Device Power Ratings			
Device	**IGBT-Infineon SKW30N60HS**	**MOSFET-CREE CMF20120D**	**Diode-CREE C4D20120A**
Break-Down Voltage	$V_{(BR)CE}$=600 V	$V_{(BR)DS}$=1200 V	V_R=1200 V
Max allowed. J/C Temperature	T_J= 135 °C T_C= 100 °C	T_J= 135 °C T_C= 100 °C	T_J= 175 °C T_C= 135 °C



(a)3L-D NPC (b)3L-BS NPC

Fig. 3. Three phase 3L-NPC topologies for PV-inverter

B. LCL-filter design

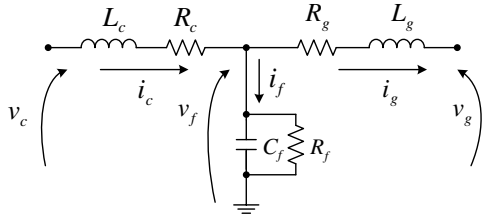


Fig. 4. Single phase LCL-Filter representation

Fig. 4 presents an LCL-filter where L_c and R_c are the converter side inductance and its series resistance, L_g and R_g are the grid side inductance with its series resistance and C_f is the capacitor bank, which is connected to a parallel damping resistance R_f. The converter, capacitor and the grid currents are represented by i_c, i_f and i_g respectively. Furthermore the converter, capacitor bank and PCC voltages are represented by v_c, v_f and v_g. Based on Kirchhoff's laws, the filter model F_{LCL} transfer function is obtained in (1) by defining the converter voltage as the input and the grid current as the output of the system.

$$F_{LCL} = \frac{I_g(s)}{V_c(s)} = \frac{K}{s^3 + \lambda_2 s^2 + \lambda_1 s + \lambda_0}$$

$$K = \frac{R_f}{L_c C_f R_f L_g}$$

$$\lambda_2 = \frac{C_f R_f R_g L_c + C_f R_f R_c L_g + L_c L_g}{L_c L_g C_f R_f} \quad (1)$$

$$\lambda_1 = \frac{R_c R_g C_f R_f + R_g L_c + R_c L_g + R_f L_c + R_f L_g}{L_c L_g C_f R_f}$$

$$\lambda_0 = \frac{R_c R_g + R_c R_f + R_g R_f}{L_c L_g C_f R_f}$$

When dealing with 3L converters, the phase voltage seen by the load is composed of $\Delta V = V_{DC}/6$ voltage steeps. Therefore, the minimum inductor required L in order to have a maximum current ripple of 10% from the rated peak current ($\Delta i = 0.1 \cdot 25A$), can be calculated according with (2).

$$L = \frac{\Delta V \Delta t}{\Delta i} = \frac{1}{\Delta i} \cdot \frac{V_{DC}}{6} \cdot \frac{T_{s\omega}}{4} \quad (2)$$

$$2\pi \cdot f_{rez} = \frac{1}{\sqrt{\frac{L_c L_g}{L_c + L_g} C_f}} \Rightarrow C_f = 0.5\mu F \quad (3)$$

Where T_{sw} is the switching period.

Afterwards, a proper sharing of L into L_c (0.7L) and L_g (0.3L) is done in order to achieve minimum reactive power consumption of the filter. As the filter inductances have been previously determined, the C_f parameter will be obtained in (3) by selectively placing the resonant frequency at f_{res}=35 kHz (70% of F_{sw}) in order to achieve high current controllability when using a high F_{sw}. The used filter parameters can be found in Table II.

TABLE II. LCL-FILTER PARAMETERS

Converter Side	L_C = 0.175 mH	R_C = 7 mΩ
Grid Side	L_g = 0.075 mH	R_g = 3 mΩ
Filter Capacitor	C_f = 0.5 µF	R_f = 10 kΩ

III. PROPOSED CONTROL STRATEGY

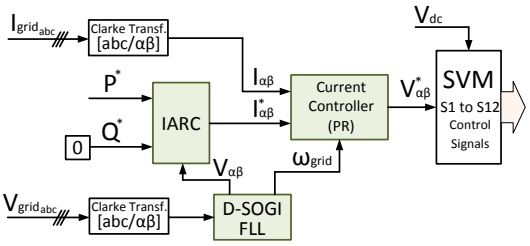


Fig. 5. Control strategy structure

The overall system simulation (control and model of the converter) has been performed by using Matlab/Simulink and the Plecs toolbox. In Fig. 5, the system uses: the grid current ($Igrid_{abc}$) for loop feedback and the grid voltage ($Vgrid_{abc}$) for synchronization.

In order to achieve the desired system functionalities a resonant current controller for fundamental frequency is used. Hence, an accurate current control will be achieved, as the current controller poles will be placed to provide infinite gain for 50 Hz [12].

The synchronization method used in this control strategy is based on a double SOGI frequency locked loop algorithm [13]. As a result, the fundamental frequency is continuously estimated for online tuning of the resonant controllers.

In simulation, the control has been implemented in C-code by using S-Function Builder blocks from Matlab/Simulink in order to achieve a more realistic approach to the real system behaviour. Therefore, it is necessary to design the current controller for a discrete time system. In the stationary reference frame, high performances are achieved by designing a controller with a complex pole with a very low damping factor and characteristic frequency equal to the desired one (ω).

Considering that a point in the continuous time s-plane is mapped to the discrete time z-plane as z = exp (sΔt), a complex pole in s = $\pm j\omega_g$ is mapped in discrete as a pole in z=cos($\omega\Delta$t) + jsin($\omega\Delta$t). In this case the discrete resonant controller transfer function will have the following form (4):

$$C[z] = K\frac{z^2+\alpha_1 z+\alpha_2}{z^2-2\cos(\omega_g \Delta t)z+1} = 2.31\frac{z^2-1.782z+0.891}{z^2-1.895z+1} \quad (4)$$

Where K and the zeros of the controller transfer function are the design parameters, and Δt is the sampling period. By taking into consideration the controller transfer function and the discrete transfer function of the filter it is possible to obtain the final model, as it is shown in Fig. 6. Furthermore, a unit sample delay has been introduced in order to represent the sampling and the calculation time of the processor.

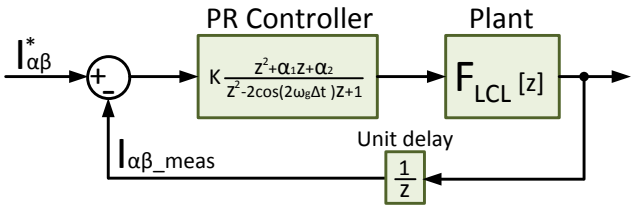


Fig. 6. Current control design loop

The design parameters have been obtained by introducing the current control design loop into MATLAB/Sisotool graphical interface. The obtained results for the 50 Hz current controller are given in (4). The root-locus and the closed loop bode diagram in Fig. 7(a) shows that the system is stable and that the controller is selective for the frequency of 50 Hz. When a step in active power from 0 to 12 kW (rated converter power) is provided as a reference, according to Fig. 7(b) the converter is injecting the rated peak current (alpha axis) to the grid (25 A).

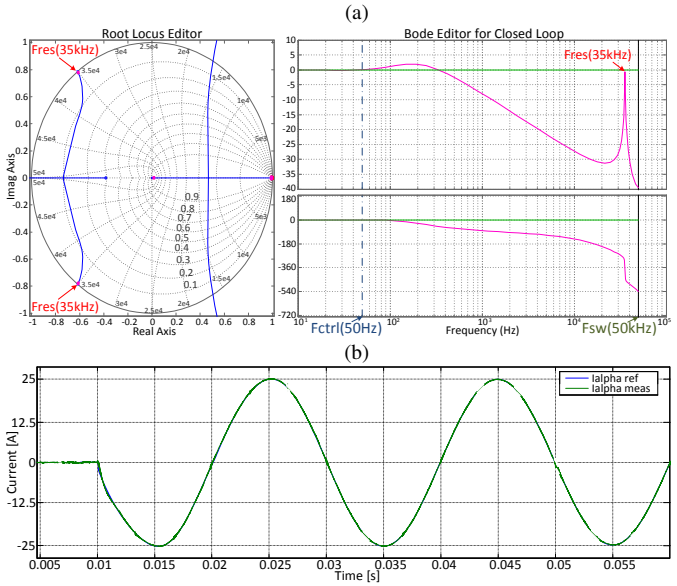


Fig. 7(a) Root-locus and closed loop bode response for 50 Hz current control design parameters. (b) Alpha axis current reference and measured

IV. HEATSINK REPARTITION SELECTION

The junction and case temperature estimation of devices mentioned in Table I (MOSFET, IGBT and Diode) have been performed by implementing the Electro-Thermal Model according with [15]. The input signals for the model are measured from the converter considering Fig. 3: the current which is flowing through the devices (I_M-MOSFET current, I_{MD}-MOSFET diode current, I_T-IGBT current, I_{TD}-IGBT diode current, I_D-SiC Diode current) and the DC-link voltage. Fig. 8 shows that three types of models are involved: device model, power loss model and thermal model. Details about the proposed Electro-Thermal Model are provided in [15].

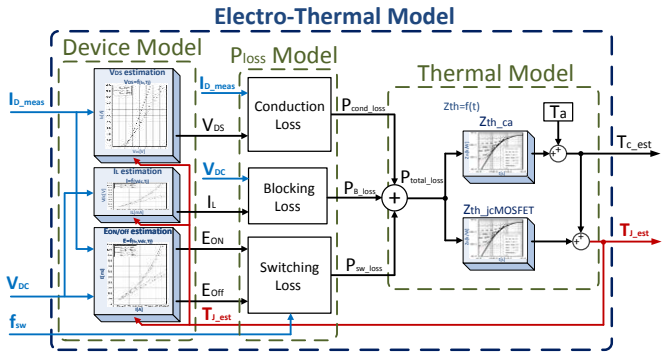


Fig. 8. Proposed Electro-Thermal model structure for device junction and case temperature estimation

The obtained parameters, for devices thermal impedance estimation, can be seen in Table III.

TABLE III. ESTIMATED THERMAL IMPEDANCE OF DEVICES

	IGBT+D-Infineon(Si)				*MOSFET CREE(SiC)*		*Diode CREE(SiC)*	
	IGBT		**D**					
No.	Rth[k/w]	τ[s]	Rth[k/w]	τ[s]	Rth[k/w]	τ[s]	Rth[k/w]	τ[s]
1.	0.3681	0.0555	0.358	9.02e-2	0.1225	7.7e-4	9.634e-5	3.692
2.	0.0938	1.26e-3	0.367	9.42e-3	0.3003	1.547e-2	0.01513	3.67
3.	0.038	1.49e-4	0.329	9.93e-4	0.5574	37.43	0.2524	1.536e-3
4.	-	-	0.216	1.19e-4	0.565	31.05	0.3576	3.271e-2
5.	-	-	0.024	1.92e-5	-	-	-	-

Another important aspect in the thermal model design is the heatsink thermal impedance. First, the ambient temperature T_a is considered constant to 30°C. The Z_{th_ha} has been determined for the conditions (worst thermal loading case scenario) when the converter is injecting the rated power to the grid and the devices case temperature should not exceed 100°C. Moreover, three cases were considered for the calculations. In the first case it is considered that each device is mounted on its own heatsink. According with the implemented PV-inverter topology there are devices which have the same current loading, therefore as it was expected they will have the same value of the heatsink thermal impedance. For the second case two heatsinks are used, first one for the first two devices with the highest losses and the second one for the remaining devices. In the last case a common heatsink is used for all the devices. By analyzing the obtained results from Table IV, it can be stated that due to the lower losses achieved in 3L-BS NPC, the heatsink thermal impedance values are significantly higher than in 3L-D NPC. Therefore a smaller hetsink is required.

TABLE IV. HEATSINK THERMAL IMPEDANCE

***3L-D NPC Z_{th_ha}* [k/w]**						
Case No.	**D1**	**D2**	**IGBT1**	**IGBT4**	**IGBT2**	**IGBT3**
1.Individual Heatsink	5.75	5.75	3.2	3.2	1.85	1.85
2.Shared Heatsink	1.2				1	
3.One-leg Heatsink	0.55					
***3L-BS NPC Z_{th_ha}*[k/w]**						
Case No.	**MOSFET1**		**MOSFET2**		**IGBT1**	**IGBT2**
1.Individual Heatsink	3.7		3.7		2.54	2.54
2.Shared Heatsink	1.72				1.25	
3.One-leg Heatsink	0.75					

V. SIMULATION RESULTS

The simulation of a grid connected 3L-D/BS NPC PV-inverter application has been performed by considering the mentioned specifications. A comparison study between 3L-D NPC and 3L-BS NPC in terms of losses, efficiency and thermal loading distribution is performed.

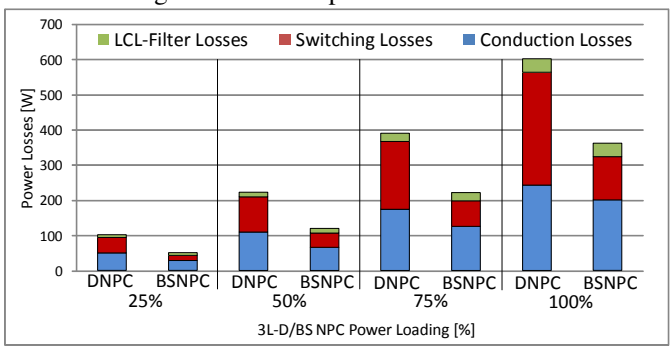


Fig. 9. Total losses distribution in 3L-D/BS NPC PV-inverters

The study case emphasized in Fig. 9. shows the conduction, switching and LCL-filter losses distribution when the 3L-D/BS NPC inverters are injecting 25%, 50%, 75% and 100% of its rated active power into the grid. As it was expected the 3L-DNPC inverter has considerably higher losses than 3L-BS NPC. It is worth to mention that due to the lower Eon/Eoff energies of SiC MOSFET a positive impact in switching losses of the BS NPC topology is achieved.

Finally, the efficiency of PV-inverter topologies is calculated for progressively/different power ratings from 0 to 12 kW with steps of 0.6 kW. By analysing the obtained results presented in Fig. 10. , the efficiency of 3L-BS NPC is higher than 3L-D NPC with 1%, when comparing the peak efficiencies, and with 1.4%, when comparing the efficiency at rated power. Moreover the estimated efficiency curve for 3L-BS NPC PV-inverter is similar with the one measured by SMA for STP 20000 TLHE-10 [3].

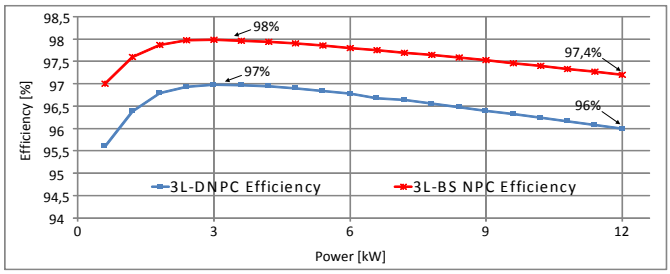


Fig. 10. Efficiency curve of 3L-D/BS NPC PV-inverters

The thermal loading transient behavior/study of the PV-inverters devices has been also performed. As an example, in Fig.11. is emphasized the thermal loading/cycling/temperature transient of the SiC-MOSFET mounted on common heatsink, when the 3L-BS NPC injected power is changed from 12 kW (25A) to 7.3 kW (15A) at time 25 s. According to the obtained simulations results shown in Fig. 11. it is worth to mention that, after 25 s from the mentioned current step, the temperature is stabilizing at the final peak value of 81.6°C for the SiC chip and 70°C for the device case temperature.

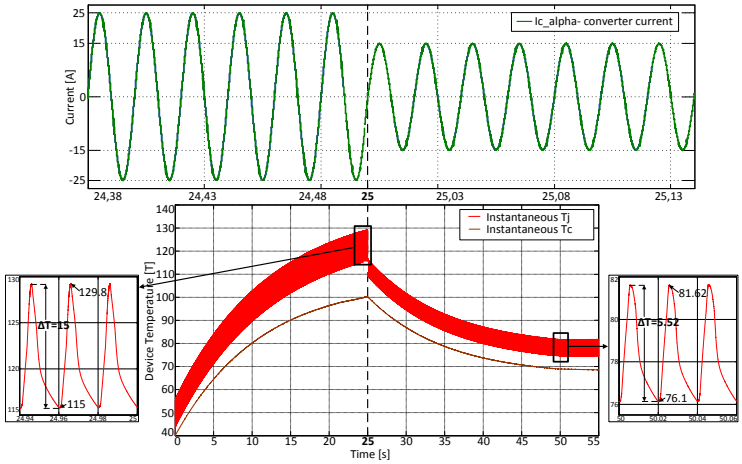
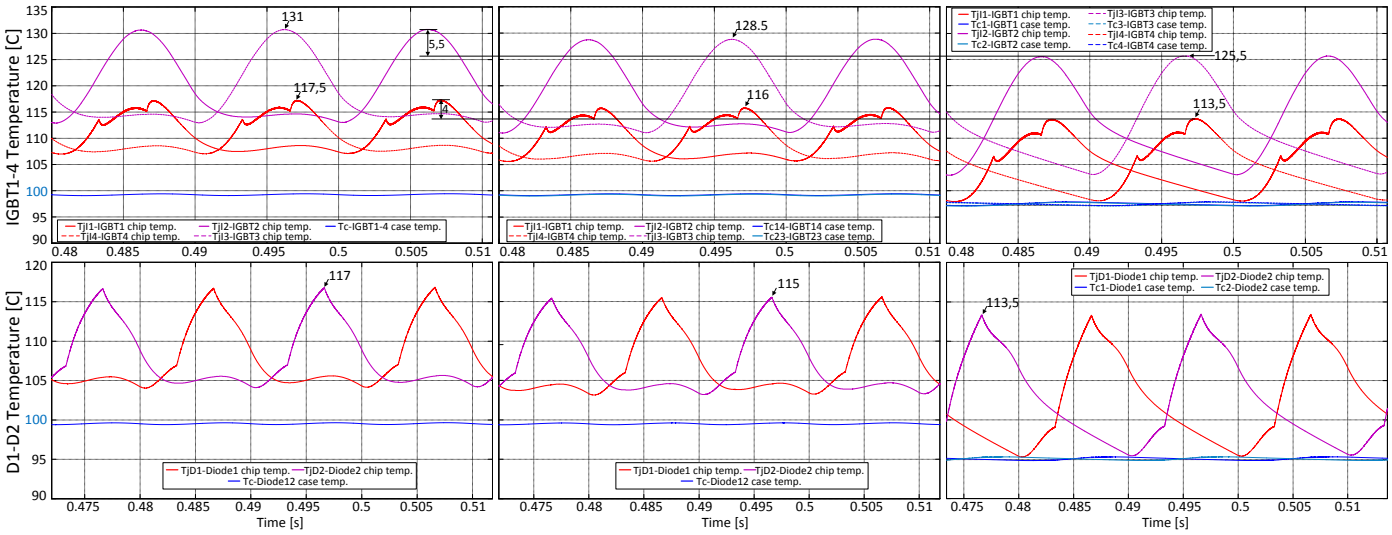
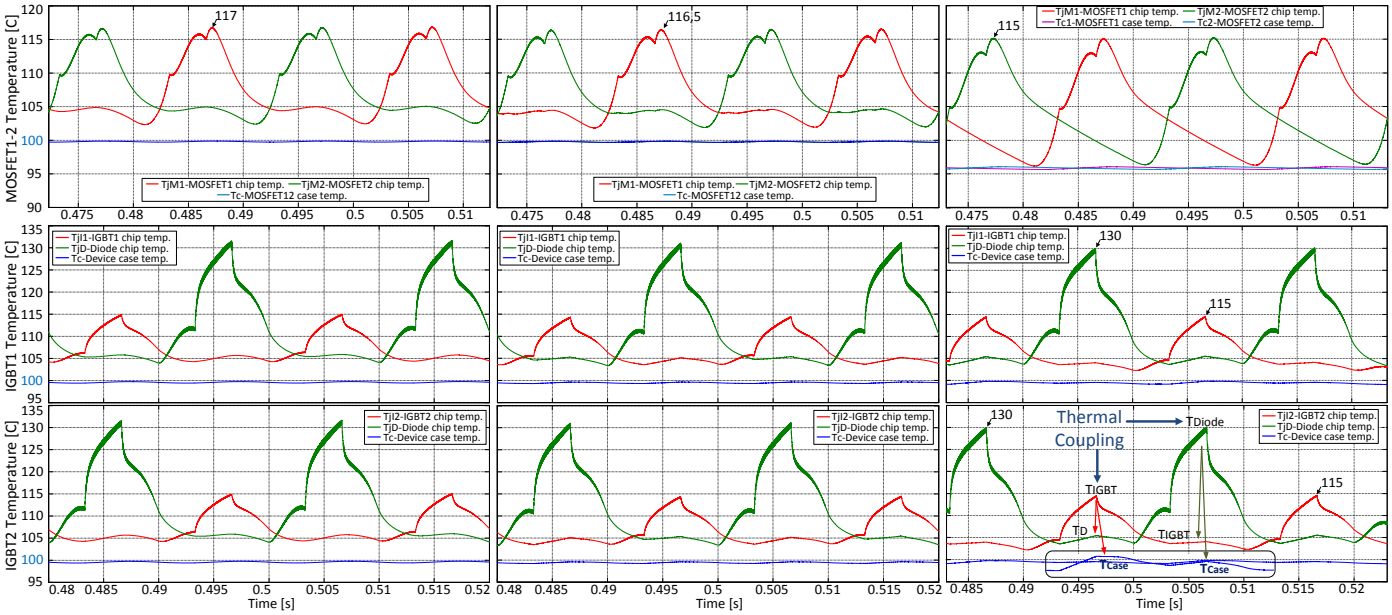


Fig. 11. Transient response of the thermal cycling variation of the junction and case temperatures when the converter current Ic is changing from 25A to 15A at time 25s



(a) One Leg Heatsink (b) Shared Heatsink (c) Individual Heatsink

Fig. 12. Thermal loading estimation of the 3-L D NPC PV-inverter devices



(a) One Leg Heatsink (b) Shared Heatsink (c) Individual Heatsink

Fig. 13. Thermal loading estimation of the 3L-BS NPC PV-inverter devices

Fig. 12 and Fig. 13 present the thermal loading of the converter devices for the worst case scenario respectively when the rated active power is injected into the grid. Three different cases are simulated considering the heatsink repartition as discussed in the previous chapter.

Fig. 12 shows the 3L-DNPC converter devices thermal loading. As it was expected due to the current stress repartition, the IGBT2/3 chip temperature is higher than IGBT1/4. According to the obtained values (Table V) there is a considerable difference between the device ΔT and T_{MAX} obtained in case (a) and (c). So when a common heatsink for all devices is used (a), due to its increased capacity the ΔT is decreasing considerably and the peak temperature is increasing (+5.5 for IGBT2/3, +4 for IGBT1/4, and +3.5 for Diode1/2).

TABLE V. 3L-DNPC THERMAL LOADING

	Peak Temperature T_{MAX} [°C]			***Temperature Variation ΔT*** [°C]		
Case	**(a)**	**(b)**	**(c)**	**(a)**	**(b)**	**(c)**
IGBT1/4	117,5	116	113,5	9,5	11	16
IGBT2/3	131	128,5	125,5	16	18	22
Diode1/2	117	115	113,5	12	12	18

Even there is a considerable difference of the chip temperature within IGBT1/4 and IGBT2/3, the case temperature of all devices is kept under the maximum allowed limits (100°C), therefore a proper heatsink thermal impedance has been determined for all three studied cases.

The thermal loading of 3L-BS NPC topology devices is presented in Fig. 13. According to the obtained values (Table VI) for MOSFET1/2, when a common heatsink for all devices is used (a), due to its increased capacity the ΔT is decreasing considerably and the peak temperature is increasing.
For the IGBT1/2 it is plotted also its freewheeling Diode1/2 temperature, because in this topology the current stress of the neutral point clamping IGBT is the same with the freewheeling diode (Fig. 3). Even they have the same current stress, the temperature of IGBT and Diode differs considerably due to the thermal impedance, which in case of diode is doubled. The Diode/IGBT temperature varies also due to IGBT/Diode losses, and the device case temperature varies due to P_{tot} (Fig 13(c)), therefore IGBT-Diode Thermal Coupling was achieved by implementing the proposed model.

TABLE VI. 3L-BS NPC THERMAL LOADING

	Peak Temperature T_{MAX} [°C]			***Temperature Variation*** ΔT [°C]		
Case	**(a)**	**(b)**	**(c)**	**(a)**	**(b)**	**(c)**
MOSFET1/2	117	116,5	115	14	15	118.5
IGBT1/2	130	130	130	10	11	12
FDiode1/2	115	115	113,5	25	25	25

VI. CONCLUSIONS

The design and control of a 12 kVA grid connected converter according to the power ratings parameters and topologies of PV-inverters produced by Danfoss (3L-DNPC) and SMA (3L-BS NPC), has been implemented.

According to the desired switching frequency and with the system specifications, an LCL-filter has been designed.

A control for the fundamental frequency current component (50Hz) has been designed by using resonant controllers in the stationary reference frame.

Moreover a novel Electro-Thermal Model for discrete devices, able to consider the thermal-coupling within the Transistor-Diode integrated on the same package, has been proposed. Considering the designed converter and the proposed Electro-Thermal Model, the thermal cycling estimation of the devices has been performed for the worst case scenario, respectively when the rated active power is injected into the grid. The obtained simulation results are able to predict the thermal loading repartition within the converter devices, by estimating their ΔT and T_{MAX}. It is important to mention that as it was expected, for 3L-D NPC configuration, the predicted IGBT2/3 chip temperature is higher than IGBT1/2. In case of 3L-BS NPC topology, the most stressed device is the IGBT freewheeling diode, due to its higher thermal impedance. This thermal loading difference within the devices will have a negative impact in converter reliability.

For each topology, three different cases have been simulated according to the heatsink repartition: one-leg heatsink, shared heatsink and individual heatsink.

It has been determined the minimum heatsink thermal impedance required in order not to overpass the maximum allowed junction and case temperature limits by considering also the heatsink repartition and the converter topology.

When a common heatsink for all devices has been used, due to its increased capacity, the ΔT is decreasing considerably and T_{MAX} is increasing, compared with individual heatsink repartition. Shared heatsink repartition is proposed as a compromise within low ΔT and high T_{MAX}.

Moreover the obtained results concluded that a proper heatsink thermal impedance has been obtained for all three studied cases.

As a final conclusion, when comparing the associated Si-SiC based PV-inverters, it can be stated that the 3L-BS NPC topology has a higher efficiency and a better thermal loading distribution within the devices.

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