




Review Paper

# Comprehensive study of 1-Bit full adder cells: review, performance comparison and scalability analysis

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## Abstract

Full Adder (FA) circuits are integral components in the design of Arithmetic Logic Units (ALUs) of modern computing systems. Recently, there have been massive research interests in this area due to the growing need for low-power and high-performance computing systems. Researchers have proposed a variety of FA cells with diverse design techniques, each having its pros and cons. As a result, a systematic method for performance comparison of FA cells using a common simulation platform has become necessary. In this work, we present an extensive study of FA cells. We have compared the performance of thirty-three (33) existing 1-bit FA cells. The drive powers of these FA cells have been compared by applying a variety of load conditions. In addition, the 1-bit FA cells have been extended to 32-bit structures to test their scalability and to investigate their performance in wide-word structures. We have determined that twenty-one (21) of the thirty-three (33) FA cells cannot operate in a 32-bit structure, even though some of them exhibit excellent performance as a 1-bit cell. The main finding of this research is that the single-bit performance parameters of FA cells should not be considered as the main basis for performance comparison. Any FA cell should be analyzed in a multi-bit structure to determine its practical effectiveness.

## Article Highlights

- Hybrid full adders offer better performance than single logic full adders
- Many existing full adder cells are not scalable
- Conventional Mirror CMOS full adder offers better performance than many recent full adders in wide adder structure

**Keywords** Full adder · Hybrid adder · 1-bit adder · Single logic · Hybrid logic · Ripple carry adder

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## 1 Introduction

Due to the massive use of battery-powered, portable electronic gadgets, the use of VLSI circuits, that require high speed and consume less power, has become crucial [1–3]. Full Adders (FAs) form a vital component in the VLSI system design of advanced microchips. FAs are essential for the implementation of certain mathematical operations such as magnitude comparison [4], multiplication [5, 6], subtraction [7], etc. In most cases, adder falls within the critical path of these operations which govern the comprehensive performance of the overall system [8]. Moreover, the implementation of a wide adder tree requires full adder cells [9–11]. Due to the towering utilization and crucial role in various operations, a multitude of FA cells have been implemented, each having its advantages and disadvantages.

Since numerous FA topologies have been proposed, especially in recent times, it is necessary to evaluate their performance metrics using a common platform to enable VLSI designers to pick the right FA topology that best suits their system requirements [12]. In many recent works, comparative analyses of FA designs have been discussed. For example, Prasad et al. [13] and Wariya et al. [14] compared XOR-XNOR-based FA circuits. A comparative study of FAs conducted in by Singh et al. [15] and Harish et al. [16] explored FAs that are implemented using various logics. However, the investigation was only conducted for four FAs in [15] and five FAs in [16]. FA comparison in [17] compared 7 cells. The study conducted in [18] provided the impact of voltage variation on FA cells. Research conducted in [19] analyzed the performance of FA in tree-structured arithmetic units. In [20], only 4 FA cells have been analyzed and compared. However, these studies are not up-to-date as they do not have the FA designs developed in the past 10 years. In [21], an extensive investigation among various FA cells has been conducted for 180 nm CMOS process node, which is rarely applied to modern-day circuits. FA comparison in [22] contains simulation results for only 14 FA cells, which may not be enough for a comprehensive study.

To have a complete overview of FA cells, recent contributions need to be considered and performance comparison should not be limited to 1-bit cell. Therefore, FAs should be analyzed in multiple-bit structures. Moreover, the drive power of VLSI circuits is an important parameter. However, comparative analysis of FA drive power is missing in the existing literature.

In this work, we report an extensive analysis of 33 existing FA cell designs utilizing Cadence tools. The benefits and drawbacks of each FA design have been thoroughly

discussed and summarized to allow VLSI designers to select the desired FA for circuit implementation.

The organization of the remaining portion of this research is as follows. In Sect. 2, a comprehensive review of FA cells has been provided. Section 3 provides information on circuit simulation parameters, transistor sizing, and simulation testbench. In Sect. 4, a comprehensive comparison of FA cells has been conducted based on the simulated results. Section 5 provides the major findings of this research. At last, concluding statements are provided in Sect. 6.

## 2 Literature review of existing full adder cells

Various FA designs using different techniques have been realized with the aim to enhance performance parameters. Although the FA cells perform exactly the same operation, design patterns for generating internal nodes, logic design techniques and the number of transistors utilized are completely different. Variations in logic designs increase some performance parameters while degrading others. Some cells utilize only one logic design technique for the implementation of the entire FA cell. This sort of FA cell is known as single logic FA. FA cells employing more than one logic style is known as hybrid logic FA [23].

### 2.1 Single logic full adders

The early age of CMOS VLSI design highly relied on Complementary Pass Logic (CPL) where n-channel CMOS (NMOS) transistors were utilized for logic interpretation [24]. This logic technique is proficient in terms of logic swing. However, due to the utilization of only NMOS transistors, the design technique can only provide strong logic 0. In the case of providing logic 1, the output voltage becomes  $V_{dd} - V_t$  (here,  $V_{dd}$  = supply voltage,  $V_t$  = threshold voltage of NMOS). Therefore, CPL is unable to provide strong logic 1. FA employing CPL utilizes 32 NMOS for logic interpretation [25]. In addition to providing weak logic 1, high transistor count (TC) of CPL FA causes high power dissipation which is responsible for creating hot spots in IC [26]. Another FA employing CPL logic presented in [27] requires only 12 transistors (addressed as 12-T FA in this article). Although low TC reduces power dissipation and area requirements in IC, voltage degradation remains the key concern. Due to voltage degradation, CPL has been supplemented by Complementary CMOS (CCMOS) logic which is widely used in modern ICs [28]. In addition to providing strong logic 0 and 1, the CCMOS logic family is highly robust against voltage scaling [29]. Moreover, due

to having ample drive power, CCMOS logic is highly suitable for high-fan out conditions [28]. FA employing CCMOS logic presented in [30] requires 28 transistors (14 NMOS and 14 PMOS). FAs in [25, 27, 30] fall under the realm of single logic devices.

## 2.2 Hybrid logic full adders

Hybrid logic-based FA circuits have become popular because they leverage the benefits of various logic designs within the same circuit [31]. Transmission gate (TG) based logic implementation solves the issue of voltage degradation of CPL logic by adding swing restoring PMOS transistors [32]. Transmission Gate FA (TGA) in [33] and Transmission Function FA (TFA) in [34] employ TGs for FA logic interpretation. Although the issue of voltage degradation is solved, poor drive power is the major issue associated with these FA designs [33, 34].

FAs employing 10 transistors (10-T) [35], 16 transistors (16-T) [36], 14 transistors (14-T and New 14-T) [37], 18 transistors (18-T) [38], and 26 transistors in [39] utilize hybrid logic style designs, unlike TGA and TFA FAs. 24-T FA employs a 3-input XOR gate to compute Sum. Carry-out bit calculation is the same as CCMOS based FA in [30]. In 14-T FA [36], a hybrid XOR gate works as the soul of the design since the output from the XOR gate is used for computing both sum and carry-out signals.

Two more hybrid FA cells named Hybrid Pass Static CMOS (HPSC) and Novel HPSC (NHPSC) are presented in [40, 41]. HPSC uses Pass Transistor (PT) for XOR-XNOR function generation which works as internal nodes. The output side employs CCMOS logic to provide the circuit with ample drive power required in high-fan out cases.

Low-Power High-Speed (LPHS) FA design in [43] employs only 15 CMOS transistors for FA function implementation. However, threshold voltage drop remains the major issue associated with this design. Double Pass Logic (DPL) FA and Swing-Restored CPL (SRCPL) FA design in [44] utilize 3 logic techniques: PTL, CCMOS logic, and TG logic. More hybrid FA cells are available in [45–54] (referred to as HBD 1 – HBD 12 in the latter part of this article).

Nowadays, the Gate Diffusion Input (GDI) method of implementing logic functions has become quite popular for implementing low power circuits [55–58]. GDI method was first introduced in [59] which later became a popular method for VLSI circuit design [60]. Logic implementation using the GDI technique can be realized from [61], where basic logic gates using the GDI technique, have been presented. The major issue regarding GDI method-based circuit is its voltage degradation which reduces drive capability significantly [62]. Several FAs employing the GDI technique have been developed for low-power applications which require less surface area due to low TC

[63]. GDI FA in [64] suffers from low drive power due to threshold voltage drop in GDI logic gates. However, low TC and low-power dissipation make them suitable for low-power applications. To provide full swing output in GDI gates, modified GDI gate-based FA designs have been implemented in [65, 66].

## 3 Circuit simulation in cadence

To evaluate the performance metrics of various designs of FA cells, circuits are required to be simulated in a common simulation environment to ensure a fair comparison. Therefore, circuit simulation parameters need to be fixed and a proper transistor sizing technique needs to be applied for all FA cells. These are discussed in the following sub-sections.

### 3.1 Circuit simulation parameters

To simulate FA circuits to investigate their performance, a 45 nm CMOS process has been utilized. Supply voltage has been set to 1.0 V. Average power, propagation delay, and Power Delay Product (PDP) are the performance metrics that are used to compare the effectiveness of various FA cells. The input waveform for power and delay calculation is presented using Fig. 1, where it can be visualized that all possible input combinations from 000 to 111 are present in the waveform. In VLSI circuits, power and delay vary for different input combinations since pull-up and pull-down transistor paths for different input combinations are different. Therefore, to determine the average power dissipation of a FA cell, all possible input combinations are applied to the testbench and total power consumption due to each input combination is calculated. Later, an average value of total power, due to all input patterns, was taken as the average power. In the case of propagation delay calculation, 50% of input–output signal swing for the critical path (worst case delay path) has been chosen. For delay, all input–output combinations from 000 to 111 are generated separately and delay occurred due to all possible input combinations were calculated individually. Then, only the maximum delay has been considered as propagation delay of the circuit. PDP is simply the product of average power and propagation delay.

### 3.2 Transistor sizing

In the case of VLSI design, optimal implementation of circuits plays a crucial role [67, 68]. In general, transistor sizing refers to increasing or decreasing the width of transistors to optimize the performance parameters of circuits. Due to its effectiveness in optimizing the

performance of VLSI circuits, transistor sizing should be handled in a proper manner [69]. Transistor sizing for circuits comprising of a small number of transistors can be done manually. However, modern-day ICs are comprised of millions of transistors for which it becomes impossible to optimize transistor sizes manually. Therefore, bringing automation in design optimization becomes inevitable to cope up with the high integration density and complexity of modern IC designs.

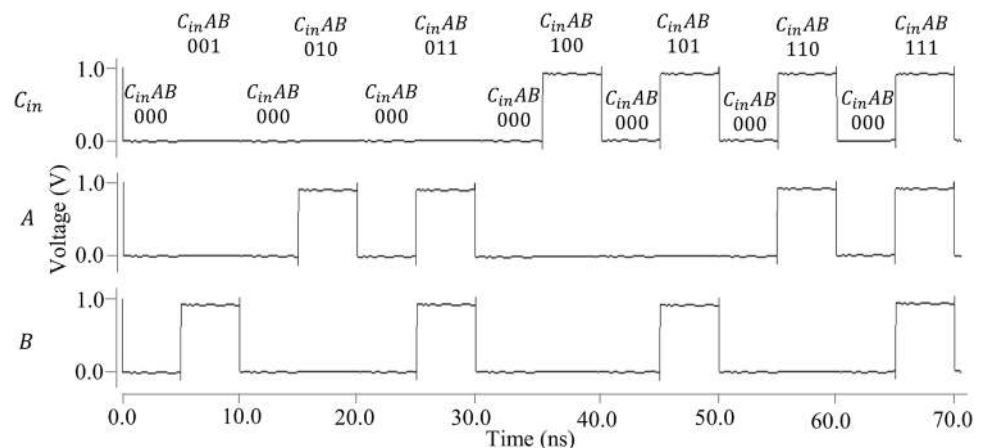
The transistor sizing method in [70] presents a linear method of performing a trade-off between CMOS circuit parameters: power, delay, and area. However, modern-day VLSI circuits behave in a non-linear manner for which this algorithm is unable to yield optimal performance. Transistor sizing methods in [19, 33, 71] present a simple but effective way of determining transistor sizes for delay optimization. However, only the critical path is considered in these two methods, for which power consumptions of circuits are not optimized. Nowadays, Power-Delay Product (PDP), which is simply the product of power consumption and delay of a circuit, has become the vital parameter and transistors have been sized for obtaining minimum PDP [35–54, 64–66]. Particle Swarm Optimization (PSO) has become a popular method for optimization of VLSI design [72, 73]. PSO-based inverter circuit optimization is presented in [74]. However, the algorithm is not tested for circuits having a large number of transistors and hybrid logic styles. Another PSO-based transistor sizing method is presented in [75]. But the algorithm is only tested for CCMOS logic-based designs. Simple Exact Algorithm (SEA) based transistor sizing presented in [76] has been specially designed for arithmetic circuits, taking into account various hybrid logic design methodologies. The authors have tested the algorithm for various FA cells such as: CPL [25], CCMOS [30], TGA [33], TFA [34], 14-T [37], NHPSC [41]. Due to the ability to optimize hybrid logic cells, the SEA transistor sizing method in [76] has been used in this paper for optimizing FA cells.

### 3.3 Simulation testbench

To inspect the performance parameters of FA cells, a feasible structure is required to perform simulations. Various simulation testbench, reported by researchers for FA simulation, have been illustrated in Fig. 2. In the case of testbench in Fig. 2a, three stages of FAs are connected having buffers in the input and output terminals. Delay for this testbench is measured from input terminals of the 1st FA stage to the last signals in the 3rd FA. Hence, it does not represent the delay of a single FA block. Moreover, inputs are only applied to the 1st FA stage. Therefore, the 2nd and 3rd FA stages are not tested properly. As a result, the power consumed by various FA stages is different. In addition, the fan-out of Sum is 1 whereas the fan-out of  $C_{out}$  is 2. Therefore, the FA blocks are not similarly loaded. FA test benches in Fig. 2b and c are similar except for the last parts. Both of the test benches are free from the limitations of the testbench in Fig. 2a. Since the SEA transistor sizing method, described in sub-Sect. 3.2 used the simulation test bench in Fig. 2c, we have also used this test bench for FA simulation in this work.

The testbench in Fig. 2c, which is used in this research contains a set of buffers attached to the input terminals. In fabricated processors or ICs, the signals pass through several non-ideal circuit components which make the signals distorted. Therefore, while generating input signals for simulation, it is necessary to replicate the real-time scenario by introducing signal distortion. For this reason, the buffers are attached to input terminals to bring distortions in the input signals. On the other hand, the output of a circuit is always connected to other components in an IC which work as a load to the circuit. Therefore, in the case of simulation, it becomes necessary to attach a load circuit with an output terminal to work as load. The testbench demonstrated in Fig. 2c comprises buffers in the output terminals as load circuits to the output terminals.

**Fig. 1** Input waveform for power and delay calculation





## 4 Simulation results and performance comparison

For comparative investigations of performance parameters, simulations have been conducted considering various aspects and operating conditions. Obtained simulation results for FA cells are presented in the following sub-sections.

### 4.1 Performance of FAs as single cells

Obtained simulation results using simulation testbench in Fig. 2c has been presented in Table 1 and Fig. 3. It can be observed from Fig. 3a that HBD 6 FA design in ref. [49] obtained superior performance in terms of average power consumption. This FA design provides full swing operation utilizing only 16 transistors. The circuit has no threshold voltage drop issue in the internal nodes. Due to having a low transistor count with no threshold voltage drop issue, the circuit could provide low power operation. CPL FA in [25] is considered to be the highest power-consuming FA as per simulation results. As per Table 1, CPL FA has the highest transistor count among FA cells. Moreover, since only the NMOSs are used in CPL FA, the pull-up circuit is subjected to the threshold voltage drop issue. Due to these reasons, CPL FA has very high average power. Although 12-T [27], 10-T [35] and 14-T [37], LPHS [43], and GDI 1 [64] FA cells have low transistor count, yet

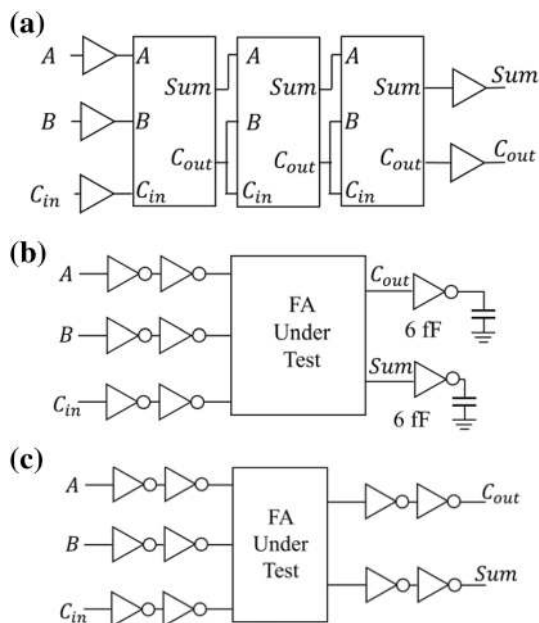
their corresponding average power is high due to loss in threshold voltage. Among single logic FAs, CCMOS [30] has the least power consumption. Moreover, it can be noticed that CCMOS has better performance in power compared to some of the recent hybrid FA designs. Among GDI cells, GDI 3 design in [66] obtained superior performance in power dissipation.

In the case of speed (propagation delay), HBD 7 FA in [50] obtained predominant performance. HBD 7 FA cell used input signal  $C_{in}$  as the gate control of transistors in the outermost terminals. As a result, the portion of the outermost terminal got switched on before the time it takes to generate signals in the internal nodes. Once the internal signals are generated, they instantly appear in the output terminals since the output terminal has been turned on beforehand. By this scheme, the circuit could ensure better speed. HBD 3 [46], GDI 2 [65], and GDI 3 [66] are close contenders of HBD 7 [50] in speed. Speed of CPL [25] and CCMOS [30] FAs are quite satisfactory in spite of being some of the oldest FA topologies. 12-T [27], 10-T [35], 14-T [37], NHPSC [41], and HBD 6 [48] FA cells have a very high level of propagation delay which limits their application in high-speed systems. 12-T [27], 10-T [35], 14-T [37] and NHPSC [41] FAs have threshold voltage drop issues in the internal nodes for which the internal nodes are subjected to voltage degradation. When this degraded voltage is used as the gate control of a transistor, it takes more time for the transistor to turn on. For this reason, 12-T [27], 10-T [35], 14-T [37] and NHPSC [41] FAs have severe speed issues. In HBD 6 FA design [48], at first, input terms A and B are used in an XNOR circuit. Then, an inverter is used to invert the XNOR signal into XOR. Later, these XOR-XNOR signals are used in sum and carry-out circuits to generate the final outputs. Since, the XOR signal faces one inverter stage delay than the XNOR signal, the sum and the carry-out circuits become slower. This is the main reason behind the speed issues of HBD 6 FA [48].

In terms of PDP, HBD 7 [50] acquired the highest performance. HBD 7 obtained the best performance in speed while maintaining quite satisfactory performance in power consumption. For this reason, HBD 7 could attain the best performance in PDP. In spite of excellent performance in speed, CPL [25] has very high PDP due to its high average power. 16-T [36], HBD 1 [45], HBD 2 [45], HBD 3 [46], HBD 4 [47], GDI 1 [64], GDI 2 [65], GDI 3 [66], GDI 4 [66] and GDI 5 [66] have considerably low PDP compared to other FAs.

### 4.2 Performance of FAs in various load conditions

Drive power of VLSI circuits is an important parameter that is highly required for high-fan out conditions. High-performance circuits (high speed and low power circuits),



**Fig. 2** Various simulation testbench for FA **a** simulation testbench in [49], **b** simulation testbench in [33, 36, 41, 44–46, 50], **c** simulation testbench in [76] obtained from SEA transistor sizing method

**Table 1** Performance of Full Adders as single cells

Full Adder	Ref. no	Transistor Count	Power ( $\mu$ W)	Delay (ps)	PDP (aJ)
CPL	[25]	32	2.79	54.21	151.25
12-T	[27]	12	1.89	116.62	220.41
CCMOS	[30]	28	1.31	66.28	86.83
TGA	[33]	20	1.01	83.29	84.12
TFA	[34]	16	0.97	88.20	85.55
10-T	[35]	10	0.99	101.51	100.49
16-T	[36]	16	0.92	56.23	51.73
14-T	[37]	14	1.72	105.86	182.08
18-T	[38]	18	0.98	68.49	67.12
24-T	[39]	24	1.18	82.65	97.53
HPSC	[40]	22	1.42	58.82	83.52
NHPSC	[41]	24	1.39	109.28	151.89
ULPFA	[42]	24	1.53	81.47	124.65
LPHS	[43]	15	0.84	88.56	74.39
DPL	[44]	22	1.31	60.95	79.84
SR-CPL	[44]	20	1.26	74.2	93.49
Hbd 1	[45]	23	0.87	50.75	44.15
Hbd 2	[45]	21	0.93	60.85	56.59
Hbd 3	[46]	27	1.21	44.23	53.52
Hbd 4	[47]	16	0.73	55.46	40.49
Hbd 5	[48]	22	1.18	67.74	79.93
Hbd 6	[49]	16	0.65	99.57	64.72
HBD 7	[50]	22	0.83	38.7	32.12
HBD 8	[51]	26	1.18	73.12	86.28
HBD 9	[52]	32	1.45	61.28	88.86
HBD 10	[53]	20	0.95	69.76	66.27
HBD 11	[54]	16	0.75	82.13	61.59
HBD 12	[54]	14	0.82	91.23	74.81
GDI 1	[64]	14	0.81	60.92	49.35
GDI 2	[65]	22	1.03	41.02	42.25
GDI 3	[66]	18	0.79	50.27	39.71
GDI 4	[66]	22	1.24	44.25	54.87
GDI 5	[66]	21	0.96	55.56	55.34

with low drive power, might fail to operate in an IC. Therefore, the drive power of VLSI circuits is a critical parameter that needs to be optimized. To analyze the drive power of FA cells, unit size inverter cells have been utilized as load. Load conditions, ranging from Fan-Out of 4-unit size inverters (FO-4) to FO-64, have been applied to each FA cell and propagation delays corresponding to the different load conditions have been calculated. Results are recorded in Table 2.

After extensive investigation of the data presented in Table 2, FA cells are categorized in three major groups: low drive power FA (marked by ***bold italic*** texts in the Drive Power column of Table 2), moderate drive power

FA (marked by *italic* texts in the Drive Power column of Table 2) and high drive power FA (marked by **bold** texts in the Drive Power column of Table 2). Simulation data of each group (low drive power, moderate drive power and high drive power FA) are displayed in Fig. 4a, b and c, respectively. CPL [25], 12-T [27], 10-T [35], 14-T [37], LPHS [43], HBD 4 [47], and GDI 1 [64] FAs fall in low drive power group. TGA [33], TFA [34], 16-T [36], 18-T [38], DPL [44], SR-CPL [44], HBD 1 [45], HBD 2 [45], HBD 3 [46], HBD 5 [48], HBD 6 [49], HBD 7 [50], HBD 10 [53], HBD 11 [54], HBD 12 [54], GDI 3 [66], GDI 4 [66], and GDI 5 [66] are medium drive power FAs. As last, CCMOS [30], HPSC [40], NHPSC [41], ULPFA [42], HBD 8 [51], HBD [52], and GDI 2 [65] consist of high drive power group.

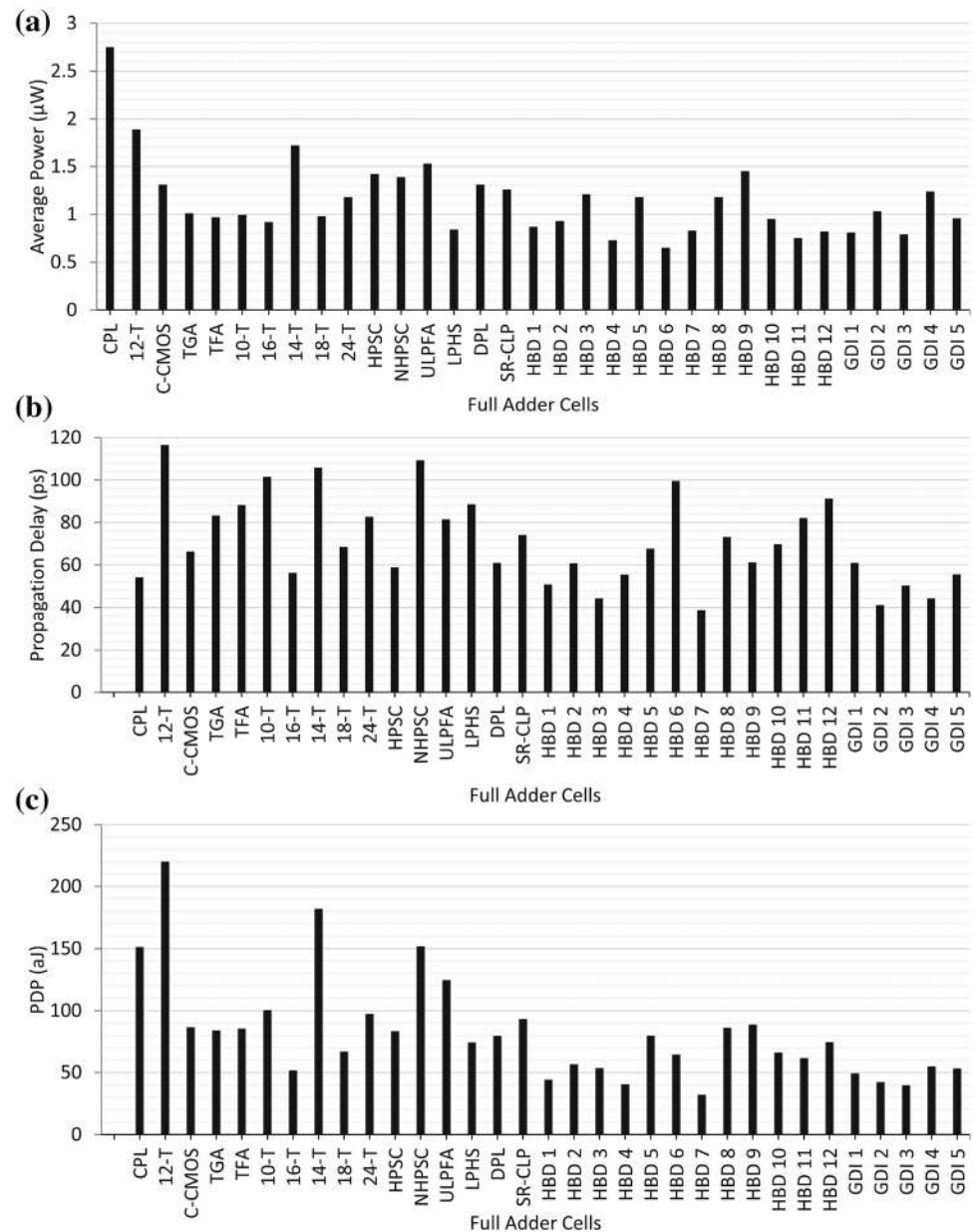
To compare among the groups, three FA cells from each group have been selected as representatives. The representatives from each group are: (1) FA that achieved best drive power, (2) FA that has least drive power and, (3) FA having middle-most drive power data between type (1) and type (2) FAs. The associated propagation delays for each type are shown in Fig. 4d. In Fig. 4d, CPL [25], 14-T [37], and GDI1 [64] FAs are the representatives from low drive power FA group. TFA [34], HBD 7 [50], and HBD 10 [53] represent moderate drive power FA group whereas ULPFA [42], HBD 8 [51], and GDI 2 [55] represent high drive power FA. It can be seen that, with increasing fan-outs, propagation delays for moderate drive power FAs rise at a higher pace compared to the graphs representing high drive power FAs. In the case of low drive power FAs, the propagation delay increased quite rapidly compared to the other groups. Output terminals of FAs that have voltage degradation issues mainly fall in the low drive power group.

### 4.3 Performance of FAs in wide adder structure

Modern ALUs require wide adder structures (16-bit, 32-bit, etc.) to perform computation [77]. Therefore, it is important to compare the performance of FAs operating in wide adder architecture. To do so, the FA cells have been extended up to 32-bits using the Ripple-Carry Adder style [78]. Simulation results on performance parameters have been recorded in Table 3. No voltage level restoring buffers have been added while extending the FA cells to a wide adder structure.

It has been observed that 21 out of 33 FA cells (marked with 'F' in Table 3) could not operate when they were extended to 32-bits. This occurred due to the degradation of signal strength while propagating through a series of logic circuits. To eliminate this issue, level restoration buffers are required to be installed, which costs additional circuitry. As a result, delay and power consumption will increase. Therefore, circuits that can be incorporated

**Fig. 3** Performance comparison of Full Adders **a** Average Power, **b** Propagation Delay, **c** Power Delay Product (PDP)



directly in a system without the need of additional hardware are preferred by industrial circuit designers and academic researchers. Figure 5 presents a comparison of carry-output graph between a scalable and a non-scalable FA cell extended using RCA style. CCMOS FA [30] represents scalable FA while HBD 1 [45] represents non-scalable FA in Fig. 5. For CCMOS FA in Fig. 5a, no voltage degradation in carry signals could be seen. On the other hand, carry signals  $C_4$  and  $C_8$  of HBD 1 in Fig. 5b seem to have voltage degradation issues. Due to this voltage degradation issue, the carry signal gets below threshold voltage at a point while propagating through series of FA cells. As a result, the signal becomes unable to drive the next stage and the circuit fails to operate. Due to this reason, carry

signals  $C_{16}$  and  $C_{32}$  of HBD 1 FA are not available in Fig. 5b. Unlike HBD 1 FA, the condition is applicable for the circuits that could not operate in multiple-bit structures.

Among the remaining 12 FAs, output terminals of CCMOS [30], 24-T [39], HPSC [40], NHPSC [41], ULPFA [42], HBD 8 [51], HBD 9 [52] and GDI 2 [65] FA cells are comprised of CCMOS logic circuits. The pull-up network of the CCMOS logic circuit is connected to  $V_{dd}$  and the pull-down network to Ground. As a result, while extended to wide adder architecture, output signal voltage gets replenished after every FA stage. For the remaining 4 FA cells, which could be extended to 32-bits, the same output-carry signal does not propagate throughout the entire 32-bit stages. Hence, voltage strengths of signals

**Table 2** Performance of Full Adders in different load conditions

Full Adder	Ref. no	Delay due to different loads (ps)				Drive Power
		FO-8	FO-16	FO-32	FO-64	
CPL	[25]	173.2	538.9	2710.1	F	<b>Low</b>
12-T	[27]	375.6	1360.4	F	F	<b>Low</b>
CCMOS	[30]	71.5	83.6	107.2	152.9	<b>High</b>
TGA	[33]	119.6	175.7	458.8	2160.7	<i>Moderate</i>
TFA	[34]	128.1	196.4	552.7	2924.9	<i>Moderate</i>
10-T	[35]	346.6	1324.5	F	F	<b>Low</b>
16-T	[36]	74.19	96.71	174.1	542.1	<i>Moderate</i>
14-T	[37]	363.6	1405.3	F	F	<b>Low</b>
18-T	[38]	89.7	118.2	213.5	644.9	<i>Moderate</i>
24-T	[39]	90.48	106.23	138.22	197.67	<b>High</b>
HPSC	[40]	64.2	76.1	98.8	141.3	<b>High</b>
NHPSC	[41]	120.1	141.5	191.2	273.8	<b>High</b>
ULPFA	[42]	95.1	115.9	156.3	238.8	<b>High</b>
LPHS	[43]	314.1	991.2	4983.5	F	<b>Low</b>
DPL	[44]	78.2	94.3	168.3	522.7	<i>Moderate</i>
SR-CPL	[44]	90.6	110.5	199.2	623.5	<i>Moderate</i>
HBD 1	[45]	62.4	77.9	142.5	448.8	<i>Moderate</i>
HBD 2	[45]	68.3	84.6	155.4	488.1	<i>Moderate</i>
HBD 3	[46]	54.8	68.5	127.2	401.5	<i>Moderate</i>
HBD 4	[47]	178.6	556.3	2902.9	F	<b>Low</b>
HBD 5	[48]	87.7	113.6	204.7	633.8	<i>Moderate</i>
HBD 6	[49]	119.4	144.8	257.5	795.1	<i>Moderate</i>
HBD 7	[50]	46.8	59.4	106.9	295.3	<i>Moderate</i>
HBD 8	[51]	81.7	99.3	134.9	207.1	<b>High</b>
HBD 9	[52]	74.3	91.1	123.5	207.1	<b>High</b>
HBD 10	[53]	87.5	110.7	203.8	671.7	<i>Moderate</i>
HBD 11	[54]	99.5	123.1	225.8	710.3	<i>Moderate</i>
HBD 12	[54]	115.6	149.3	279.5	906.3	<i>Moderate</i>
GDI 1	[64]	189.7	586.1	3022.7	F	<b>Low</b>
GDI 2	[65]	45.8	55.8	74.6	113.5	<b>High</b>
GDI 3	[66]	61.8	89.5	162.8	497.5	<i>Moderate</i>
GDI 4	[66]	57.7	72.9	135.4	415.9	<i>Moderate</i>

do not decline [50]. As a result, the FA cells could operate successfully in wide adder architecture without using voltage restoring buffers.

## 5 Major finding and discussion

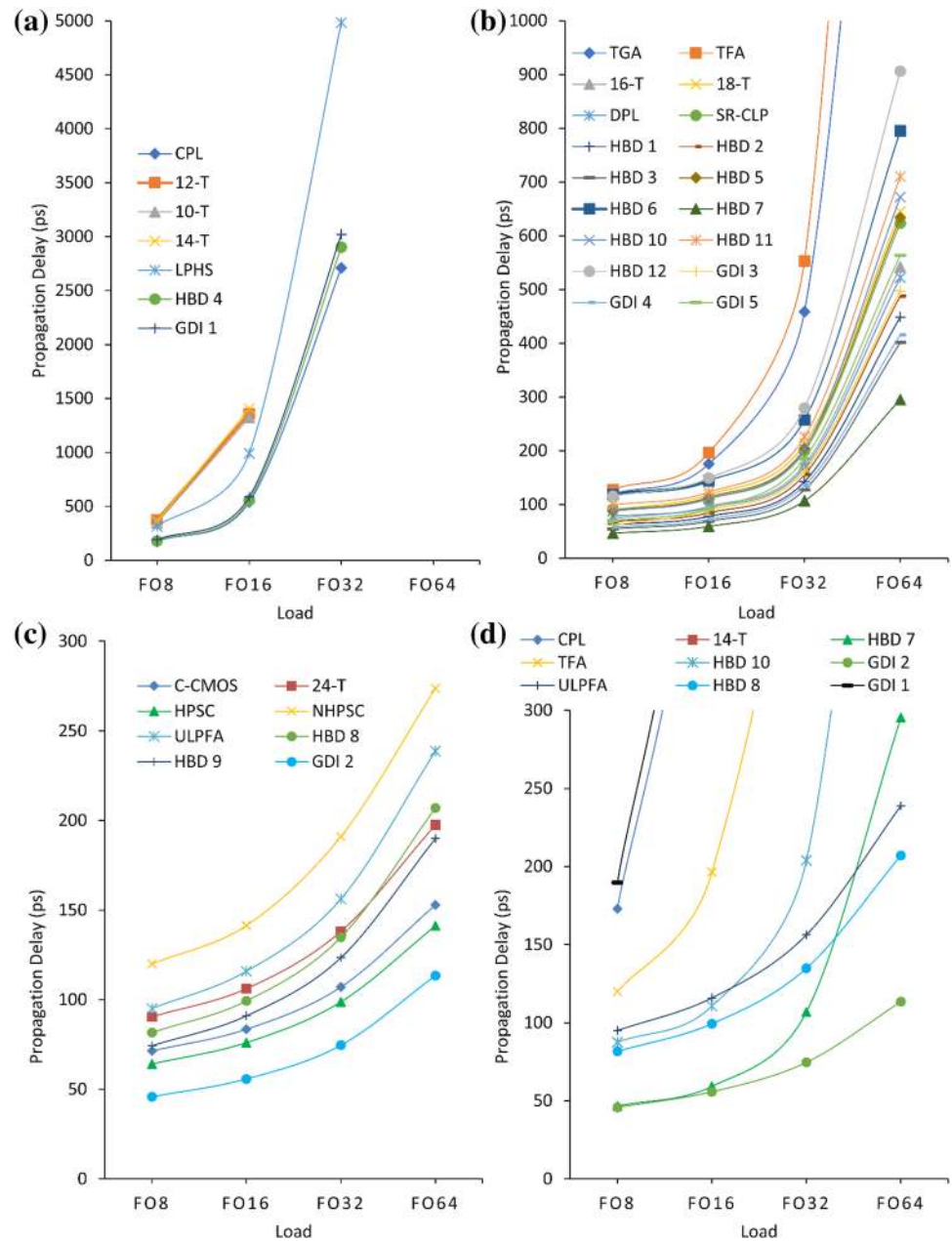
As modern microprocessors are not limited to only a 1-bit addition operation, FA cells need to have the ability to be scaled up to wide word-length adders. Therefore, scalability is a major factor that needs to be investigated while analyzing FA cells. In this research, the scalability test conducted in Sect. 4.3 reveals that only one-third (11 out of 33) of the FA designs could be scaled up to multiple bits in the simple RCA style. The remaining 22 FA cells failed to operate while scaled up to 32-bits. After

extensive analysis of Table 1, Fig. 3, and Table 3, it was found that some FAs, having high-performance parameters as single cells were unable to operate in 16-bit or 32-bit structure. For instance, performance of 16-T [36], 18-T [38], HBD 1–4 [45–47], HBD 6 [49], HBD 10–11 [53, 54], GDI 1 [64] and GDI 3 [66] FAs are quite satisfactory as per simulation data presented in Table 1 and Fig. 2. However, they could not operate while extended to 16-bits and 32-bits. Based on this analogy, it can be said that the performance comparison of adders based on only a 1-bit operation should not be the main parameter for analyzing FAs. Rather, it should be analyzed if the 1-bit adder cells are scalable or not.

Moreover, based on data presented in Table 3, it is essential to mention that the classic CCMOS FA cell obtained better performance than many FA cells in case



**Fig. 4** Performance of Full Adders in various load conditions **a** low drive power Full Adders, **b** moderate drive power Full Adders, **c** high drive power full adders, **d** comparison among low, moderate and high drive power Full Adder graphs



of operating in a wide word-length structure. This is the main reason for which CCMOS logic remains as the prominent circuit design methodology despite of being one of the oldest VLSI circuit design methods.

In recent research activities, the concept of fast parallel prefix adder has evolved which aims to generate carry terms in parallel to reduce carry propagation delay [79]. Most of the parallel prefix adders require carry-propagate and carry-generate to perform addition [80]. Carry propagate is the XOR function between the input bits that are required to be added. On the other hand, carry generate is the AND function between the input bits. Therefore, for

fast parallel adders, FA cells incorporating XOR and AND functions will be highly suitable. Among FAs analyzed in this research, DPL [44], SR-CPL [44], HBD 7 [7], and GDI 4 [66] FAs have AND and XOR functions for which they will be able to create carry generate and carry propagate signals without any extra hardware. As a result, these FAs will be more suitable for modern fast adder architectures.

The multiplier is another potential application of FA. In multiplier, carry output of on stage do not need to propagate through several stages for which scalability is not the major concern [81, 82]. For this reason, FA cells having good performance parameters while operating

**Table 3** Performance of Full Adders cells in wide word-length RCA structure

Average power ( $\mu$ W)					
Full adder	Refs. no	Bit number			
		4 Bit	8 Bit	16 Bit	32 Bit
CPL	[25]	10.96	21.68	F	F
12-T	[27]	7.51	F	F	F
CCMOS	[30]	4.95	9.65	19.07	37.85
TGA	[33]	4.19	8.97	F	F
TFA	[34]	3.91	8.06	F	F
10-T	[35]	4.22	F	F	F
16-T	[36]	3.64	7.31	F	F
14-T	[37]	7.05	F	F	F
18-T	[38]	3.97	8.21	F	F
24-T	[39]	4.62	9.02	17.69	35.15
HPSC	[40]	5.55	10.86	21.62	43.09
NHPSC	[41]	5.34	10.29	20.14	39.81
ULPFA	[42]	5.68	10.93	21.27	41.85
LPHS	[43]	3.81	8.09	F	F
DPL	[44]	5.36	11.23	F	F
SR-CPL	[44]	3.11	6.69	F	F
Hbd 1	[45]	3.59	7.56	F	F
Hbd 2	[45]	3.83	8.05	F	F
Hbd 3	[46]	4.95	9.85	F	F
Hbd 4	[47]	2.94	6.08	F	F
Hbd 5	[48]	4.92	9.95	20.02	41.39
Hbd 6	[49]	2.69	4.93	F	F
HBD 7	[50]	3.31	6.34	12.36	24.35
HBD 8	[51]	4.61	8.89	17.67	35.55
HBD 9	[52]	5.52	10.47	20.16	40.07
HBD 10	[53]	3.91	8.16	F	F
HBD 11	[54]	3.07	6.42	F	F
HBD 12	[54]	3.34	7.01	F	F
GDI 1	[64]	3.19	6.19	F	F
GDI 2	[65]	4.21	8.672	18.03	37.68
GDI 3	[66]	3.32	6.92	F	F
GDI 4	[66]	4.39	9.05	18.96	39.78
GDI 5	[66]	3.94	7.94	16.35	34.31

## Propagation delay (ns)

Full adder	Refs. no	Bit number			
		4 Bit	8-Bit	16-Bit	32-Bit
CPL	[25]	0.294	2.349	F	F
12-T	[27]	0.885	F	F	F
CCMOS	[30]	0.253	0.517	1.041	2.272
TGA	[33]	0.441	3.358	F	F
TFA	[34]	0.451	3.455	F	F
10-T	[35]	0.752	F	F	F
16-T	[36]	0.279	2.293	F	F
14-T	[37]	0.829	F	F	F
18-T	[38]	0.356	2.674	F	F
24-T	[39]	0.332	0.685	2.005	4.231

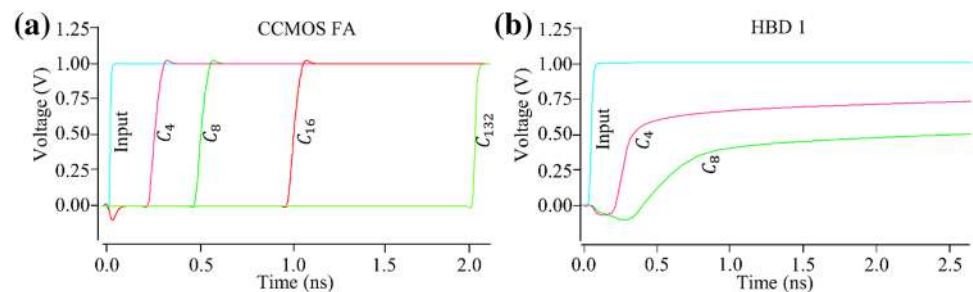
**Table 3** (continued)

Propagation delay (ns)					
Full adder	Refs. no	Bit number			
		4 Bit	8-Bit	16-Bit	32-Bit
HPSC	[40]	0.233	0.473	0.978	1.969
NHPSC	[41]	0.438	0.892	1.854	3.898
ULPFA	[42]	0.331	0.669	1.386	2.897
LPHS	[43]	0.453	3.358	F	F
DPL	[44]	0.362	2.651	F	F
SR-CPL	[44]	0.429	3.427	F	F
Hbd 1	[45]	0.280	2.549	F	F
Hbd 2	[45]	0.325	2.821	F	F
Hbd 3	[46]	0.275	2.379	F	F
Hbd 4	[47]	0.308	2.652	F	F
Hbd 5	[48]	0.276	0.575	1.155	2.316
Hbd 6	[49]	0.722	4.749	F	F
HBD 7	[50]	0.154	0.311	0.634	1.323
HBD 8	[51]	0.286	0.572	1.183	3.387
HBD 9	[52]	0.243	0.508	1.082	2.307
HBD 10	[53]	0.367	2.551	F	F
HBD 11	[54]	0.411	2.834	F	F
HBD 12	[54]	0.478	3.325	F	F
GDI 1	[64]	0.428	3.125	F	F
GDI 2	[65]	0.162	0.333	0.601	1.313
GDI 3	[66]	0.248	1.563	F	F
GDI 4	[66]	0.181	0.378	0.793	1.601
GDI 5	[66]	0.229	0.478	0.952	1.875
PDP (fJ)					
Full adder	Refs. no	Bit number			
		4 Bit	8-Bit	16-Bit	32-Bit
CPL	[25]	3.22	50.92	F	F
12-T	[27]	6.65	F	F	F
CCMOS	[30]	1.25	4.99	9.85	85.99
TGA	[33]	1.85	30.12	F	F
TFA	[34]	1.76	27.84	F	F
10-T	[35]	3.17	F	F	F
16-T	[36]	1.02	16.76	F	F
14-T	[37]	5.84	F	F	F
18-T	[38]	1.41	21.95	F	F
24-T	[39]	1.53	6.18	35.47	148.72
HPSC	[40]	1.29	5.14	21.14	84.84
NHPSC	[41]	2.34	9.18	37.34	155.18
ULPFA	[42]	1.88	7.31	29.48	121.24
LPHS	[43]	1.73	27.17	F	F
DPL	[44]	1.94	29.77	F	F
SR-CPL	[44]	1.33	22.92	F	F
Hbd 1	[45]	1.01	19.27	F	F
Hbd 2	[45]	1.24	22.71	F	F
Hbd 3	[46]	1.36	23.43	F	F
Hbd 4	[47]	0.91	16.21	F	F

**Table 3** (continued)

PDP (fJ)					
Full adder	Refs. no	Bit number			
		4 Bit	8-Bit	16-Bit	32-Bit
Hbd 5	[48]	1.36	5.72	23.12	95.86
Hbd 6	[49]	1.94	23.42	F	F
HBD 7	[50]	0.51	1.97	7.84	32.2
HBD 8	[51]	1.32	5.09	20.9	120.4
HBD 9	[52]	1.34	5.32	21.81	92.44
HBD 10	[53]	1.43	20.82	F	F
HBD 11	[54]	1.26	18.19	F	F
HBD 12	[54]	1.59	23.31	F	F
GDI 1	[64]	1.37	19.34	F	F
GDI 2	[65]	0.68	2.89	10.84	49.47
GDI 3	[66]	0.82	10.82	F	F
GDI 4	[66]	0.79	3.42	15.04	63.69
GDI 5	[66]	0.9	3.8	15.57	64.33

F: Failed to Operate

**Fig. 5** Example of carry output signals of **a** scalable FA **b** non-scalable FA

as 1-bit are quite suitable for utilization in multipliers. As per performance analysis of 1-bit cells, 16-T [36], HBD 1 [45], HBD 2 [45], HBD 3 [46], HBD 4 [47], HBD 7 [50], GDI 1 [64], GDI 2 [65], GDI 3 [66], GDI 4 [66] and GDI 5 [66] FAs have good performance due to which they will be good candidates for utilization in multipliers.

If transistors are scaled to lower technology nodes, then parasitics associated with the transistors will decrease for which any circuit operating in lower technology nodes will exhibit better performance than operating in higher technology nodes. However, if FAs are simulated in lower technology node than the 45 nm CMOS process, then the performance difference among FA cells will likely remain the same since parasitics will decrease in the same manner for all FA cells. But in the case of lower technology nodes, interconnect parasitics does not decrease in the same manner as transistor parasitics do [83]. For this reason, interconnect widths are required to be optimized in lower technology nodes to maintain the performance levels of FA cells [83].

## 6 Conclusion

A comprehensive literature review and performance comparison of various FA designs have been conducted in this research. The performance of FA cells, operating both as single bit and wide-adder structures, has been investigated. The simulation results include average power, propagation delay, and PDP (Power-Delay-Product) that covers most of the main performance metrics. To determine the effectiveness of FAs in high fan-out cases, and to have a comparative analysis of their drive powers, the FA designs have also been simulated using various load conditions. According to this study, only a few of the existing FA cells are capable of performing well when they are scaled up to multiple-bit structures. Hence, although it is popular to compare FA cells by comparing their performance parameters in the 1-bit structure, this research recommends that the practical



effectiveness of FA cells be compared using their wide-word structures.

#### Declarations

**Conflict of interest** The authors declare no conflict of interest.

**Availability of data and material** The manuscript has no associated data/ materials obtained from external sources.

**Code availability** No code is available for this research.

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