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Computational light junction temperature estimator for active thermal control

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***Abstract*—The junction temperature of power semiconductors in power converters must not exceed its maximum limits and it is of major importance for several failure mechanisms. But still, the junction temperature is hard to access. Direct measurement is not practical for industrial applications, indirect measurements require substantial effort and available junction temperature models have high calculation effort. This work develops a simple junction temperature estimator, which is applied for a maximum junction temperature limitation and the capability to be applied for further algorithm relying on the junction temperature, referring to active thermal control. It is experimentally shown, that a second order estimator is sufficient to achieve high bandwidth estimation.**

***Index Terms*—Power Electronics, Reliability, Active Thermal Control, Junction Temperature**

I. Introduction

Reliability of power semiconductors has become one of the key-requirements in the design of today's power electronic systems [1]. To ensure reliability, the thermal management of the power semiconductors is part of the design process, but still most failures are caused by insufficient thermal management [2]. Active thermal control refers to an online junction temperature manipulation and is an opportunity to thermally protect the system and to reduce the thermal stress without increasing the manufacturing costs or the footprint [3], [4]. However, a big challenge remains the cheap access to the junction temperature with high time resolution.

In systems with high modularity, such as the modular multilevel converter, a high number of junction temperatures need to be known [5] with sufficient bandwidth for enabling active thermal control algorithms. The measurement of the junction temperature can either be done directly with thermocouples, thermo-sensitive parameters, optic fibers or infrared cameras. Most of these methods require access to the chip surface, which is covered by gel for electric isolation and protection against corrosion, but additional measurement equipment is required, even if the junction temperature is measured indirectly [6]. These additional sensors are associated with costs and have limited bandwidth. Another opportunity for junction temperature modeling are thermal models and observers, which often imply higher calculation effort [7]. This calculation effort is especially critical for systems operating at high sampling frequencies and systems consisting of many power semiconductors and thus junction temperatures [8]. For these systems, complex thermal models, such as Kalman filters, would not be an adequate solution. Furthermore, many thermal models in literature are either based on finite element analysis or are tested for fundamental frequencies, which are significantly lower than the fundamental grid frequency of $50/60\ Hz$ [9], [10].

This work proposes to use a thermal model in combination with the commonly available case temperature measurement for junction temperature estimation. No confidential information of the manufacturers is needed. The requirements for the implementation are described and the effectiveness of the approach is demonstrated on a laboratory setup with a high speed infrared camera. For the protection against excessive junction temperatures, a PI controller based junction temperature limitation is implemented and validated experimentally. The influence of the number of RC-elements for the model of the estimator on the precision of the junction temperature estimation is evaluated.

In section II failures of power electronic modules are reviewed and junction temperature modeling is introduced, while section III introduces the system and the applied thermal model. In section IV the model is parametrized and in section V an overtemperature protection is introduced before an experimental validation is presented in section VI. Finally, the conclusions are given in section VII.

II. Failures in power electronic modules and junction temperature modeling

In this section common failure mechanisms for power electronic modules are described to be related to the junction temperature and then junction temperature modeling in power electronics is introduced.

A. Failures in power electronic modules

Most failures of power electronic modules are caused by the temperature fluctuations [2], [11]. The stress occurs at the interconnections in the module between materials with different coefficients of thermal expansion, which are needed to ensure electrical isolation on the one hand and good heat transfer capability on the other hand. Fluctuations of the

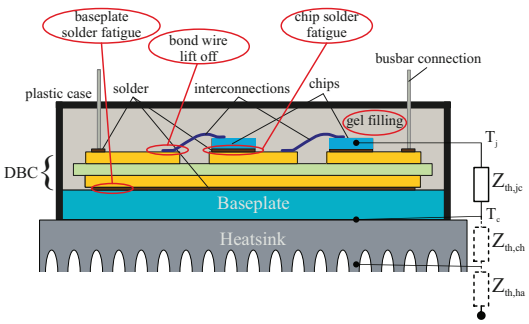


Fig. 1: Scheme of a power electronic module with heatsink, common failures and thermal impedances.

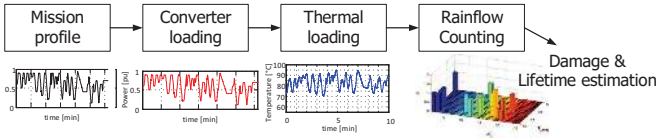


Fig. 2: From mission profile to lifetime estimation.

temperature cause mechanical stress between these layers, which leads to wear out and finally failure. The scheme of a power electronic module with the direct bonded copper (DBC) structure and the common failures, such as chip solder fatigue, bond wire lift off and baseplate solder fatigue, is shown in Fig. 1. For protection against corrosion and environmental influences, a gel filling immerses the module to guarantee dielectric strength. The main aging processes of the silicone gel are water trees, partial discharge and electrical trees, which are degrading effects causing aging but not the immediate destruction [12].

Additionally, in Fig. 1, the heat sink, the thermal impedance between junction and case $Z_{th,jc}$, the thermal impedance between case and heatsink $Z_{th,ch}$ and the thermal impedance between heatsink and ambient $Z_{th,ha}$ are shown.

For a lifetime estimation, the described failure mechanisms need to be considered. Remarkably, the most relevant failure mechanisms (bond wire lift off and solder fatigue) are related to the junction temperature of the power semiconductors in the converter. This requires the knowledge of the junction temperature for the lifetime estimation. The procedure, which needs to be made is schematically shown in Fig. 2. Starting with the mission profile of the converter, the loading of the devices needs to be extracted, which results in the junction temperature profile. The Rainflow algorithm is usually adopted to extract the thermal cycles from the mission profile in the time domain and to group them in histograms. With a lifetime model these histograms are used to derive the accumulated damage, which leads to the consumed lifetime [13].

B. Thermal modeling in power electronic modules

For a precise thermal model, the temperature fluctuations need to be modeled in three dimensions by also considering the cross-coupling between the chips. However, due to the

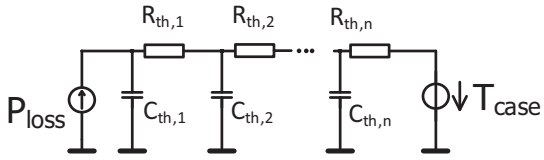


Fig. 3: Cauer network: electric circuit representing the thermal impedance $Z_{th,jc}$.

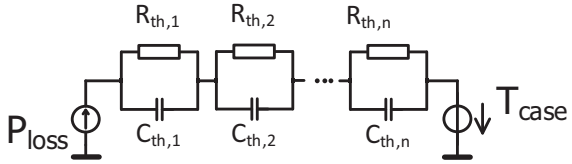


Fig. 4: Foster network: electric circuit representing the thermal impedance $Z_{th,jc}$.

complexity and the existence of a dominant heat flow path to the heat sink, in power electronics usually only a single dimension is modeled. The thermal impedances shown in Fig. 1 link the losses of the power semiconductors P_{loss} with a convolution to the junction temperatures of the IGBTs T_j and the case temperature $T_{case}(t)$ with (1).

$$T_j(t) = T_{jc}(t) + T_{case}(t) = Z_{th,jc}(t) * P_{loss}(t) + T_{case}(t) \quad (1)$$

The thermal impedances $Z_{th,jc}$ can be modeled by thermal resistors R_{th} and thermal capacitors C_{th}. In case that the impedances are obtained by finite element analysis, the Cauer network shown in Fig. 3 is usually used. Each chain link represents a layer of the module and is calculated by material constants. Therefore the Cauer network has a physical background. But beside the effort to be made for the modeling, the materials and the thickness of the layers are generally not provided by the manufacturer, which makes these models based on finete element analysis not practical. As an alternative, the thermal impedances can be obtained from fitting the measured cooling down curves. For the reason of simplicity, this cooling curve is fit to the thermal impedance of a Foster network shown in Fig. 4. The series connected RC chains are represented with (2).

$$Z_{th(jc)}(t) = \sum_{\nu=1}^{n} R_{th\nu} \cdot (1 - e^{-\frac{t}{\tau_{th\nu}}}) \quad (2)$$

There is the possibility to transform a Foster network into a Cauer network, but the transformation implies the deprivation of the physical background. In many cases the Foster network parameters are actually provided by the manufacturer in the datasheet. For both, Cauer and Foster networks, the number of chain links (order) is arbitrary. More chain links increase the precision of the model with the downside of higher complexity.

Unfortunately, the simple combination of the thermal impedances of the module and the heat sink causes errors and cannot just be done, even if both models are provided by

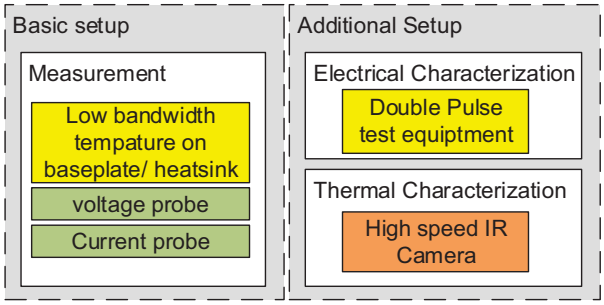


Fig. 5: Configuration of the laboratory equipment: Basic setup for active thermal control with datasheet parameters and potential additional setup for improved parametrization. green: Available measurements, yellow: Often available measurements or equipment and orange: Advanced but not mandatory equipment.

TABLE I: Source of parameters. green: parameter is constant over time; orange: parameter might be affected by aging

Parameter	Source
$E_{on},\ E_{off}$	datasheet or electrical characterization
$r_{ce},\ v_{ce,0}$	datasheet or electrical characterization
$R_{th,i}$	datasheet or thermal characterization
τ_i	datasheet or thermal characterization

the manufacturer and base on Foster RC-elements. At least the thermal grease needs to be taken into account and the reference point of the case temperature is not modeled anymore in the combined model [14]. However, since many power converters have a case temperature measurement, it is proposed to be used for the estimator. As an alternative, a low bandwidth heat sink temperature measurement can be used and the thermal impedance is obtained experimentally.

In order to apply (1) in real time application, it is transferred into a differential equation and discretized. For a single order estimator, this is shown in (3) for the junction to case temperature T_{jc}, the sampling frequency f_0, the thermal capacitance C_{th} and the thermal resistance R_{th}.

$$T_{jc}(k+1) = e^{-\frac{T_0}{R_{th,1}\cdot C_{th,1}}} \cdot T_{jc}(k) + \frac{1}{f_0 C_{th}} \cdot P_{loss}(k) \quad (3)$$

III. System Description and Model Description

The thermal Foster network shown in Fig. 4 is used to model the thermal behavior of the power semiconductors in the power electronic module. For the model parametrization, the thermal impedance needs to be known and the losses of the power semiconductors as the input variable. The losses can be derived with the knowledge of the operation point defined by the current and the voltage, the switching characteristics and the conduction characteristics of the power semiconductors. Based on a low bandwidth case temperature and the prior junction temperature, the influence of the junction temperature on the losses can be included.

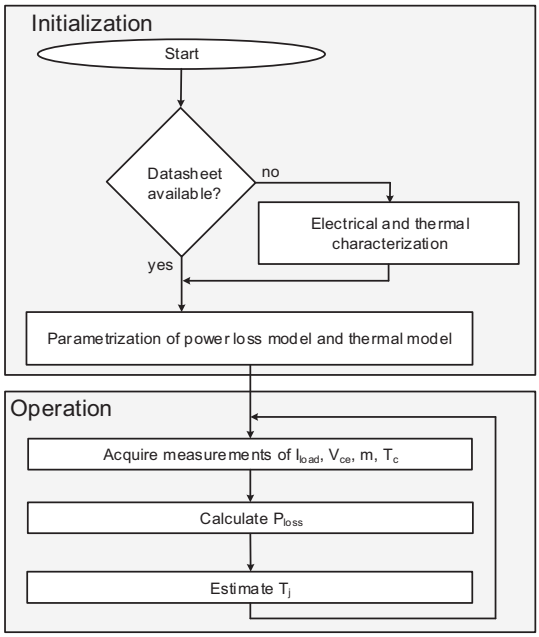


Fig. 6: Flowchart of the temperature estimator for active thermal control application.

The configuration of the required measurements and hardware is shown in Fig. 5. In the figure, it is indicated in green, which things are commonly available in each converter controller, while yellow indicates potentially additional effort. Additional equipment, such as a double pulse test setup for the power semiconductor characterization and a high speed temperature measurement improve the parametrization of the estimator. The infrared camera for the thermal characterization requires the gel filling to be removed, which is the reason for the orange marking. The electrical and thermal parameters, which are need for the model are summarized in Tab. I with their possible sources. All required parameters of the electrical and thermal characteristics can be found in the datasheet, while better results are obtained with measurements. The switching and conduction characteristics can be obtained from a double pulse test and the thermal characteristics by measurement of the cooling down curve. Particularly problematic is the variation of the thermal resistance affected by aging.

For the mitigation of the losses, the conduction losses P_{con} and the switching losses P_{sw} are derived based on the measurement of the semiconductor current I_c, the collector emitter voltage V_{ce}, the modulation index m and f_{sw}. The switching losses are additionally divided into the turn on losses $P_{sw,on}$ represented with (4) and the turn off losses $P_{sw,off}$ expressed with (5).

$$P_{sw,on} = f_{sw} \cdot E_{on} \cdot \left(\frac{I_{out}}{I_{ref}}\right)^{K_{I,on}} \cdot \left(\frac{V_{ce}}{V_{ref}}\right)^{K_{V,on}} \quad (4)$$

$$P_{sw,off} = f_{sw} \cdot E_{off} \cdot \left(\frac{I_{out}}{I_{ref}}\right)^{K_{I,off}} \cdot \left(\frac{V_{ce}}{V_{ref}}\right)^{K_{V,off}} \quad (5)$$

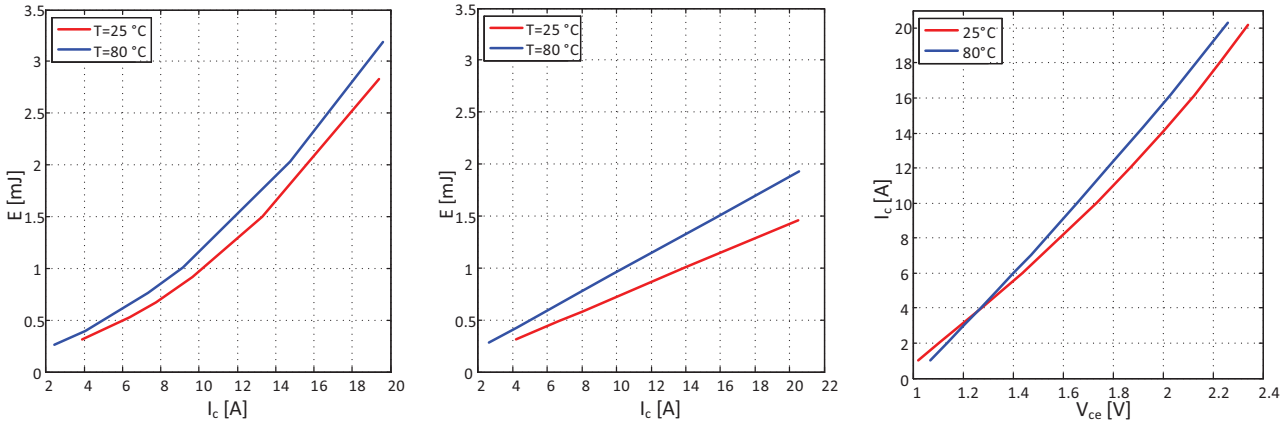


Fig. 7: Losses of the used IGBT: (a) Turn on losses, (b) Turn off losses, (c) Conduction losses.

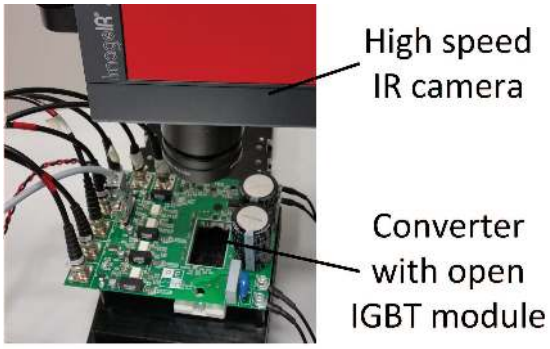


Fig. 8: Picture of the laboratory setup.

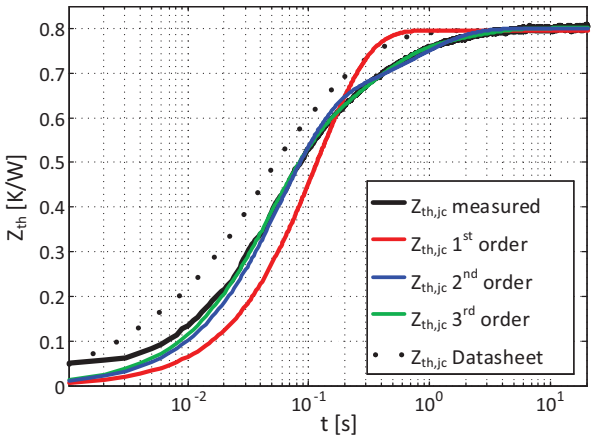


Fig. 9: Thermal impedance measurement of IGBT 1 indicating the influence of the number of thermal chains on the curve fit with the parameters of Tab. II.

I_{ref} and V_{ref} are the values for which E_{on} and E_{off} are given. $K_{I,on}$, $K_{V,on}$, $K_{I,off}$ and $K_{V,off}$ are the exponents that allows scaling the losses to voltages or currents different than the reference ones. The conduction losses are linearized for IGBTs with the constant voltage drop V_{ce0} and the resistance r_{ce} (6).

$$P_{con} = u_{ce0} \cdot i_c + r_{ce} \cdot i_c^2 \tag{6}$$

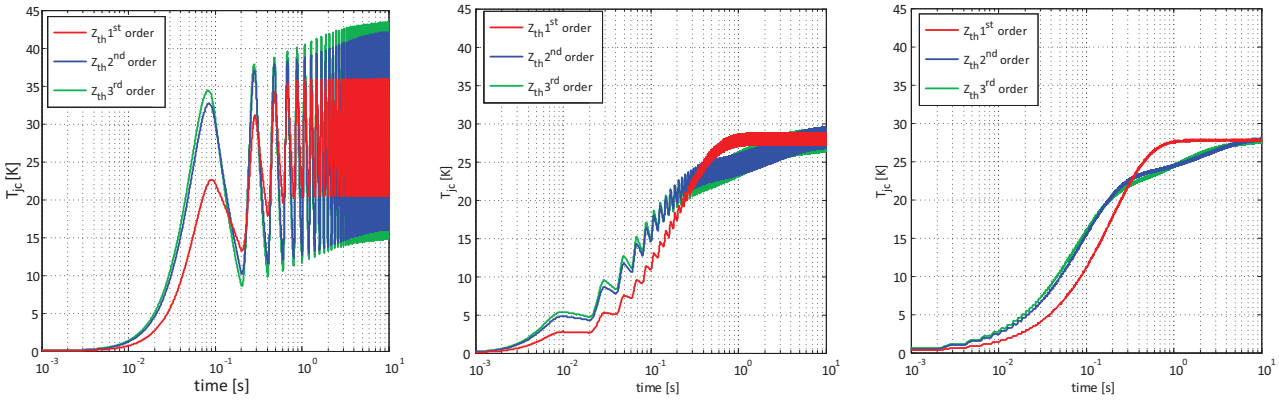
The total losses are fed to the thermal model for the junction temperature estimation (1). This model calculates T_j based on the low bandwidth T_c measurement. Therefore $Z_{th,ch}$ and $Z_{th,ha}$ are not needed in this thermal model (see Fig. 1). As a summary, the procedure for parametrization and operation of the estimator is visualized in Fig. 6.

With the estimator, the junction temperature is obtained with high bandwidth and can be processed with Rainflow counting for an estimation of the remaining lifetime or it can be used in data logging to identify correlating parameters in fault analysis. Apart from condition monitoring, the information about the junction temperature can be used for active thermal control.

IV. Characterization and Model Parameterization

The electrical characterization is done for the Danfoss (DP25H1200T101667-101667, $V_{ce} = 1200\ V$, $I_c = 25\ A$) module with a double pulse test setup. The results for the turn on losses are shown in Fig. 7 (a), the turn off losses in Fig. 7 (b) and the conduction losses in Fig. 7 (c). These characteristics are fit to 4-6 to derive the losses of the system online.

The thermal characterization of the module is done by measuring the cooling curve after heating up the chips with a DC-current and turning off the power. A high speed infrared camera, which is shown in Fig. 8, is used to measure the IGBT junction temperature with high bandwidth. Afterwards a curve fit with a Foster thermal network is done by using the least mean square algorithm. The measured cooling curve is divided by the losses of the DC current to obtain the thermal impedance. This shown in Fig. 9 for the measured



(a) (b) (c)

Fig. 10: Simulation: Step response of the thermal impedances $Z_{th,jc}(t)$ to sinusoidal power losses with different fundamental frequencies: (a) $f_0 = 5\ Hz$, (b) $f_0 = 50\ Hz$, (c) $f_0 = 500\ Hz$.

TABLE II: Parameters of the thermal impedance obtained from the fitting curve in Fig. 9.

	$R_{th}\ [K/W]$	$\tau\ [s]$
1 RC-Element	0.7981	0.197
2 RC-Elements	[0.1532, 0.6521]	[2.4837, 0.0911]
3 RC-Elements	[0.5934, 0.1768, 0.042]	[0. 0739, 1.0995, 11.7802]
Manufacturer datasheet	[0.09025, 0.3612, 0.2031, 0.1403]	[0.0023, 0.0282, 0.1128, 0.282]

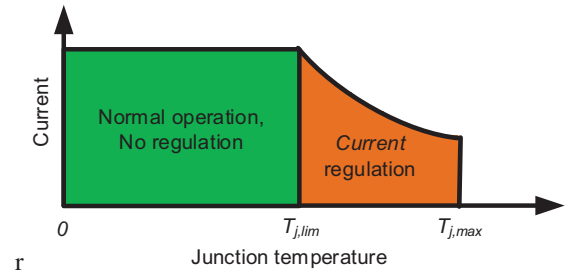


Fig. 11: Region for the juction temperature regulation.

curve and for different orders of RC-elements achieving a different precision in the curve fit with the parameters in Tab. II. The higher the order of RC-elements and thus of the designed estimator, the better the fit of the measured thermal impedance. For comparison with the parameters of a typical thermal impedance in a comparable module, the parameters of thermal resistors and time constants are shown in the table for the Infineon FP25R12KE3 module. In order to test the thermal model under realistic operation conditions, the estimator with the obtained parameters is tested with sinusoidal positive half wave excitation, which corresponds to the loading of power electronics in a converter. The response is shown in Fig. 10 for different fundamental frequencies of $5\ Hz$, $50\ Hz$ and $500\ Hz$. Similar to the fit of the thermal impedance, the difference between the second order estimator and the third order estimator is low, while the first order estimator has a slower response than the others. For the fundamental frequency of $f_0 = 5\ Hz$, the thermal swing is high and it decreases for the case of $f_0 = 50\ Hz$ and even more for $500\ Hz$. The magnitude of the thermal swing in the fundamental frequency is smallest for the first order estimator and maximum for the third order estimator. Remarkably, the steady state average temperature estimation is independent from the estimator order in all cases.

V. Dynamic Overtemperature Protection

An excess of the maximum junction temperature $T_{j,max}$ of an IGBT module causes destruction, e.g. by melting of the solder in the module. In order to prevent this, a dynamic junction temperature limitation is implemented, which is a simple active thermal control algorithm with protection capability. For not disturbing the normal operation, the limitation is only implemented for an excess of the chosen limited temperature $T_{j,lim}$ as shown in Fig. 11. The advantage compared to an overall maximum current limitation is the capability to operate with an increased current until the thermal limitations of the system are reached. With respect to a maximum case temperature limitation, the dynamic response is much higher, which requires a smaller safety margin, consequently a better utilization of the power semiconductors. Furthermore, during high ambient temperatures, the junction temperature limitation is superior to the case temperature limitation, because a maximum case temperature limitation does not respect the power processed by the converter and thus does not model the temperature between junction and case. As a consequence, it needs to be tuned for the worst case conditions, while a junction temperature limitation can reduce the safety margin.

The limitation of the junction temperature is implemented with a PI-controller and tuned to regulate the temperature to a maximum by reducing the load current as shown in Fig. 12.

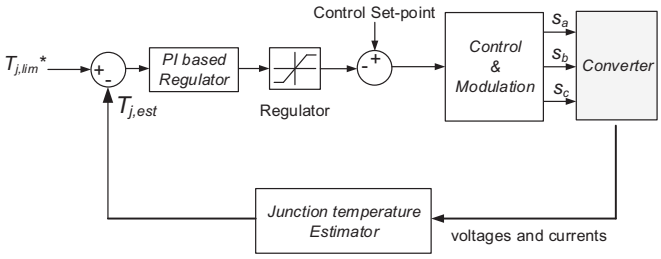


Fig. 12: Control circuit of the PI control with temperature feedback for T_j regulation.

It needs to be pointed out, that the thermal regulation has no impact when $T_{j,est}$ does not exceed $T_{j,lim}$.

The control loop is modeled with the transfer function of the thermal impedance obtained from the cooling down curve in Fig. 9. After transforming them into the frequency domain, the transfer function of (7) is obtained in dependence of the order of the approximation.

$$G_{th,jc}(s) = \sum_{\nu=1}^{n} \frac{R_{th\nu}}{1 + s \cdot \tau_{th\nu}} \tag{7}$$

This results in a control loop only consisting of time delays, which can be controlled by a PI controller. The transfer function of this PI-controller is shown in (8).

$$G_{PI}(s) = k_p \cdot (1 + \frac{1}{s \cdot T_I}) \tag{8}$$

The PI controller can be optimized in dependence of the requirement in terms of dynamic performance. Another constraint can be the maximum allowable overshoot in the junction temperature. As a tuning algorithm for current controller, the technical optimum is well known for high dynamic response and is used to tune the controller in this work.

VI. Experimental validation

The estimator is implemented on a dSpace System driving a full bridge connected to a passive load with the parameters ($R = 10\ \Omega, L = 3.5\ mH$). The dc-link voltage is set to $V_{dc} = 400\ V$, the switching frequency to $f_{sw} = 25\ kHz$ and the fundamental frequency of the output voltage to $f = 50\ Hz$. For the validation of the estimator, the junction temperature is measured with the camera shown in Fig. 8. First, the steady state behavior is tested and afterwards the dynamic behavior.

A. Stationary estimator validation

The estimators with first, second and third order are implemented and tuned with the parameters of Tab. II. All three estimators run in parallel for a comparison of the precision and potential delays in stationary conditions. The results are shown in Fig. 13, where $T_{j,meas}$ is the measured junction temperature with a sampling frequency of $f_{s,cam} = 400\ Hz$ and $T_{j,esti}$ is the temperature estimation with the estimator order $i = \{1, 2, 3\}$. The measured junction temperature has

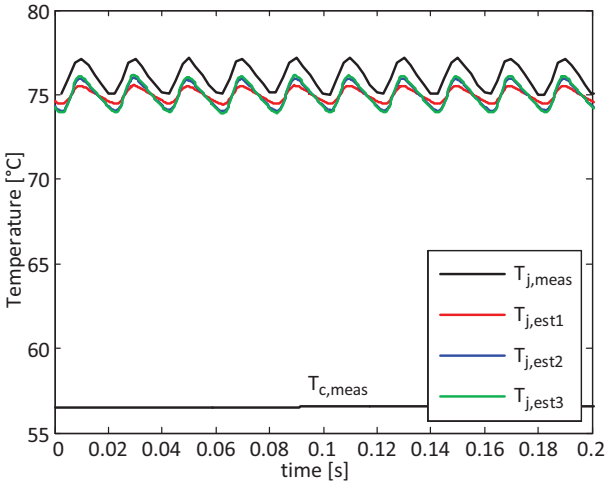


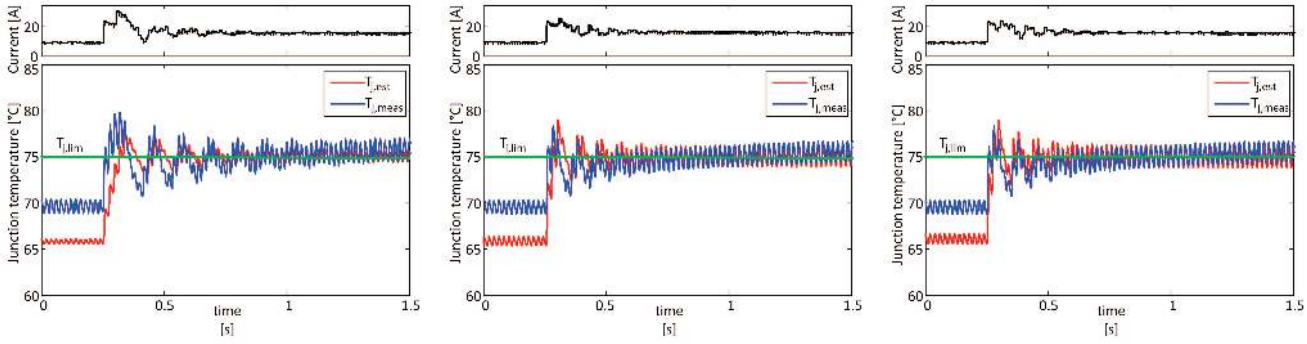
Fig. 13: Measurement: Thermal cycling in the fundamental period ($50\ Hz$) measured and modeled with different number of RC-elements.

thermal cycles of $\Delta T = 2\ K$ with an average junction temperature of $T_{j,av} = 76\ °C$. Compared to the estimated junction temperature, the average temperature is $1\ K$ higher than the average junction temperature $T_{j,av} = 75\ °C$. Remarkably, the thermal swing in the fundamental period for the second and third order model is similar to the measured thermal swing. The thermal swing of the first order estimator is only $\Delta T = 1\ K$, which is lowest compared to the other models and fits worst while the results for the second and third order estimator are comparable.

B. Junction temperature limitation validation

In this subsection, the model is tested for active thermal control application by means of the described dynamic limitation of the maximum junction temperature to $T_{j,lim} = 75\ °C$. The results for the control system modeled with the different order are shown in Fig. 14. During stationary conditions, a step variation in the output power occurs, which leads to higher losses and consequently an increase of the junction temperature. Without the limitation, the junction temperature would exceed $T_{j,lim}$, which affects the regulation of the junction temperature. This is tested by using the estimators of different orders.

For the junction temperature of the first order estimator, shown in Fig. 14 (a), the response of the estimator is slower than the measured junction temperature. Due to the resultant delay, the regulation of the current is causing an oscillation in the output current and the junction temperature. This causes additional thermal stress. Instead, the junction temperature regulation with the estimators of second order shown in Fig. 14 (b) and third order demonstrated in Fig. 14 (c) show a faster response. Their response is very similar and the overshoot is smaller compared to the first order feedback. In all cases, the stationary junction temperature limitation holds with a deviation of maximum $1\ K$ to the mean value.



(a) (b) (c)

Fig. 14: Measurement: Limitation of the junction temperature to $T_{j,lim} = 75\ °C$ by feedback of different order estimations: (a) Regulation with the first order estimation $T_{j,est1}$, (b) Regulation with the second order estimation $T_{j,est2}$, (c) Regulation with the third order estimation $T_{j,est3}$.

The first order estimator can be used for junction temperature estimations, but is problematic in active thermal control applications, where high dynamics are required. Instead the second and third order estimator achieve a good fit with the measured thermal response. The second order estimator is considered to fit best, because its performance is comparable to the third order estimator, while the calculation effort is lower.

VII. Conclusion

A simple estimator of the junction temperature of power semiconductors in power electronic modules has been proposed with the aim of allow an easy implementation of the active thermal control. The tuning can be made based on the information given in the datasheet provided by the manufacturer. The influence of the estimator order on the stationary and dynamic temperature estimation has been experimentally investigated. The second order estimator has been found to be the optimal choice for application of active thermal control even when an high dynamic response, to protect the system, is needed.

Acknowledgment

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References

[1] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, no. 1, pp. 97–114, 2014.

[2] N. Valentine, D. Das, B. Sood, and M. Pecht, "Failure analyses of modern power semiconductor switching devices," in *International Symposium on Microelectronics*, vol. 2015, pp. 000690–000695, International Microelectronics Assembly and Packaging Society, 2015.

[3] M. Andresen, G. Buticchi, and M. Liserre, "Study of reliability-efficiency tradeoff of active thermal control for power electronic systems," *Microelectronics Reliability*, 2015.

[4] D. Kaczorowski, B. Michalak, and A. Mertens, "A novel thermal management algorithm for improved lifetime and overload capabilities of traction converters," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, pp. 1–10, IEEE, 2015.

[5] M. K. Bakhshizadeh, K. Ma, P. C. Loh, and F. Blaabjerg, "Indirect thermal control for improved reliability of modular multilevel converter by utilizing circulating current," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pp. 2167–2173, IEEE, 2015.

[6] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *Industrial Electronics Magazine, IEEE*, vol. 8, no. 3, pp. 17–27, 2014.

[7] K. Ma, N. He, F. Blaabjerg, M. Andresen, and M. Liserre, "Frequency-domain thermal modelling of power semiconductor devices," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, pp. 2124–2131, IEEE, 2015.

[8] M. Liserre, G. Buticchi, M. Andresen, G. D. Carne, L. F. Costa, and Z. X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, pp. 46–58, Summer 2016.

[9] M. A. Eleffendi and C. M. Johnson, "Application of kalman filter to estimate junction temperature in igbt power modules," *Power Electronics, IEEE Transactions on*, vol. 31, no. 2, pp. 1576–1587, 2016.

[10] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete loss and thermal model of power semiconductors including device rating information," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2556–2569, 2015.

[11] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics reliability*, vol. 42, no. 4, pp. 653–667, 2002.

[12] J.-H. Fabian, S. Hartmann, and A. Hamidi, "Analysis of insulation failure modes in high power igbt modules," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 2, pp. 799–805, IEEE, 2005.

[13] M. Musallam and C. M. Johnson, "An efficient implementation of the rainflow counting algorithm for life consumption estimation," *Reliability, IEEE Transactions on*, vol. 61, no. 4, pp. 978–986, 2012.

[14] K. Ma, N. He, F. Blaabjerg, M. Andresen, and M. Liserre, "Frequency-domain thermal modelling of power semiconductor devices," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2124–2131, Sept 2015.