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Concurrent sub-thermionic and strong thermionic transport in inkjet-printed indium zinc oxide/ silver hybrid-channel field-effect transistors

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Contents

A. Subthreshold slope calculated for different orders of magnitude of drain currents

The subthreshold slope has been calculated for the MIMSFETs with a-IZO processed at different temperatures are calculated and summarized in Table S1. The suffix of SS indicates the order of magnitude of drain currents that has been considered in the calculation. Interestingly, the minimum values are obtained for 350 ºC, with as low as 16 mV/dec. However, as has been discussed in the manuscript, these numbers are related to the printing accuracy or parasitic capacitance and may actually be further lowered with precise printing practices.

Table S1: Subthreshold slope calculated for different orders of magnitude of drain currents for MIMSFET devices processed at different temperatures

Temperature (°C)	**SS (mV/dec)**		
	SS_1	**SS_2**	**SS_3**
300	27.6	38.4	48.4
350	16.2	19.0	23.6
400	20.7	23.9	32.0

B. Comparison of normalized On-currents with literature data

Table S2: Comparison of On-currents ($I_{D,ON}$) of solution-processed oxide FETs in the literature

Semiconductors	**Processing route**	**Process temperature (°C)**	**$I_{D,ON}$ (µA/µm)**	**Year published**
a-ZTO	Spin coating	600	0.7	2009[S1]
Li:ZnO	Spray pyrolysis	350	7.5	2010[S2]
a-ZTO	Spin coating	450	0.1	2013[S3]
In_2O_3	Spin coating	350	0.4	2013[S4]
SnO_2	Spin coating	450	0.4	2014[S5]
ZnO	Spray coating	400	1.3	2014[S6]
In_2O_3	Inkjet printing	400	2	2015[S7]
ZnO	Spray coating	380	2.3	2015[S8]
In_2O_3	Spin coating	250	2.5	2015[S9]
In_2O_3	Inkjet printing	400	2.8	2015[S10]
a-ZTO	Spin coating	500	0.5	2016[S11]
ZnO	Spray coating	400	1	2017[S12]
In_2O_3	Spin coating	250	0.5	2017[S13]
In_2O_3	Spray pyrolysis	300	5	2017[S14]
a-IGZO	Inkjet printing	500	0.4	2018[S14]
In_2O_3	Inkjet printing	400	3	2016[S14]
a-IZO/Ag	**Inkjet printing**	**400**	**195**	present study

C. STEM elemental mapping of a-IZO film at higher magnification

The energy dispersive X-ray spectroscopy (EDX) elemental mapping of printed, annealed (at 400 ºC) a-IZO film has been performed at high resolution; however, the result also demonstrates intermixing of In, Zn atoms at this finer length scale, and fails to provide clear indication of In- or Zn-segregation.

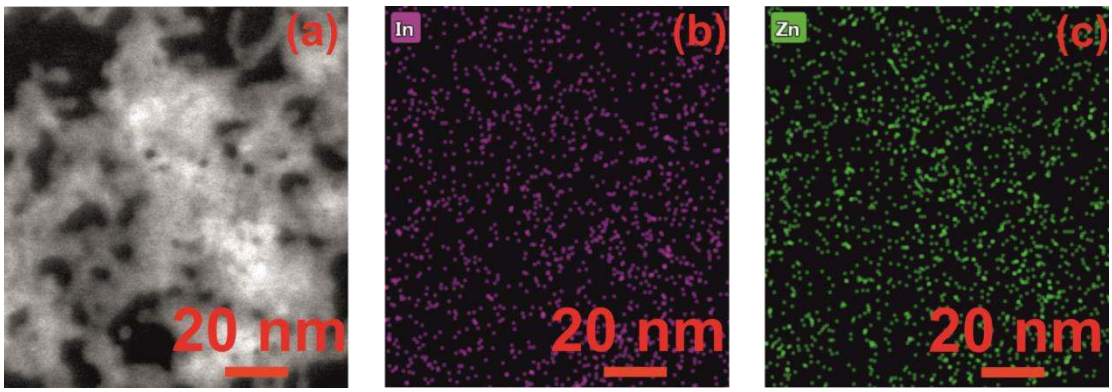

Figure S1. (a) High resolution STEM image taken at a representive area of the printed a-IZO amorphous film. (b-c) STEM elemental mapping of (b) indium and (c) zinc.

D. Additional STEM image of printed a-IZO film

Figure S2 shows STEM image of the a-IZO film, where, alongside the unifor amorphous film morphology, occasional nanocrystals can be seen (bright spots).

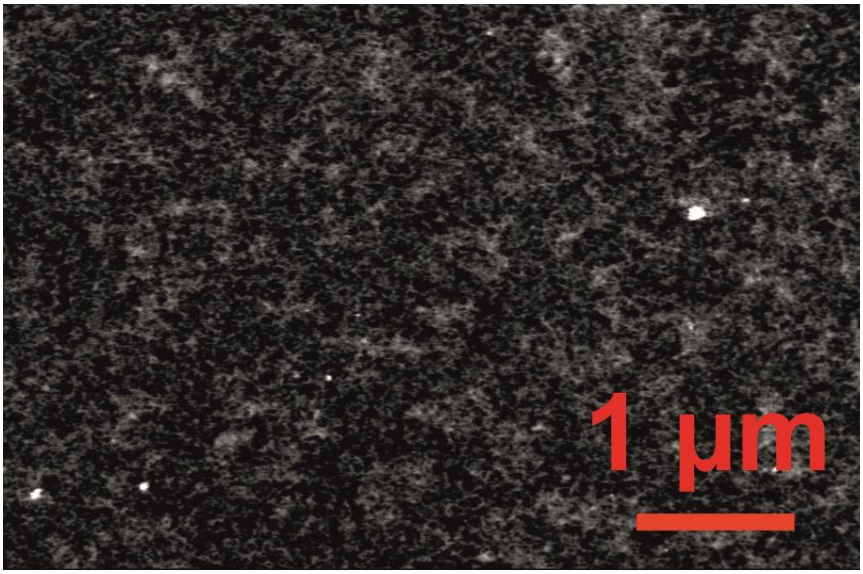

Figure S2 Sacnning transmission electron micrograph shows scatterned nanocrystals in the homogeneous and predominantly amorphous background.

E. Photolithographically patterned in-plane/ displaced gate device architecture

The device structure has been photolithographically patterned using commercially available high quality float glass. An in-plane or displaced gate architecture has been used (as shown) large gate electrode size as compared to the channel dimension that will later be covered with the printed CSPE layer. Identical channel dimensions have been maintained in the entire study, with channel width and length of 60 and 40 μm, respectively.

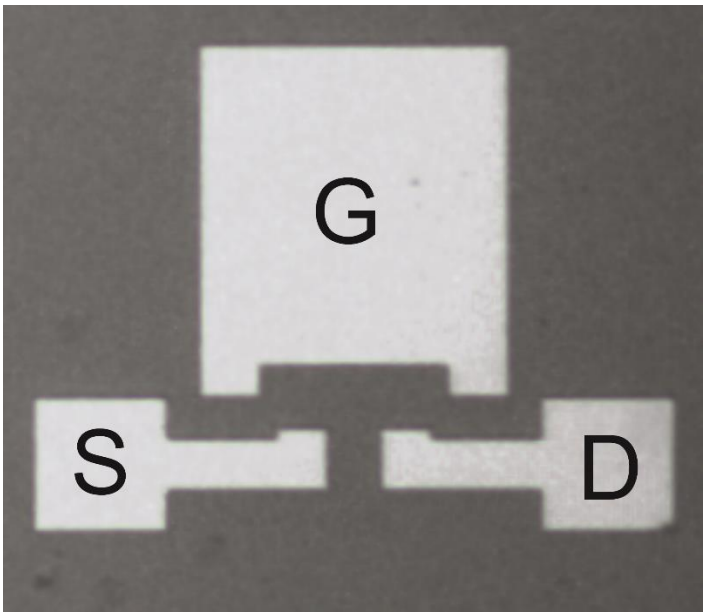

Figure S3: Optical micrograph of the patterned in-plane/ displaced-gate transistor geometry

F. Electrical characterization of inkjet- printed electrolyte gated a-IZO FETs

The IZO devices have been fabricated with the channel length and width of 40 µm and 60 µm, respectively; The electrical characterization of the printed electrolyte gated FETs have been shown in the Figure S4.

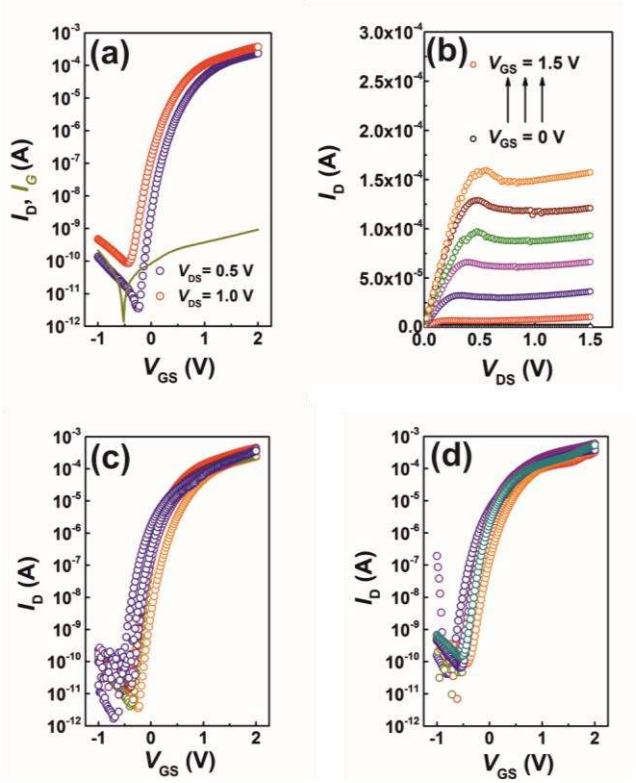

Figure S4: (a) Typical transfer characteristics of inkjet-printed and electrolyte-gated a-IZO channel FET with drain voltage of 0.5 and 1 V, respectively; the dark yellow line denotes the gate current, recorded during the gate voltage sweep for V_{DS}= 0.5 V. (b) The output characteristics of the same device, measured for V_{GS}= 0 to 1.5 V, respectively, with an gate voltage interval of 0.25 V. Estimation on variability of inkjet-printed, a-IZO channel FETs, (c) and (d) depicts the transfer characteristics of 8 devices, measured with drain voltage of 0.5 V and 1 V, respectively.

G. Statistical spread of electrical performance parameters of printed a-IZO FETs showing average $I_{D,ON}$, On-Off ratio, subthreshold swing, field-effect mobility, turn-on and threshold voltage values with standard deviation

The electrical performance parameters have been extracted from different batch of amorphous indium zinc oxide FETs and have been summarized in Figure S5. The statistics shows performance variability observed within different batches (fabricated on different date with new inks and substrates) of printed a-IZO FETs.

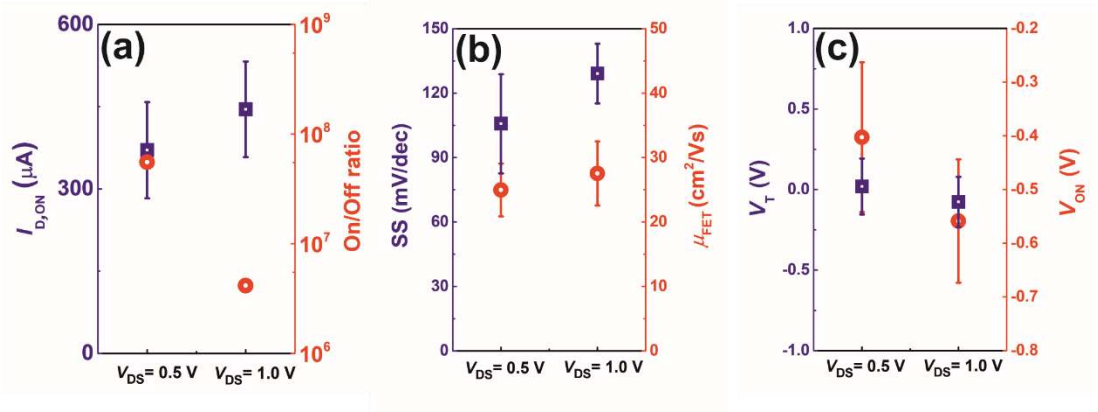

Figure S5: (a-c) Average $I_{D,ON}$, on-off ratio, subthreshold swing, field-effect mobility, turn-on and threshold voltage values with standard deviation, summarized for different batches of a-IZO FETs; the data has been extracted from electrical measurements performed with drive voltages of 0.5 and 1 V, respectively.

H. Estimated average saturation mobility of the IZO channel printed FETs as a function of the applied gate voltages

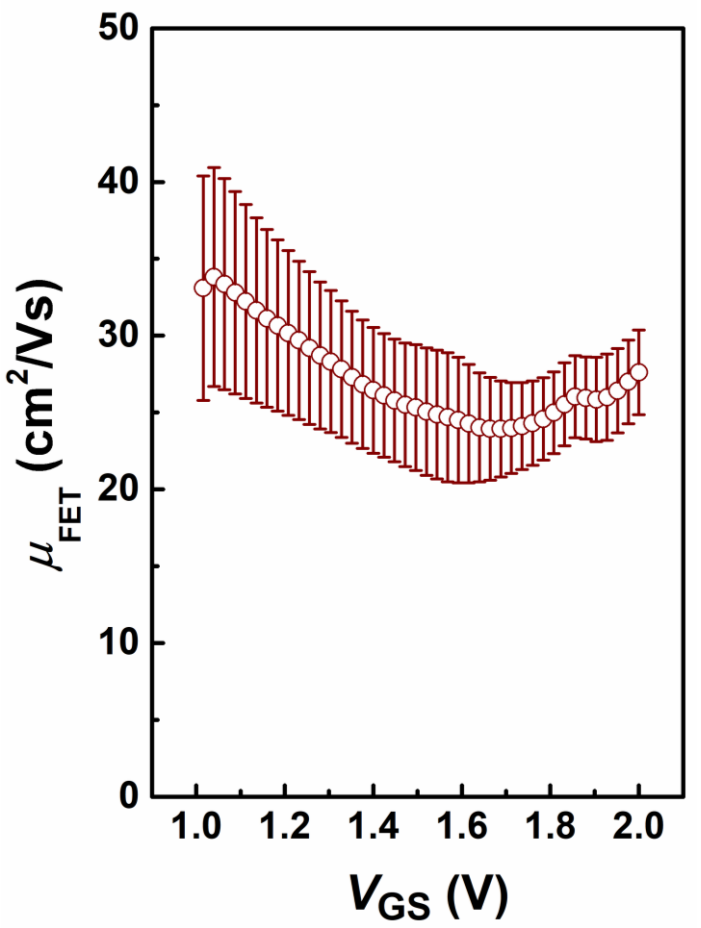

Figure S6. Estimated saturation mobility values calculated using equation (2) for an applied drain voltage of V_D= 1 V, and varied V_{GS} values.

I. Optical micrograph demonstrating step-by-step fabrication of the printed IZO/Ag hybrid channel MIMSFET devices

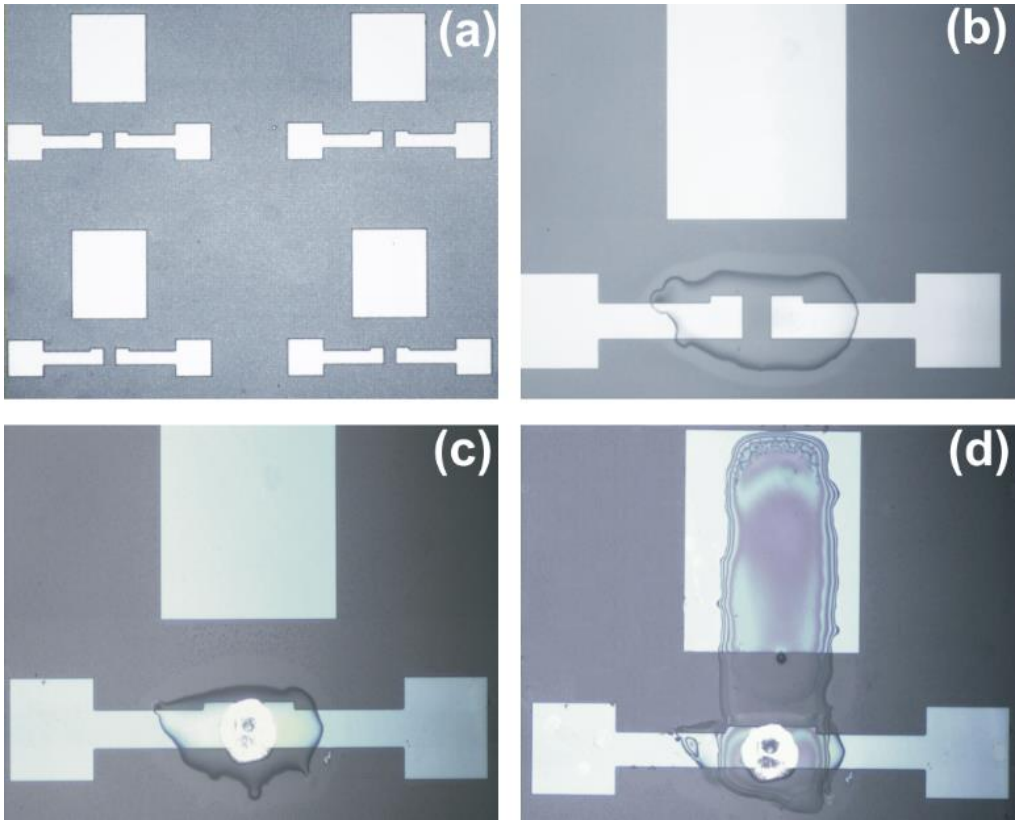

Figure S7: (a) Optical image showing the passive elements (electrodes) of the in-plane or displaced gate device; (b) Printed semiconductor layer (IZO) on the channel area; (c) Printed silver layer on top of the IZO channel; (c) The complete in-plane gate, and electrolyte-gated device with printed CSPE layer covering the entire channel and a large portion of the gate electrode.

J. Schematics of the MIMSFET device that can be represented as two common-gate asymmetric FETs in series

Schematic cross-section view of the MIMSFET devices is shown, which may actually be thought of two common-gate asymmetric FETs in series. The drive electrodes of the devices are ITO/ Ag and Ag/ ITO respectively, the channel length is the height of the a-IZO layer, and the externally applied drive voltage actually splits among the two asymmetric FETs.

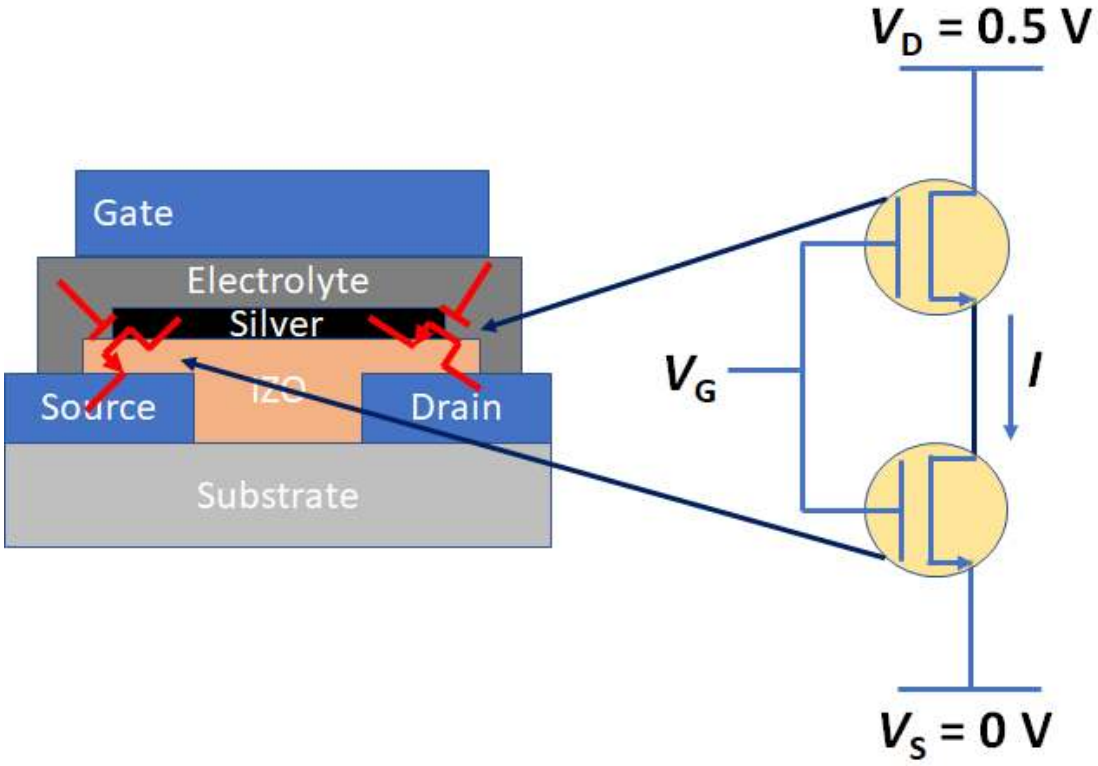

Figure S8: Schematic showing that the MIMSFET device can be represented as two common-gate asymmetric FETs in series

K. Gate voltage-gate current characteristic of the Ag on ITO electrode, without the active semiconducting channel layer

In order to verify the origin of the negative capacitance effect, capacitors have been prepared using printed silver layer and ITO gate as the respective electrodes, without the a-IZO semiconductor channel. Completely identical decreasing current behaviour have been noted for the Ag/ ITO couple at around 1.5 V, V_{GS}, corroborating the fact that the observed NC-effect is associated to a passivation/de-passivation phenomenon at the silver surface. At the next step, a home-made silver nanoparticle dispersion/ ink has been used/ printed to replace the commercial silver nanoink, however, only to obtain an identical result as has been shown in Figure S7. These investigations further validate the fact that the observed NC-effect is related to sudden disappearance and reappearance of capacitance of the printed silver layer which again is an out of an electrolytic passivation/ de-passivation phenomenon.

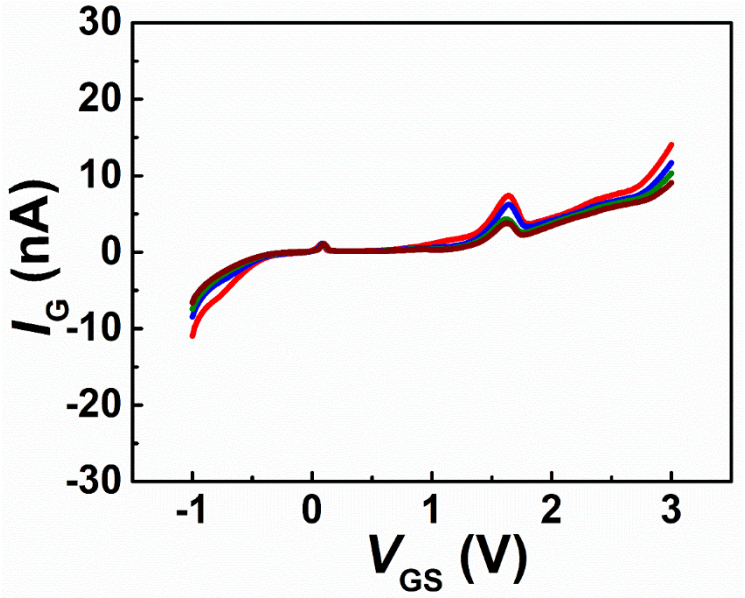

Figure S9: Negative capacitance effect in Ag on ITO electrode without the a-IZO channel layer.

L. Representative double loop transfer and output characteristics of a MIMSFET device, a-IZO film has been annealed at 350 °C

A representative double loop transfer and out characteristics of a MIMSFET device are presented in the Figure S8. The negative capacitance behaviour shown in the forward and reverse sweep of the gate voltage-gate current plot (Figure S8a) is related to the passivation/ de-passivation effect of the printed silver layer, which in turn causes the steep-slope transfer characteristics as observed. The output characteristics recorded by sweeping the drain voltage between 0 to 1 V with varying the gate voltage 0 to 2.5 V at 500 mV interval (Figure S8b).

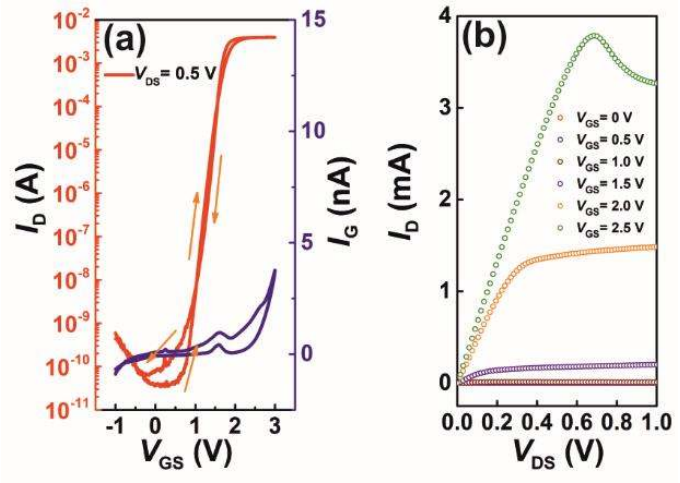

Figure S10: (a) Transfer characteristic of an archetypal MIMSFET device (V_D = 0.5 V); (b) Drain voltage-drain current characteristic of the same device.

M. Comparison plot of maximum On-currents observed for MIMSFETs with a-IZO annealed at different annealing temperatures.

The Maximum On-current observed for the MIMSFET devices with a-IZO annealed at different temperatures, are shown. The device dimensions have been kept constant at *W*/*L*= 60 µm/ 40 µm. The On-current values are noted to be 5.2 mA and 4.7 mA, for 60 µm channel width and V_D= 0.5 V applied voltages. This translates to a channel resistance of 96 Ω and 106 Ω, for the MIMSFETs, where the a-IZO annealed at 400 ºC and 350 °C, respectively.

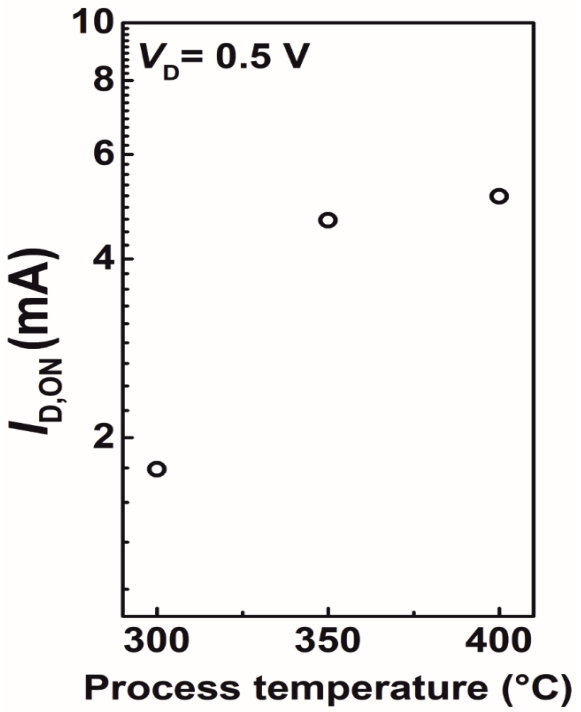

Figure S11: Maximum On-currents observed (with applied drain voltages of V_D= 0.5 V) for MIMSFETs, with the printed a-IZO semiconductor layer having different process temperatures.

N. Comparison plot of transconductance for MIMSFET devices with a-IZO annealed at different temperatures.

The transfer curves and corresponding transconductance have been plotted for MIMSFETs processed at different temperatures. Notably, both for 350 ºC and 400 °C processed FETs, a transconductance values well over 200 µS/µm have been regularly observed.

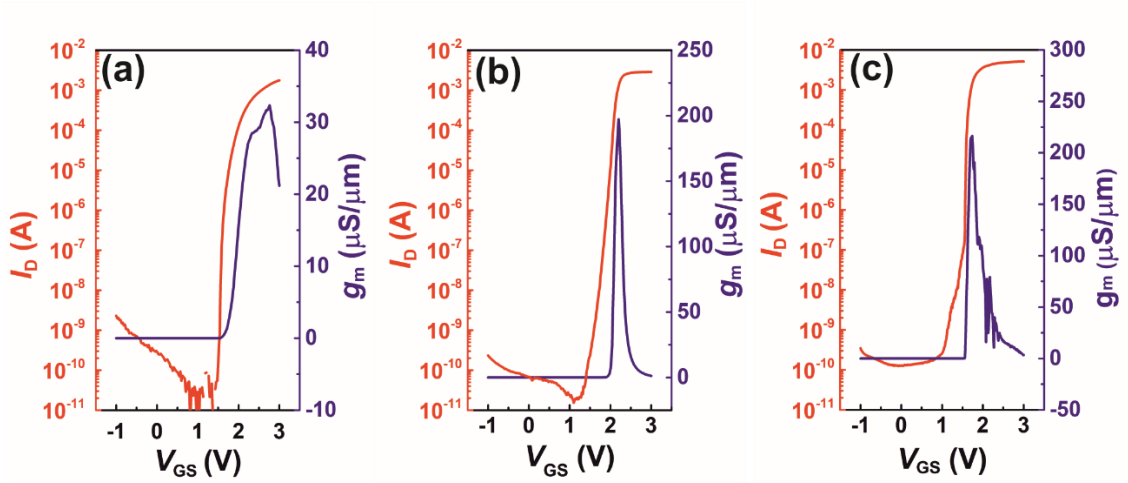

Figure S12: (a-c) Transfer characteristic along with transconductance with respect to applied gate voltages, plotted for MIMSFETs, where, the a-IZO layer annealed at 300, 350 and 400 °C, respectively.

O. MIMSFET devices (annealed at 400 °C) with different film thickness of a-IZO

A nearly thickness independent transport has been observed for the MIMSFET devices. Here, the molar strength of the a-IZO ink and the number of printing passes has been varied in order to obtain a variation in the film thickness. The height profiles of the printed layers have been measured using Dektak XT profilometer. No significant change in the subthermionic transport has been noted, the low Off-current has been maintained, and however a counterintuitive observation can be noted with higher On-currents for the thicker films. Nevertheless, the line profiles (Figure S9b-d) helps to understand the recorded data; the thicker films show maximum thickness at the centre only, which is higher for multi-pass printing. However, it is a continuously decreasing thickness from that peak height and hence the actual vertical distance the carriers need to travel through the a-IZO phase from the ITO electrode to the Ag-layer may remain virtually unchanged.

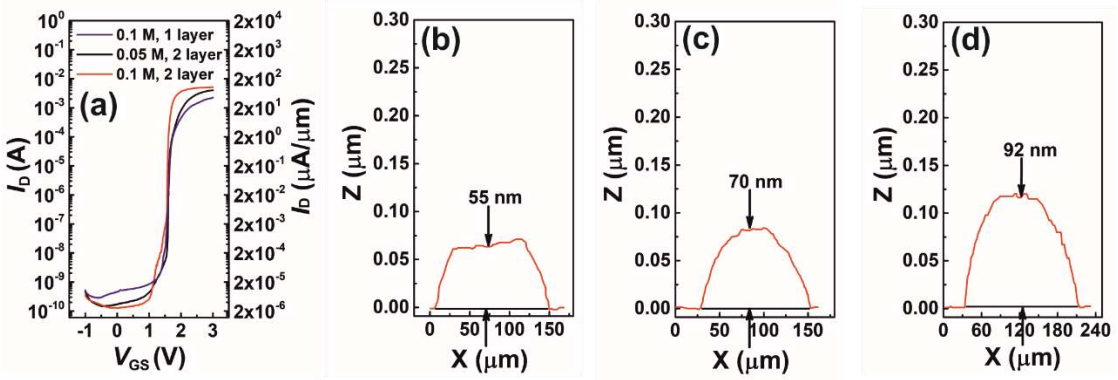

Figure S13: MIMSFET performance with respect to the thickness of the printed channel layer. (a) Comparison of transfer characteristics of MIMSFETs with a-IZO channel having different film thickness; (b-d) Line profile of the printed a-IZO layers, used in the MIMSFETs shown in Figure (a), measured with Dektak profilometer; the film thickness of the single-pass printed 0.1 M precursor (b), double pass printed 0.05 M precursor (c) and double pass printed 0.1 M precursor (d) turns out to be 55, 70 and 92 nm, respectively.

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