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Condition Monitoring of DC-link Electrolytic Capacitor in Back-to-Back Converters Based on Dissipation Factor

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***Abstract*— Condition monitoring systems are used to determine the best timing for predictive maintenance of power electronics converters. These monitoring systems can significantly reduce a converter repair time and increase system availability. In this paper, an investigation has been conducted on the possibility of using the dissipation factor as a lifetime indicator of electrolytic capacitors. A criterion is also proposed based on the dissipation factor to detect electrolytic capacitors end of useful life. A method has been presented for measuring the dc-link capacitor dissipation factor in a back-to-back converter. Using this technique, it is possible to estimate the switching component of the capacitor current by measuring the output currents of the converter without a need to measure the capacitor current directly. The proposed method is simulated, and the impact of various factors such as switching frequency, capacitor series inductor, and the network filter on the accuracy of the dissipation factor measurement are discussed. Experimental results are also provided to validate the acceptable accuracy of the proposed method.**

***Index Terms*—Back-to-back converter, condition monitoring, dc-link capacitor, dissipation factor, electrolytic capacitor, loss angle, predictive maintenance, switching frequency.**

NOMENCLATURE

δ	Loss angle (deg)
φ	Capacitor impedance angle (deg)
X_c	Capacitor reactance (mΩ)
ω	Angular frequency (rad/s)
ESR	Capacitor Equivalent Series Resistance (mΩ)
C	Capacitor capacitance (mF)
ESL	Capacitor Equivalent Series Inductance (μH)
ESR_0	Capacitor ESR initial value (mΩ)
C_0	Capacitor capacitance initial value (mF)
V_e	Electrolyte volume
V_{e0}	Electrolyte initial volume
ρ_e	Electrolyte resistivity (Ω.m)
ε	Dielectric permittivity (F/m)
w_e	Volume of ethylene glycol molecules
j_{eo}	Evaporation rate (mg/min.area)
d_c	Cathode oxide layer thickness
P_E	Correlation factor related to electrolyte spacer porosity and average electrolyte pathway
i_x	Output current pf phase x (A)
i_{inv}	Inverter input current (A)
i_{sw}	Switching harmonic of inverter current (A)
$i_{N,sw}$	Switching harmonic of network current (A)
$i_{C,sw}$	Switching harmonic of capacitor current (A)
$v_{C,sw}$	Switching harmonic of capacitor voltage (V)
ω_s	Switching angular frequency (rad/s)
f_o	Power supply frequency (Hz)
L_{net}	Network equivalent inductance (mH)
R_{net}	Network equivalent resistance (mΩ)
θ_e	Phase difference between i_{sw} and $i_{C,sw}$ (deg)

I. INTRODUCTION

NOWADAYS, power electronic converters have become an indispensable part of many industries. Power electronic equipment is widely used in electrical transportation and vehicles, as well as power transmission and generation systems, home appliances, and other industries. Therefore, maintaining its proper operation is of high priority [1]-[3]. Generally, the reliability of power electronic converters can be improved by 1) utilizing better quality equipment, 2) optimizing the design of the converter structure, and 3) using fault detection and condition monitoring systems. [4]-[5].

The end of useful life (EUL) of a device can be estimated by the degradation indicators measured in the condition monitoring process. Necessary arrangements can be made for predictive maintenance based on the outputs of the condition monitoring system. Using this type of maintenance system, the converter downtime may be reduced and its availability can be increased by repairing or replacing the elements before any failure occurs.

Although, there is a possibility of failure in all the elements of a power converter or its connections, since capacitors and semiconductor switches are the most susceptible devices to failure, their condition is mostly monitored [5]-[7]. Fig. 1 shows the failure rate of a converter due to the failure of its various components [7].

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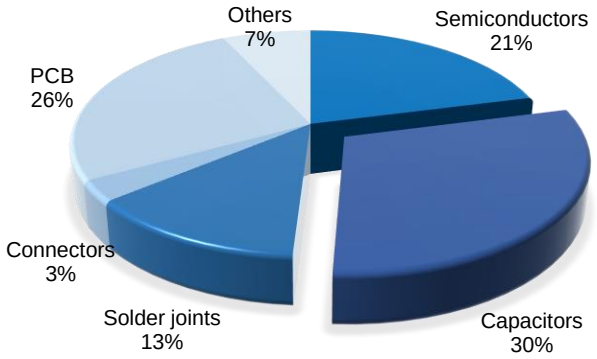

Fig. 1. Distribution of failure for power converter elements [7]

An overview of the applicable methods for monitoring the condition of semiconductors in a power converter is provided in [8]-[9]. Similarly, a thorough evaluation of the existing condition monitoring methods for different types of capacitors including electrolytic capacitors and film capacitors is provided in [10]-[11]. Different lifetime indicators have been proposed to monitor the condition of capacitors some of which are preferred over others depending on the type of the capacitor. For example, film capacitor condition monitoring is usually done by measuring its capacitance. The equivalent series resistance (ESR) cannot be a suitable indicator for this type of capacitor. Fig. 2 classifies the lifetime indicators proposed for capacitors into electrical and non-electrical categories [10]-[11].

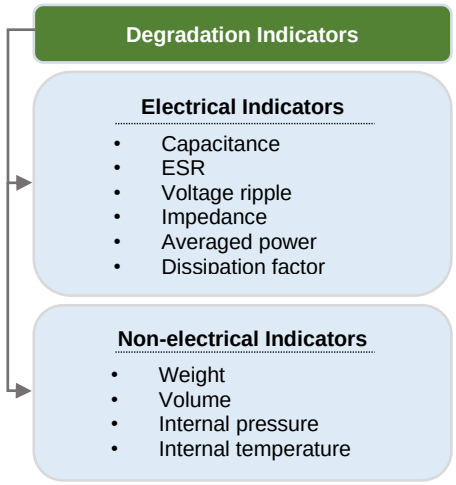

Fig. 2. Capacitor lifetime indicators

As mentioned earlier, the appropriate lifetime indicator for the condition monitoring process must be selected according to the capacitor type. The dominant aging mechanism of different types of capacitors is different. Thermal stress and increase in ambient temperature, as the main factors of aging of Aluminum Electrolytic Capacitors (Al-Caps), cause gradual evaporation of the capacitor electrolyte, resulting in a significant reduction in the capacitance and an increase in the ESR. Therefore, the capacitance and ESR can be good degradation indicators for this type of capacitor [12]. In the case of Metallized Polypropylene Film Capacitors (MPPF-Caps), the predominant aging mechanism is overvoltage stress, which reduces the capacitance of the capacitor and gradually increases its ESR [12]. However, due to the small changes in the ESR, the capacitance of these capacitors is usually preferred as a lifetime indicator. X-ray imaging [13] or optical inspection meters [14] can also be used to detect capacitor aging by analyzing the capacitor physical structure. However, high cost, extra equipment, and the need to separate the capacitor from the converter have made electrical indicators preferred.

Dissipation factor (DF) is another electrical life indicator that can be used to monitor the condition of an electrolytic capacitor. By definition, the Dissipation factor is the ratio of the power dissipated in the ESR to the oscillating reactive power in the capacitor. Reference [11] has mentioned the possibility of using this indicator to monitor the condition of the capacitor, however, due to the difficulty in measuring and determining the level of capacitor degradation, this study does not propose the DF as the best possible indicator to detect the capacitor aging. The amount of DF at the grid frequency, especially in film capacitors, is very small, and therefore at the first glance, it seems complicated to measure.

However, it is possible to define this index at higher frequencies because this factor increases by increasing frequency. On the other hand, it is possible to measure this factor in a simpler way. Representing the electrical parameters as vectors in a complex plane, the dissipation factor is equal to the tangent of the angle between the capacitor impedance vector and the negative reactive axis. This angle, i.e. the loss angle, is the complement of the angle between the capacitor voltage and current vectors (impedance angle). Therefore, by measuring the impedance angle, the amount of the dissipation factor, and consequently the health condition of the capacitor can be estimated. The possibility of measuring the impedance angle by measuring the delay time between the current and the voltage of the capacitor, similar to what [7] has proposed, is one of the advantages of this method.

Time duration can be measured more accurately than electrical parameters. For this reason, many studies have tried to monitor the condition of capacitors by measuring time constants. For example, [15] has estimated the capacitance of a capacitor by measuring the discharge time of the capacitor in a converter supplying motor load. Similarly, [16] has proposed a method to monitor the condition of capacitors in a multi-module converter (MMC), in which the capacitances of the capacitors are calculated by measuring the duration of the capacitors discharge in the bleeding resistors. Reference [17] has used a similar method for this purpose.

In order to measure the phase difference between the capacitor current and voltage vectors, it is necessary to measure the current in addition to the capacitor voltage. In general, two methods are used to find the capacitor current. In the first method, using a series sensor with the capacitor, its current can be measured directly, which of course, requires the additional hardware increasing the costs [18]-[19]. In the second method, based on the converter topology, the capacitor current is calculated according to other measured parameters [20]-[23]. The second method, although seems more complicated, will reduce the price of the monitoring system.

As an example, in [24], a method for monitoring the DC-link capacitor of a three-phase pulse-width modulation rectifier based on ESR measurements is provided. In this technique, a low-frequency current is injected into the capacitor during no-load conditions causing a ripple on the DC-link voltage. It is possible to identify the voltage due to the presence of the ESR by measuring the capacitor voltage at normal conditions and when applying zero vectors. Then, by measuring the input currents and using the rectifier switching pattern, the capacitor current is calculated and the ESR is estimated. To calculate the capacitor current using this method, the rectifier must operate at no-load conditions. The method does not require any extra sensors, and offers the advantage of correcting the ESR based on the temperature.

Reference [25] proposes an offline method to monitor the capacitor condition by measuring the converter output currents. In this method, the capacitor is first charged through a switch. The capacitor is then disconnected from the source and discharged in two stages into a motor load. The capacitance is then calculated by measuring the resonant current and capacitor voltage.

Neural network-based methods have also been proposed to monitor the condition of the DC-link capacitor without a need to measure its current [4], [26]. In these methods, the converter is considered as a black box system, and by measuring the input or output currents of the converter and the capacitor voltage ripple, a neural network is trained whose output is the capacitor capacitance. By incorporating more affecting factors such as input voltage harmonics, temperature, etc. in the training, the neural network will be able to provide more accurate responses under varying operating conditions. However, to obtain more reliable results from the network, the process of data mining and network training must be repeated for each converter. A comprehensive comparison of the state-of-the-art methods applicable to capacitor monitoring is summarized in Table I.

TABLE I
COMPARISON OF THE PRIOR-ART CM TECHNIQUES FOR CAPACITOR

Degradation indicator		Method description	Advantages (+)	Disadvantages (-)	Reported max. error
Non-electrical		[13]: A non-destructive method using X-ray imaging to find cracks in multilayer ceramic capacitors	Non-invasive, finding cacks that cannot be identified by external optical inspection.	Off-line, requires expensive X-ray equipment	-
		[14]: Nondestructive detection and localization of defects in multilayer ceramic chip capacitors using electromechanical resonances	Non-invasive	Off-line, requires expensive optical inspection meters	-
Electrical	C	[15]: Capacitance estimation by discharging the capacitor into a motor inductor at shut-down condition	High accuracy, suitable for both MPPF-Caps and AL-Caps	Off-line, Complex, changes in motor parameters can affect the accuracy	1%
	C	[16]: Capacitance estimation using discharging curve of SM capacitors in connection with parallel bleeding resistors in a multi-module converter	No extra hardware and sensor, low sampling frequency required	Only suitable for multi-module converters	Not reported
	C/ESR	[17]: Capacitance/ESR estimation by measuring the time constants of the capacitor discharge into two different resistors	Saving a current sensor	Extra hardware, can only be processed during shut-down, only suitable for AL-Caps	C: 2.54% ESR: 2.75%
	C/ESR	[18]: Calculating capacitance/ESR by measuring capacitor voltage and current at low/high frequencies	Simplicity, No need for extra sources	Addition of a current sensor in series with the capacitor, requires highly-tuned filters, suitable for AL-Caps	C: 1% ESR: 3%
	C/ESR	[19]: Capacitance estimation by injecting sinusoidal current and calculating the average power	Simplicity	Off-line, Extra hardware and source, low measurement accuracy	C: 4.9% ESR: 3.6%
	C	[20]: Calculation of capacitance by measuring the capacitor voltage and estimating its current based on PV and grid currents	No extra hardware and sensor	High sampling frequency required, only suitable for single-phase H-bridge inverters	2.56%
	C/ESR	[21]: Calculation of capacitance/ESR by measuring the capacitor voltage and estimating its current based on the inductor current in a boost converter	No extra hardware and sensor	Low measurement accuracy, only suitable for boost converters	C: ±5% ESR: ±10%
	C	[22]: Capacitance estimation by measuring the capacitor voltage and BLDCM current during the generation mode.	No extra hardware and sensor	Only can be implemented in BLDC drivers	2%
	C	[23]: Calculation of the capacitance by measuring the capacitor voltage and estimating its current based on PV and grid currents	No extra hardware and sensor, suitable for AL-Caps	Only suitable for 3-phase inverters	2-5%
	ESR	[24]: ESR estimation using the switching frequency harmonics at no load condition	No extra sensors, compensation of temperature effect	Signal injection, extra hardware and filters, suitable for AL-Caps	ESR: 3.2%
	C	[25]: Capacitance estimation by discharging the capacitor into a motor load at shut-down condition	Suitable for both MPPF-Caps and AL-Caps	Off-line, Complex, changes in motor parameters can affect the accuracy	C: 1%
	C	[26]: Training a neural network based on the load current and dc-link voltage ripple of 3-phase AC drive	No extra hardware and sensor	Complex, accuracy depends on the load, all the affecting parameters must be considered for training	C: 2%
	ESR	[27]: ESR calculation by temporarily Short-circuiting one of inverters legs	CM of both Capacitor and IGBTs	Adjustable gate voltage needed for short-circuit test, only suitable for AL-Caps	ESR: 6%

In this study, the second method is used to achieve the capacitor current in a back-to-back converter, and the switching harmonic of the capacitor current is calculated based on the output currents of the converter.

The main contributions of this paper are as follows.

• Measuring the capacitance impedance angle at the switching frequency to minimize the effect of angle measurement error on the angle tangent calculation error.

• Investigating the possibility of using the DF as an indicator for detecting the capacitor EUL and introducing a detection criterion.

• Measuring the capacitor impedance angle at the switching frequency to eliminate the need for a series current sensor.

The paper continues as follows. In Section II, the possibility of using the DF as a degradation indicator of a capacitor is examined and a criterion based on the DF is introduced to detect the capacitors EUL. In Section III, the proposed method for measuring the DF is described in detail. In sections IV and V, the simulation results are presented, and proper operating conditions of the proposed method are discussed. In section VI, the experimental results are presented, and finally, Section VII concludes the paper.

II. Dissipation Factor As A Degradation Indicator

As mentioned in the previous section, the DF expresses the ratio of the energy lost in the ESR to the energy stored in a capacitor. Although this factor is not the preferred indicator for monitoring the condition of the capacitor, the possibility of using it for this purpose has not been ruled out. The amount of energy lost in the ESR of MPPF-Caps is usually much smaller than that in Al-Caps. For this reason, although the use of the ESR as a lifetime indicator of Al-Caps is widely accepted, this indicator is not applicable to monitor the condition of MPPF-Caps [11]. Therefore, the use of the DF as a degradation indicator will be only acceptable for Al-Caps.

The practical capacitor circuit model is usually considered as a set of an ideal capacitor, an ESR, and a series inductor (ESL) [7], [18]. At common operating frequencies of power electronic converters, the effect of the ESL can be neglected, and the model shown in Fig. 3 is usually considered as a simple electrical model of a capacitor. The ESR of Al-Caps consists of three components as:

$$ESR = R_o + R_e + R_d, \tag{1}$$

which 'R_o' indicates the ohmic resistance of the aluminum plates and terminals, and 'R_e' is the electrolyte resistance which depends on the number and mobility of carriers. As the temperature rises, the mobility of the carriers increases and 'R_e' decreases [7]. On the other hand, over time, high temperature causes the electrolyte to evaporate and increases its resistance as the number of carriers decreases. Evaporation of the electrolyte, even in an unused capacitor may end the useful life of Al-caps [12]. 'R_d' represents the dielectric frequency dependent losses that occur if the dielectric is exposed to a variable electric field. Therefore, the ESR of an Al-Cap depends on the temperature and frequency, and this must be taken seriously in order to accurately measure the degradation indicator.

The DF, based on definition, is equal to the tangent of the angle between the capacitor impedance vector and the negative reactive axis (Fig. 3), which is also called the loss angle (δ), which is the complement of the capacitor impedance angle (φ). Therefore, if the capacitor impedance angle is measured, the DF is also known. The relationship between the DF and the capacitance and ESR of the capacitor is given in (2) and (3).

$$DF = tan(\delta) = \frac{Energy\ Dissipated/cycle}{Energe\ stored/cycle} \tag{2}$$

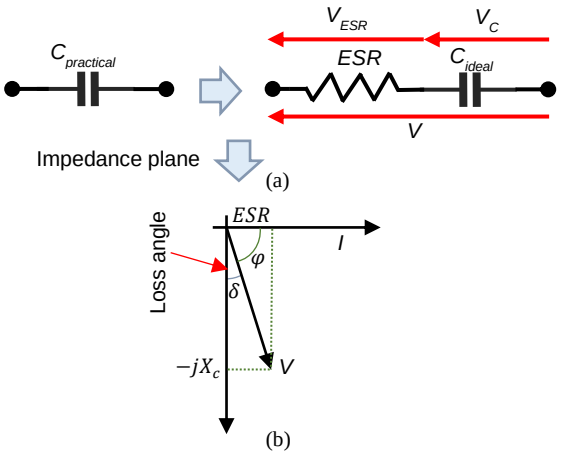

Fig. 3. Capacitor (a) equivalent circuit, and (b) V/I phasor diagram

$$DF = \frac{ESR.i^2}{X_c.i^2} = ESR.C\omega \tag{3}$$

The relationships between the DF and the capacitor impedance angle can be expressed as:

$$\varphi = tan^{-1}\left(\frac{X_c}{ESR}\right) = \frac{\pi}{2} - tan^{-1}(DF) \tag{4}$$

What is important about using the DF as a degradation indicator is to determine a criterion for detecting the capacitor EUL. At the first glance, this criterion is available based on the criteria set for the capacitance and ESR of Al-Caps. Equation (5) shows the ratio of the DF at each instant to its initial value based on the capacitance and ESR of the capacitor.

$$\frac{DF}{DF_0} = \frac{ESR.C.\omega}{ESR_0.C_0.\omega} = \frac{ESR}{ESR_0} \times \frac{C}{C_0} \tag{5}$$

Since different criteria for capacitance and ESR changes during a capacitor useful life have been reported, DF changes criterion has been determined by summarizing the results of various studies and laboratory data.

According to [7], [12], and [27], the capacitance of Al-Caps, as following, is directly related to the volume of the electrolyte, and its ESR, according to (6), is inversely related to the square of the electrolyte volume.

$$\frac{C}{C_0} = \frac{V_e}{V_{e0}} \tag{6}$$

$$\frac{ESR}{ESR_0} = \left(\frac{V_{e0}}{V_e}\right)^2 \tag{7}$$

By Substituting (6) and (7) in (5), the DF changes can be obtained based on the electrolyte volume as:

$$\frac{DF}{DF_0} = \frac{ESR}{ESR_0} \times \frac{C}{C_0} = \frac{V_e}{V_{e0}} \times \left(\frac{V_{e0}}{V_e}\right)^2 = \frac{V_{e0}}{V_e} \tag{8}$$

According to (8), the DF during the life of a capacitor varies inversely with the volume of the electrolyte. However, since the electrolyte resistance according to (1) is only one of the three components of the ESR, (7) does not seem to be entirely accurate, and the ESR probably increases at a faster rate than predicted in (7) over the life of the capacitor.

Reference [28] also, by analyzing the capacitor geometry, presents the capacitance and ESR of the capacitor as a function of the electrolyte volume (Equations (9) and (10)).

$$C(t) = \left[\frac{2\varepsilon}{d_c}\right]\left[\frac{V_e(t)}{j_{eo} t w_e}\right] \tag{9}$$

$$ESR(t) = \left[\frac{\rho_e d_c P_E}{2}\right]\left[\frac{j_{eo} t w_e}{V_e(t)}\right] \tag{10}$$

In these models, t is the aging time.

Based on the model presented in (9) and (10), DF can be obtained as:

$$DF(t) = \omega C(t) ESR(t) = \omega \varepsilon \rho_e P_E \tag{11}$$

According to (11), the DF apparently remains constant with the change in electrolyte volume, but due to the increase in the temperature, the correlation factor 'P_E' increases as the average pathway of the liquid decreases, and therefore, an increase in the DF is also expected.

For a more accurate assessment, the capacitance and ESR parameters of 18 electrolytic capacitors have been measured in the laboratory. The capacitors understudy had a nominal capacitance of 560μF and a nominal voltage of 35 volts. In this test, the capacitors were exposed to an average voltage of 35V for about 2,500 hours with a current ripple of 1.4 amp at 100 Hz and an environment stress at the temperature of 105 °C. The device used to measure the capacitor parameters was of 'Aglinet E4980' type. The results of the measurements are shown in Fig. 4. To better evaluate the changes of the capacitance, ESR, and DF, the measured values are normalized with respect to their initial values. Fig. 4 shows that the DF clearly increases as a capacitor gets older.

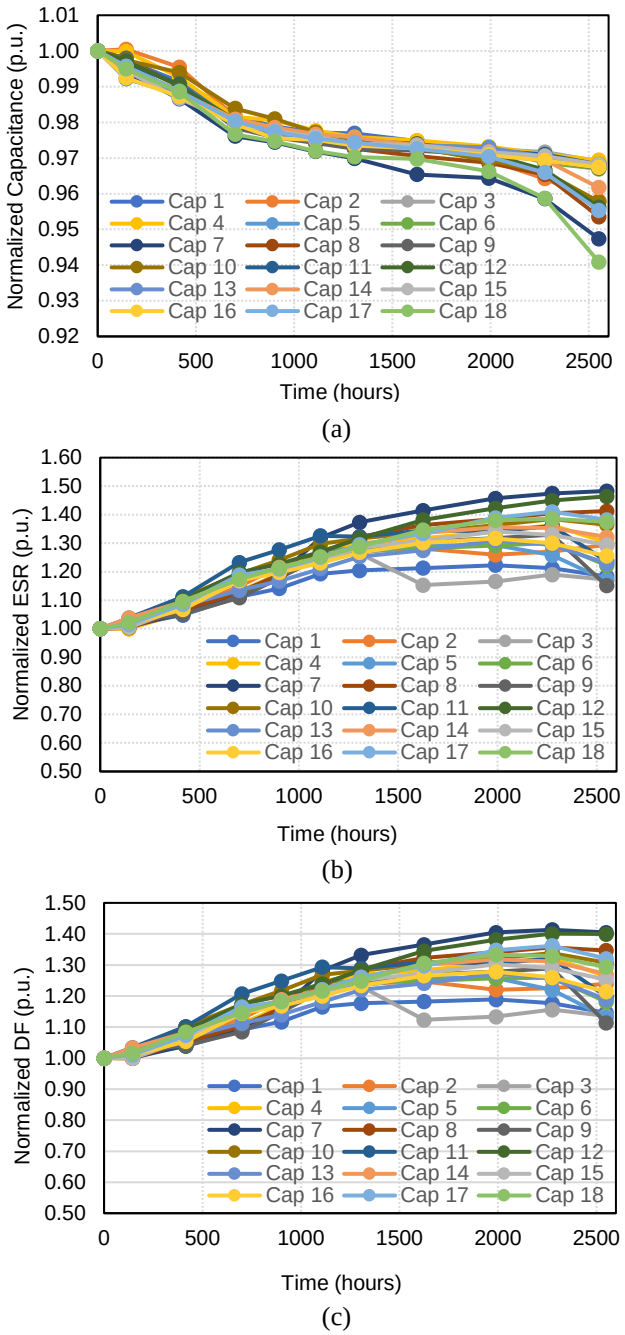

Fig. 4. Impact of capacitor aging on the normalized values of the (a) capacitance, (b) ESR, and (c) DF

The average values of the measured parameters of all capacitors are calculated and shown in Fig. 5. According to the data shown in this figure, after 2000 hours of testing, the average capacitance of the capacitors decreased by about 4%, and the average ESR increased by about 35%. If the amount of change in electrolyte volume based on (6) is considered to be equal to the change in the capacitor capacitance, the ESR increase is much greater than the expected value according to (7).

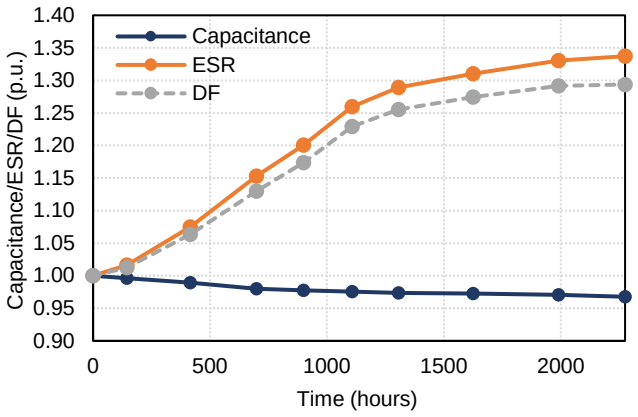

Fig. 5. Impact of aging on the Al-Caps capacitance, ESR, and DF

According to the results of the experimental test, the change in the DF is similar to but less than the ESR. To obtain a criterion for detecting the capacitor EUL based on the DF, the criteria that currently exist for the capacitor capacitance and ESR can be used. Given that the existing criteria for the capacitance and ESR occur simultaneously at the EUL, it will be possible to define a new criterion based on the DF and (5). Most studies cite an increase in the ESR of more than twice the initial value and a decrease in capacitance of more than 20% as indicators for determining the capacitor EUL [11]. In such a case a more than 60% increase in the DF with respect to its initial value can be considered as a criterion for determining the Al-Caps EUL.

III. Proposed Method To Measure the DF

The loss angle is the complement of the capacitor impedance angle. Therefore, if one considers an increase of more than 60% in the $tg(\delta)$ as a criterion for a capacitor EUL, then a decrease of more than 40% in the tangent of the capacitor impedance angle can also be another criterion to detect the capacitor EUL based on (12).

$$if\ \frac{DF}{DF_0} = \frac{tan(\delta)}{tan(\delta_0)} = \frac{tan(\varphi_0)}{tan(\varphi)} > 1.6 \rightarrow \frac{tan(\varphi)}{tan(\varphi_0)} < 0.6 \tag{12}$$

To measure the capacitor impedance angle, it is necessary to extract a specific frequency component from the capacitor current and voltage and measure the delay between them. In order to eliminate the need for a series current sensor with the capacitor, and accurately measure the DP, a method is proposed to calculate the switching frequency harmonic of the capacitor current from the converter output currents.

At low frequencies, the capacitor impedance angle is very close to 90 degrees and the loss angle is very close to zero. In such cases, a small amount of angle measurement error leads to an unacceptable amount of error in the angle tangent. However, as the measurement frequency increases, the impedance angle becomes smaller and the loss angle becomes larger. As these angles approach 45 degrees, the influence of the angle measurement error on the angle tangent error is minimized.

In most studies on capacitor condition monitoring, current measurement is performed using a series current sensor with the capacitor regardless of the converter topology. It is usually possible to apply these methods to monitor capacitor condition in converters with different structures. However, adding a current sensor will increase the final cost of the condition monitoring system. In another group of studies, the capacitor current is calculated using the currents measured in the converter.

In the proposed method of this paper, the input current of the inverter in a back-to-back converter is calculated based on the output phase currents and the inverter switching pattern at each instant as:

$$i_{inv} = S_a i_a + S_b i_b + S_c i_c \tag{13}$$

In (13), if the upper switch in phase *x* is conducting, S_x will be 1 and otherwise 0. As the output currents are typically measured for control purposes, there is no need to add extra sensors.

According to what is shown in Fig. 6, the calculated current is passed through a band-pass filter (Fourier transform) to extract the switching frequency harmonic of the inverter input current. In order to extract the switching component from the directly measured DC-link voltage, a high-pass filter with a low cut-off frequency is used initially to eliminate the DC component, and a band-pass filter similar to the previous one is then applied. The most challenging aspect of implementing the proposed method in real-time is the design of the filters that extract the switching components of the inverter current and capacitor voltage. Filters must be designed such that at the switching frequency, they either cause no phase shifts or cause equal phase shifts in the switching components of the capacitor voltage and inverter current.

Since the phase difference between the capacitor current and voltage must be measured to find the capacitor impedance angle, it is necessary to find a relationship between the capacitor current and the inverter input current. The converter equivalent circuit at the switching frequency is shown in Fig. 6. Based on this equivalent circuit, the switching components of the capacitor current ($I_{C,sw}$) and network current ($I_{N,sw}$) can be found using (14) and (15).

$$I_{C,sw} = \frac{R_{eq} + jL_{eq}\omega_s}{\left(R_{eq} + ESR\right) + j\left(L_{eq}\omega_s - \frac{1}{C\omega_s}\right)} I_{sw} \tag{14}$$

$$I_{N,sw} = \frac{ESR - \frac{j}{C\omega_s}}{\left(R_{eq} + ESR\right) + j\left(L_{eq}\omega_s - \frac{1}{C\omega_s}\right)} I_{sw} \tag{15}$$

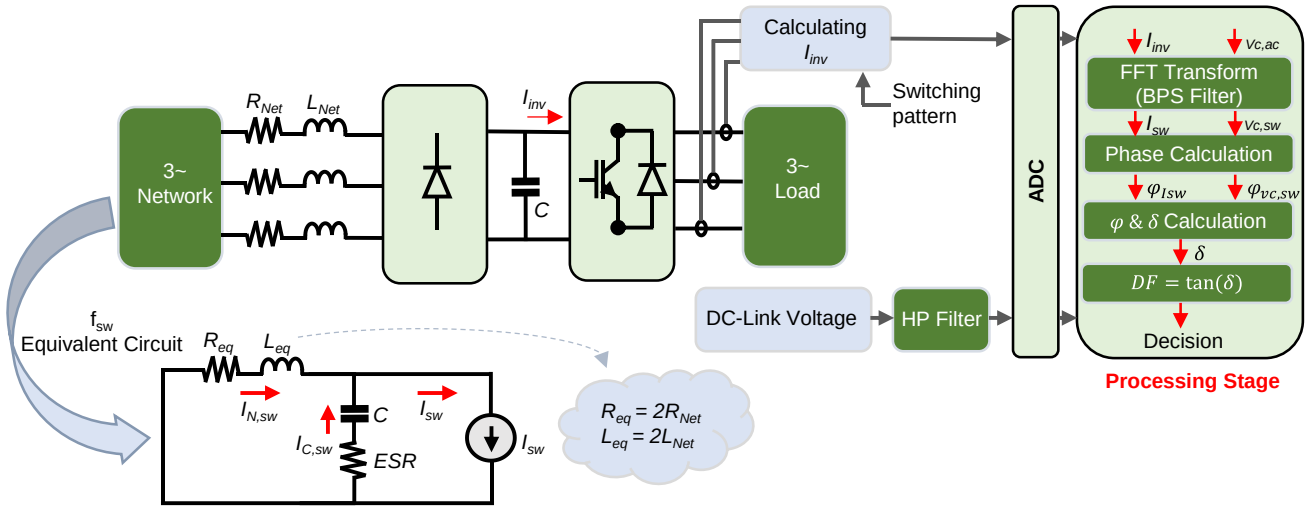

Fig. 6. Proposed measurement method and the converter switching frequency equivalent circuit

According to (15), network equivalent inductors cause the supply share of the switching current to decrease sharply as the frequency increases. Therefore, a small amount of the inverter switching current is injected into the network. Even if the network equivalent inductors are small, series inductors with the converter inputs are usually used as filters to completely mitigate the high-frequency components [29]. Therefore, if the switching harmonic is properly removed from the network current, the switching component of the capacitor current can be assumed to be somewhat equal to the switching harmonic of the inverter input current. In this case, by calculating the capacitor current and measuring its voltage directly, it is possible to measure the time delay between the switching components of the capacitor current and voltage and calculate the impedance angle. By measuring the capacitor impedance angle, it will be possible to monitor its condition based on (12). If the converter input voltage contains a switching component, the equivalent circuit in Fig. 6 will no longer be valid. In such a case, the proposed method cannot be applied due to the inequality of the inverter and capacitor currents switching components. However, such a high-frequency transient is very unlikely to occur in the input voltage and coincide with the monitoring test.

IV. Numerical Analysis

As already discussed, there are factors that cause errors in the measurement results of the proposed system. For example, the capacitor ESL can affect the measurements and cause the aging to not have the expected effects on the capacitor impedance angle. Furthermore, changing the switching frequency affects the changes in the impedance angle during the capacitor life, and therefore, it seems that this must be considered in choosing the timer with appropriate measurement accuracy. In addition, if the switching component of the supply current is not effectively blocked, the switching harmonic of the capacitor and inverter currents will not be equal, and the measurement error of the impedance angle may not be acceptable.

Film capacitors, on the other hand, are commonly used in parallel with electrolytic capacitors to improve their poor high-frequency performance. The capacitance of the parallel film capacitor is set to be much lower than that of the electrolytic capacitor. Thus, at frequencies smaller than the electrolytic capacitor cut-off frequency, the impedance of the film capacitor is much higher than that of the electrolytic capacitor, and its effect on the impedance angle can be neglected. In this study, the impedance angle is measured at the switching frequency, which is always smaller than the electrolytic capacitor cut-off frequency. Therefore, the presence of a film capacitor will not affect the efficiency of the proposed method.

In the following, the effects of the aforementioned factors are discussed through calculation or simulation to determine the optimal operating conditions of the monitoring system.

A. *Impact of capacitor ESL on the monitoring system*

The cut-off frequency of the electrolytic capacitors is in the order of a few tens of kHz. Thus, there is a possibility that the ESL will affect the capacitor impedance angle at switching frequencies. Increasing the switching frequency to about the capacitor cut-off frequency causes the impedance angle to decrease drastically. Furthermore, since only the effect of the ESR and capacitance is considered in determining the capacitor EUL criterion based on the DF, the switching frequency must be selected such that the effect of the ESL at that frequency can be completely ignored. To investigate this, the characteristics of an electrolytic capacitor based on its manufacturer datasheet are used according to Table II [30]. Capacitor impedance angles are calculated with and without considering the ESL based on the specifications of Table II. Then, by decreasing the capacitance by 20% and increasing the capacitor ESR by 100%, the possible values of the impedance angle at the end of the capacitor useful life are calculated to determine the ESL effect on the system error by comparing the impedance angles at the beginning and end of the capacitor useful life (Table III).

TABLE II
Specification of the Electrolytic Capacitor

Manufacture Part No.	Capacitance (mF)	Max. ESR 25 °C, 10kHz (mΩ)	Cut-off Freq. (kHz)
Cornell Dubilier 500R112M500BC2B	1.1	108.8	10

In Table III, 'φ_1' is the impedance angle of the capacitor at the beginning of its life, and 'φ_2' is the estimated impedance angle of the capacitor at the end of its useful life. In this table, the errors are calculated by comparing the ratio of the impedance angles tangent at the beginning and end of the capacitor useful life in the presence of the ESL with the expected ratio without it. According to the data presented in Table III, by increasing the switching frequency, the amount of the error caused by the ESL increases. However, since the switching frequency is usually not higher than 4 kHz to prevent the increase of switching losses, this error is limited to a maximum of 2.5%.

TABLE III
ANALYSIS OF THE ESL EFFECT ON THE CAPACITOR IMPEDANCE ANGLE

Switching Freq. (kHz)	With ESL			Without ESL			Er. (%)
	φ_1 (deg)	φ_2 (deg)	$\frac{tan(\varphi_2)}{tan(\varphi_1)}$	φ_1 (deg)	φ_2 (deg)	$\frac{tan(\varphi_2)}{tan(\varphi_1)}$	
1	52.7	39.0	0.626	52.7	39.5	0.625	0.13
2	32.1	21.8	0.630	33.2	22.3	0.625	0.52
3	21.8	14.3	0.637	23.5	15.5	0.625	1.23
4	15.5	10.3	0.649	18.3	11.5	0.625	2.38
5	10.9	7.4	0.667	14.9	9.2	0.625	4.16

B. *Impact of switching frequency on the accuracy of the monitoring system*

As the switching frequency increases, the DF and the loss angle increase according to (3). But on the other hand, as the switching period decreases, the measured time difference between the capacitor voltage and current vectors decreases. To measure this delay more accurate timers are needed. To investigate the effect of switching frequency on the measured time duration and required timer accuracy, the impedance angles for the capacitor of Table II, at the beginning and end of its useful life are calculated and the results are presented in Table IV. Similar to the previous section, a 100% increase in the ESR and a 20% decrease in the capacitance are considered as limit changes at the end of capacitor useful life. The ESL effect is neglected in this analysis.

TABLE IV
ANALYSIS OF THE SWITCHING FREQUENCY EFFECT ON THE ACCURACY OF TIME DIFFERENCE MEASUREMENT

Switching Freq. (kHz)	δ_1 (deg)	δ_2 (deg)	φ_1 (deg)	φ_2 (deg)	t_1 (µs)	t_2 (µs)	Δt (µs)
1	37.2	50.4	52.76	39.42	146	109	37.0
2	56.7	67.6	33.33	22.34	46.3	31.0	15.2
3	66.5	74.5	23.67	15.32	21.9	14.2	7.73
4	71.6	78.5	18.20	11.61	12.6	8.06	4.57
5	75.1	80.8	14.74	9.33	8.19	5.19	3.00

In Table IV, 't_1' and 't_2' are the time differences between the switching components of the capacitor voltage and current at the beginning and end of its useful life. According to the data in Table IV, although δ has increased significantly with increasing the switching frequency, but decreasing the switching period causes the absolute values of t_1 and t_2 to decrease significantly. Δt also shows the changes of t_2 compared to t_1 during the life of the capacitor, and according to the data in the table, the value of Δt has also decreased with increasing the switching frequency. Therefore, it seems that if a timer with the same sensitivity is used, the capacitor condition can be monitored with better accuracy at lower frequencies.

C. *Impact of line filters on the accuracy of the proposed method*

Since in the proposed method, the switching components of the inverter current and the capacitor current are considered equal, the practical phase difference between these two currents is of special importance in the accuracy of the capacitor impedance angle measurement. Based on (14) and ignoring the network resistance, the phase difference between the switching components of the inverter current and the capacitor current (θ_e) can be calculated as:

$$\theta_e = \frac{\pi}{2} - tan^{-1}\left(\frac{L_{eq}\omega_s - \frac{1}{C\omega_s}}{ESR}\right) \quad (16)$$

Similar to the previous section, considering $L_{Net} = 3.6\,mH$, for the capacitor with the specifications given in Table II, the values of θ_e and the resulting error in estimating φ for different switching frequencies are calculated and the results are summarized in Table V.

TABLE V
ANALYSIS OF LINE FILTER EFFECT ON THE CAPACITOR IMPEDANCE ANGLE MEASUREMENT ACCURACY

Switching Freq. (kHz)	Expected φ (deg)	Expected θ_e (deg)	Er. (%)
1	52.76	0.140	0.265
2	33.33	0.070	0.209
3	23.67	0.046	0.196
4	18.20	0.035	0.191
5	14.74	0.028	0.189

According to the data in Table V, for all studied switching frequencies, the impedance angle measurement error is always below 0.26%, which is negligible. Of course, this was predictable because line filters specifications are usually chosen to completely eliminate network current switching harmonics.

V. SIMULATION RESULTS

This section presents the results of the simulations performed for a back-to-back converter with the specifications of Table VI. The simulations are performed taking into account all the influencing factors, including the line filters and the capacitor ESL. MATLAB Simulink® is used for the simulations, and the solver is selected automatically by the software. In Table VII, the errors are calculated by comparing the ratio of the impedance angles tangent at the beginning and end of the capacitor useful life obtained by simulation with the expected ratio by calculation.

TABLE VI
SIMULATED BACK-TO-BACK CONVERTER SPECIFICATIONS

Parameter	Value
Rectifier type	Diode based
System rated apparent power	4 kVA
Nominal line voltage	380 V
Main grid frequency	50 Hz
Line filter inductance	3.6 mH

TABLE VII
COMPARISON OF THE SIMULATION RESULTS AND THE EXPECTED VALUES OF THE CAPACITOR IMPEDANCE ANGLE

Switching Freq. (kHz)	Expected values based on calculation					Simulation results					Er. (%)
	t_1 (µs)	t_2 (µs)	φ_1 (deg)	φ_2 (deg)	$\frac{tan(\varphi_2)}{tan(\varphi_1)}$	t_1 (µs)	t_2 (µs)	φ_1 (deg)	φ_2 (deg)	$\frac{tan(\varphi_2)}{tan(\varphi_1)}$	
1	146.55	109.51	52.8	39.4	0.625	148.01	110.61	53.3	39.8	0.622	0.32
2	46.29	31.04	33.3	22.3	0.625	46.60	31.83	33.6	22.9	0.637	1.25
3	21.92	14.19	23.7	15.3	0.625	21.94	14.98	23.7	16.2	0.661	3.60
4	12.64	8.07	18.2	11.6	0.625	12.36	8.57	17.8	12.3	0.682	5.67
5	8.19	5.19	14.7	9.3	0.625	7.75	5.64	13.9	10.1	0.721	9.60

Similar to the previous sections, first for the capacitor with the characteristics of Table II, the impedance angle is calculated by measuring the time difference between the switching frequency components of the DC-link voltage and the inverter current as shown in Fig. 7.

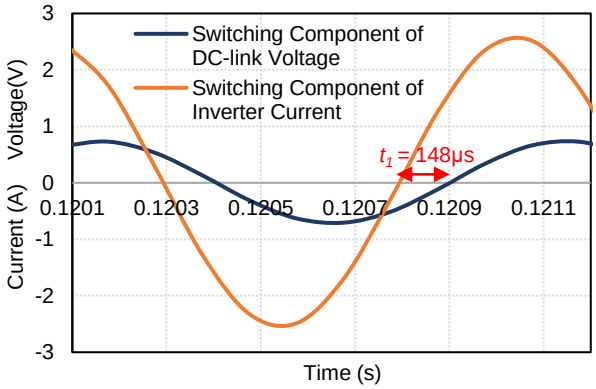

Fig. 7. Measurement of the impedance angle

With a 20% decrease in the capacitance and a 100% increase in the ESR, the capacitor impedance angle at the end of its useful life is calculated and the results are presented in Table VII. In this table 't_1' and 't_2' are the time differences between the switching components of the capacitor voltage and the inverter current at the beginning and end of the capacitor useful life, and 'φ_1' and 'φ_2' are the calculated impedance angles. The expected values are calculated without considering the ESL or the line filters. Based on the simulations results, by increasing the switching frequency, the effect of the ESL sharply increases worsening the estimated error. Therefore, to eliminate the effect of the ESL, the switching frequency should be selected one decade lower than the capacitor cut-off frequency.

VI. EXPERIMENTAL RESULTS

As a testbed for the proposed method, a diode bridge front-end back-to-back converter with the specifications listed in Table VIII is used. To reduce the number of current sensors, the inverter input current (i_{inv}) is measured directly. However, in industrial-scale converters, because output phase currents are typically measured, the inverter current can be calculated.

Fig. 8 depicts the laboratory setup for the experiments. In order to determine how the switching frequency affects the measurement error, the harmonic spectrums of the inverter input current (i_{inv}) and capacitor current (i_C) are measured and compared. The results are summarized in Fig. 9. In this figure, the continuous line and the dashed line represent the frequency spectrums of the inverter input current and capacitor current,

TABLE VIII
BACK-TO-BACK CONVERTER SPECIFICATIONS

Parameter	Value
Rectifier type	Diode based
System rated apparent power	1.2 kVA
Nominal input line voltage/frequency	190 V/50 Hz
Nominal DC-link voltage	260 V
DC-link capacitor capacitance/ESR	235 µF/200 mΩ
Line filter inductance	3.377 mH
Processing unit	STM32H743ZI2
Current sensor	LA55-p

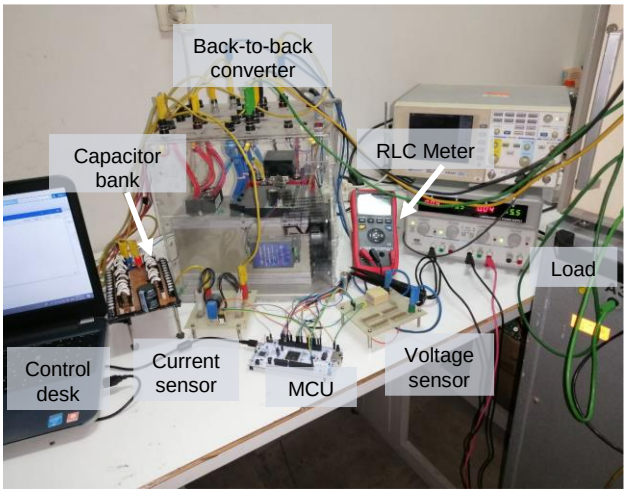

Fig. 8. The experimental setup

respectively. The phase difference between the switching components of these currents, which directly affects the final measurement accuracy, is also measured and shown in the figure. In order to measure the frequency spectrum, an array of 1000 samples is collected at 100 kHz and transmitted via UART to the computer. To minimize the measurement error, a data average is calculated from the results after the measurements are repeated 20 times with 5-second intervals.

As the results show, the switching components of the inverter and the capacitor currents have the same amplitude and the phase difference between these two components is 1.021 degrees at the switching frequency of 1 kHz and drops to 0.023 degrees with increasing the switching frequency up to 5 kHz. Of course, this was predictable based on (16). However, since this phase difference does not change significantly during the lifetime of the capacitor, it will not have a significant impact on the efficiency of the proposed method at any of the studied frequencies. Therefore, the switching frequency for subsequent measurements has been set at 1 kHz in order to eliminate the effect of the ESL.

In the second part of the experiments, the phase difference between the switching components of the DC-link voltage and the inverter input current is measured based on the proposed method for different capacitors. To measure the DC-link voltage, a high-pass active filter with a very low cut-off frequency is used to eliminate the DC component while causing no phase shift at the switching frequency. High-pass filtering is implemented using a first-order active filter with an 8.8 Hz cut-off frequency, and the Fourier transformation is employed to extract the switching components of signals as a band-pass filter. Hardware filters can also be used, but the resulting phase shifts need to be well compensated.

Different capacitances are created by placing different numbers of similar 10 microfarad capacitors in parallel and connecting resistors of 0.1, 0.22, and 0.34 ohm in series. For each set, the capacitance and series resistance are measured by an RLC meter and the expected load angle is calculated. Then, the impedance angle is measured based on the proposed method by measuring the time difference between the switching components of the capacitor voltage and the inverter input current, and the results are compared in Table IX.

In Table IX, the parameters marked with the '*RLCm*' subscript are measured by an RLC meter and those with '*m*' subscript are measured or calculated based on the proposed method. The maximum measurement error of the proposed method is 5.6%, as shown in the last column of the table.

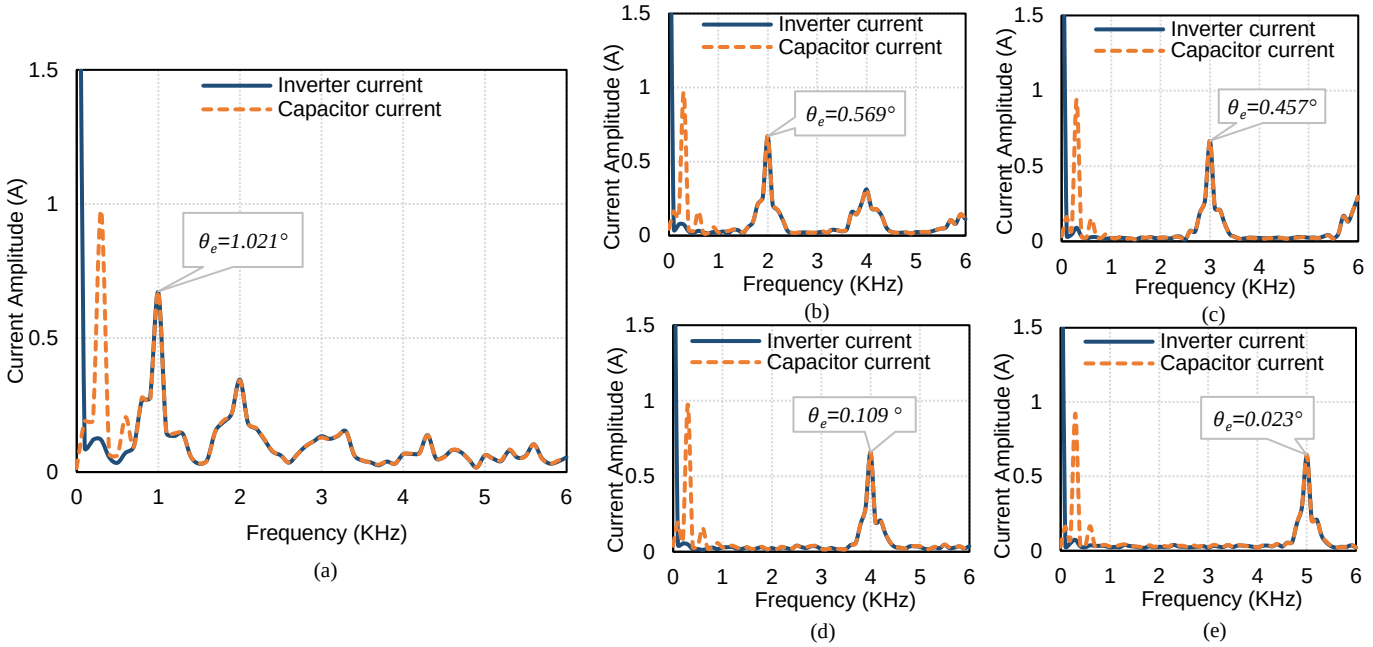

Fig. 9. Frequency spectrums of the inverter and capacitor currents at (a) 1kHz, (b) 2kHz, (c) 3kHz, (d) 4kHz, and (e) 5kHz switching frequency

TABLE IX
COMPARISON OF THE EXPERIMENTAL RESULTS MEASURED BY AN RLC-METER AND THE PROPOSED METHOD

No.	Values measured by the RLC meter				Values measured based on the proposed method				Er. (%)
	C_{RLCm} (μF)	ESR_{RLCm} (mΩ)	φ_{RLCm} (deg)	δ_{RLCm} (deg)	t_m (μs)	φ_m (deg)	δ_m (deg)	$1-\frac{tan(\delta_m)}{tan(\delta_{RLCm})}$	
1	234.6	0.211	72.723	17.277	200.9	72.306	17.694	-0.026	2.6
2	217.8	0.214	73.677	16.323	204.4	73.576	16.424	-0.007	0.7
3	201.5	0.221	74.368	15.632	206.4	74.307	15.693	-0.004	0.4
4	185.02	0.245	74.102	15.898	206.9	74.481	15.519	0.025	2.5
5	168.68	0.271	73.975	16.025	207.8	74.818	15.182	0.055	5.5
6	235.3	0.289	66.865	23.135	185.5	66.793	23.207	-0.003	0.3
7	217.9	0.302	67.536	22.464	189.9	68.355	21.646	0.040	4.0
8	201.2	0.318	68.099	21.901	191.4	68.905	21.095	0.040	4.0
9	184.75	0.337	68.635	21.365	191.8	69.042	20.959	0.021	2.1
10	168.47	0.367	68.770	21.230	193.3	69.587	20.413	0.042	4.2
11	234	0.427	57.879	32.121	156.9	56.467	33.533	-0.056	5.6
12	216.7	0.441	59.017	30.983	161.6	58.175	31.825	-0.034	3.4
13	199.98	0.459	60.026	29.974	166.4	59.892	30.108	-0.005	0.5
14	183.65	0.485	60.767	29.233	170.3	61.316	28.684	0.022	2.2
15	167.48	0.514	61.592	28.408	171.4	61.695	28.305	0.004	0.4
16	234	0.517	52.761	37.239	143.3	51.577	38.423	-0.044	4.4
17	216.8	0.53	54.172	35.828	149.6	53.840	36.160	-0.012	1.2
18	200.2	0.546	55.518	34.482	152.1	54.762	35.238	-0.029	2.9
19	183.84	0.569	56.685	33.315	156.5	56.325	33.675	-0.014	1.4
20	167.72	0.6	57.695	32.305	162.1	58.338	31.662	0.025	2.5

According to (12), $tan(\delta)$ will increase by approximately 60% over a capacitor lifetime. Thus, the proficiency of the proposed method is verified since its maximum error is less than one-tenth of the total expected changes.

VII. Conclusion

In this paper, the possibility of using the capacitor dissipation factor as an aging indicator is studied. A method is then proposed for measuring the dissipation factor at the inverter switching frequency. Measuring the DF at switching frequency yields the following two important advantages. First, it alleviates the main problem of using the DF as a degradation indicator for determining a capacitor EUL in a power electronics converter. The loss angle at the grid frequency is very close to zero, and a small error in measuring δ can significantly affect its tangent. However, if the DF is measured at a higher frequency, δ also increases, and as this angle approaches 45°, the effect of δ measurement error on $tan(\delta)$ is minimized. The second advantage of measuring the DF at the switching frequency is the possibility of calculating the capacitor current by measuring the converter output currents. Therefore, no extra current sensor is required to directly measure the capacitor current. In this case, most of the high-frequency components of the inverter current flow into the capacitor, and the input filters reject almost all the high-frequency components. Based on experimental results, the maximum DF measurement error is less than 6%. Considering the expected changes in the DF over the life of a capacitor, the measurement accuracy of the proposed method is acceptable.

In this article, in a nutshell:

- by increasing the frequency of impedance angle measurement, the accuracy of the DF estimation is improved,
- by calculating capacitor current from output currents at the switching frequency, an online monitoring method has been developed that eliminates the need for additional sensors to measure capacitor currents, and
- the experimental results have shown a measurement error of less than 6% for the proposed method.

Future studies can concentrate on the impact of temperature on the DF. Temperature measurement may be required to make possible corrections. Finally, further statistical studies must be performed to determine the range of possible changes in the DF due to capacitor aging.

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