CONDITION MONITORING OF ELECTROLYTIC CAPACITORS FOR POWER ELECTRONICS APPLICATIONS

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CONDITION MONITORING OF ELECTROLYTIC CAPACITORS FOR POWER ELECTRONICS APPLICATIONS

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To my loving mother, and fond memories of my father

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SUMMARY

The objective of this research is to advance the field of condition monitoring of electrolytic capacitors used in power electronics circuits.

The construction process of an electrolytic capacitor is presented. Descriptions of various kinds of faults that can occur in an electrolytic capacitor are discussed. The methods available to detect electrolytic capacitor faults are discussed. The effects of the capacitor faults on the capacitor voltage and current waveforms are investigated through experiments. It is also experimentally demonstrated that faults in the capacitor can be detected by monitoring the capacitor voltage and current.

Various ESR estimation based detection techniques available to detect capacitor failures in power electronics circuits are reviewed. Three algorithms are proposed to track and detect capacitor failures: an FFT based algorithm, a system modeling based detection scheme, and finally a parameter estimation based algorithm. The parameter estimation based algorithm is a low-cost real-time scheme, and it is inexpensive to implement.

Finally, a detailed study is carried out to understand the failure mechanism of an electrolytic capacitor due to inrush current.

CHAPTER 1

INTRODUCTION AND OBJECTIVE OF RESEARCH

1.1 Problem statement

Aluminum electrolytic capacitors are used in most power electronic circuits because they can achieve high capacitance and voltage ratings in small, cost efficient case sizes. The high volumetric efficiency of an electrolytic capacitor is achievable because of its enhanced plate surface area and a very thin dielectric layer. This type of capacitor has traditionally been used for filtering, timing networks, by-pass, coupling, and other applications requiring a cost effective, volumetrically efficient, and highly reliable component. Unfortunately, electrolytic capacitors are considered to be a weak link in all of these applications [1].

Condition monitoring of the electrolytic capacitor is therefore assuming a new importance in critical high performance applications. Early detection of faults would allow preventive maintenance to be performed, and provide sufficient time for the controlled shutdown of the process, thereby reducing the costs of outage-time and repairs. The common faults in electrolytic capacitor include initial catastrophic failures because of misapplication or manufacturing defect, and wear-out faults. However, some research works have been reported in literature for the diagnosis of the electrolytic capacitor faults, most of these research focuses on the capacitor fault because of aging [18-31]. These reported research works are difficult to implement in a cost-effective way, which is

further explained in Chapter 2. A new low-cost online monitoring scheme for an electrolytic capacitor failure is presented in Chapter 5.

1.2 Objective

The objective of this research is to advance the field of fault monitoring of an electrolytic capacitor operating in a power electronic circuit in a cost-effective way. This objective is addressed as three parts in this thesis. The first part, Chapter 3, experimentally characterizes the effects of the capacitor wear-out faults on the capacitor ripple voltage, and the capacitor ripple current. The second part, Chapter 4, develops methods to detect the capacitor faults by system modeling using the converter input current. A cost-effective method, Chapter 5, for the condition monitoring of the electrolytic capacitor, is presented using parameter-estimation technique. The parameters of the capacitor change because of aging and misapplication. Therefore, the condition of an electrolytic capacitor can be monitored by monitoring the parameters of the capacitor in real-time.

Finally, electrolytic capacitor faults caused by inrush current due to line surge-voltage are studied in Chapter 6, and a model of the capacitor is developed to explain the failure of an electrolytic capacitor due to inrush current. A summary of contributions appear in Chapter 7.

CHAPTER 2

BACKGROUND MATERIAL AND PREVIOUS WORK

2.1 Introduction

To facilitate a clear understanding of the proposed condition monitoring schemes, the construction of an electrolytic capacitor is now considered in more detail. The various modes of the capacitor failures are discussed. In addition, this chapter reviews and summarizes the existing research for condition monitoring of an electrolytic capacitor.

2.2 Electrolytic capacitor

The aluminum electrolytic capacitor is a passive component that has kept pace with advancements in technology. Aluminum electrolytic capacitors are used in various applications because they can achieve high capacitance and high voltage ratings in small, cost-efficient case sizes. This type of capacitor has traditionally been used for filtering, timing networks, bypassing, coupling, and other applications requiring a cost-effective, volumetrically efficient, and highly reliable component. To understand how this is accomplished, it is important to examine some of the basic properties of capacitors [2, 3].

A capacitor is made up of two parallel plates, the electrodes, with a dielectric between them. The amount of capacitance is directly proportional to the surface area of the electrode, but inversely proportional to the dielectric thickness. If the thickness is

reduced by one-half, the capacitance is doubled. The high volumetric efficiency of an electrolytic capacitor is due to its enhanced plate surface area, which is enhanced by an etching process. A large internal surface can be created on the aluminum electrodes by electrochemical etching. The dielectric is typically an oxide with a high dielectric strength, which is electrochemically deposited in thin layers. This combination produces a high capacitance in a small volume [2-7]. The aluminum electrolytic capacitor consists of an anode foil, a cathode foil, and a separator paper that are wound together and impregnated with an electrolyte. The anode foil has an aluminum oxide layer acting as the dielectric. After the thin aluminum foil (65 to 100 microns) is electrochemically etched to increase the plate's surface area, the dielectric is produced by anodic oxidation on its surface. The cathode foil, in general, utilizes no oxidation process. An illustration of a typical aluminum electrolytic capacitor is shown in Figure 2.1.

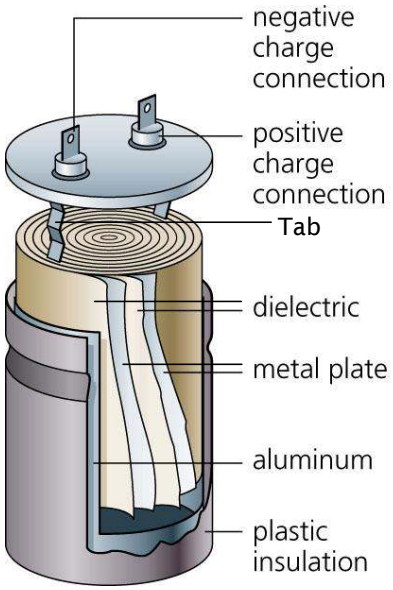


Figure 2.1 Cross section of an electrolytic capacitor. (*Source: Precision Graphics)*

2.3 Electrolytic capacitor construction process

2.3.1 Etching [3]

The plates, or electrodes, are made of high-purity thin aluminum foil (0.05 to 0.1 mm thick). To get the maximum capacitance for a given electrode surface area, an electrochemical process called "etching" is used to dissolve some of the surface material and increase the surface area of the foil in the form of a dense network of microscopic channels. The etching process consists of continuously subjecting the aluminum foil to a chloride solution with an AC, DC, or AC/DC voltage applied between the etch solution and aluminum foil. The increase in surface area is referred to as foil gain, and can be as much as 100 times for foil being used in low-voltage capacitor applications, and 20 to 25 times for higher-voltage applications [2].

2.3.2 Formation [3]

The dielectric of the aluminum electrolytic capacitor is composed of a thin layer of aluminum oxide (Al_2O_3), which develops or “forms” on the surface of the etched aluminum foil during a process called “formation.” This process of forming the dielectric oxide on the aluminum foil (electrode) requires a continuous application of DC voltage at 140% to 200% of the rated voltage for the capacitor being manufactured. The dielectric thickness of this aluminum oxide film is approximately 15 Å/volt [2]. The insulation strength is approximately 10^7 V/cm. Since capacitance is inversely proportional to the dielectric thickness and the dielectric thickness is proportional to the forming voltage, the relationship between capacitance and forming voltage is given by [2]

$$C \times V = const \tag{2.1}$$

where C = capacitance, and V = forming voltage

This is true for high-voltage foil, which has a relatively coarse etch structure. However, for foils that have extremely fine etch structures, the conversion of aluminum to aluminum oxide has a significant smoothing effect on the etch structure, resulting in a non-linear relationship.

2.3.3 Slitting [3]

The etched and formed foil is then slit into various widths, depending on the specific size of the capacitor.

2.3.4 Winding [3]

Each capacitor contains two foils, the positive foil is called the anode and the negative is called the cathode. The anode and cathode foils, along with a separator paper, called the "separator," are rolled into a cylindrical shape. The separator paper prevents the anode and cathode foils from coming into contact with each other, and shorting. As part of a highly automated winding process, aluminum tabs are attached to the anode and cathode foils. This completed assembly of etched and formed foil, separator paper, and attached tabs is called the capacitor "element" as shown in Figures 2.1, 2.2 and 2.3.

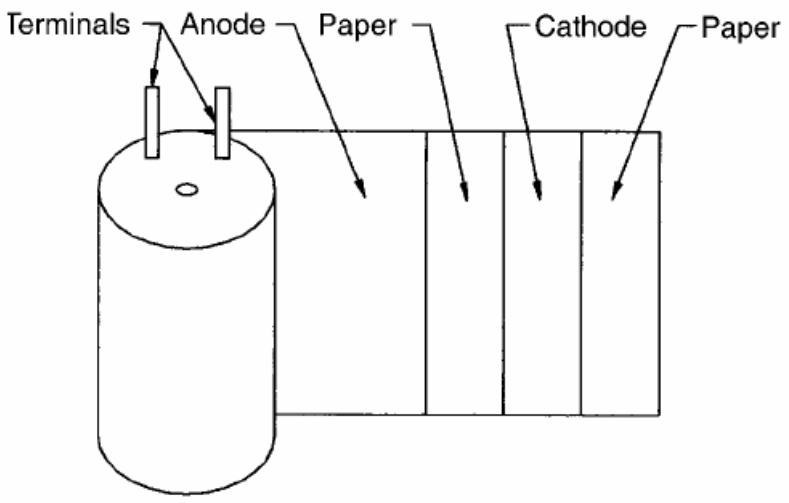


Figure 2.2 Wound capacitor elements.

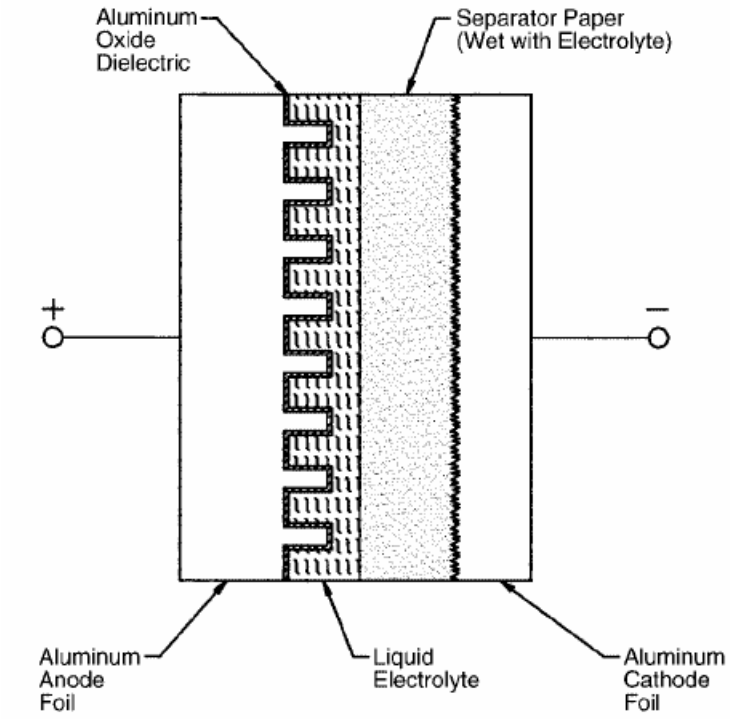


Figure 2.3 Cross section of wound capacitor element materials.

2.3.5 Impregnation [3]

The electrolyte is now added to the assembly by a process called "impregnation." The method of impregnation requires the wound element to be immersed into the electrolyte by a vacuum/pressure cycle either with or without applied heat or simple

absorption. The electrolyte contains a solvent such as ethylene glycol and a solute such as ammonium borate. Should the dielectric film be damaged, the presence of the electrolyte will allow the capacitor to heal itself by forming more oxide. By selecting different electrolytes, capacitor characteristics such as operating temperature range, frequency response, shelf life, and load life, can be further improved.

2.3.6 Sealing and aging [3]

The impregnated element is then sealed in an aluminum can. The sealing material may be rubber, rubber-backed phenolic, molded phenolic resin, or polyphylenesulfide (PPS). The final process is "aging," during which a voltage greater than the rated voltage of the capacitor is applied at elevated temperatures. The purpose is to reform (or repair) any oxide film that may have been damaged during the slitting, winding, and assembly processes.

2.4 Application guide

2.4.1 Dielectric absorption [2]

Dielectric absorption may be observed as the re-appearance of a voltage across a capacitor after the terminals have been shorted for a brief period, and the short removed. This characteristic is important in RC timing circuits, triggering systems, and phase shift networks. For aluminum electrolytic capacitors, dielectric absorption will allow up to 10% recovery of the charging voltage between 100 s and 1000 s at 25°C and it is more pronounced at higher temperatures. Maximum dielectric absorption can be obtained by charging capacitors for 1 hour at rated voltage and discharging through a dead short for 1 minute. Subsequent measurements over time can be made using a high impedance probe.

With high-voltage aluminum electrolytic capacitors, rebound voltages of 40 to 50 V are possible [2]. Rebound voltages are caused by internal chemical process in which there exists a small voltage across the capacitor terminals due to charge polarization in the capacitor dielectric-layer even in the absence of any external applied voltage. While such voltages are not a safety hazard, they can certainly create a frightening distraction if the terminals are shorted by a tool during installation. Conductive tape and wire shorting straps can be supplied to avoid this problem. The tradeoff is extra cost and the labor to remove them.

2.4.2 Insulation and grounding [2]

With non-solid electrolyte, aluminum electrolytic capacitor cans connect to the negative terminals through the electrolyte of the capacitor. The resulting isolation resistance may vary from a few ohms to a few thousand ohms. For axial-leaded capacitors and flat packs, the case is connected to the negative lead. If objects contacting the cases are to be at a potential other than the negative terminals, capacitors with insulating sleeves are used. The plastic insulation sleeve can withstand 3000 Vdc or 2500 Vac at 60 Hz [2].

2.4.3 External pressure [2]

Aluminum electrolytic capacitors can operate at altitudes to 80,000 feet and at pressures as low as 3 kPa, and maximum air pressure depends on the size and style of the capacitor. Exceeding the maximum value can damage the capacitor by rupturing the case, opening the pressure-relief vent, or causing a short circuit.

2.4.4 Mechanical vibration [2]

Aluminum electrolytic capacitors can generally withstand 10 g vibration forces. To test vibration resistance, a capacitor is clamped to a vibrating platform and subjected to a simple harmonic motion having maximum peak-to-peak amplitude of 0.06 inches and a maximum acceleration of 10 g or 15 g as specified. The frequency of vibration is varied linearly between 10 and 55 Hz. The entire frequency range is traversed in 1 minute. Unless specified otherwise, capacitors are vibrated for one and half hours with the direction of motion being parallel to the axis of the capacitor; then the capacitor is placed so that the direction of motion is perpendicular to the axis and vibration is continued for another one and half hours. During the last half hour of the test, the capacitor is connected to a bridge measuring circuit, and observations are made for any mechanical damage for a 3-minute period. In addition, there should not be any evidence of loosening of the capacitor element within the container when shaken by hand following the test. There should not be any indication of intermittent contact, open or shorting during the 3-minute observation period.

2.4.5 Pressure-relief vents [2]

During operation of an aluminum electrolytic capacitor with non-solid electrolyte, gas pressure normally increases. The gas is mostly hydrogen and excess pressure is avoided by permeation of the gas through the capacitor's seal. However, in some cases like the application of an overvoltage, reverse voltage, AC voltage or capacitor failure, excess pressure can cause the capacitor to explode. To avoid the risk of explosion, aluminum electrolytic capacitors are usually equipped with pressure-relief vent structures. These safety vents are intended to rupture and release the gas pressure. After

rupture, the capacitor has a limited life because it loses electrolyte and dries out. Care should be taken to avoid interfering with the operation of the vent, for instance by mounting elements, such as clamps, glue or potting compounds. In the case of large capacitors with the capacitor elements secured by thermoplastic potting, it should not be mounted with the safety vents down, as the potting may flow when the capacitors overheat, and block the vents. In rare cases, for capacitors mounted alone, and more often for capacitors in multiple-unit parallel capacitor banks, a fully functioning pressure relief device may not react in time. This could be from extreme overload or ignition of gas inside the capacitor through sparking caused by breakdown. Personnel should be protected from possible rupture of high-energy capacitors with substantial shielding. Examples of appropriate shielding for testing are quarter-inch thick steel or half-inch thick polycarbonate enclosures with one end open to redirect the explosion rather than contain it. The excess internal pressure will be relieved without violent expulsion of the capacitor element, or cover, or ignition of surrounding material.

2.4.6 Contact with electrolyte [2]

The electrolyte in non-solid electrolyte capacitors is a biodegradable liquid based on a stable solvent with a high boiling point as the main ingredient. Common solvents are ethylene glycol (EG), dimethylformamide (DMF), and gammabutyrolactone (GBL) [2]. The electrolyte includes an acid base system, and other chemicals. The electrolyte is chemically neutral and contains no lead compounds, or halogenated compounds. It has a low toxicity but contact with the skin or eyes should be avoided, and avoid prolonged inhalation. Contact with electrolyte can be treated by rinsing the exposed area with water. If the electrolyte contacts eyes, it should be flushed for 10 minutes with running water. If

vapors are present, the room should be ventilated. Smoke from burning electrolyte is irritating but does not contain dioxins or similar toxic substances.

2.4.7 Charge-discharge [2]

Frequent, rapid charging and discharging of aluminum electrolytic capacitors which were not designed for such service, can damage the capacitors by overheating, and overpressure, or breakdown with consequent failure by open or short circuit.

2.4.8 Polarity – reverse voltage [2]

The polarity of each capacitor should be checked, both in circuit design and in mounting. While the capacitors can withstand continuous application of 1.5 V reverse voltage, exceeding that value can damage the capacitor by overheating, overpressure, and dielectric breakdown. This can result in associated open-circuit or short-circuit failures and rupture of the capacitor's pressure-relief vent.

2.4.9 Flammability [2]

Aluminum electrolytic capacitors contain materials, which can catch fire and support combustion when contacted by flames. Flammable parts include plastic parts, insulating sleeves, paper, and the electrolytes. Most capacitors will pass the needle-flame test requirements of UL 94V-O [48], and do not support combustion to the requirements of category B or C. In rare cases, the capacitor may self-ignite from heavy overload (high-ripple current) or capacitor defect. Hydrogen in the capacitor can ignite if sparking occurs during capacitor failure. In critical applications such as mining applications, fire-resistant shields should be provided.

2.5 Capacitor parameters and equivalent circuit [2]

The equivalent circuit of an aluminum electrolytic capacitor is shown in Figure 2.2. Because of the physical design elements and construction, a capacitor not only has capacitance, but it also has a series resistance and an inductance as well as a parallel resistance allowing the flow of current.

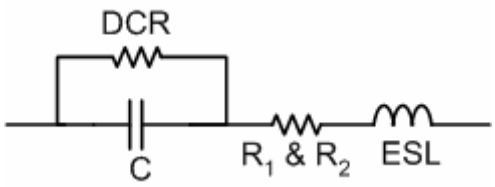


Figure 2.4 Electrolytic capacitor equivalent circuit, where C = capacitance, ESL = equivalent-series-inductance, DCR = dielectric-leakage-resistance, R_1 = electrolyte resistance, R_2 = tab resistance.

2.5.1 Capacitance

The capacitance of aluminum electrolytic capacitor as well as other capacitors, is expressed by

$$C = \frac{\mu_{\circ}\mu_r A}{d} \tag{2.2}$$

where μ_o = Dielectric constant in free space (8.8542×10^{-12} F/m)

μ_r = Relative dielectric constant of the material

A = Surface area of the dielectric (m^2)

d = Thickness of the dielectric (m)

A large capacitance can be obtained when

- The dielectric constant is high
- The surface area is large
- The dielectric is thin

In aluminum electrolytic capacitors, the relative dielectric constant is about 8 to 10, and the aluminum oxide dielectric layer is thin (about 15 Å per volt). However, high gain foil produced by the electrochemical etching, creates a surface magnification, or gain, as much as 100 times for the low voltage foil, and 20 to 25 times for the high voltage foil. Therefore, an aluminum electrolytic capacitor can provide a large capacitance compared to other types of capacitors of the same volume. In addition, capacitance tolerance is the permitted minimum and maximum capacitance values expressed as a percentage decrease and increase from the rated capacitance, $\Delta C/C$. Typical capacitance tolerances are ±10%, and ±20%, however, tighter tolerances are more readily available in high voltage capacitors, e.g., above 150 V, but tolerances tighter than ±10% are generally not available [3-7]. However, tighter tolerance parts may meet other tolerance rating requirements, and are readily substitutable if available. Finally, the capacitance also varies with temperature and frequency, and the variation itself is dependent on the rated voltage and the capacitor size.

2.5.2 Dielectric leakage resistance (DCR)

The dielectric of a capacitor has a high resistance, which prevents the flow of DC current. However, some defect areas in the dielectric allow a small amount of current to pass, called leakage current [8]. The areas allowing current flow are due to small foil impurity sites that are not homogeneous, and the dielectric formed over these impurities does not create a strong bond. These bonds break down when the capacitor is exposed to high DC voltages, and hence the leakage current increases. Leakage current is also determined by the following factors:

- Capacitance value

- Applied voltage versus rated voltage
- Previous history

The leakage current is proportional to the capacitance and decreases as the applied voltage is reduced [2]. If the capacitor has been at elevated temperatures without voltage applied for an extended time, some degradation of the oxide dielectric may take place, which will result in a higher leakage current. Usually this damage will be repaired when voltage is reapplied.

2.5.3 Equivalent series inductance (ESL)

The inductance of a capacitor is a constant, and is due primarily to the capacitor terminal connection. The inductance varies anywhere from 10 nH for miniature radial capacitors to as high as 100 nH for large can type capacitors. Generally, the inductance does not affect the overall impedance unless the capacitor is operating at high frequencies, as shown in the Bode-plot of the equivalent-circuit impedance of an electrolytic capacitor in Figure 2.5 for a 1 mF, 85 ºC, 100 volt rated electrolytic capacitor.

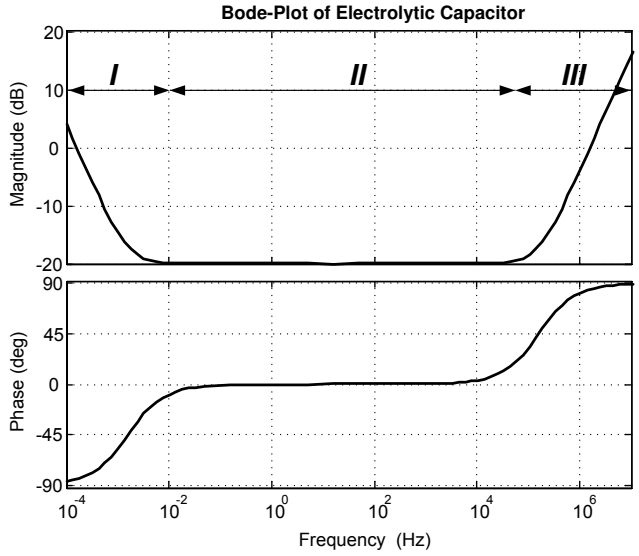


Figure 2.5 Bode-plots of the electrolytic capacitor equivalent circuit impedance.

2.5.4 Equivalent Series Resistance (ESR)

ESR leads to heat generation in the capacitor because of AC ripple current. The equivalent equation for ESR is shown in (2.3) [9].

$$ESR = R_1 + R_2 + R_3 \tag{2.3}$$

where R_1 = Frequency-sensitive resistance as a result of oxide thickness

R_2 = Temperature-sensitive resistance as a result of electrolyte

R_3 = Resistance because of the following components:

- Foil length
- Tabs
- Lead wires
- Ohmic contact resistance

The effect of the frequency-dependent part, R_1, appears in the ripple current multipliers provided by manufactures [7]. This effect is caused by energy losses in the alignment of dipoles in the dielectric, and the time it takes for the dipoles to become oriented [8]. It becomes more significant for higher rated voltage capacitors because their oxide layer is thicker. For applications with a single frequency ripple current, the ESR can be simply adjusted by using a multiplier [2]. The amount of heat generated by the ripple current depends upon the ESR of the capacitor [13]. To have a low ESR, it is necessary to control the characteristics of the electrolyte, the separator paper, the winding alignment of the element, the position of the tabs, and the magnification and pit construction of the etched foil. All these factors contribute to the ESR of the capacitor [13-16]. The parallel combination of DCR and C models the dielectric oxide layer of the

capacitor, as shown in Figure 2.2. Equation (2.4) describes the complex impedance of the capacitor in Figure 2.4.

$$Z_{cap} = \frac{1}{\frac{1}{DCR} + j2\pi fC} + R_2 + R_3 + j2\pi fESL \tag{2.4}$$

where Z_{cap}= complex impedance of the capacitor, and f = frequency (Hz).

The value of ESR can be calculated as, ESR = Real part of (Z_{cap})

$$\text{Real part of } (Z_{cap}) = \frac{DCR}{1 + (2\pi f)^2 C^2 DCR^2} + R_2 + R_3 \tag{2.5}$$

$$ESR = R_1 + R_2 + R_3 = \frac{DCR}{1 + (2\pi f)^2 C^2 DCR^2} + R_2 + R_3 \tag{2.6}$$

Hence, the frequency-dependent part of ESR can be written as

$$R_1 = \frac{DCR}{1 + (2\pi f)^2 C^2 DCR^2} \tag{2.7}$$

2.5.5 Operating temperature range [2]

The operating-temperature-range is the temperature-range over which the component will function, when energized, within the limits given in the specification. Capacitors are designed to operate over a range of ambient temperatures; moreover, the formation-voltage sets the high-temperature limit. Higher formation-voltages permit operation at higher operating temperatures but reduce the capacitance. The low-temperature limit is set largely by the cold resistivity of the electrolyte. A higher value of cold resistivity increases the capacitor's ESR 10 to 100 fold and reduces the available capacitance. Typical temperature ranges are: –20°C to +55°C, –25°C to 85°C, –40°C to 85°C, –55°C to 85°C, –40°C to 105°C, –55°C to 105°C, and –55°C to 125°C.

2.5.6 Storage temperature range [2]

The storage temperature range is the temperature range to which the part can be subjected while un-energized while it retains conformance to specified electrical limits. It is the ambient temperature range over which the capacitors may be stored without damage for short periods. For longer period of storage, capacitors should be kept at cool room temperatures, and in an atmosphere free of halogen gases like chlorine and fluorine that can corrode the aluminum. Typical storage temperature ranges are from –55°C to the upper limit of the operating-temperature ranges.

2.5.7 Rated DC voltage [2]

Rated DC voltage is the maximum peak voltage including ripple voltage that may be applied continuously between the terminals, and over the rated temperature range. Higher rated voltage capacitors may be substituted for lower rated voltage capacitors as long as case size, dispersion factor (DF), and ESR ratings are compatible [2].

2.5.8 Rated surge voltage [2]

Rated surge voltage is the maximum DC overvoltage to which the capacitor may be subjected at 25 °C for short periods not exceeding approximately 30 s at infrequent intervals of not less than 5 min. The surge voltage can be measured as follows: subject the capacitors to their rated surge voltage at normal room temperature and through a 1000 Ω ±10% resistor. Cycle the voltage 30 s on followed by 4.5 minutes off during which each capacitor is discharged through the charging resistor or equal resistor, and repeat the cycle for 120 h. Post-test requirements are for the DCL, ESR, and DF to meet the initial requirements, and for there to be no evidence of mechanical damage or electrolyte

leakage. In addition, the electrolyte residue with no droplets or visible flow is permitted [2].

2.5.9 Transient over voltage [2]

Aluminum electrolytic capacitors can generally withstand extreme overvoltage transients of limited energy. An application of overvoltage more than about 50 V beyond the capacitor's surge voltage rating causes high leakage current, and a constant-voltage-operating mode similar to a zener diode operation. The capacitor may fail as a short-circuit if the electrolyte cannot take the voltage stress, but even if it can, this operating mode cannot be maintained for long because hydrogen gas is produced by the capacitor, and the pressure build up will cause the capacitor to rupture. However, special designs are available that use the overvoltage, zener-clamping-effect to successfully protect equipment from overvoltage transients such as lightning strikes.

2.5.10 Ripple current [2]

Ripple current is the AC current flowing in the capacitor. It is called ripple current because the associated AC voltage rides like ripple on water on the capacitor's DC bias voltage. The ripple current heats the capacitor, and the maximum permitted ripple current is set by the capacitor's load life specification. A significant temperature rise above the maximum permitted core temperature, will cause failure, even operation close to the maximum permitted core temperature dramatically shortens the expected life of the capacitor. The load life specifications for aluminum electrolytic capacitors operating at maximum permitted core temperature are typically 1000 to 10,000 hours. Ripple current ratings are specified for an expected temperature rise above the rated temperature.

Commonly, capacitor types rated at 85°C permit a temperature rise of 10°C, and have a maximum permitted core temperature of 95°C. However, types rated 105 °C permit a temperature rise of only 5°C, and have a maximum core temperature of 110 °C. Moreover, actual maximum permitted core temperatures may vary by type and manufacturer. Ripple current ratings usually assume that the capacitor is convection cooled and that the entire can is in contact with air. A convection coefficient of 0.006 W/°C/in^2 is used [2] to calculate the temperature rise from air to the case, and the core temperature is assumed to be same as the case temperature. The power dissipated is the ripple current squared times the ESR. Often the ESR value at 25°C, 120 Hz is used to calculate the power dissipated. With large-can capacitors, neglecting the temperature rise from the case to the core, can seriously overstate the ripple current capability. With some constructions, the core is 3 to 5°C per watt of ripple power hotter than the case. Therefore, the total temperature rise would be more than double the intended 10°C with rated ripple current and maximum ESR. However, generally it is safe to assume that the core temperature is the same as the case temperature for capacitors smaller than 25 mm in diameter [2].

2.6 Capacitor bank configuration [2]

2.6.1 Parallel connection

Capacitors may be connected in parallel for increased capacitance and ripple-current capability. Parallel-connected capacitor banks have a minimum series inductance, and it requires a laminated bus or strip-line structure. Generally, one plane of the circuit board acts as the positive-connection and another plane as the negative-connection to all

capacitors in the bus. The circuit resistance external to each capacitor should be equal to ensure equal current sharing. While the ripple-current divides among the capacitors in proportion to capacitance values for low-frequency ripple, and high frequency ripple-current divides in proportion to ESR values and the path resistance. In order to fuse the individual capacitors, a slow-start circuit should be included at equipment turn-on, and the fuse used for each capacitor should be rated at twice its expected, maximum ripple-current [10]. The slow start circuit can be a resistor in series with the capacitors that is shorted after initial charging.

2.6.2 Series connection

Capacitors can be connected in series for increased voltage withstanding capability. During charging, the voltage across each of the capacitors connected in series is proportional to the inverse of the individual capacitance, but upon reaching the final voltage, the voltage across each capacitor is proportional to the inverse of the capacitor's leakage current. Of course, in a series-string, all leakage currents are the same, and the capacitors with a propensity for higher leakage current will get less voltage. Since leakage-current increases with applied voltage, a higher voltage results in higher leakage-resistance and the voltages tend to equalize. High voltage bus capacitors in series pairs connected to supply voltages 10% above twice the rated voltage have good voltage sharing over the full temperature range. Moreover, two capacitors in series will seldom require balancing resistors for voltage sharing. As an alternative, capacitors from the same manufacturing lot should be used to ensure equal leakage currents, or a higher rated voltage can be used to permit voltage imbalance with different manufacturers. In addition, capacitors in series should have the same thermal environment.

2.6.3 Parallel-series connection

Capacitors connected as shown in Figure 2.6 with a common connection between multiple series combinations have the following considerations.

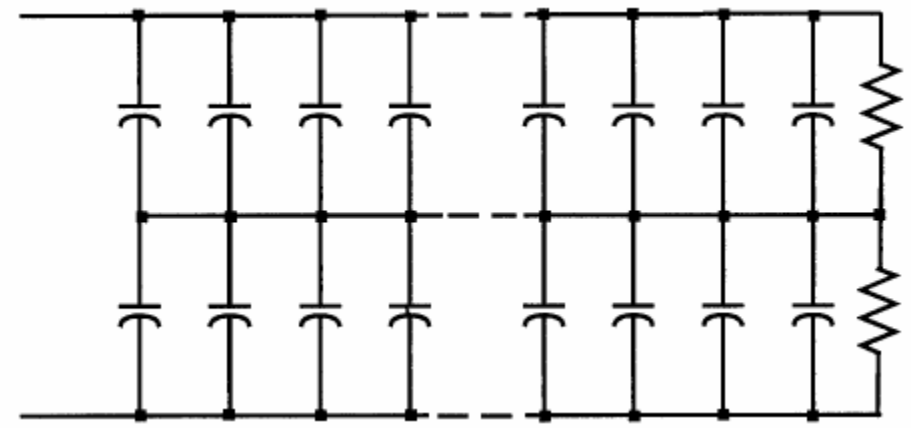


Figure 2.6 Parallel-series connection.

Advantages: As the number of capacitors in parallel increases, the total capacitance of the top group tends to equal the total capacitance of the bottom group even if individual capacitor values are not identical. This improves voltage balance during transients. In addition, the leakage current of the top group tends to equal the leakage current of the bottom group, so that voltage balance improves during steady-state conditions. Finally, only two balancing resistors are needed, and the top and bottom resistors are carefully matched so that it eliminates the need for any other balancing resistors.

Disadvantage: If one capacitor fails short, the other half of the bank gets the entire bus voltage, so other capacitors will fail as well. Therefore, one capacitor failure can cause failure of the entire bank unless the shorted capacitor is blown open.

2.6.4 Series-parallel connection

Capacitors connected as shown in Figure 2.7 with multiple series combinations in parallel have the followings considerations. This configuration is the clear choice when balancing resistors are not used.

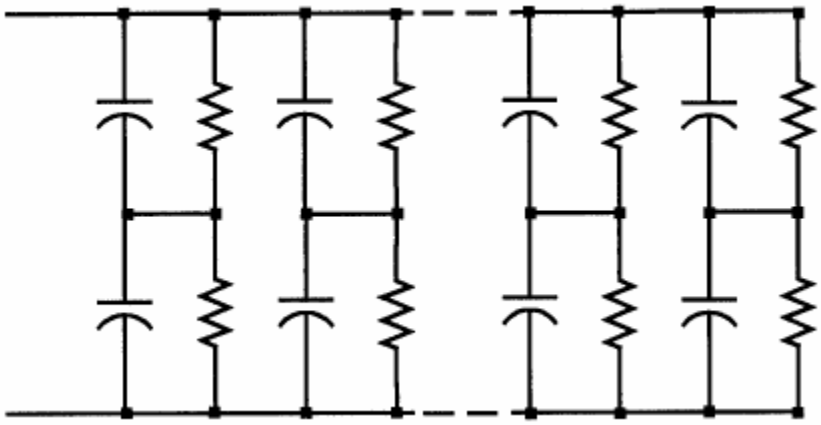


Figure 2.7 Series-parallel connection.

Advantages: If one capacitor fails short then the capacitor in series with it also fails, but other capacitors in the bank are unaffected. If balancing resistors are not used, then a high leakage current of one capacitor affects only a single pair of capacitors. The independent, series pairs permit fusing.

Disadvantages: With balancing resistors, the construction is more complex; many resistors need to be fitted, and the cost increases.

2.6.5 Non-polarized connection

If two, same-value, aluminum electrolytic capacitors are connected in series, back-to-back with the positive terminals or the negative terminals connected, then the resulting combined equivalent single capacitor is a non-polarized capacitor with half the capacitance to either of the original pair. Each capacitor individually rectifies the applied

voltage, and act as if they had been bypassed by diodes. When voltage is applied, the correct-polarity capacitor gets the full voltage. In non-polarized aluminum electrolytic capacitors and motor start aluminum electrolytic capacitors, a second anode foil substitutes for the cathode foil to achieve a non-polarized capacitor in a single can. While non-polar aluminum electrolytic capacitors are available for momentary-duty AC applications like motor starting and voltage-reversing applications, the high dispersion factor (DF) of aluminum electrolytic capacitors, from 2% to 150%, causes excess heating and a short life in most AC applications.

2.7 Cooling strategies [2]

Capacitors conduct heat from the core to the bottom of the can more effectively than outwards to the sides. Advantage can be taken of this heat path can be taken by mounting the bottom of the capacitor cans directly to a metal chassis. In many can sizes, this method of mounting doubles the permitted ripple-current for the same temperature rise. Mounting can be done by using capacitors with special mounting studs and screwing the studs directly into the chassis plate, or it can be done by pressing the capacitors against a plate using the interconnecting bus structures. The seal pads create smooth bottoms by eliminating the steps at the sleeve rollovers [11]. The thermal resistance between the can and the chassis plate for capacitors merely sitting on the plate is about 2.5°C/W. This decreases to less than 1°C/W if the capacitors are pressed into place. In large-can capacitors, especially ones with potting, there is a significant temperature rise from the case to the core, and the center of the capacitor is the hottest spot. As an illustration, 20 amps of ripple-current at 120 Hz with a maximum ESR of 20 mΩ, dissipates 4 W of power. Consider, a total thermal resistance of 3.07°C/W for air on all

sides and 1.02°C/W for the capacitor can pressed against a large metal plate, or chassis. With 4 W, the 3.07°C/W thermal resistance results in a temperature rise of 12.3°C, and the 1.02°C/W results in a 4.1°C rise. The 1.02°C/W assumes that there is no temperature rise in the metal plate.

2.8 Shelf life [2]

Aluminum electrolytic capacitors stored for more than 5 to 10 years may have increased levels of DC leakage current. Leakage current should be measured before use to check whether it meets application requirements before placing in the service. High leakage current units should be reconditioned by applying rated voltage through 1,000 Ω resistor for 30 minutes. Shelf life is a measure of how the capacitors will withstand storage for longer durations of time, especially at high temperature.

2.9 Process considerations [2]

2.9.1 Soldering

Strict soldering conditions such as temperature, duration, and minimum distance of solder from body should be considered for the protection of the capacitor. Contact with the insulating sleeve or other plastic parts with a soldering iron or molten solder should be avoided. In addition, any mechanical force like bending, straightening, twisting, or tilting of capacitors after soldering them into a printed circuit board, should be avoided.

2.9.2 Mounting

At lower ambient temperatures aluminum electrolytic capacitors have longer operating lives, therefore, the capacitors should therefore be installed at the coolest place

on the circuit board. Aluminum electrolytic capacitors should be kept away from hot components like power resistors, power transistors, diodes, and transformers. Adequate space should be used to place the components for cooling air to circulate. This is especially important when high ripple current or charge/discharge loads are applied. In addition, aluminum electrolytic capacitors are normally polarized, and care should be taken to connect them with correct-polarity during installation in the circuitry. Adequate clearance should be provided for proper operation of the pressure-relief devise. The capacitors should be mounted such that the vent is at the top, or at least in the upper part of the capacitor. This assures that the least amount of the electrolyte will be expelled if the vent operates. Capacitors that include thermal-plastic potting should be mounted such that the potting cannot block the vent, should the potting melt during the capacitor failure.

2.10 Disposal of electrolytic capacitors [2]

Aluminum electrolytic capacitors with non-solid electrolyte principally include high-purity aluminum foils, capacitor paper, electrolyte, aluminum case, cover and sealing parts (phenolic, thermoplastic, rubber and phenolic board), insulating sleeve (polypropylene, polyester or polyvinylchloride) and, perhaps, safety-vent plugs made of synthetic rubber [12]. It should be incinerated above 1200 °C, and residue can be disposed in appropriate landfills.

2.11 Comparison to other types of capacitors [2]

2.11.1 Ceramic capacitors

Ceramic capacitors have become the preeminent, general-purpose non-polarized capacitor, especially in surface mount technology (SMT) chip devices where their low

cost makes them especially attractive [2]. With the emergence of thinner dielectric, multilayer units with rated voltages of less than 10 V, capacitance values in the hundreds of microfarads have become available. This intrudes on the traditional, high-capacitance province of aluminum electrolytic capacitors. Ceramic capacitors are available in three classes according to dielectric constant and temperature performance. Class 1 (NPO, COG) is suitable for low capacitance, tight tolerance applications in the range of 1 pF to a few mF. Class 2 (X7R) has 20 to 70 times as much capacitance per case size, but the capacitance typically varies about ±10 % over its –55 to 125°C temperature range, with a maximum change of +15 % to –25 %. Class 3 (Z5U) with about 5 times the capacitance of Class 2 has large variations of capacitance with voltage and temperature. The temperature range is –25°C to 85°C, and capacitance varies by about +20 % to –65 % over this range [2].

Ceramic capacitors are brittle and sensitive to thermal shock, so precautions need to be taken to avoid cracking during mounting, especially for high-capacitance large sizes. The typical temperature range for ceramic capacitors is –40°C to 85°C or 105°C, and their capacitance varies about +5 % to –40 % over this range, with a reduction in capacitance at cold temperatures. For example, capacitors rated at –55°C generally only have –10 % to –20 % capacitance losses at –40°C. Cold temperature performance for rated voltages of 300 V and higher is often worse, and temperature performance varies by manufacturer. Thus, Class 1 and 2 ceramic capacitors perform better than electrolytic capacitors at cold temperatures, and Class 3 ceramic capacitors perform worse at all temperatures [2].

Electrolytic capacitors give more capacitance and energy storage per unit volume than ceramic capacitors for all types except for low-voltage, Class 3 ceramic SMT chip type capacitors. While tolerances of ±5% and ±10% are routine for ceramic capacitors, ±20%, and −10% to +50% are the norms for electrolytic capacitors. This makes electrolytic capacitors the choice for high capacitance applications like rectification filters and power hold up where more capacitance is a bonus and accuracy is not important. The low DF and high capacitance stability of Class 1 and 2 are ceramic capacitors especially suited to AC and RF applications. By comparison, electrolytic capacitors are polarized, and cannot withstand reverse voltages in excess of about 1.5 V. However, non-polar electrolytic capacitors are available for momentary duty AC applications like motor starting and voltage-reversing applications. High DF of electrolytic capacitors, from 2% to 150%, causes excess heating and short life in most AC applications. Ceramic capacitors are generally no more reliable than electrolytic capacitors because electrolytic capacitors have self-healing properties. Since high capacitance ceramic capacitors may develop micro-cracks, electrolytic capacitors are preferred for high capacitance values. However, small sizes of electrolytic capacitors may have limited life due to dry-out, and reliability becomes an issue when operating at high ambient temperatures, over 65 °C.

2.11.2 Film capacitors [2]

Film capacitors offer tight capacitance tolerances, low leakage currents, and small capacitance changes with temperature. They are especially suited to AC applications through their combination of high capacitance, and low DF that permits high AC currents. However, they are relatively large in size and weight. The popular polymers used for plastic-film dielectric capacitors are polyester and polypropylene. The popular

polymer for SMT devices is polyphenylene sulfide (PPS). While film/foil construction is often used for small capacitance values less than 0.01 μF, and for high-current applications, the metallized-film types on the hand are usually preferred because they have smaller size, lower cost, and are self-healing. Film capacitors are general-purpose capacitors for through-hole applications and have special uses for tight-tolerance, AC voltage, high voltage, and snubbing. Polyester film capacitors operate from at –55°C to 85°C at rated voltage; in addition, +85°C to 125°C with linear voltage derating to 50 % of rated voltage. The typical capacitance change over the entire range is less than –5 % to +15%, and as low as ±1% from 0°C to 50°C. Capacitance values are readily available up to 10 μF, and with special large sections up to 100 μF. Generally, available voltages are 50 to 1000 Vdc and 35 to 600 Vac. AC current handling is limited by polyester's high temperature DF of about 1%. Polypropylene film capacitors operate from –55°C to 85°C at rated voltage; in addition, 85°C to 105°C with linear voltage derating to 50 % of rated voltage. The typical capacitance change over the entire range is less than +2% to –4% with as low as ±1% from – 20°C to 60°C. Capacitance values are readily available up to 65 μF, and with special large sections up to 1000 μF. Generally, available voltages are 100 to 3000 Vdc and 70 to 500 Vac. AC current handling permits use in motor-run and other continuous duty AC applications. Compared to aluminum electrolytic capacitors, film capacitors take the lead in high voltage, AC voltage, and tight tolerance applications. However, aluminum electrolytic capacitors excel in capacitance and energy storage.

2.11.3 Solid tantalum capacitors [2]

Like aluminum electrolytic capacitors, solid tantalum capacitors are polarized devices (1 V maximum reverse voltage), having distinct positive and negative terminals,

and are offered in a variety of styles. Case styles include both molded and conformal-coated versions of radial, axial, and surface mount configurations. Typical capacitance values are from 0.1 μF to 1000 μF in voltage ratings from 2 V to 50 V. Typical maximum capacitance-voltage combinations are approximately 22 μF at 50 V for leaded styles, and 22 μF at 35 V for surface mount. Advantages of solid tantalum capacitors are temperature stability, volumetric efficiency, and compatibility with all automated assembly systems. However, weaknesses are the limited voltage and capacitance ranges, and a short-circuit failure mode accompanied by catching fire. The operating temperature range is -55°C to 85°C at rated voltage; in addition, + 85°C to 125°C with linear voltage derating to 2/3 of rated voltage. The typical capacitance change over the entire range is less than ±5%. Thus, electrolytic capacitors have a much broader voltage and capacitance ranges than solid tantalum capacitors but perform worse at cold temperatures. Solid tantalum capacitors are generally considered more reliable than electrolytic capacitors because solid tantalum capacitors do not wear out. Their failure rate decreases with time, while electrolytic capacitors wear out by drying-out of the electrolyte. As a practical matter, dry-out only affects the smallest capacitors operating in high-temperature environments. Larger electrolytic capacitors do not dry-out fast if operated in their specified conditions, and these are expected to last for 10 to 20 years for most applications. In addition, the open-circuit, dry-out failure in the electrolytic capacitors is benign compared to solid-tantalum's short circuit failure mode.

2.12 Failure modes [2]

Failure modes of electrolytic capacitors can be classified as follows, Figure 2.8 [2].

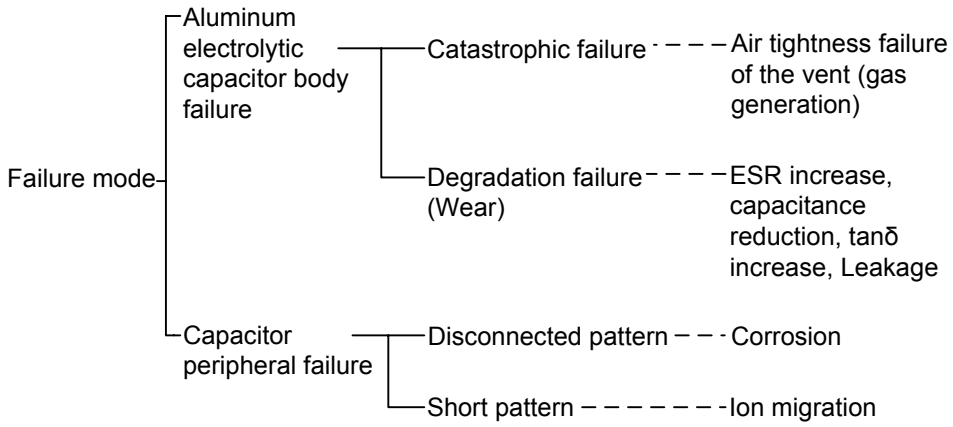


Figure 2.8 Failure mode chart.

In catastrophic failure, the function of the capacitor is completely lost; therefore, it is easily detected as a failure. In degradation failure, the characteristics such as, ESR, capacitance, tanδ, and leakage resistance, gradually deteriorate to the stage at which it is judged as a failure. However, the point of failure will vary greatly with the performance required by the power electronics system in which it is used.

2.12.1 Air-tightness failure of the vent (gas generation) [2]

Aluminum electrolytic capacitors have characteristics, which quickly repair film defects by the mechanism shown in Figure 2.9 and equation (2.8). Oxidation at the anode will cause reduction at the cathode, resulting in the generation of hydrogen gas (H_2). However, when used under a condition within the guaranteed ranges noted in the manufacturers' catalog or delivery specifications, the generated hydrogen gas is extremely small, and any generated such gas is dissipated by the depolarization action of the electrolyte or through the sealing element, so there is no problem. However, if used under extreme conditions, such as high temperature, over voltage, reverse voltage, and excess ripple-current, exceeding the guaranteed ranges, damage to the dielectric film will increase, causing a sudden increase in hydrogen gas generated by the self-repairing

action. This will cause the internal pressure to rise rapidly, which leads to opening of the pressure-vent, or rupture of the capacitor can.

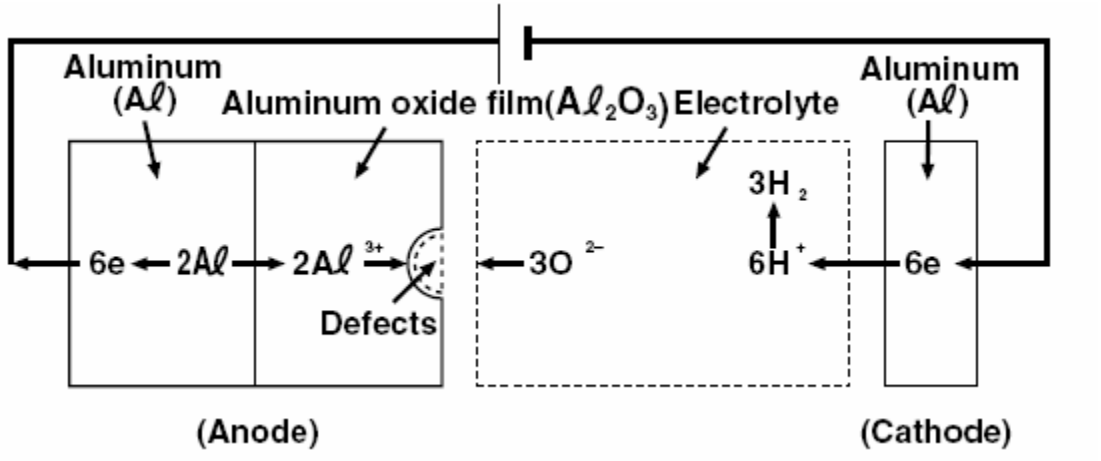


Figure 2.9 Chemical characteristics of an electrolytic capacitor.

$$2Al \rightarrow 2Al^{3+} + 6e^{-} \quad (2.8\text{ a})$$

$$3H_2O \rightarrow 6H^{+} + 3O^{2-} \quad (2.8\text{ b})$$

$$2Al^{3+} + 3O^{2-} \rightarrow Al_2O_3 \quad (2.8\text{ c})$$

$$6H^{+} + 6e^{-} \rightarrow 3H_2 \uparrow \quad (2.8\text{ d})$$

2.12.2 Open failure

Open failure can occur because of any of the following reasons [2]:

- mechanical damage to the lead connection,
- corrosion because of the infiltration of a corrosive material,
- evaporation of the electrolyte because of opening of the vent,
- final stage of gradual deterioration.

The first one occurs because of improper connection at the time of production or the lead being subjected to excessive stress, vibration, or impact. The second one occurs when halogenated ions (Cl^{-}) enter during production, or the capacitor is cleaned with a halogenated cleaner, or is reinforced with a resin containing halogenated compounds and halogenated substances enter the capacitor. These corrode the leads or electrode foils

until an open condition results. Third occurs when the internal electrolyte evaporates thereby causing the capacitor to dry-up. This reduces the capacitance and increases the tanδ of the capacitor. The fourth reason occurs at the end of the life of the capacitor through the process of deterioration, i.e. the final stages of degradation failure in which the electrolyte gradually penetrates through the seal causing the capacitance to drop, and tanδ to increase.

2.12.3 Short circuit

A good electrolyte quickly repairs any defect in the oxide film damage at the electrodes [2]. However, a significant amount of damage in oxide film causes local concentrations of current, and this leads to catastrophic failure, such as short circuits of the capacitor electrodes. In addition, defects such as metal or other conductive particles on electrode foils during production can provide conducting paths for the current, resulting in a short circuit of the electrodes. Moreover, mechanical stress of the capacitor leads may also lead to short-circuiting of the capacitor electrodes.

2.12.4 Degradation failure

The capacitor parameters change (capacitance decreases and ESR increases) because of emission of electrolyte from sealing surface. However, the assessment of degradation depends on the type of applications, which is further explained in detail in Chapter 3.

2.12.5 Failures of capacitor periphery

Electrolyte leaking from aluminum electrolytic capacitors may influence areas around their periphery on a PCB (especially, wiring pattern), in the following two ways:

- Disconnected pattern: The electrolyte corrodes the metal traces on the PCB board, and leads to a disconnected pattern of traces on the PCB.
- Shorted pattern: Emitted electrolyte ions from the capacitor seal may migrate between two traces under the influence of the electric field, and lead to a short circuit between traces.

A detailed chart of different failure modes of an aluminum electrolytic capacitor is shown in Figure 2.10 [7].

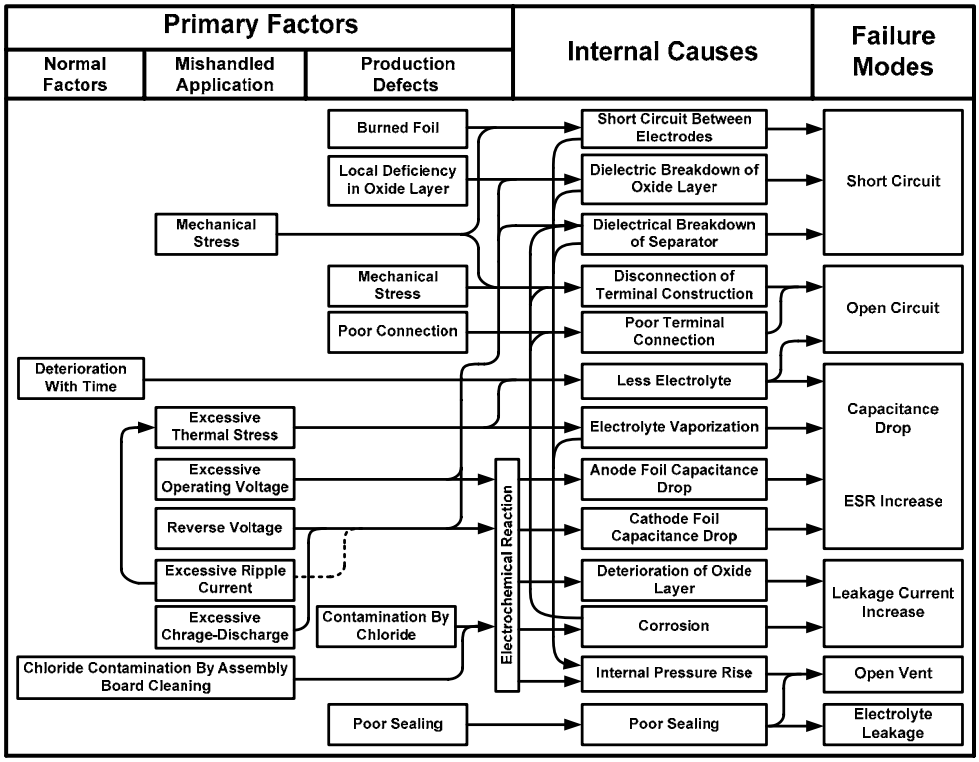


Figure 2.10 Failure modes of an electrolytic capacitor [7].

2.13 Need of condition monitoring for electrolytic capacitor

Condition monitoring is defined as the continuous evaluation of the health of the plant and equipment throughout its service life. It is important to be able to detect faults while they are still developing, called incipient failure detection. A timely warning that

can be followed by maintenance can avoid catastrophic failures and costly down times, and can provide a safe environment for human operators [18-31].

An aluminum electrolytic capacitor is often utilized to smooth the output of a switching regulator, DC bus filtering in motor drives, and in many other applications. These capacitors are generally thought to be the weak link in the life expectancy of the system, as shown in Figure 2.11 [1].

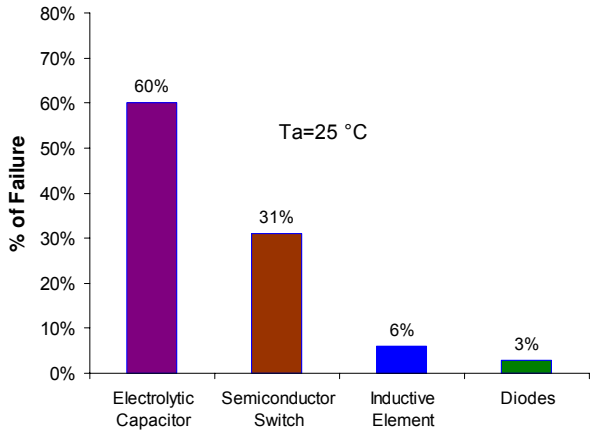


Figure 2.11 Distribution of failure for various power components [1].

Figure 2.11 displays the failure distribution of different components in a static converter. In 60% of the failures, electrolytic capacitors are responsible for the failure of the static converter. This shows that by monitoring the condition of the electrolytic capacitor can drastically improve the reliability of the static converter.

2.14 Reliability and fault detection

With the advancements in aluminum electrolytic capacitor technology, capacitors can be used in equipment that must have long life or must operate under severe conditions. For example, the capacitors used in telecommunication applications have an expected life of more than 20 years [6]. On the other side, aluminum electrolytic

capacitors have run continuously at ~130 °C for more than one year. The careful selection of a capacitor for a particular application and proper installation in the circuit will assure good service life. All components will eventually fail. Usually this occurs by a slow, steady drift of parameters called wear-out. Sometimes there is a sharp change in capacitor properties, which is called a catastrophic failure. The failure rate of aluminum electrolytic capacitors follows a bathtub curve with time, as shown in Figure 2.12 [6].

Early failures are caused by deficiencies in design, structure, manufacturing processes, or severe misapplications. Such failures occur soon after the components are exposed to circuit conditions. In aluminum electrolytic capacitors, these failures are either corrected through aging or found during the inspection process. The initial failures resulting from capacitor misapplication such as inappropriate ambient conditions, over voltage, reverse voltage, or excessive ripple current can be avoided with proper circuit design and installation.

The failure rate is the lowest during the normal useful life, as shown in Figure 2.12. The failures during this period are not related to operating time but to application conditions. Aluminum electrolytic capacitors feature fewer catastrophic failures during this period than semiconductors and solid tantalum capacitors.

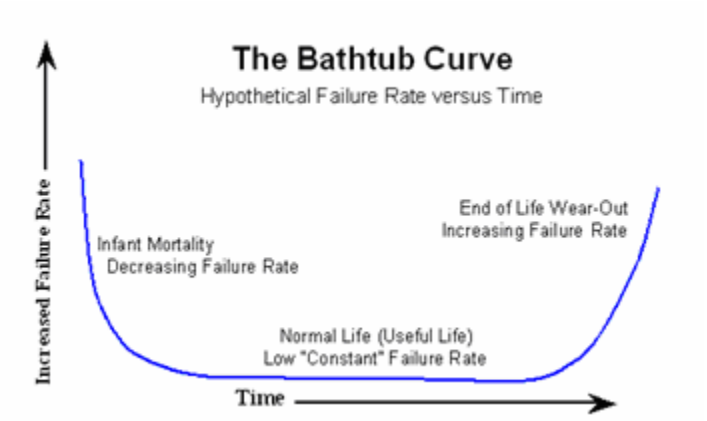


Figure 2.12 Bathtub curve [6].

The wear-out failure period is a period during which the properties of components gradually deteriorate, and the failure rate increases with time. Aluminum electrolytic capacitors end their useful life during this period. The criteria for judging failures vary with an application design factors. According to the failure criteria specified in [1], capacitance values should not fall below 80% of the rated value and the tanδ value should not change by more than 175% of its initial value. The capacitance decrease and the tanδ increase are caused by the loss of electrolyte in the wear-out failure period. This is due primarily to loss of electrolyte by diffusion (as vapor) through the sealing material. Gas molecules can diffuse out through the material of the end seal. If the electrolyte vapor pressure within the capacitor increases, by high temperatures for example, the diffusion rate increases. Swelling of the seal material by the electrolyte vapor pressure may also occur at elevated temperatures [17]. This swelling may further enhance diffusion and mechanically weaken the seal. Factors that can increase the capacitor temperature, such as ambient temperature and ripple current can further accelerate capacitor wear-out. Wear-out can also be increased by high internal pressure caused by gas generation from excessive leakage current or attack of the cathode foil by electrolyte.

In summary, the life of aluminum electrolytic capacitors depends on environmental and electrical factors. Environmental factors include temperature, humidity, atmospheric pressure, and vibration. Electrical factors include operating voltage, ripple current, and charge-discharge duty cycle. Among these factors, temperature (ambient temperature and internal heating resulting from ripple current) is the most critical to the life of aluminum electrolytic capacitors, whereas conditions such as vibration, shock, and humidity will have little effect on the actual life of the capacitor.

Voltage within the allowed operating range has little effect on the actual life expectancy of a capacitor. The life of electrolytic capacitors is affected less by applied voltage than by operating temperature. Because a capacitor is essentially an electrochemical device, increased temperatures accelerate the chemical reaction rates within the capacitor (usually a 10°C rise in temperature will double the chemical reaction rate) [17]. Therefore, higher temperatures cause accelerated changes in decreasing capacitance and increasing tanδ because of the gradual evaporation of the electrolyte through the capacitor seal. The equivalent-series-resistance change (ΔESR) can be a measure of electrolyte loss and has been found experimentally to be dependent on temperature.

2.15 Previous work

Some work is reported in the literature for the condition monitoring of electrolytic capacitors in power electronic circuits, and some of these are summarized below [18-31].

2.15.1 Diagnosis of electrolytic capacitor using capacitor ESR

The most common monitoring methods include ESR-based monitoring. Changes in chemical and physical properties of the capacitor electrolyte will affect the value of ESR [19, 20]. The conductivity of the capacitor electrolyte increases because of a rise in the temperature; hence, the value of the ESR will decrease with temperature. At the same time, higher temperature will accelerate the electrolyte vaporization. However, continued higher temperature will reduce the amount of electrolyte considerably, and it will lead to a rise in the ESR value [18, 26]. In these references, a life prediction model is presented by estimating the ESR value using the estimated core temperature of the capacitor. The value of cold ESR is calculated using

$$ESR / ESR_o = (V_o / V)^2 \tag{2.9}$$

where ESR = equivalent-series-resistance, ESR_o = initial ESR, V = volume of electrolyte, and V_o = initial volume of electrolyte.

For this model, it is important to know the accurate value of the initial electrolyte volume in the capacitor but in practice, it is difficult to know the value of electrolyte volume for each capacitor. The model presumes that the rate of electrolyte loss is directly proportional to the vapor pressure of the electrolyte, as shown in equation (2.10) [18, 26]. A constant *k* in (2.10) is used to characterize the quality of the end seal.

$$dV / dt = kP \tag{2.10}$$

where t = time (hr), k = leak rate constant (Units/mmHg/hr), P = vapor pressure of the electrolyte (mmHg)

The vapor pressures of liquids are a function of absolute temperature and chemical properties of the liquid, as shown in equation (2.11). Handbook [12] typically presents the data and tables of chemical formulas with their A and B values. Electrolytes are not simple compounds and ideally should have their A and B values measured, but the primary constituent is known to be Ethylene Glycol.

$$P = e^{\left(-\frac{A}{T}+B\right)} \tag{2.11}$$

For the Ethylene Glycol, A = 7060 and B = 21.63.

In the next step, the value of the hot ESR (ESR_{hot}) is estimated using equation (2.12). The value of the capacitor core temperature T is calculated using

$$ESR_{hot} / ESR = D + Ye^{-T/F} \tag{2.12}$$

The values of constants are experimentally found in [18] for a 400 V capacitor and it is given as

D = 0.4

Y = 5.26E+8

F = 14.23 (1/K)

The change in the capacitor core temperature is estimated as

$$T = T_{Ambient} + \Delta T \tag{2.13}$$

where $T_{Ambient}$ = Ambient air temperature (°K), and ΔT = capacitor core temperature rise. The value of ΔT can be calculated as

$$\Delta T = \frac{ESR_{hot} I^2}{H \quad S} \tag{2.14}$$

where I = Capacitor ripple-current (rms)

H = Heat transfer per unit surface area (W/m^2C)

S = Surface area (m^2)

For natural convection, the resistance from the case to the air is the largest contributor to the total thermal resistance from the element to the ambient air temperature. Typically, the radius of the element is smaller than the inside of the can, which creates a dead air space that should be accounted for. Equation (2.15) from [9] accounts for both.

$$H = \frac{G}{1 + 110R \ln(R / R_E)} \tag{2.15}$$

where R_E = element radius (m), and R = capacitor radius (m)

It is experimentally found for the sleeved capacitors [12] that

G = 6.8 ($W/m^2°C$)

Typically a capacitor would have conductive heat transfer to either a circuit board or bus bars, but for simplicity, the capacitor surface-area will be assumed to behave with natural convection. Equation (2.16) is the total surface area of the capacitor as a cylinder along with two end surfaces of the capacitor.

$$S = 2\pi(RZ + R^2) \tag{2.16}$$

where Z = capacitor height (m), R = radius of the capacitor cylinder (m).

Equation (2.10) cannot be integrated to create a closed-form equation for electrolyte volume as a function of time and other physical parameters. It can be integrated numerically using equation (2.17), where Δt is chosen to be sufficiently small. At each time step the new values for ESR, ESR_{hot}, T, and P, are calculated to establish the new volume of the electrolyte V_t for the next time step.

$$V_t = V_{t-1} - kP\Delta t \tag{2.17}$$

where Δt = Integration time step (hr)

This method proceeds until the ESR exceeds some established limit, and the device is considered to have failed; Figure 2.13 demonstrates a flow-chart for these calculations.

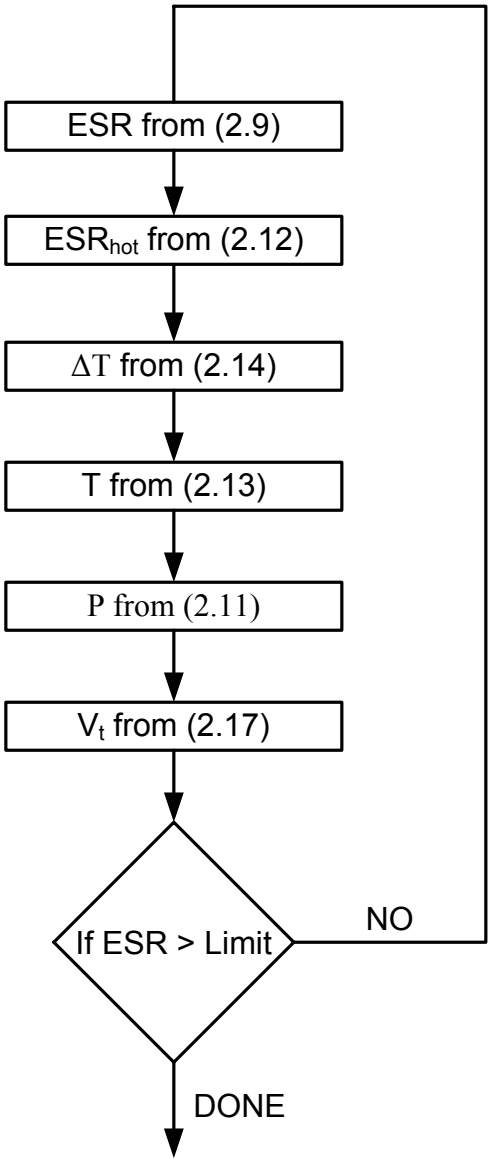


Figure 2.13 Flow-chart for the capacitor ESR estimation.

The model in [18] is based on the primary wear-out mechanism of electrolyte vaporization and loss through the end seal. The model incorporates relationships for ESR change with electrolyte loss, ESR change with temperature, and heat transfer value with geometric dimensions. Also included in the model is the effect of can diameter on the expected life. The capacitor life is proportional to the capacitor volume divided by seal circumference. As the can diameter increases, the circumference increases linearly, while

the capacitor volume increases with the square of the diameter. A detailed analysis of the work in [18] is presented in [21], which shows that the model in [18] overpredicts the life of the electrolytic capacitor. The electrolyte leakage and electrolyte deterioration characteristics have to be further understood and models should account for continuous and intermittent operation of the component [21].

2.15.2 Diagnosis of electrolytic capacitor using voltage and current signature

A change in the value of capacitor ESR will affect the capacitor ripple current and voltage waveforms. Harada et al. [22] used two DC/DC converters to show how the capacitor voltage and current waveforms can be used to monitor the condition of an electrolytic capacitor. In this work [22], it is assumed that the time constant of the circuit is substantially longer than the period of the switching, and the state averaging method is used to calculate the capacitor ripple voltage and current. The ratio, γ_1, of the capacitor ripple voltage and ripple current is plotted with load current for a normal and deteriorated capacitor, as shown in Figure 2.14. Harada et al. show that the ratio, γ_1, is directly proportional to the value of the capacitor ESR, therefore, it can be used for condition monitoring of the capacitor [22]. However, it should be noted that it uses the converter mathematical model to estimate the capacitor voltage and current [22]. Therefore, it is dependent on the converter topology, and the model should be modified before using it in different circuit topologies.

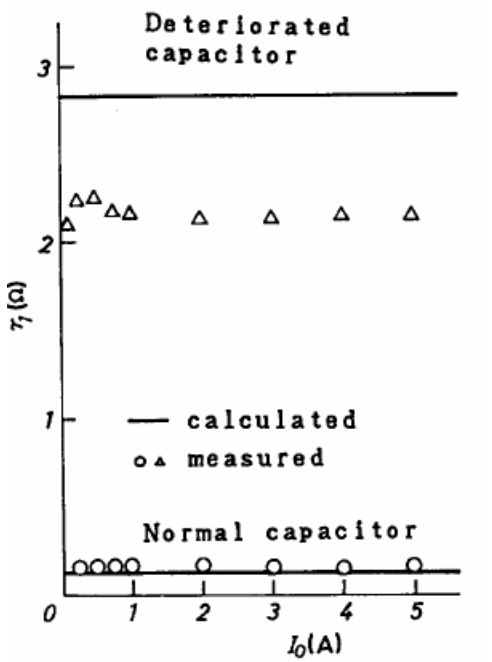


Figure 2.14 γ_1 versus load current, I_o (where γ_1 = (ripple-voltage peak to peak)/ ripple current peak to peak)).

The value of the capacitor ripple-voltage is directly proportional of the capacitor ESR. Using this concept, Lahyani et al., [23-25] present an alternate algorithm to predict the failure of an electrolytic capacitor in a static converter using capacitor ripple voltage. In order to justify the aging status of the electrolytic capacitor, P. Venet [24] compared the measured ESR, determined by capacitor voltage and current, with the pre-calculated ESR, which is determined by the measured ripple voltage, ripple current, and operation temperature of a sound one. To avoid the wrong prediction caused by the load variation, Lahyani et al. proposed a computer-aided approach to determine a more accurate ESR. They [23] use a computer model along with capacitor ripple voltage at switching frequency, and temperature to estimate the ESR value of the capacitor. The model in [23] uses *Arrhenius' law* [27] along with a *linear inverse model* for the ESR [18, 28] to develop a computer program. The computer program can predict and show the capacitor's lifetime directly on a display-panel. It [23] presents a detailed algorithm to

estimate the value of the ESR for stationary system for any combination of load and operating temperature [23-25]. However, implementation of this method is difficult and expensive and it cannot be used for a non-stationary system because the model uses filtered components of the capacitor ripple voltage at the switching frequency, and the switching frequency is not constant in a non-stationary system.

The work reported in [31] presents a method to determine the electrolytic capacitor parameter for an LC-filter type of applications. However, the presented work cannot be used for a real-time monitoring scheme because the capacitor has to be taken out of the circuit to measure the deterioration in the capacitor parameters. An external power source with varying frequency is utilized to estimate the parameters of the capacitor.

Most of these reported works [18-31] address the detection of a failure because of aging of the capacitor. In addition, these schemes depend on the circuit topologies, are computationally demanding, and therefore, difficult to use in actual application.

2.16 Summary

This chapter has briefly reviewed the construction, electrical characteristics, and operation of an electrolytic capacitor. Further, a description has been presented of various kinds of faults that can occur in an electrolytic capacitor. Some methods available to detect such faults in an electrolytic capacitor have been discussed. Various ESR estimation-based techniques available to detect the capacitor faults have been reviewed. Most of the presented works are offline techniques, and cannot be used in real-time. In the next few chapters, new offline techniques are proposed, followed by parameter estimation technique for real-time fault monitoring.

CHAPTER 3

FFT BASED FAILURE PREDICTION OF AN ELECTROLYTIC CAPACITOR

3.1 Introduction

The objective of this chapter is to identify experimentally potential capacitor failure by observing capacitor terminal quantities such as ripple voltage and ripple current. An electrolytic capacitor is considered failed if the value of the capacitance goes below 80% of its rated value and the ESR goes above 175% of the rated value [1].

3.2 Experimental setup

A basic boost converter with constant load, Figure 3.1, is used to carry out experiments on the aging of an electrolytic capacitor. The experimental setup for the boost converter is shown in Figure 3.2, and the *National Instrument* (NI) data acquisition system appears in Figure 3.3. The switching frequency is held constant at around 10 kHz with a duty cycle of 0.6. The capacitor is placed in a temperature controlled oven at 115 °C for accelerated aging, Figure 3.4. The capacitor voltage, the switching-signal, and the capacitor current appear in Figure 3.5. The sampling rate for data acquisition is 100 kHz which is well above the *Nyquist limit*. Moreover, aging of an electrolytic capacitor is a slow process, and a continuous data-acquisition will result in a large amount of data for further processing. It also requires large memory space to store this data. However, due to

the slow aging process, 5000 points of data are captured at 15 minute intervals to ensure an efficient use of the memory. With 100 kHz sampling frequency and 10 kHz switching frequency, 5000 data points amounts to 50 milliseconds of time duration. This gives sufficient resolution in the frequency domain because the minimum frequency in the system is 120 Hz, and this corresponds to around 8.3 ms.

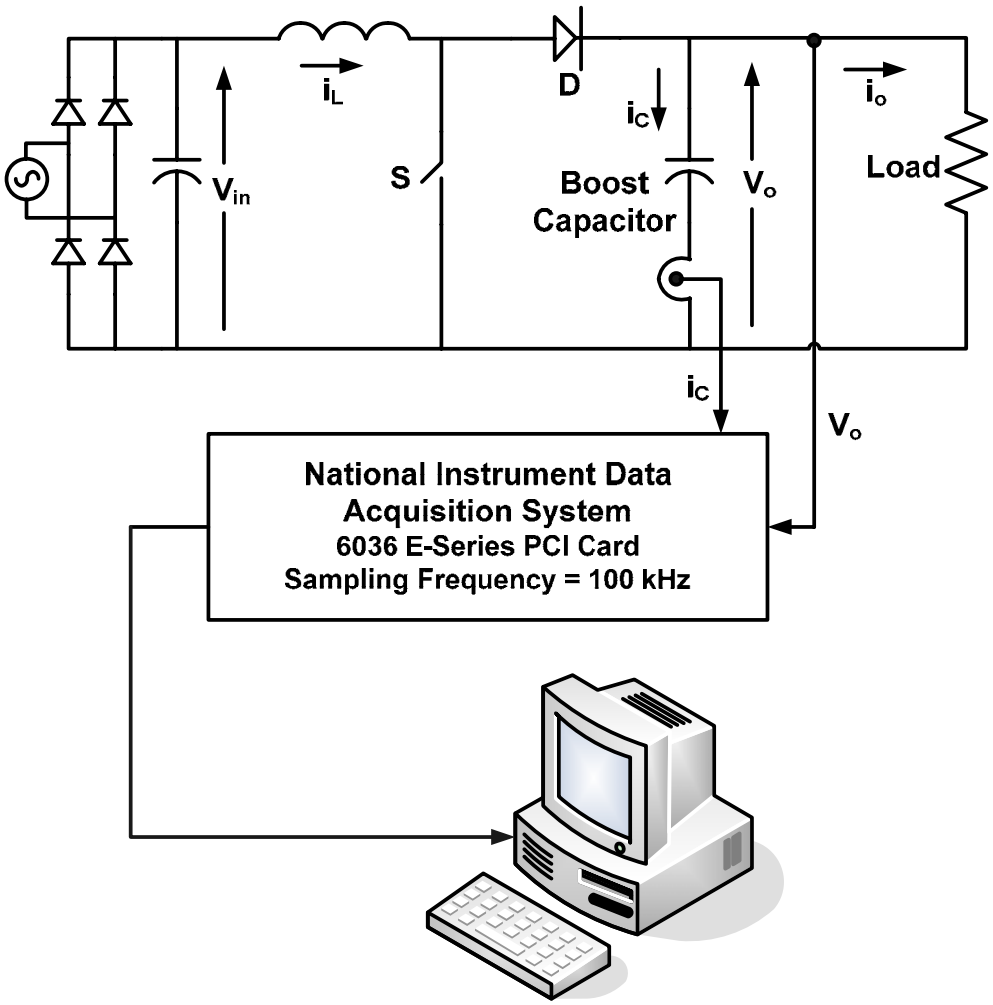


Figure 3.1 Boost-converter.

It is demonstrated in section 3.2 that the capacitor aging process can be monitored by storing 5000 points at any given point of time, and it does not require storing any previous data. The NI data acquisition card 6036E along with Labview 7.1 is used for

acquiring the data. A detailed description of the data acquisition card 6036E is given in Appendix A.

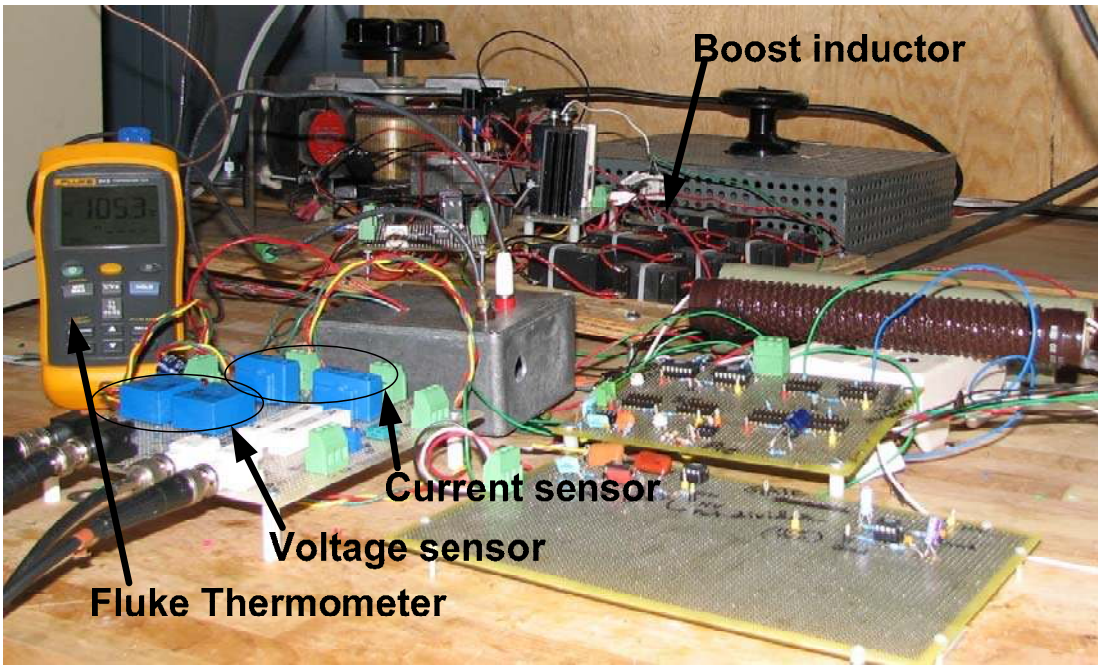


Figure 3.2 Boost converter experimental setup.

Figure 3.3 Interface with NI data acquisition system.

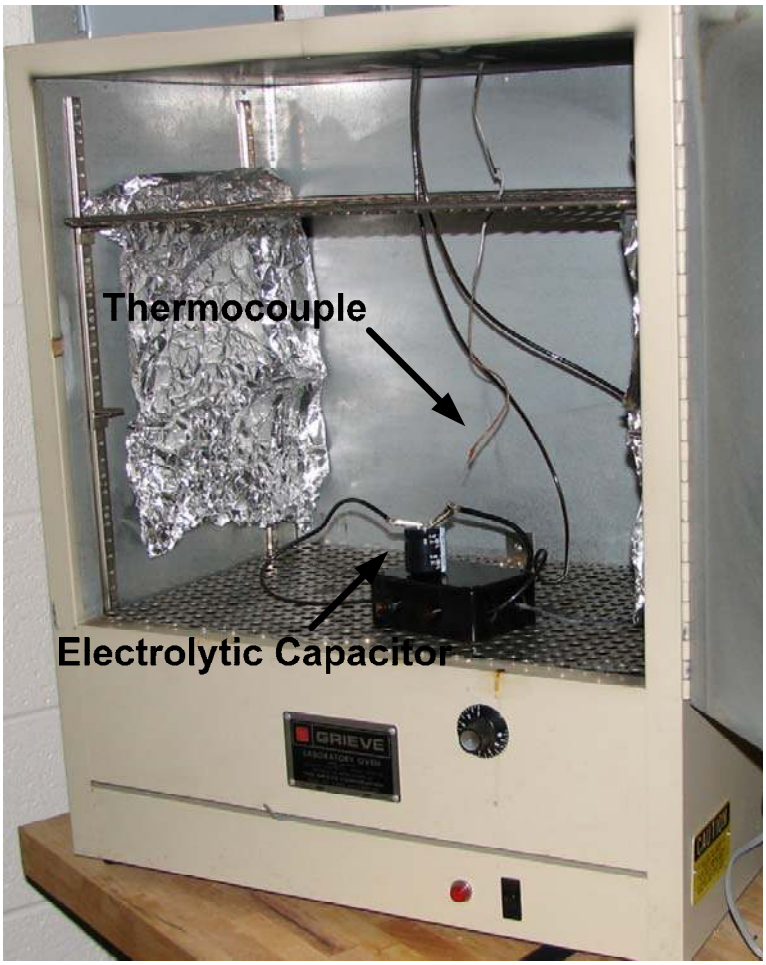


Figure 3.4 Temperature controlled oven.

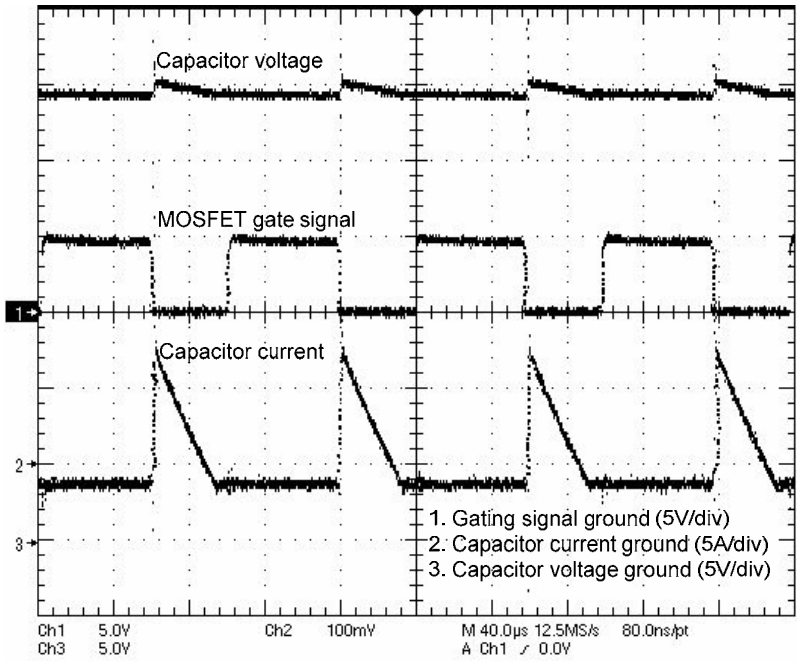


Figure 3.5 Waveforms of capacitor voltage, switching-signal, and capacitor current.

The amplitude of the capacitor ripple voltage and current change because of a variation in the capacitor parameters. To observe the changes in these parameters over time because of aging, an electrolytic capacitor rated at 100 µF, 63 V, 85 °C is tested.

Further, the test is repeated with other electrolytic capacitors, and it is observed that the results in this chapter are similar and consistent with results for other electrolytic capacitors. Each test is run for several days until there are significant changes in the capacitor ripple-voltage and ripple-current.

3.3 Experimental results and discussion

Table 3.1 shows the measured values of the capacitor parameters before and after aging for an electrolytic capacitor rated at 100 µF, 63 V, 85 °C. The capacitance decreases by more than 1000 times, while ESR increases by about 11 times, after about 575 hours of continuous accelerated aging process, and these changes affects the

capacitor ripple voltage and ripple current. The Bode-plots of the capacitor impedance for new and worn-out condition are shown in Figure 3.6 and 3.7 respectively. Bode-plots of the capacitor impedance are plotted using a *4194A HP Impedance Analyzer,* and the frequency is swept from 100 Hz to 4 MHz. Bode-plots are showing the variation in impedance and corresponding phase-angle frequency for a new capacitor and a worn-out capacitor.

Table 3.1 Electrolytic capacitor parameters of new and worn out capacitor

	New Capacitor	Worn out Capacitor (at 575 hours)
Capacitance (C)	98.65 µF	89.23 nF
Effective Series Resistance (ESR)	317.85 mΩ	3.69 Ω

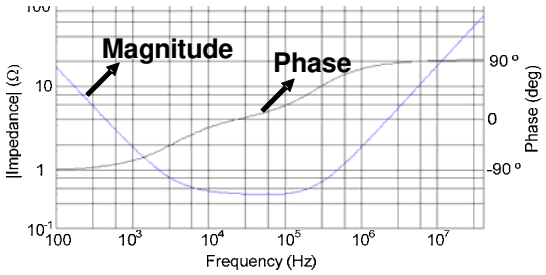


Figure 3.6 Bode plot of a new capacitor.

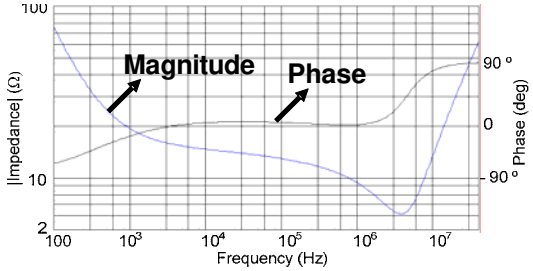


Figure 3.7 Bode plot of a worn-out capacitor at 575 hours.

The effect of the parameter changes will reflect in the capacitor voltage and the capacitor current waveforms. Therefore, capacitor ripple voltage and current are monitored to monitor the condition of the capacitor.

Fast-Fourier-transforms (FFT) plots for the capacitor ripple-voltage and capacitor ripple current are calculated as shown in Figure 3.8 and 3.9 respectively. As expected, it

can be observed from these plots that the dominant components of the capacitor ripple voltage and the capacitor ripple current are present at integer multiples of the switching frequency of 10 kHz.

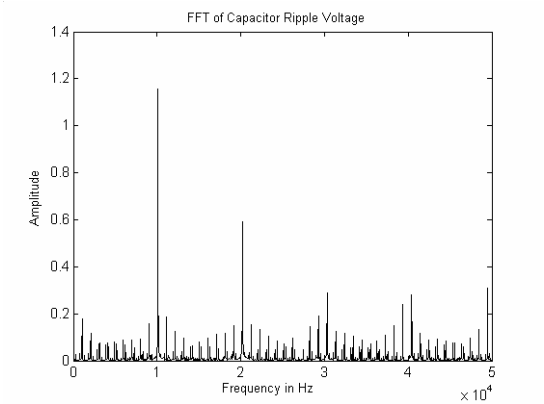


Figure 3.8 FFT plot for capacitor ripple voltage.

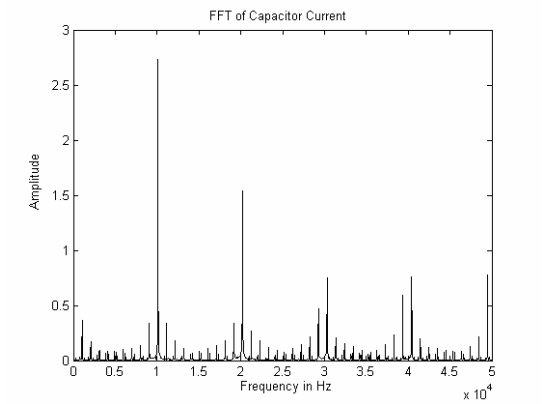


Figure 3.9 FFT plot for capacitor current.

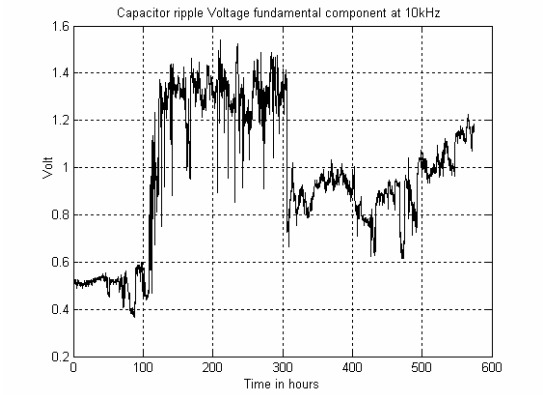


Figure 3.10 Capacitor ripple-voltage fundamental component at 10 kHz variation with time.

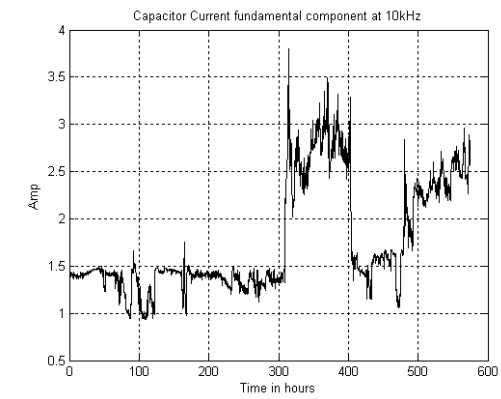


Figure 3.11 Capacitor current fundamental component at 10 kHz variation with time.

As explained in the previous section, the value of the capacitor parameters will change over time because of the aging effect [22, 32]. These changes in the parameter values will result in variations in the different frequency components of the capacitor ripple voltage, and the capacitor ripple current. In the proposed technique, only the variations in the fundamental frequency component are used to monitor the health of the capacitor. The fundamental frequency components of the capacitor ripple voltage and capacitor ripple current are plotted over time in Figures 3.10 and 3.11 respectively. Further, data in Figures 3.10 and 3.11 are used to plot the evolution of the impedance parameter over time in Figure 3.12, which is calculated using (3.1).

$$Z(n) = \frac{V(n)}{I(n)} \tag{3.1}$$

where $V(n)$ = RMS value of fundamental component of capacitor ripple voltage at any time n

$I(n)$ = RMS value of fundamental component of capacitor ripple current at any time n

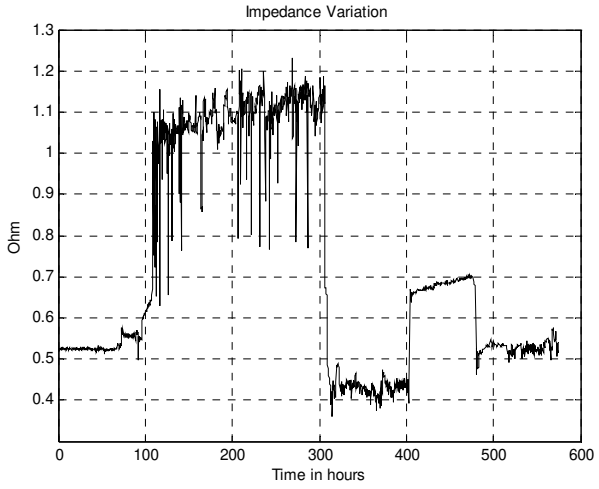


Figure 3.12 Capacitor impedance variation over time.

A significant change in the capacitor parameters starts to appear after 100 hour of operation and is reflected in the capacitor ripple voltage. It is observed that the fundamental frequency component of the capacitor ripple voltage changes significantly during the period from 100 to 125 hours of continuous operation, as shown in Figure 3.10. However, it is observed that there are not large changes in the capacitor parameters during the period from 125 to 300 hours of operations. During this period, the electrolyte is vaporizing at a much faster rate and the capacitor fails after 300 hours of operation. In addition, it can be seen in Figure 3.11 that there is a large change in capacitor ripple current at around 300 hours, and it is believed that this is because of the breakdown in the dielectric oxide layer of the capacitor, which results in a large rise in the capacitor ripple current. Therefore, plots in Figures 3.10 and 3.11 together show that there are significant changes in the capacitor ripple voltage and ripple current because of changes in the capacitor parameters. However, these plots are oscillatory in nature, and it is difficult to set a threshold point for the fault prediction. This problem can be solved by using a time-average plot for the fundamental component of the capacitor ripple voltage and the ripple current.

The time-average formula can be written as

$$V_{TA}(n) = \frac{\sum_{k=1}^{n} V(k)}{n} \tag{3.2}$$

where $V(k)$ = Capacitor ripple-voltage sample at any given instant k.

$V_{TA}(n)$ = Time-average capacitor ripple-voltage at any given time n.

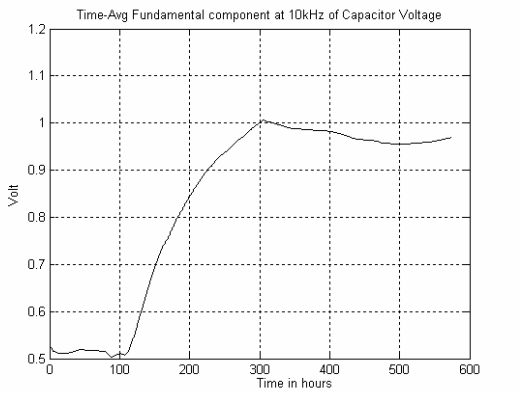


Figure 3.13 Time-average plot of RMS values of fundamental component of the capacitor ripple voltage.

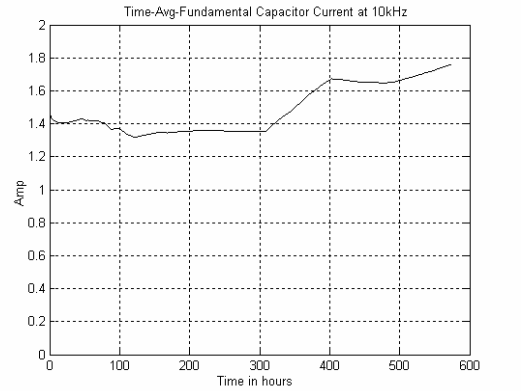


Figure 3.14 Time-average plot of RMS values of fundamental component of the capacitor ripple current.

The time-average formula is further used to calculate the time-average value of the capacitor impedance. Figures 3.13, 3.14 and 3.15 show the time-average plots for the fundamental components of the capacitor ripple voltage, capacitor ripple current, and capacitor impedance respectively.

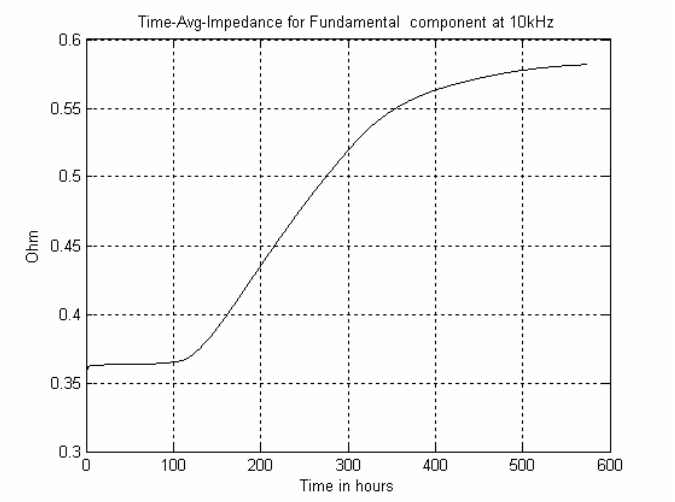


Figure 3.15 Time-average plot of capacitor impedance.

Equation (3.2) appears computationally intensive, but it can be simplified further as

$$V_{TA}(n) = \frac{V(n) + \sum_{k=1}^{n-1} V(k)}{n} \tag{3.3}$$

Using equation (3.2) in (3.3), and re-arranging it yields

$$V_{TA}(n) = \frac{V(n) + (n-1)V_{TA}(n-1)}{n} \tag{3.4}$$

Equation (3.4) allows a significant reduction in the required memory for actual implementation of the algorithm, as it is required to store only two data points.

By comparing the plots in Figures 3.13, 3.14, 3.15 with the plots in Figures 3.10, 3.11 and 3.12, it is clear that changes in the capacitor parameters are taking place at the same instant of time for time-average plots compared to the instantaneous time plots. However, the time-average plots are monotonic in nature, and it is easier to observe the status of the capacitor.

3.4 Summary

The effect of changes in the ESR, and the capacitance value of the electrolytic capacitor are reflected in the capacitor ripple voltage and capacitor ripple current. It has been demonstrated that the capacitor ripple voltage signature analysis techniques can be applied to the diagnosis of an electrolytic capacitor in a power converter. In some applications, access to capacitor ripple voltage is not possible; however, it can be estimated by using some other accessible signals in the system, which is explained in next chapter.

CHAPTER 4

FAILURE PREDICTION OF AN ELECTROLYTIC CAPACITOR USING SYSTEM MODELING

4.1 Introduction

This chapter is an extension of the work presented in Chapter 3. It was demonstrated in Chapter 3 that the effect of the changes in the capacitor parameters will reflect in the capacitor ripple voltage and the ripple capacitor current. Therefore, it was concluded that the capacitor ripple voltage and the capacitor ripple current signature analysis could be used in the diagnosis of an electrolytic capacitor. In this chapter, it is demonstrated that the converter input current can also be used to predict the failure of the output side capacitor using the converter system modeling and the principles of correlation among various signals in the system [37-40], which is further explained in later sections of this chapter.

4.2 Experimental setup

The basic boost converter with constant load, as in Chapter 3, is used to carry out experiments on the aging of the electrolytic capacitor. However, a different electrolytic capacitor with rating 100 volt, 85 °C, 1000 μF by Panasonic is used as the boost-capacitor. The experimental setup is similar to that in Chapter 3 but the sampling rate for

data acquisition is 20,000 samples per second. As aging of an electrolytic capacitor is a slow process, therefore, at every 15 minutes interval 10,000 points are captured using the *National Instrument* (NI) data acquisition system, which is similar to the system described in Chapter 3. These 10,000 data points represent 500 ms for a sampling rate of 20,000 samples per second. The switching frequency is held constant at around 5 kHz with a duty cycle of 0.6. The capacitor is placed in a temperature-controlled oven at around 115 °C for accelerated aging.

4.3 Theory of system modeling

In the presented work, it is assumed that the electrolytic capacitor installed in the system is not accessible; therefore, the capacitor ripple voltage required for the condition monitoring technique demonstrated in Chapter 3 cannot be implemented. However, the system input voltage and the input current can be accessed. It is demonstrated in this section that capacitor ripple voltage can be estimated using converter input current.

Figure 4.1 depicts the block diagram of an adaptive filter. *G(z)* represents an actual physical plant, and *W(z)* is the digital model of the actual system *G(z)*. The aim is to estimate the parameters of the model *W(z)*. Based on a-priori knowledge of the plant, *G(z)*, a transfer function *W(z)*, with a certain number of adjustable parameters is selected first. The parameters of *W(z)* are then chosen through an adaptive filtering algorithm such that the difference *e(n)* between the plant output *d(n)*, and the adaptive filter output *y(n)*, is minimized. In this application, the circuit of Figure 3.1 is the actual system *G(z)*, which is being modeled using the digital filter *W(z)*.

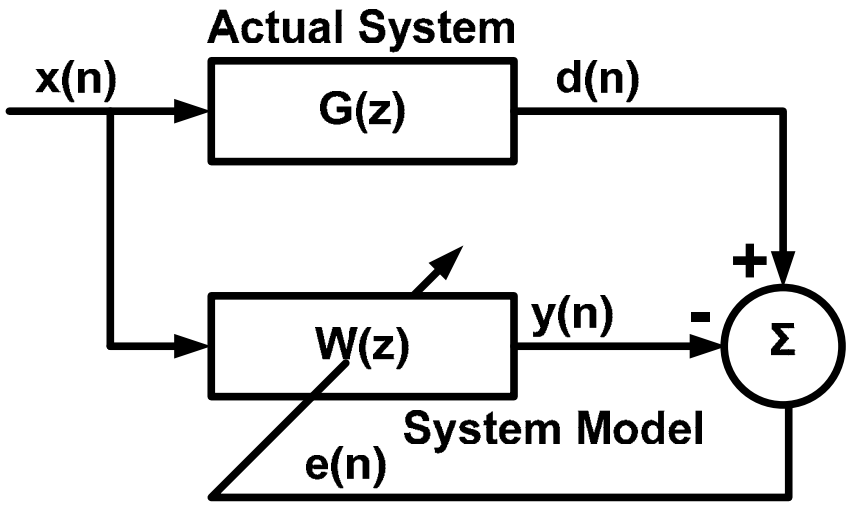


Figure 4.1 Structure of the adaptive filter model.

4.3.1 Correlation coefficient [38]

In a system, various signals correlate with each other to varying degrees. Therefore, it is possible to estimate a signal that is not easily accessible in a system using other signals of the system, if the signals are strongly correlated with each other. Moreover, the amplitude of the error between the actual and the estimated signal depends on the value of the correlation coefficient between the signals [39-41]. Further, it is demonstrated that the capacitor ripple voltage is strongly related to the input current of the converter compared to input voltage. Therefore, it is possible to estimate the capacitor ripple-voltage with a small error using the converter input current.

Figure 4.2 demonstrates the cross correlation coefficient (using a MATLAB function) variation between input voltage, v_{in}, in Figure 3.1, and the capacitor ripple-voltage, v_o; the converter input current, i_{in}, and the capacitor ripple-voltage, v_o. It also shows that there is a stronger correlation between i_{in} and v_o compared with the correlation between v_{in} and v_o. This property is used in section 4.4 to demonstrate that the input current of the converter can be used to predict the failure of the capacitor in a converter,

by using adaptive filter modeling. First, a general least-mean-square-error (LMS) based adaptive filter theory is presented in sections 4.3.2 and 4.3.3, followed by derivation of the results in section 4.4.

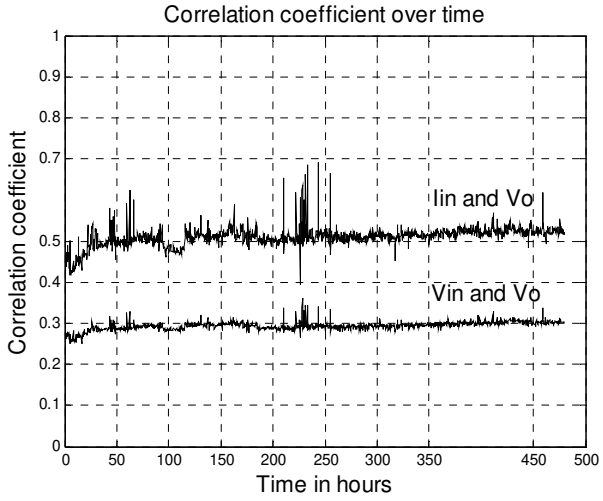


Figure 4.2 Correlation coefficient plots over time.

4.3.2 LMS based Wiener adaptive filter theory

According to the Wiener filter theory [41], which comes from the stochastic framework, the optimum coefficients of a linear filter are obtained by minimization of its mean-square-error (MSE). The *Least-mean-square* (LMS) algorithm is the most basic and widely used algorithm in various adaptive filtering applications, and uses the instantaneous value of the square of the error signal as an estimate of the MSE. It turns out that this rough estimate of the MSE, when used with a small step-size parameter in searching for the optimum coefficients of the Wiener filter, leads to a simple and yet reliable adaptive algorithm [41].

4.3.3 Derivation of the LMS algorithm

Figure 4.3 depicts an *N*-tap transversal adaptive filter [41]. The filter input, *x(n)*, the desired output, *d(n)*, and the filter output, *y(n)*, are related as,

$$y(n) = \sum_{i=0}^{N-1} w_i(n)x(n-i) \tag{4.1}$$

The tap weights $w_o(n)$, $w_1(n)$,……, $w_{N-1}(n)$ are selected so that the difference *e(n)* (error), is minimized in some sense.

$$e(n) = d(n) - y(n) \tag{4.2}$$

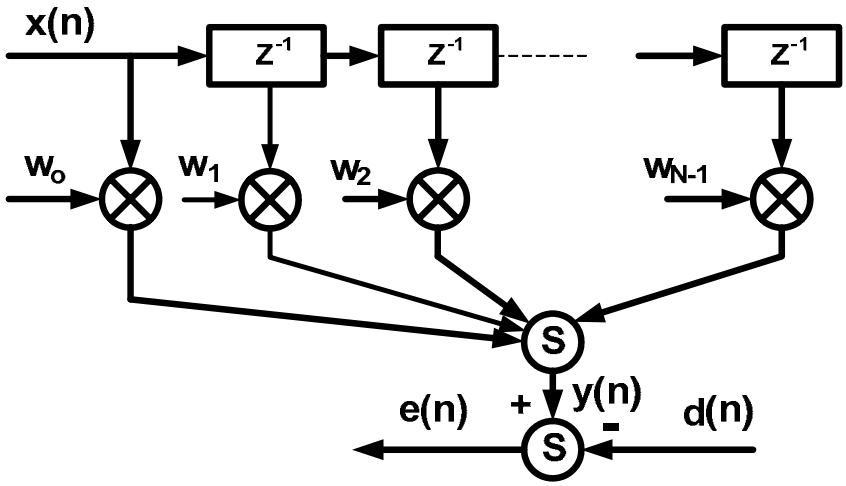


Figure 4.3 FIR based adaptive filter model.

The filter tap weights, shown in Figure 4.3 and equation (4.3) are functions of the time index, *n*, since they are continuously being adapted so that any variations in the signal's statistics could be tracked. The LMS algorithm changes the filter tap weights so that *e(n)* is minimized in the mean-square sense. The filter tap-weights and input vectors are defined by column vectors as,

$$\mathbf{w} = [w_o\, w_1 \ldots w_{N-1}]^T \tag{4.3}$$

and $$\mathbf{x}(n) = [x(n)\, x(n-1) \ldots x(n-N+1)]^T. \tag{4.4}$$

The filter output is, $$y(n) = \mathbf{w}^T\mathbf{x}(n). \tag{4.5}$$

The conventional LMS algorithm is a stochastic implementation of the steepest descent algorithm. It replaces the cost function $\xi = E[e^2(n)]$ by its instantaneous coarse estimate $\xi \approx [e^2(n)]$ in a steepest-descent recursion. Hence the tap-weight vector is updated as,

$$\mathbf{w}(n+1) = \mathbf{w}(n) - \mu \nabla e^2(n) \tag{4.6}$$

where μ is the algorithm step-size parameter and ∇ is the gradient operator defined as the column vector,

$$\nabla = \left[\frac{\partial}{\partial w_o} \quad \frac{\partial}{\partial w_1} \quad \cdots \quad \frac{\partial}{\partial w_{N-1}} \right]^T \tag{4.7}$$

The i^{th} element of the gradient vector $\nabla e^2(n)$ is

$$\frac{\partial e^2(n)}{\partial w_i} = 2e(n)\frac{\partial e(n)}{\partial w_i} \tag{4.8}$$

From equation (4.2) and (4.5),

$$\frac{\partial e(n)}{\partial w_i} = -x(n-i) \tag{4.9}$$

Using equation (4.9) in equation (4.8) yields,

$$\frac{\partial e^2(n)}{\partial w_i} = -2e(n)x(n-i) \tag{4.10}$$

which can be written further in vector form as,

$$\nabla e^2(n) = -2e(n)\mathbf{x}(n) \tag{4.11}$$

Substituting (4.11) in (4.6) results in,

$$\mathbf{w}(n+1) = \mathbf{w}(n) + 2\mu e(n)\mathbf{x}(n) \tag{4.12}$$

This is referred to as the LMS recursion. It suggests a simple procedure for recursive adaptation of the filter coefficients after the arrival of every new input sample,

x(n), and its corresponding desired output sample, *d(n)*. Equations (4.1), (4.2), and (4.12), specify the three steps required to complete the iteration steps of the LMS algorithm. Equation (4.1) is referred to as filtering. It is performed to obtain the filtered output of any signal. Equation (4.2) is used to calculate the estimation error. Equation (4.12) is the tap-weight adaptation recursion. The LMS algorithm is simple to implement as an adaptive filtering scheme. Its implementation requires $2N+1$ multiplications (N multiplications for calculating the output $y(n)$, one to obtain $(2\mu)\times e(n)$ and N for the scalar-by-vector multiplication $(2\mu e(n)) \times \mathbf{x}(n)$) and $2N$ additions, where N is the order of the filter. By trial and error it is found that $N=10$ as the filter order gives a preferred filter tap-weights to model the converter system.

4.4 Results and discussion

The equivalent circuit parameters of the 1000 μF capacitor are measured at the beginning and after 480 hours of aging using an HP impedance analyzer.

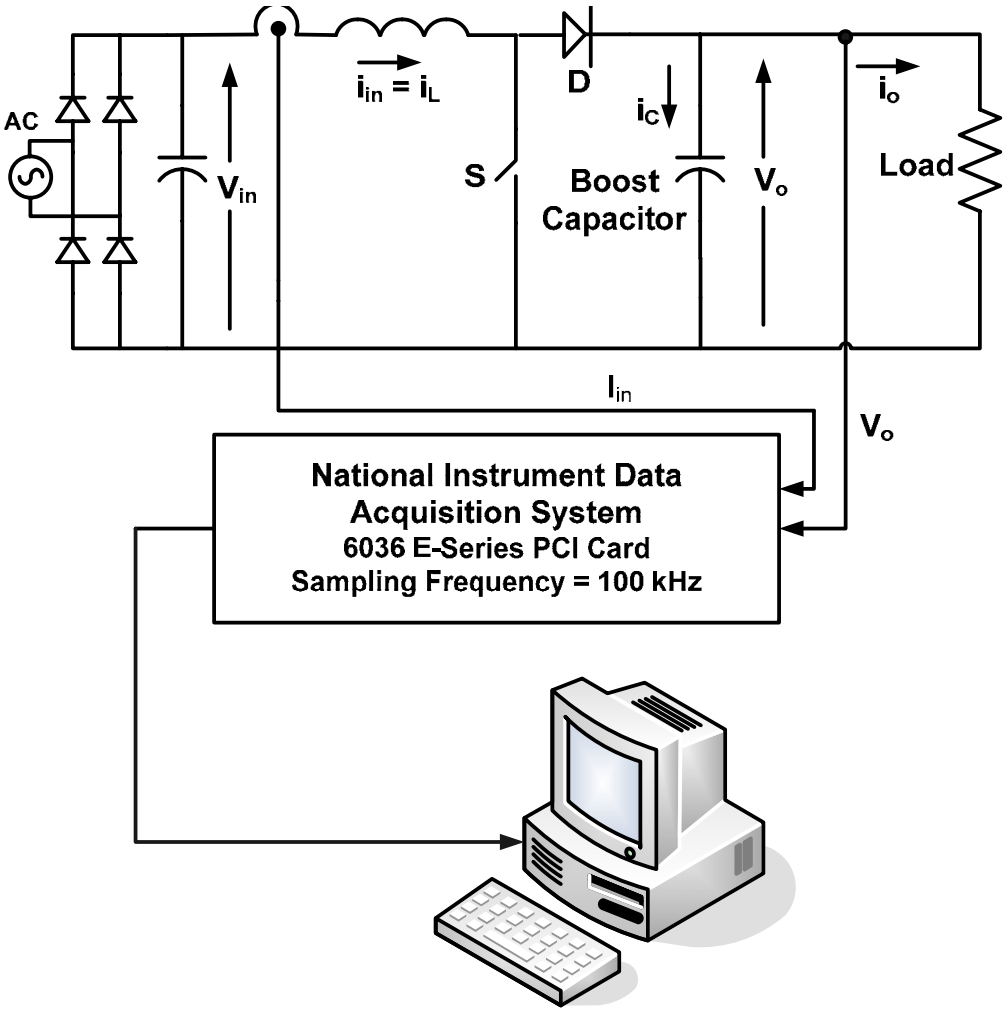


Figure 4.4 Boost-converter circuit.

A block diagram to model the system is shown in Figure 4.1. An FIR filter, Figure 4.3, with order $N = 10$ is used to model the $W(z)$ of the DC/DC boost-converter in Figure 4.4 in order to estimate the output side boost-capacitor ripple voltage, v_o, using the input current, i_{in}.

The adaptive filter tap-weights are estimated using the LMS algorithm with a step-size of μ=0.005 using equation (4.12). The input ripple current, i_{in}, is used as the input signal, $\mathbf{x}(n)$, and the capacitor ripple voltage, v_o, is used as the output signal, $d(n)$, to determine the tap-weights of the adaptive filter by recursive adaptation. Around 2000

data files, which are captured during the aging process as explained in section 4.2, are used to train the tap-weights recursively. Each of these data files contains 10000 points of capacitor ripple voltage; hence, a total $2000\times10000=20\times10^6$ data points are used for this adaptation. The LMS algorithm for filter order $N = 10$ can be written in the mathematical form for this application as follows:

Input,

$$\mathbf{x}(n)=\begin{bmatrix} i_{in}(n) \\ i_{in}(n-1) \\ \vdots \\ i_{in}(n-9) \end{bmatrix} \tag{4.13}$$

Estimated output,

$$y(n) = \mathbf{w}^{\mathrm{T}}(n)\mathbf{x}(n) \tag{4.14}$$

Tap weights,

$$\mathbf{w}(n)=\begin{bmatrix} w_o(n) \\ w_1(n) \\ \vdots \\ w_9(n) \end{bmatrix} \tag{4.15}$$

Actual output of the system,

$$d(n) = v_o(n) \tag{4.16}$$

Error signal,

$$e(n) = d(n) - y(n) \tag{4.17}$$

Weight update,

$$\mathbf{w}(n+1) = \mathbf{w}(n) + 2\mu \mathrm{e}(n)\mathbf{x}(n) \tag{4.18}$$

Figures 4.5 and 4.6 show the FFT plots for the actual and the estimated capacitor ripple voltage. The adaptive filter model is able to estimate the fundamental component at 5 kHz accurately with only a small error as shown in Figures 4.5 and 4.6.

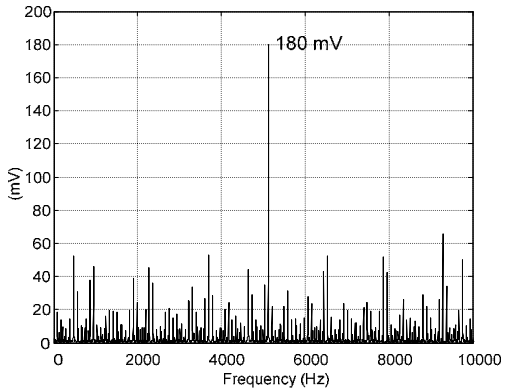


Figure 4.5 FFT plot for actual capacitor ripple voltage.

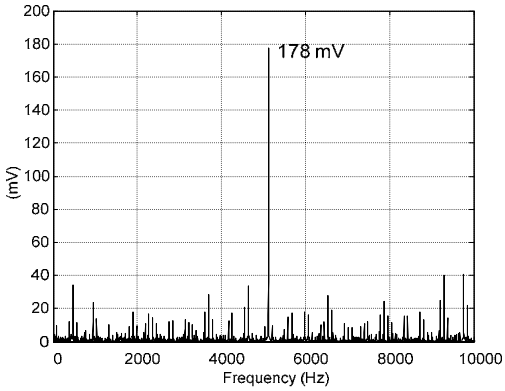


Figure 4.6 FFT plot for estimated capacitor ripple voltage.

A portion of the RMS value of fundamental component of actual and estimated capacitor ripple-voltage plot over time is shown in Figure 4.7. It can be seen that the actual and the estimated fundamental components are tracking well with only a small error shown in Figure 4.8.

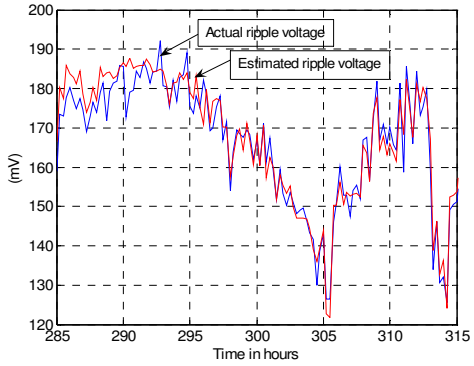


Figure 4.7 Portion of actual and estimated fundamental component of capacitor ripple voltage.

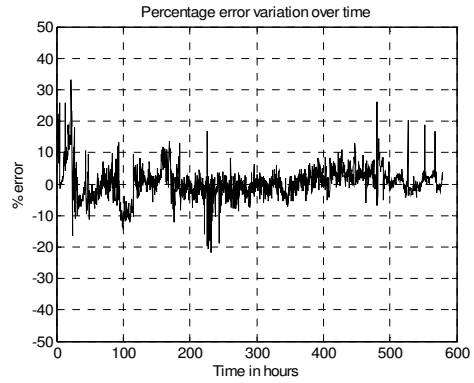


Figure 4.8 Percentage error variations over time.

The proposed time-average formula (3.4) in Chapter 3 is used to draw the time-average plot for the RMS value of fundamental components of actual and estimated capacitor ripple-voltage as shown in Figures 4.9 and 4.10 respectively. The proposed system modeling technique estimates the value of the capacitor ripple voltage accurately with only a small error using the input current of the converter, as shown in Figure 4.8. Therefore, a digital modeling technique can be used in condition monitoring of the electrolytic capacitor where capacitor ripple voltage is not accessible.

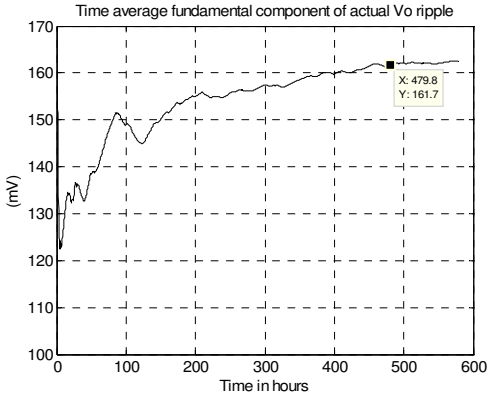


Figure 4.9 Time-average evolution of fundamental component of actual capacitor ripple voltage.

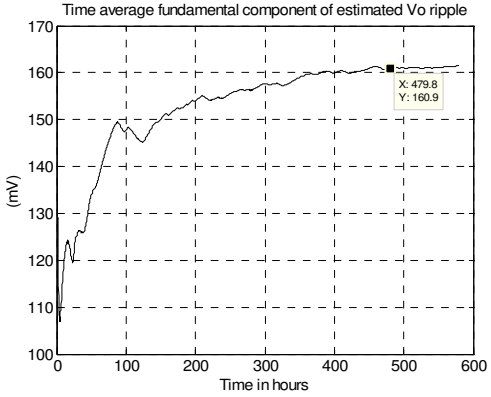


Figure 10 Time-average evolution of fundamental component of estimated capacitor ripple voltage.

4.5 Summary

Any drift in the capacitor parameters also appear in the converter input current along with the capacitor ripple-voltage because these two signals are strongly correlated. Therefore, it has been demonstrated that the converter input current can be used to predict the failure of the capacitor. The research works presented in Chapters 3 and 4 are offline techniques for monitoring the condition of an electrolytic capacitor. A real-time fault-monitoring scheme is presented in Chapter 5.

CHAPTER 5

CONDITION MONITORING OF ELECTROLYTIC CAPACITOR BY PARAMETER ESTIMATION

5.1 Introduction

Chapter 3 has demonstrated that the capacitor ripple voltage and ripple current can be tracked to monitor the condition of an electrolytic capacitor. However, it cannot give real-time monitoring information of an electrolytic capacitor, and in addition, cannot give correct information of the condition of an electrolytic capacitor used in a non-stationary system. The objective of this chapter is to propose a new low cost method to detect the changes in the equivalent series resistor (ESR) and the capacitance value of an electrolytic capacitor in order to realize a real-time condition monitoring system for an electrolytic capacitor. Results are discussed to illustrate the proposed condition monitoring technique for a stationary system; however, the proposed technique can also be used for a non-stationary system. The proposed on-line failure prediction method has the merits of low cost and circuit simplicity.

As explained in previous chapters, the electrolytic capacitors have been widely used in power electronics systems because of the features of large capacitance, small size, high-voltage, and low-cost. An electrolytic capacitor provides a low impedance path for the ac current and acts as a constant voltage source in power converters. Because of an

increase in the ESR for an aged electrolytic capacitor, the capacitor will not be able to provide a low impedance path for the ac current. Therefore, the ripple voltage across it will increase, and eventually the converter will fail to regulate the dc output voltage or even damage the converter itself. In addition, the capacitance value also changes because of the changes in the dielectric properties of the oxide layer and reduction in the amount of capacitor electrolyte. The Military Handbook [1] suggests that the capacitor should be considered as failed if there is a 20% decrease in the capacitance value, and the ESR has doubled from its initial value. Therefore, the estimation of the ESR and the capacitance are important parameters in condition monitoring of the capacitor. The main advantages of the proposed method include circuit simplicity, low-cost, and easy implementation. In the following sections, simulation results are presented to explain the proposed method. In addition, the circuit implementation of the proposed electrolytic capacitors failure-detection method is introduced.

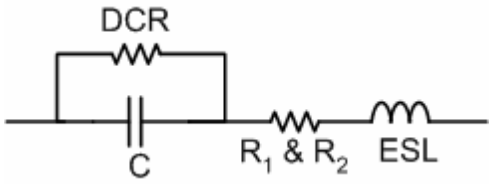


Figure 5.1 Electrolytic capacitor equivalent circuit.

The equivalent circuit of an aluminum electrolytic capacitor shown earlier in Figure 2.4, is repeated in Figure 5.1, where C = capacitance, R_1 = resistance of the foil and terminals, R_2 = temperature sensitive resistance due to electrolyte, DCR = dielectric leakage resistance, and ESL = equivalent series inductance. Equation (5.1) was derived in section 2.5.4 of chapter 2 to describe the complex impedance of the circuit in Figure 5.1.

$$Z_{cap} = \left[\frac{DCR}{1+(2\pi f)^2 C^2 DCR^2}\right] + R_1 + R_2 + \frac{1}{j2\pi fC\left[1+\frac{1}{(2\pi f)^2 C^2 DCR^2}\right]} + j\omega ESL \qquad (5.1)$$

where Z_{cap}= complex impedance of the capacitor and f = frequency (Hz). The value of ESR and the capacitance C of the capacitor are given by equations (5.2) and (5.3) respectively.

$$ESR = \frac{DCR}{1 + (2\pi f)^2 C^2 DCR^2} + R_1 + R_2 \tag{5.2}$$

$$C' = C\left[1 + \frac{1}{(2\pi f)^2 C^2 DCR^2}\right] \tag{5.3}$$

Equations (5.2) and (5.3) show that the values of the ESR and the capacitance are functions of frequency and DCR. However, for the operating frequency range of the switched-mode-converters, the effect of frequency on the value of the ESR and the capacitance is negligible. In addition, the effect of the effective series inductance (ESL) on the impedance of the capacitor is small for the operating frequency range of the converter; therefore, the effect of ESL is ignored in further analyses.

5.2 Proposed method

In this proposed method, the capacitor ripple voltage and ripple current assumed to be available and are used to estimate the capacitor parameters. Figure 5.2 shows the Bode-plot of the electrolytic capacitor impedance with equivalent series resistance, ESR = 200 mΩ, equivalent series inductance, L = 100 nH, and the capacitance C = 470 μF. The magnitude of the capacitor impedance, Z_{cap}, is dominated by the value of the ESR of the capacitor in the frequency range from a few kHz to tens of kHz switching frequency. The 5 kHz of the switching frequency of the dc-dc converter falls within this range.

5.2.1 Theory

An arbitrary shape waveform of voltage or current can be represented by the summation of different sine-wave components. In addition, at any given instant of time, the ratio of the RMS value of the different sine-wave components of the voltage and the current will be equal to the impedance of the capacitor for a particular frequency component.

The Bode-plot in Figure 5.2 shows three clearly separated frequency bands. The capacitance C of the capacitor is dominant in the low frequency band, the ESR is dominant in the mid frequency band, and the ESL is dominant in the high frequency band. Therefore, the value of the ESR can be calculated using the following relationship in the mid frequency range

$$ESR = V_{f_s} / I_{f_s} \tag{5.4}$$

where, V_{fs} = RMS voltage of the capacitor ripple voltage at the switching frequency, I_{fs} = RMS current of the capacitor ripple current at the switching frequency, and f_s = switching frequency.

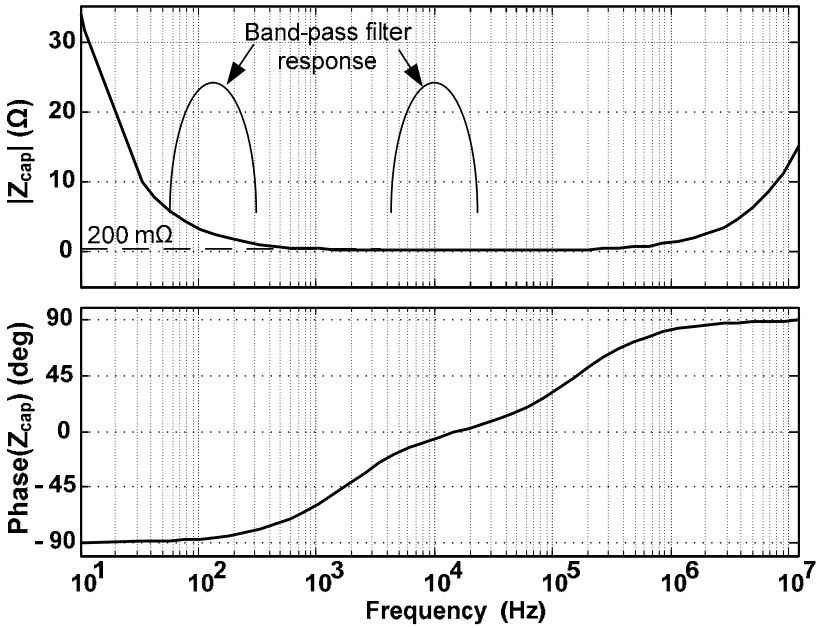


Figure 5.2 Bode-plot of electrolytic capacitor.

It can be further observed from Figure 5.3 that there is not a significant change in the value of the ESR compared to changes in the value of the X_c as the frequency moves from the mid-frequency band to the low-frequency band, where $(X_c) = 1/2\pi fC$. Therefore, it is possible to use the estimated value of the ESR from the mid-frequency band to calculate the value of the capacitance C in the low frequency band using equation (5.5). However, it is also possible to ignore the value of ESR in the calculation of the value of capacitance using equation (5.5) because the value of X_c at 120 Hz is much larger than the value of ESR.

$$(Z_{cap}) = \sqrt{(X_c^2)_{f_m} + ESR^2} = {V_{f_m}}/{I_{f_m}} \cong (X_c)_{f_m} \tag{5.5}$$

Where V_{fm} = RMS value of capacitor ripple voltage at frequency f_m, I_{fm} = RMS value of capacitor ripple current at frequency f_m, where f_m = 120 Hz, and $\left(X_c\right)_{f_m} = 1/2\pi f_m C$.

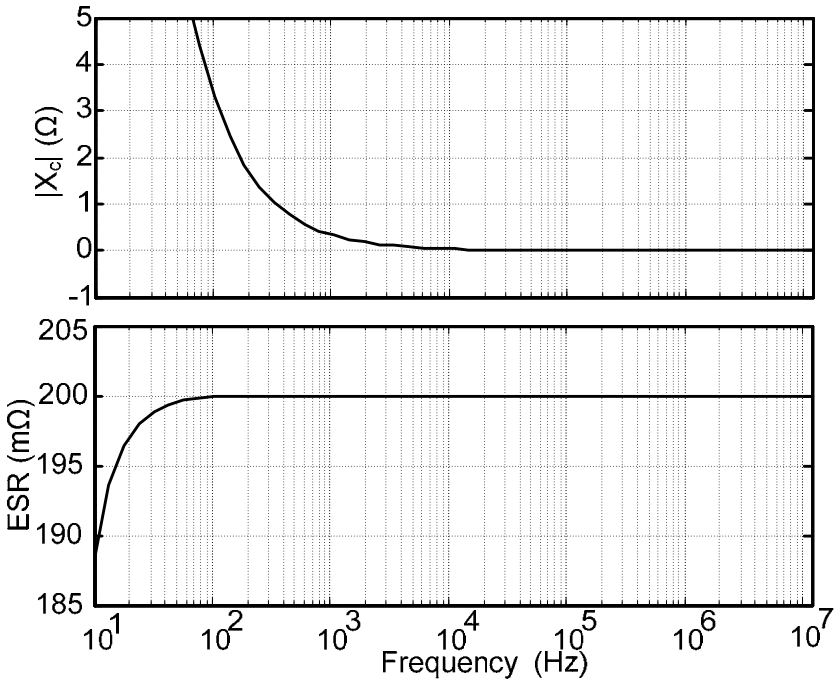


Figure 5.3 Variation in X_C and ESR with frequency.

In the proposed method, a boost-converter in Figure 5.4 is used to verify the theory. The electrolytic capacitor on the output side of the boost converter, C_o, is used as the test-element for the experiment. The scheme for the online parameter estimation is shown in Figure 5.5.

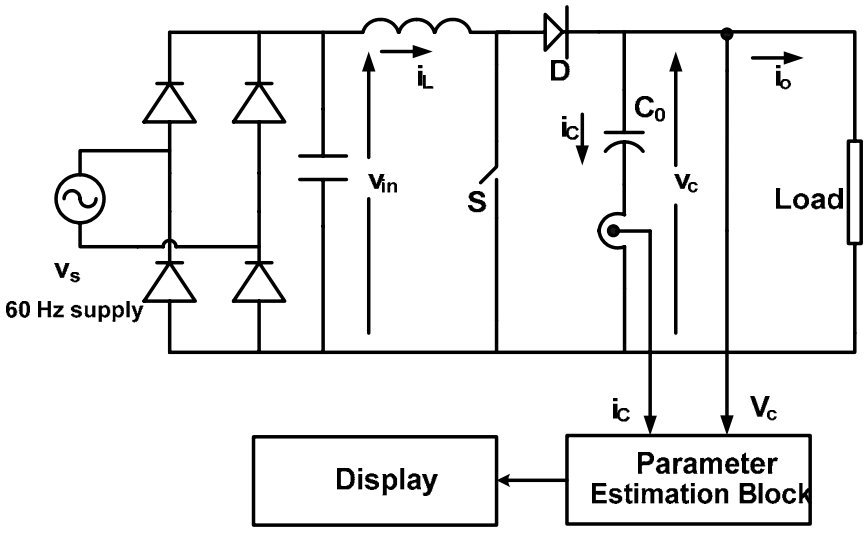


Figure 5.4 Boost-converter.

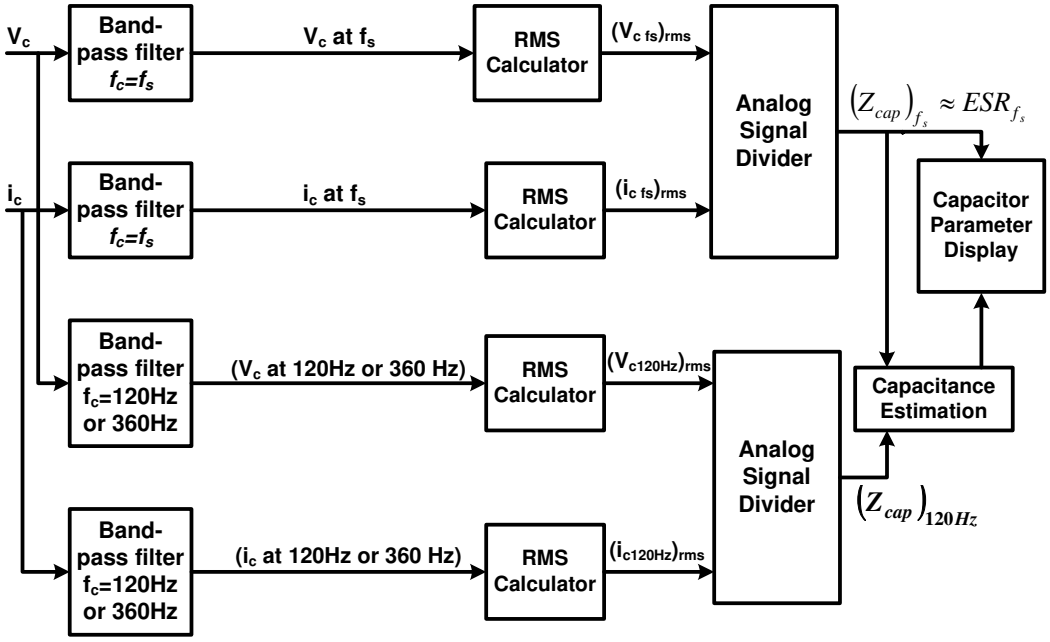


Figure 5.5 Parameter estimation scheme.

The capacitor's voltage and current are passed through the band-pass filters with centre-frequency (f_c) falling in the mid-frequency region of dominance of the capacitor ESR. The output of the band-pass filters are further passed through the RMS-calculator block, which gives the RMS values of the switching-frequency component of the capacitor ripple voltage and the capacitor current. Further, RMS values of the capacitor ripple voltage and the capacitor current are passed through analog-signal-divider blocks to give the ratio of the RMS values of the capacitor ripple voltage and current, as shown in Figure 5.5. This ratio is the impedance of the capacitor in the switching-frequency region, which is approximately equal to the ESR of the capacitor.

The impedance is dominated by $(X_c)_{fm}$, as described by equation (5.5), if the center-frequency of the band-pass-filter is around twice the line-frequency, where f_m = 120 Hz. Therefore, the capacitor voltage and current are passed through the band-pass filters with centre-frequency f_c = 120 Hz, falling in the region of dominance of $(X_c)_{fm}$.

The output of the band-pass filters are passed through the RMS-calculator blocks, which gives the RMS values of the 120 Hz frequency component of the capacitor ripple voltage and current. Further, the RMS values of the capacitor ripple voltage and current are passed through analog-signal-divider blocks to give the ratio of the RMS values of the capacitor ripple voltage and the capacitor current at 120 Hz. This ratio is the impedance of the capacitor at 120 Hz, which is approximately equal to the $(X_c)_{fm}$ of the capacitor. The operations of the RMS-calculator and the analog-signal-divider integrated circuits (ICs) are explained in Appendix B and Appendix C respectively.

5.3 Results and discussion

The boost-converter shown in Figure 5.4 is simulated using the circuit-simulation software *Saber*. Values for different components used in the simulation of the boost-converter are listed below. Further, these values are also used in the experiment to verify the proposed method.

- AC input-voltage to bridge-rectifier = 24 Vrms, 60 Hz
- Inductance of the boost-inductor = 300 μH
- Switching frequency of the boost-switch, f_s = 5 kHz
- Boost-switch duty-cycle = 0.6
- Capacitance of the boost-capacitor = 470 μF, 85 ºC, ESR = 200 mΩ
- Load resistance = 10 Ω

5.3.1 Simulation results

The capacitor voltage and current are passed through the band-pass filters with center frequency falling in the ESR dominated region. The simulated output of the band-

pass filters, which are the switching-frequency components for the boost-capacitor voltage and the current, v_c and i_c, are shown in Figure 5.6. The switching-frequency 5 kHz of the boost-switch is much greater compared to the input voltage v_{in} ripple frequency 120 Hz. The effect of the 120 Hz voltage-ripple in v_{in}, can be seen in the high-frequency capacitor ripple-voltage, v_c, and the capacitor ripple-current, i_c, as shown in Figure 5.6. This effect can be also observed in the frequency-domain in the form of side bands, as shown in the FFT plots of v_c and i_c in Figure 5.7.

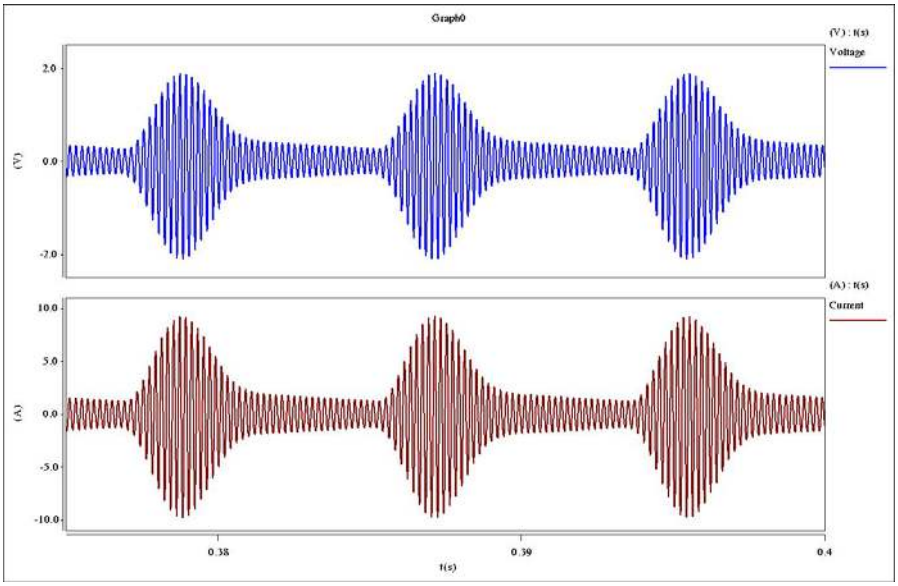


Figure 5.6 High frequency filtered waveform of capacitor voltage and current, showing the effects of 120 Hz ripple in input voltage v_{in}.

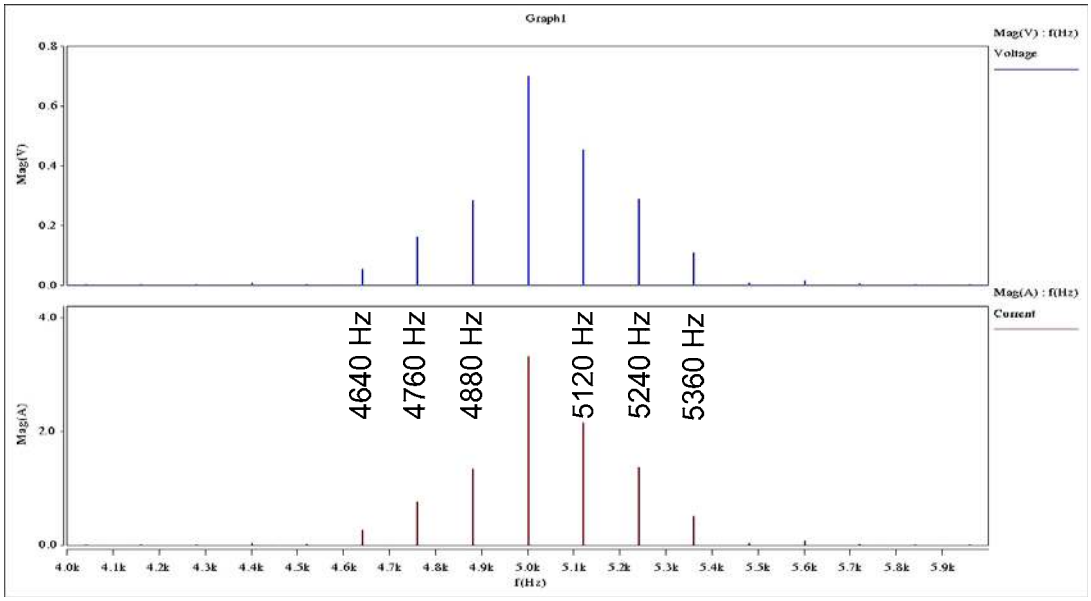


Figure 5.7 FFT plot of high frequency filtered waveform of capacitor voltage and current.

The Bode-plot of an electrolytic capacitor shown in Figure 5.2 has a wide flat region around the switching-frequency in the magnitude plot. It means that there are small changes in the impedance of the capacitor around the switching-frequency of the converter, and it is approximately equal to the ESR of the capacitor. This concept is further written in mathematical form in equation (5.6).

$$ESR^2 \approx \frac{V_{f_s}^2}{I_{f_s}^2} \approx \frac{V_{f_s \pm f_m}^2}{I_{f_s \pm f_m}^2} \approx \frac{V_{f_s \pm 2f_m}^2}{I_{f_s \pm 2f_m}^2} \approx \ldots \tag{5.6}$$

Using an algebraic analogy that $\frac{a}{b} = \frac{c}{d} = \frac{a+c}{b+d}$, then equation (5.6) can be further written as in equation (5.7).

$$ESR^2 \approx \frac{V_{f_s}^2 + V_{f_s - f_m}^2 + V_{f_s - 2f_m}^2 + V_{f_s + f_m}^2 + V_{f_s + 2f_m}^2 + \ldots}{I_{f_s}^2 + I_{f_s - f_m}^2 + I_{f_s - 2f_m}^2 + I_{f_s + f_m}^2 + I_{f_s + 2f_m}^2 + \ldots} \tag{5.7}$$

$$ESR \approx \frac{\sqrt{V_{f_s}^2 + V_{f_s - f_m}^2 + V_{f_s - 2f_m}^2 + V_{f_s + f_m}^2 + V_{f_s + 2f_m}^2 + \ldots}}{\sqrt{I_{f_s}^2 + I_{f_s - f_m}^2 + I_{f_s - 2f_m}^2 + I_{f_s + f_m}^2 + I_{f_s + 2f_m}^2 + \ldots}} \tag{5.8}$$

Where V_{fs} = RMS value of the capacitor ripple voltage at the switching frequency

I_{fs} = RMS value of the capacitor ripple current at the switching frequency

$V_{fs\pm fm}$, $V_{fs\pm 2fm}$ = RMS value of the side-band amplitude of the capacitor ripple voltage around the switching frequency

$I_{fs\pm fm}$, $I_{fs\pm 2fm}$ = RMS value of the side-band amplitude of the capacitor ripple current around the switching frequency

The RMS values of the capacitor ripple voltage and the capacitor current shown in Figure 5.7 can be calculated as follows

$$V_{f_s} = \sqrt{\begin{matrix}0.261^2+0.1619^2+0.284^2+0.701^2+0.454^2 \\ +0.287^2+0.108^2\end{matrix}} = 0.95\ volt \qquad (5.9)$$

$$I_{f_s} = \sqrt{\begin{matrix}0.261^2+0.760^2+1.336^2+3.316^2+2.153^2 \\ +1.367^2+0.515^2\end{matrix}} = 4.50\ amp \qquad (5.10)$$

The estimated value of the ESR can be calculated as

$$ESR \approx Z_{f_s} \approx \frac{V_{f_s}}{I_{f_s}} = \frac{0.95}{4.50} = 0.211\Omega = 211\ m\Omega \qquad (5.11)$$

The actual value of the ESR used in the simulation is 200 mΩ. There is only a small error of 5.5% between the estimated and the actual values of the capacitor ESR, which indicates that the proposed method can be used for the estimation of the capacitor ESR. In addition, equation (5.8) states that the band-pass filter does not need a high Q-value even in the presence of various side bands around the switching-frequency of the converter. The ratio in equation (5.8) is approximately equal to the actual value of the capacitor ESR.

Similarly, the output of the band-pass filter waveforms for the capacitor ripple voltage and current in low frequency band are used to estimate the value of $(X_c)_{fm}$, as described by equation (5.5). The output of the band-pass filters, in the time and

frequency domains are shown in Figures 5.8 and 5.9 respectively. The estimated value of $(X_c)_{fm}$ using results in Figures 5.8 and 5.9 can be calculated as

$$(X_c)_{f_m} \approx \frac{V_{f_m}}{I_{f_m}} \approx \frac{6.028}{2.131} \approx 2.829\Omega \tag{5.12}$$

where V_{fm} = RMS value of the capacitor ripple voltage at frequency f_m, I_{fm} = RMS value of the capacitor ripple current at frequency f_m, and f_m = 120 Hz.

The actual value of $(X_c)_{fm}$ can be calculated as

$$(X_c)_{f_m} = \frac{1}{2\pi f_m C} = \frac{1}{2\pi \times 120 \times 470 \times 10^{-6}} = 2.822\Omega \tag{5.13}$$

The estimated value of $(X_c)_{fm}$ shown in equation (5.12) corresponds to estimated capacitance of C = 469 μF.

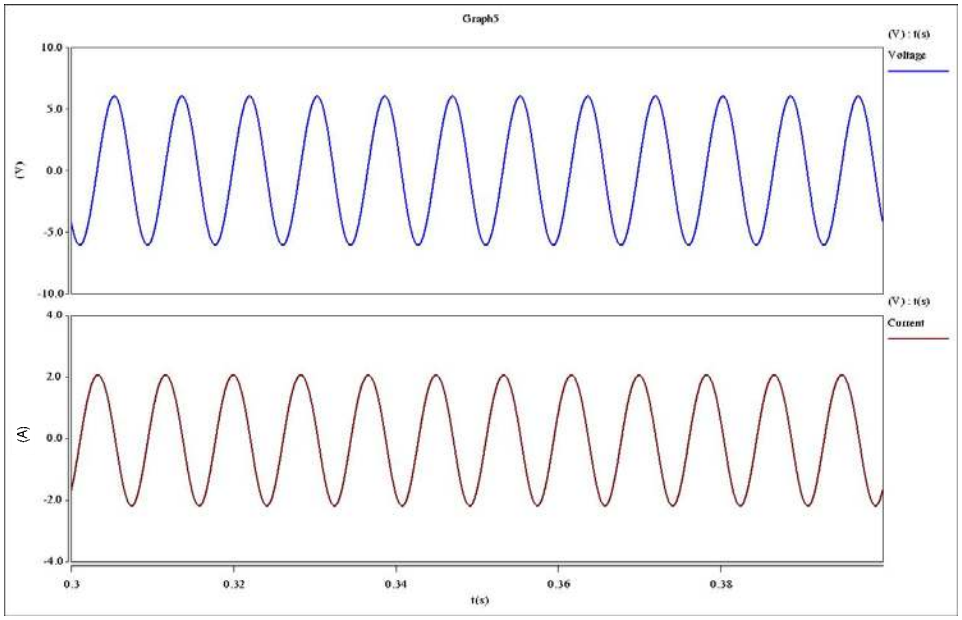


Figure 5.8 Low frequency filtered waveform of capacitor voltage and current.

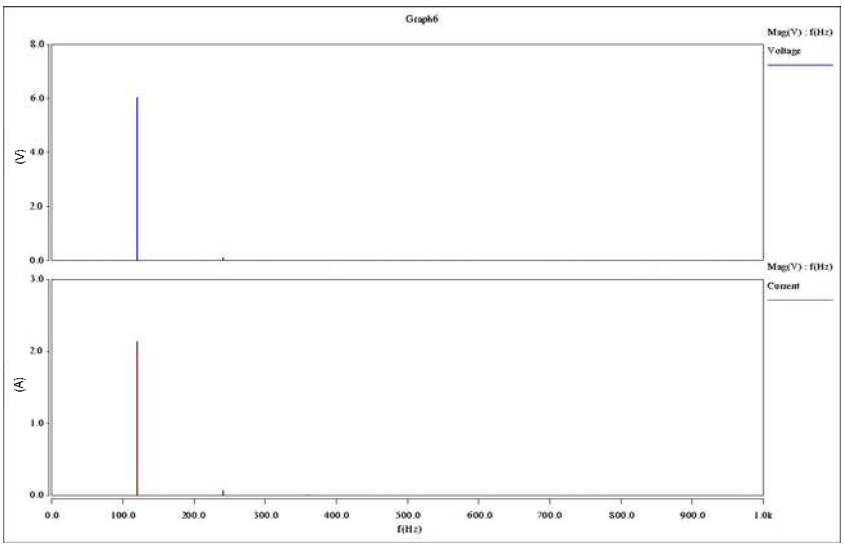


Figure 5.9 FFT plot of low frequency filtered waveform of capacitor current.

5.3.2 Experimental results

Figures 5.10 and 5.11 show the sensors and the analog band-pass filters used to sense and process the capacitor ripple voltage and ripple current to estimate the capacitor parameters.

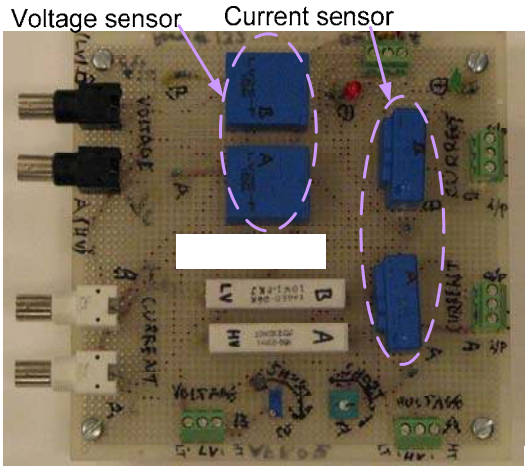


Figure 5.10 Voltage and current sensors.

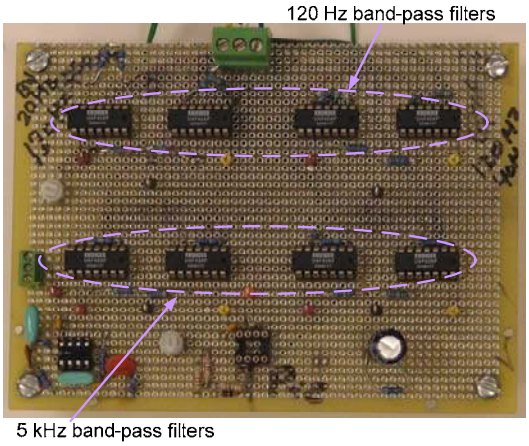


Figure 5.11 Analog band-pass filters.

Figures 5.12 to 5.15 show the measured waveforms of the band-pass filtered switching frequency components for capacitor ripple voltage and ripple current in the time and frequency domain.

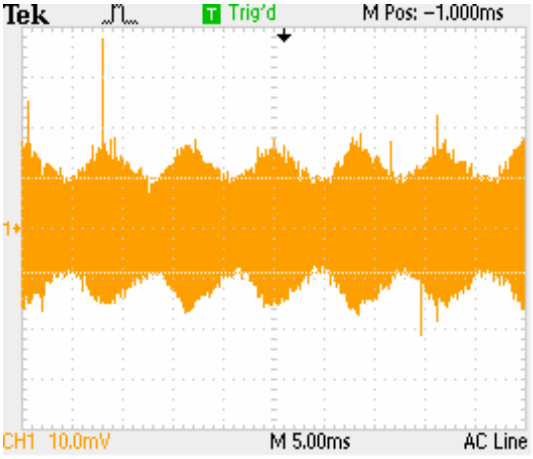


Figure 5.12 High frequency filtered waveform of capacitor voltage.

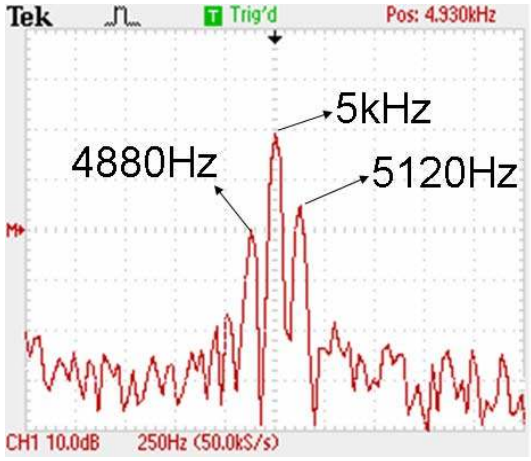


Figure 5.13 FFT plot of high frequency filtered waveform of capacitor voltage.

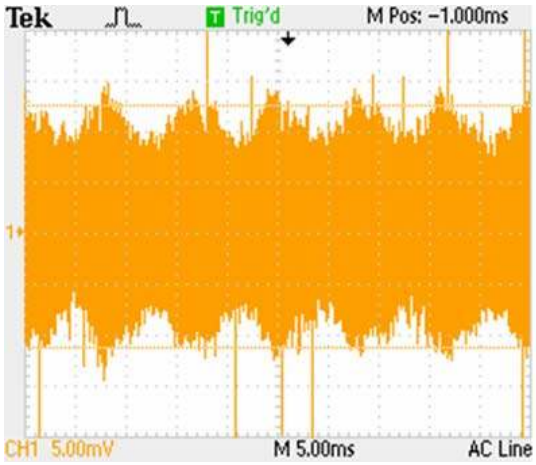


Figure 5.14 High frequency filtered waveform of capacitor current.

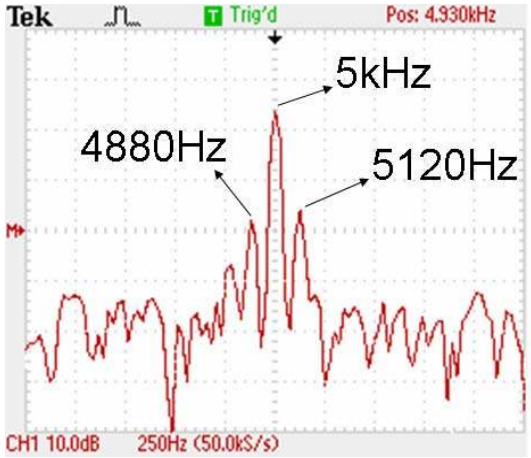


Figure 5.15 FFT plot of high frequency filtered waveform of capacitor current.

The RMS value of the band-pass filtered capacitor ripple voltage at switching frequency is

$$(V_{rms})_{f_s} = K_{Vf_s}(V_{rms_{band}})_{f_s} = 580\,mV \tag{5.14}$$

where K_{Vfs} = Gain of voltage sensor and band-pass filter.

The RMS value of the filtered capacitor ripple current at switching frequency is

$$(I_{rms})_{f_s} = K_{If_s}(I_{rms_{band}})_{f_s} = 3.7\,Amp \tag{5.15}$$

where K_{Ifs} = Gain of current sensor and band-pass filter.

The estimated ESR is given by,

$$ESR = \frac{(V_{rms})_{f_s}}{(I_{rms})_{f_s}} \approx 157\,m\Omega \tag{5.16}$$

and the measured ESR is,

$$ESR \approx 178\,m\Omega \tag{5.17}$$

Figures 5.16 and 5.17 show the waveforms of the band-pass filtered 120 Hz frequency components for capacitor ripple voltage and ripple current in time and frequency domain.

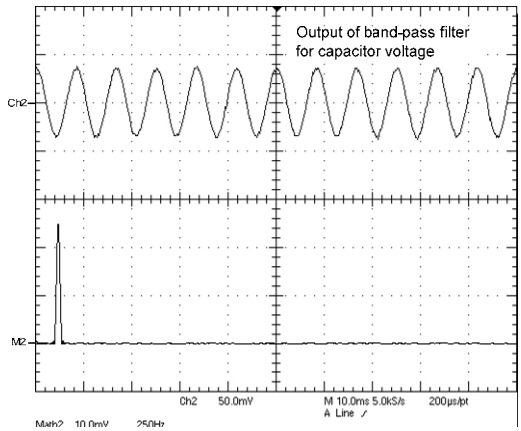


Figure 5.16 120 Hz frequency component of filtered waveform of capacitor current.

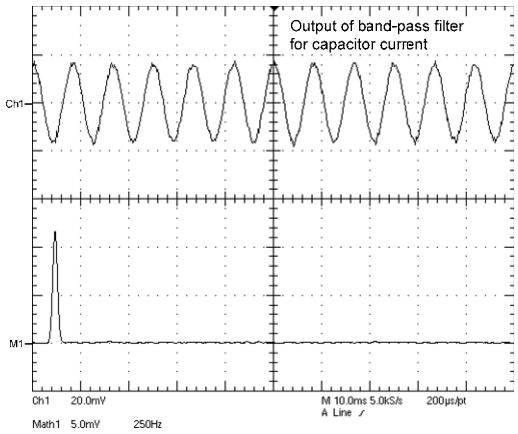


Figure 5.17 FFT plot of 120 Hz frequency component of filtered waveform of capacitor current.

The RMS value of the band-pass filtered capacitor ripple voltage at 120 Hz frequency is

$$(V_{rms})_{f_m} = K_{Vf_m}(V_{rms_{band}})_{f_m} = 980\,mV \tag{5.18}$$

where K_{Vfm} = Gain of voltage sensor and band-pass filter.

The RMS value of the filtered capacitor ripple current at 120 Hz frequency is

$$(I_{rms})_{f_m} = K_{If_m}(I_{rms_{band}})_{f_m} = 290\,mA \tag{5.19}$$

where K_{Ifm} = Gain of current sensor and band-pass filter.

The estimated value of $(X_c)_{fm}$ ESR is given by,

$$(X_c)_{f_m} = \frac{(V_{rms})_{f_m}}{(I_{rms})_{f_m}} \approx 3.4\Omega \tag{5.20}$$

The estimated value of capacitance using the experimental results is

$$C \approx 390\,\mu F \tag{5.21}$$

and the measured value of capacitance using an LCR meter is

$$C \approx 457\,\mu F \tag{5.22}$$

Results presented in this section are summarized in Tables 5.1 and 5.2.

Table 5.1 Simulation results for estimated parameters

ESR_{actual}	$ESR_{estimated}$	% Error
200 mΩ	211 mΩ	5.5
C_{actual}	$C_{estimated}$	
470 μF	469 μF	0.2

Table 5.2 Experimental results for estimated parameters

ESR_{actual}	$ESR_{estimated}$	% Error
178 mΩ	157 mΩ	11
C_{actual}	$C_{estimated}$	
457 μF	390 μF	14

5.4 Summary

A new low cost method is proposed to detect the changes in the ESR and the capacitance values of an electrolytic capacitor in order to realize the real-time failure prediction of an electrolytic capacitor. For the proposed strategy, only the capacitor voltage and current waveforms are required. The results show that the proposed electrolytic capacitor failure-prediction method can be applied to power-converters successfully. The next chapter introduces a new type of capacitor fault caused by inrush current, which is different from the research work presented in Chapters 3 to 5, which described the slow steady gradual aging of the capacitor.

CHAPTER 6

CAPACITOR FAILURE DUE TO INRUSH CURRENT

6.1 Introduction

One of the most critical application parameters of an aluminum electrolytic capacitor is its voltage capability, typically expressed in terms of rated or working voltage, surge voltage, transient voltage, etc. Exceeding the voltage capability (even for a few milliseconds) can result in the immediate failure of the capacitor, or its performance can be degraded over the longer term. However, it is often impossible to determine the exact maximum voltage that will never be exceeded in an application, especially when considering short duration transients. The question is further complicated when using capacitor banks where the voltage on an individual capacitor is influenced by the capacitance of other capacitors, which can vary from component to component, and the capacitance of the individual capacitors may also vary over time [42]. The problem can be solved by using a wide safety margin between the voltage capability of the capacitor and the expected maximum voltage in an application. However, cost optimization requirements dictate the use of minimal safety margin. To do this successfully without undue risk, it is important to know both the characteristics of the application and the actual voltage capability (steady state, surge, and transient ratings) of the capacitor being used. The objective of this chapter is to give a further insight into the

behavior of aluminum electrolytic capacitors and the impact on capacitor life of short duration transient voltages, by exploring the work presented by Klug [42].

The first part of this chapter deals with the experiments and test methods adopted in [42] to probe the voltage capabilities of high-voltage electrolytic capacitors. A comprehensive analysis of the failure mechanism and a failure model of an electrolytic capacitor, due to a surge current caused by a transient overvoltage, are presented. Experimental results are included in the second part of this chapter to give further insight into the failure mechanism due to surge current.

6.2 Test setup and results by [42]

A detailed procedure to test capacitor voltage susceptibility was developed by Klug [42]. An experimental setup similar to Figure 6.1 was used by Klug [42] to charge a capacitor bank C_{bank} to a given voltage. The equivalent capacitance value of C_{bank} is much larger than the capacitance value of C_{test}. A capacitor by Evox-Rifa with part number PEH200YU426, capacitance value of 2600 μF, rated voltage 450 V, height 115 mm, and diameter 75 mm is used as the test capacitor, C_{test}. A current limiting inductor L is used to control the amplitude of the current pulse to the test capacitor. The capacitor bank is discharged onto C_{test} by closing the switch S. The effect is a powerful but short pulse on the test object at room temperature. If the capacitor is capable of absorbing the pulse without failure, a new pulse is given with a 50 V higher bank voltage within 30 seconds. The capacitor is discharged between the pulses, for about 15 milliseconds after each pulse. The process is repeated as long as the capacitor is functioning.

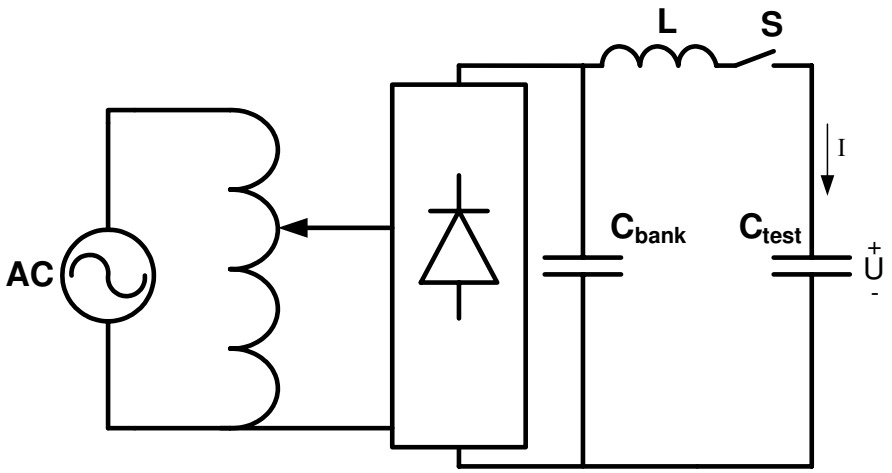


Figure 6.1 Experimental set up for transient over voltage effect.

The primary result is the highest measured voltage level U on the capacitor before failure, and a secondary result is the largest inrush current I (without failure). Figure 6.2 shows an example where the capacitor is able to absorb the pulse without failure, and Figure 6.3 shows an example where the capacitor has failed to absorb the pulse. The latter shows that the voltage, instead of remaining at a high level, drops sharply after the failure, and the C_{test} loses its property as a capacitor. Experimental data extracted from the results shown in Figures 6.2 and 6.3 are used to estimate the energy dissipated in the capacitor to calculate the excess energy responsible for the failure of the capacitor C_{test}.

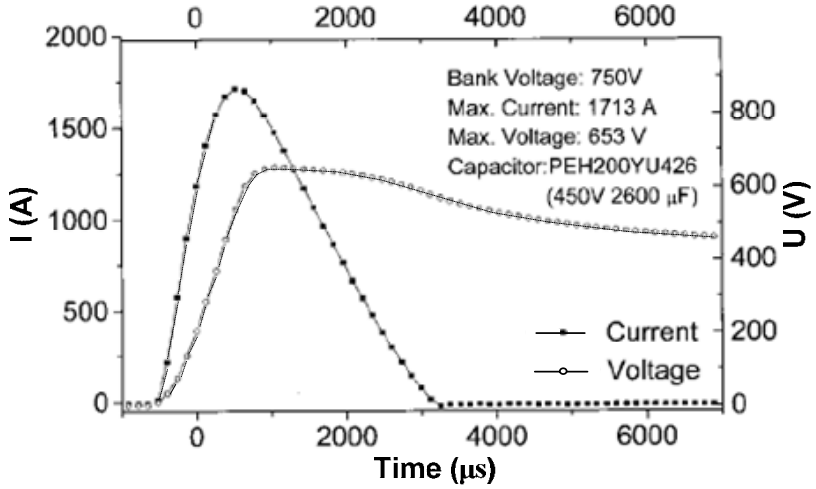


Figure 6.2 Successful pulse test result [42].

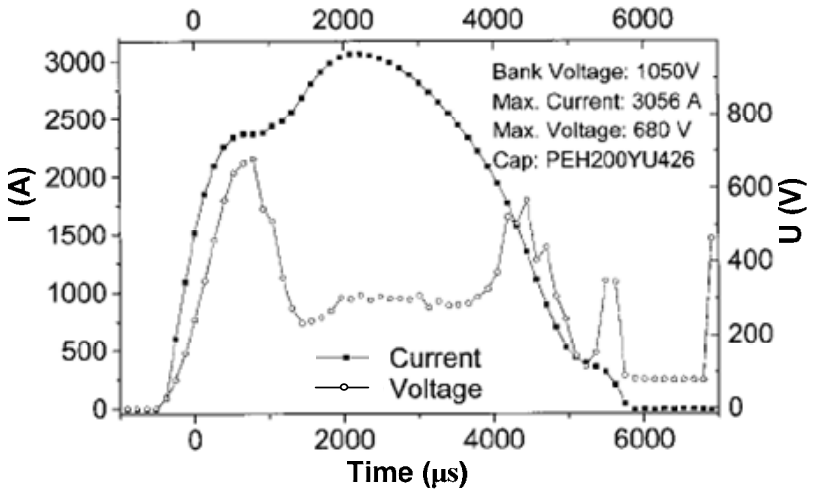


Figure 6.3 Unsuccessful pulse test result [42].

6.2.1 Discussion

Figure 6.4 shows the plot of the capacitor voltage and current for a successful pulse followed by an estimated capacitor voltage plot for an ideal capacitor in Figure 6.5. Similarly, the capacitor voltage and current for an unsuccessful pulse are shown in Figure 6.6, and corresponding plot for an ideal capacitor voltage is shown in Figure 6.7. Figure 6.4 is divided into two regions, Region 1 and Region 2. Region 1 describes approximately a linear increase in the capacitor voltage until there is a voltage clamping across the capacitor, and it enters into region 2 where the capacitor voltage is almost constant even though the capacitor current is positive. Similarly, Figure 6.6 shows the plot for an unsuccessful pulse in which region 1 describes a linear increase in the capacitor voltage until there is a voltage clamping across the capacitor. However, region 2 is much shorter compared to a successful pulse, and the capacitor voltage collapses and enters into region 3 where the capacitor has failed as short-circuit, and loses the property of a capacitor.

6.2.2 Analysis of successful pulse test results

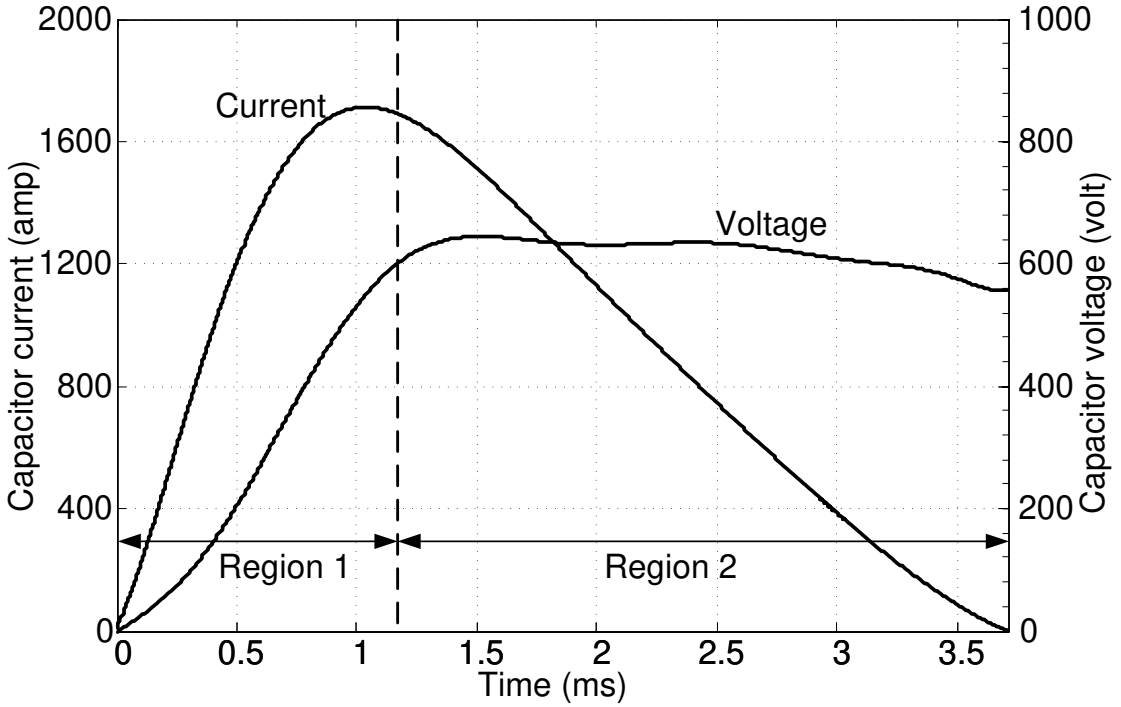


Figure 6.4 Measured voltage and current plots for successful pulse test.

The capacitor acts as an ideal capacitor in region 1, and most of the supplied electric charge is stored in the capacitor dielectric. However, as it can be observed from Figure 6.4, the capacitor voltage is almost constant in region 2 even though the capacitor current is positive. The capacitor voltage would have continued to increase if there was no voltage clamping in region 2 as shown in Figure 6.5, and it can be described in the mathematical form as follows

$$v_C = \frac{1}{C}\int i_c dt + ESR \times i_c \tag{6.1}$$

The results presented in Figure 6.4 and 6.5 are operating at close to the edge just before a failure occurs. In addition, it is important to note that the difference in the energies delivered to the capacitor under the influence of the voltage expressed by equation (6.1), and the clamped capacitor voltage in region 2, is converted into heat

energy inside the capacitor, and this heat may lead to failure of the capacitor. The energy converted to heat energy can be calculated as follows.

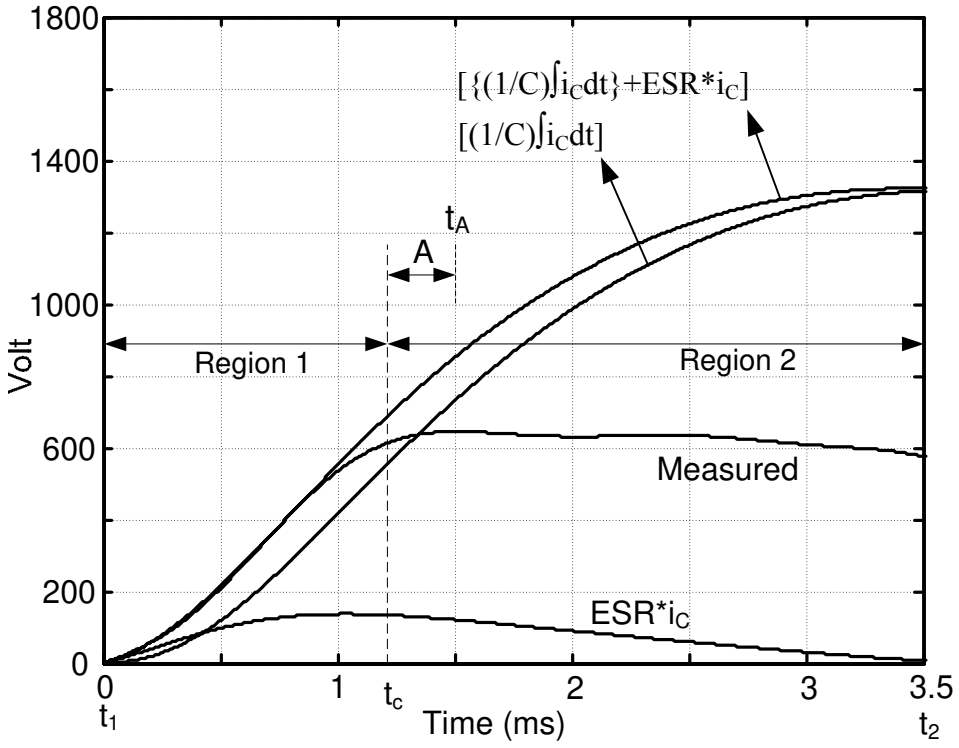


Figure 6.5 Voltage plots for successful pulse test.

The total energy delivered to the capacitor, as shown in Figures 6.4 or 6.5, for the successful pulse, can be calculated as

$$E_t = \int_{t_1}^{t_2} v(t)i(t)dt = 1795 \; joule \tag{6.2}$$

The energy delivered to the capacitor during region 1 in Figure 6.5, before voltage clamping occurs, can be calculated as

$$E_1 = \int_{t_1}^{t_c} v(t)i(t)dt = 527 \; joule \tag{6.3}$$

where t_c = Clamping time, as shown in Figure 6.5.

The energy delivered to the capacitor after clamping during region 2 in Figure 6.5 can be calculated

$$E_2 = \int_{t_c}^{t_2} v(t)i(t)dt = 1268 \; joule \tag{6.4}$$

As expected,

$$E_t = E_1 + E_2 = 1795 \text{ joule} \tag{6.5}$$

Figures 6.4 and 6.5 show that the measured capacitor voltage during region 2 is almost constant even in the presence of positive capacitor current. Therefore, this indicates that the energy delivered in region 2 is converted into heat. Further, the average power delivered to the capacitor during clamping in region 2 can be calculated as

$$(P_c)_{Avg} = \frac{E_2}{t_2 - t_c} = 552 \text{ joule/ms} \tag{6.6}$$

However, the average power delivered to the capacitor soon after clamping, region A in Figure 6.5, is much greater than in equation (6.6), as the magnitude of current in region A is high. It is calculated as

$$(P_A)_{Avg} = \frac{\int_{t_c}^{t_A} v(t)i(t)dt}{t_A - t_c} = 1017 \text{ joule/ms} \tag{6.7}$$

6.2.3 Analysis of unsuccessful pulse test results

In this section, energies delivered to the capacitor in various regions are calculated for the unsuccessful pulse, and data are compared with energies presented for a successful pulse to understand the failure mechanism of the capacitor.

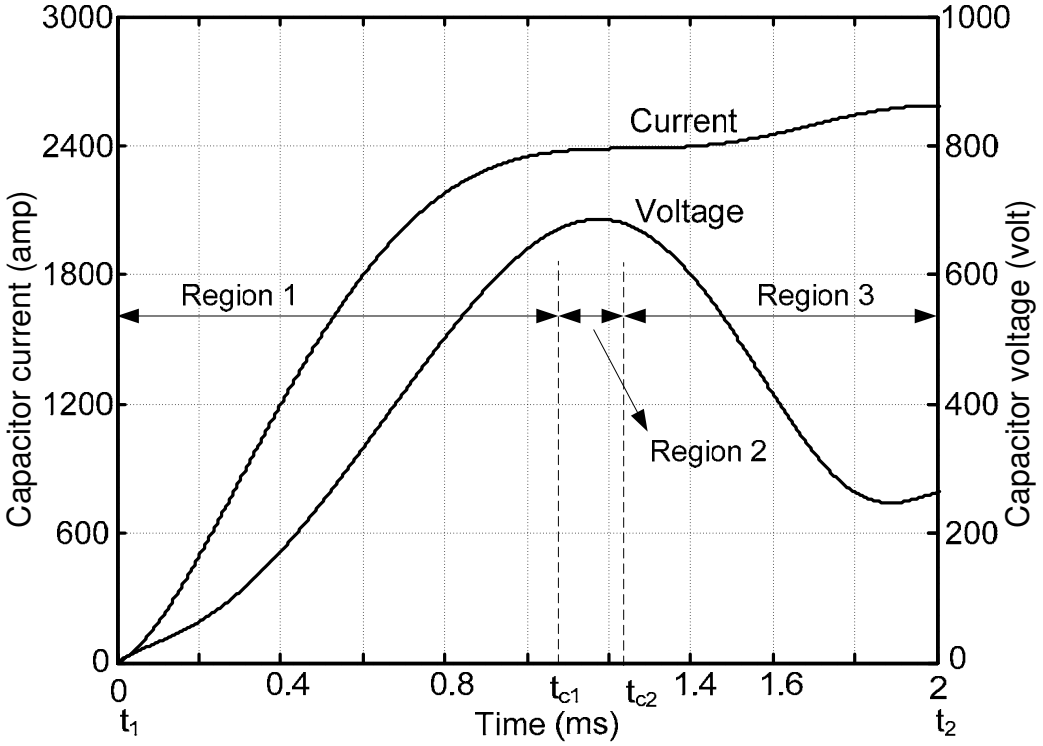


Figure 6.6 Measured voltage and current plots for unsuccessful pulse test.

As explained in section 6.2.2, the capacitor acts as an ideal capacitor in region 1, and most of the supplied electric charge is stored in the capacitor dielectric. During the short period in region 2 in Figure 6.6, the capacitor voltage is almost constant. After the failure, the capacitor-voltage collapses as shown in region 3 and the capacitor is failing into a quasi-short-circuit, and loses its property as a capacitor. However, the voltage for an ideal capacitor would have continued to increase if there was no voltage clamping in region 2 and no capacitor failure in region 3. The voltage variation for the ideal capacitor can be described by using equation (6.1) and shown in Figure 6.7.

The total energy delivered to the capacitor for the unsuccessful pulse shown in Figure 6.7 can be calculated as

$$E_t = \int_{t_1}^{t_2} v(t)i(t)dt = 1704 \; joule \tag{6.8}$$

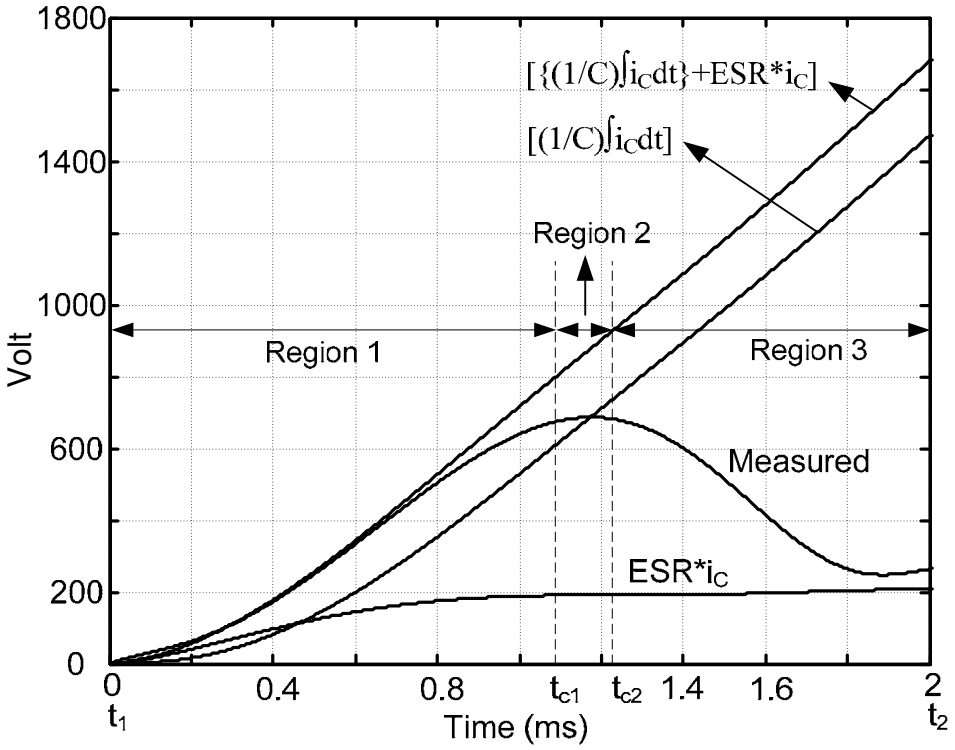


Figure 6.7 Voltage plots for unsuccessful pulse.

The energy delivered to the capacitor in Figure 6.6 before voltage clamping, indicated as region 1, can be calculated as

$$E_1 = \int_{t_1}^{t_{c1}} v(t)i(t)dt = 685 \; joule \tag{6.9}$$

The energy delivered to the capacitor in Figure 6.6 during clamping, indicated as region 2, can be calculated as

$$E_2 = \int_{t_{c1}}^{t_{c2}} v(t)i(t)dt = 244 \; joule \tag{6.10}$$

6.2.4 Conclusion of successful and unsuccessful pulse test results

Region 2 in Figure 6.7 for an unsuccessful pulse is much shorter in time compared to region 2 in Figure 6.5 for a successful pulse. Therefore, energy delivered to the capacitor in region 2 for an unsuccessful pulse is much smaller than for a successful pulse, as shown in equation (6.4). However, the average energy delivered to the capacitor per unit time is an important quantity for the failure of the capacitor. The average power delivered to the capacitor during clamping in region 2 for an unsuccessful pulse in Figure 6.6 can be calculated using equation (6.10) as

$$(P_c)_{Avg} = \frac{E_2}{t_{c2} - t_{c1}} = 1630 \text{ joule/ms} \tag{6.11}$$

The average energy per unit time delivered to the capacitor in region 2 for an unsuccessful pulse is much greater (1630 joule/ms) than for a successful pulse (552 joule/ms), as it can be observed by comparing equations (6.6) and (6.11). However, an argument can be made that the average energy delivered to the capacitor soon after the clamping in region A in Figure 6.5 for a successful pulse, is also high because the magnitude of the current in this region is high. The average energy per unit time delivered to the capacitor in region A of Figure 6.5 is shown in equation (6.7), but even the value of 1017 joules/ms in equation (6.7) as 1017 joules/ms is significantly smaller than the value in equation (6.11). Therefore, the capacitor is damaged and it fails to maintain the voltage after region 2 in Figure 6.6. The results for successful and unsuccessful pulses are summarized in Table 6.1.

Table 6.1 Energy for successful and unsuccessful pulse

	E_t (joule)	E_1 (joule)	E_2 (joule)	Energy per unit time near start of voltage clamping (joule/ms)
Successful pulse	1795	527	1268	1017
Unsuccessful pulse	1704	685	244	1630

The difference in energy between a successful and an unsuccessful pulse (61 joule), which damages the capacitor dielectric, is much smaller than the energy delivered (527 joule for successful pulse and 685 joule for unsuccessful pulse) to the capacitor in region 1. However, the difference in the average energy (613 joule/ms) delivered at the start of voltage clamping in unit time to the capacitor is much higher, which results in the failure of the capacitor. The capacitor current is concentrated in a small volume of the capacitor and results in hot spot regions inside the capacitor, which is further described in the next section.

6.3 Failure mechanism

The construction of an electrolytic capacitor is explained in detail in Chapter 2. However, it is re-visited in this section to draw an equivalent electrical circuit model for an electrolytic capacitor.

6.3.1 Construction

Figures 6.8 and 6.9 [50] show the X-ray view of an electrolytic capacitor. The actual image of an electrolytic capacitor cut in half, along with the aluminum foil and separator paper arrangement, are shown in Figure 6.10.

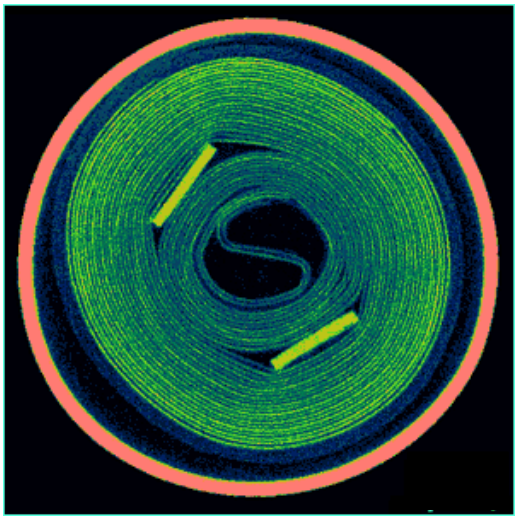


Figure 6.8 X-ray view of the electrolytic capacitor (*Source: Micro Photonics Inc*).

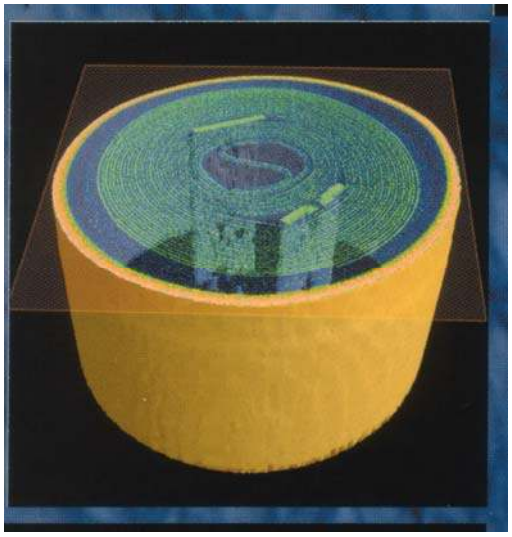


Figure 6.9 3-D X-ray view of the electrolytic capacitor (*Source: Micro Photonics Inc*).

Arrangements for the anode and cathode tabs are shown in Figures 6.8, 6.9 and 6.11. The anode and cathode aluminum foils along with the separator paper are wrapped together in the form of a spiral, as shown in Figure 6.11.

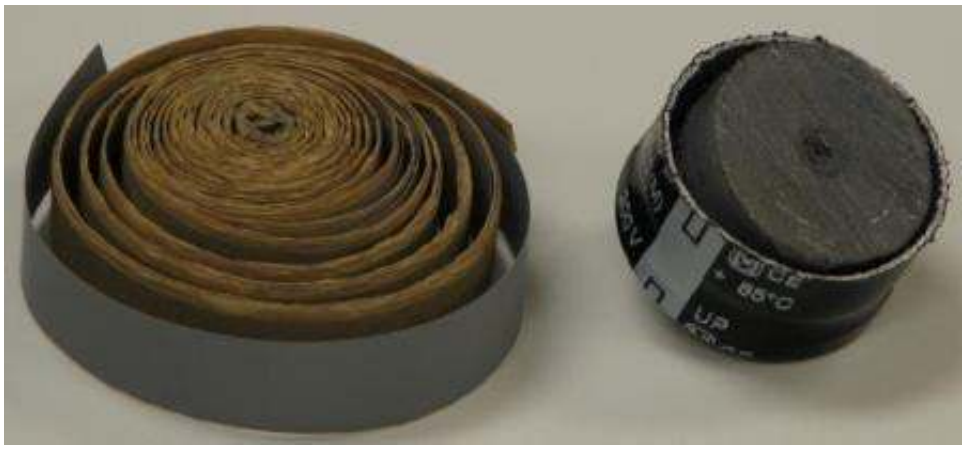


Figure 6.10 Electrolytic capacitor.

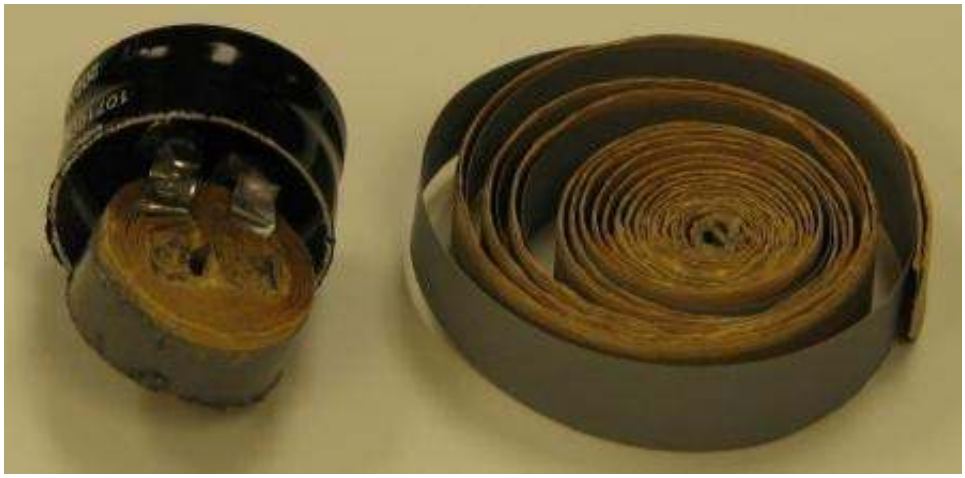


Figure 6.11 Electrolytic capacitor tab location.

The arrangement of a single layer in the spiral is shown in Figure 6.12. It consists of seven layers of aluminum anode foil, anode side oxide, anode side electrolyte, paper separator, cathode side electrolyte, cathode side oxide, and aluminum cathode foil. Thicknesses for these layers in Figure 6.12 are listed in Table 6.2. Further analysis is carried out using *Matlab* to understand the failure mechanism of an electrolytic capacitor. For simplicity, it is assumed that the capacitor has an arrangement of concentric cylindrical capacitors, instead of a spiral shown in Figure 6.11, connected in parallel with a fill-factor equal to 95 %. In addition, it is assumed that the capacitor consists of 225 concentric cylindrical capacitors. These 225 concentric cylindrical capacitors are chosen

by trial-and-error because it gives the capacitance value close to 2600 μF used in the transient-voltage effect test described in section 6.3 [42] and also gives an outer diameter close to the actual 80 mm of the capacitor. The data listed in Table 6.2 is used in *Matlab* to plot the ESR and capacitance variation with diameter for 225 cylindrical capacitors using equations (6.12) and (6.13) are shown in Figure 6.13.

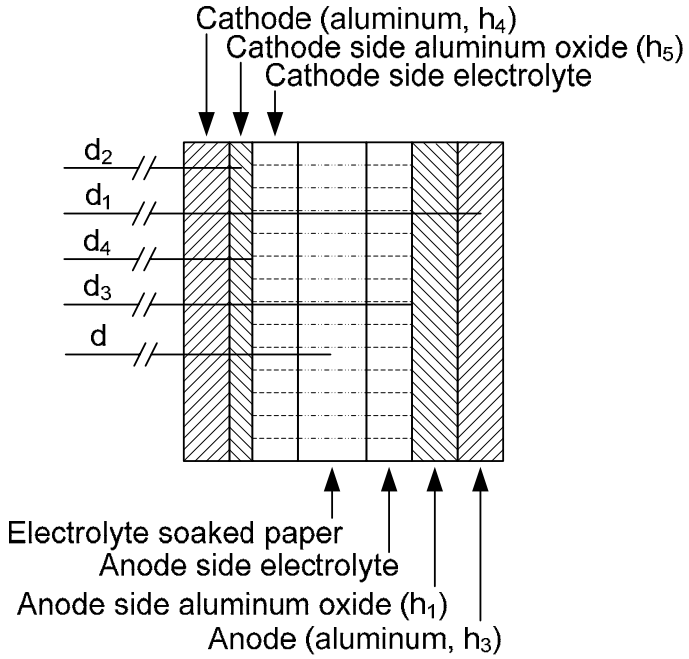


Figure 6.12 Electrolytic capacitor single layer configurations.

Table 6.2 Thickness of different layers in the cylindrical capacitor

Anode side oxide (h_1)	Combined paper and electrolyte (h_2)	Aluminum anode foil (h_3)	Aluminum cathode foil (h_4)	Cathode side oxide (h_5)
600 nm	100 μm	100 μm	25 μm	3 nm

$$C = k\frac{2\pi\varepsilon_0\varepsilon_r L}{\log\left(d_1/d_2\right)} \tag{6.12}$$

where L = height of an electrolytic capacitor (m), k = area enhancement-factor because of etching (typically 200) [7], d_1 = outer diameter of the cylindrical capacitor, d_2 = inner diameter of cylindrical capacitor.

$$ESR = \frac{\lambda}{2\pi L \log(d_3/d_4)} \tag{6.13}$$

Where λ = resistivity of paper-electrolyte system (Ω-m), d_3 = outer diameter of paper-electrolyte system cylinder, d_4 = inner diameter of paper-electrolyte system cylinder. All dimensions shown in equations (6.12) and (6.13) are in S.I. units.

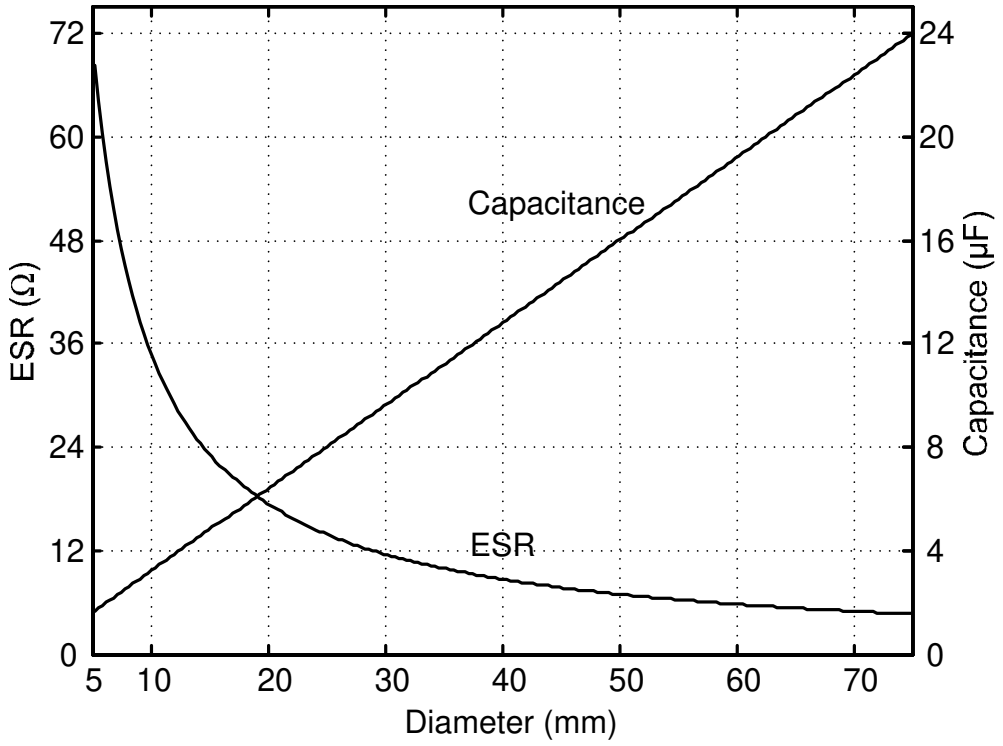


Figure 6.13 Variation of ESR and capacitance with diameter d (Figure 6.12).

Using equations (6.12) and (6.13), the capacitance and ESR of different layers of a capacitor are plotted in Figure 6.13. It can be observed that the value of ESR decreases with diameter and capacitance increases with diameter respectively. Figure 6.14 shows

the time-constant τ variation with diameter given by equation (6.14) of various cylindrical capacitors.

$$\tau = ESR \times C \tag{6.14}$$

It is interesting to note that time-constants are almost constant with variation in the diameter of the capacitors. This suggests that the rate of charging of these parallel capacitors is the same.

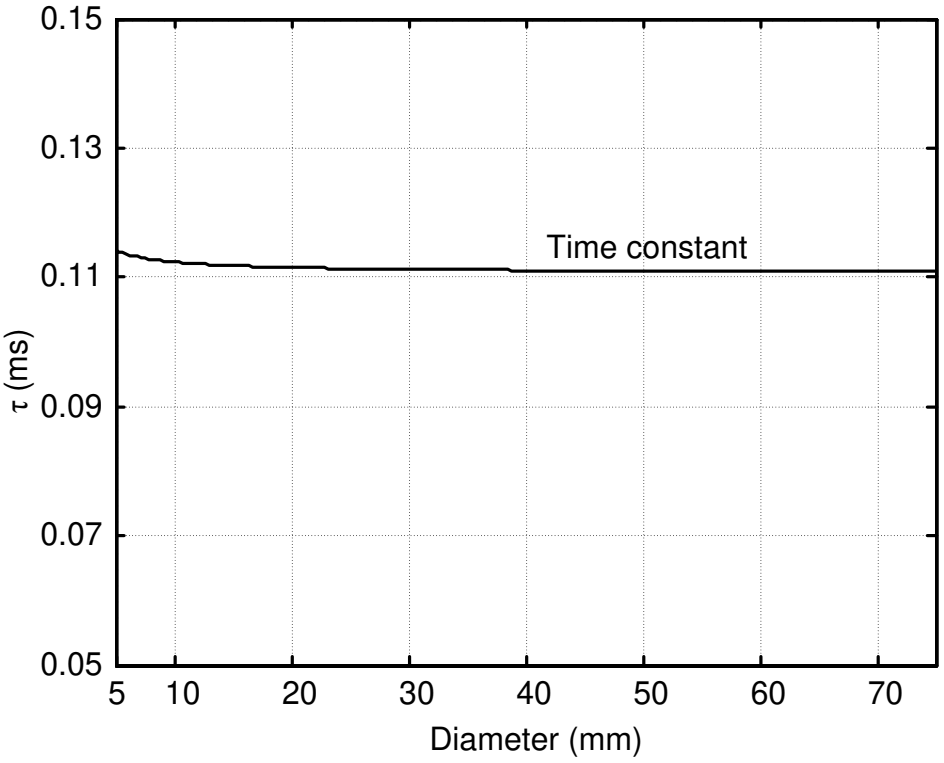


Figure 6.14 Variation of capacitor layer time-constant with diameter d (Figure 6.12).

6.3.2 Modeling and simulation results

For simplicity, and to reduce computation time, the 225 cylindrical capacitors are grouped together into nine groups with 25 adjacent cylindrical capacitors in each group. One equivalent cylinder is formed from each of the nine groups of cylinders assuming each capacitor cylinder (of the 25 in a group) is connected in parallel, and the corresponding ESR and the capacitance values are listed in Table 6.3.

Table 6.3 Estimated values of parameters for equivalent cylindrical capacitors

	C 1 (Outer)	C 2	C 3	C 4	C 5	C 6	C 7	C 8	C 9 (Inner)
ESR (mΩ)	195.4	220.6	253.6	298.1	361.5	459.1	629.0	998.4	2419.0
Capacitance (μF)	567.7	502.6	437.5	372.4	307.4	242.3	177.2	112.1	46.96

The parameters listed for the nine capacitors in Table 6.3 are used to simulate in *Saber* circuit simulation software. The current distribution in the different parallel-connected capacitor layers is shown in Figure 6.15. A triangular current pulse of time duration 2.4 ms *I_source*, shown in Figure 6.16, which closely resembles the experimental transient current shown in Figure 6.2, is applied to the parallel-connected capacitor layers. Figure 6.16 also shows the distribution of current through different capacitor layers for a successful pulse.

It was observed in Figure 6.4 that the capacitor voltage is clamped in region 2 even in the presence of positive capacitor current. Therefore, it can be interpreted that the aluminum-oxide layer inside the capacitor acts a '*zener diode*' and causes the capacitor voltage clamping. However, the voltage clamping level depends upon the quality and thickness of the aluminum-oxide at each layer. In addition, each of the capacitor layers has almost the same time-constant, as shown in Figure 6.14. Therefore, the rate of charging of each capacitor across a '*zener diode*' in Figure 6.15 is the same provided there is no voltage-clamping effect across any of these '*zener diodes*'. Furthermore, there is no dangerous concentration of current on a single layer provided each of these '*zener diodes*' reaches its voltage-breakdown level almost at the same time.

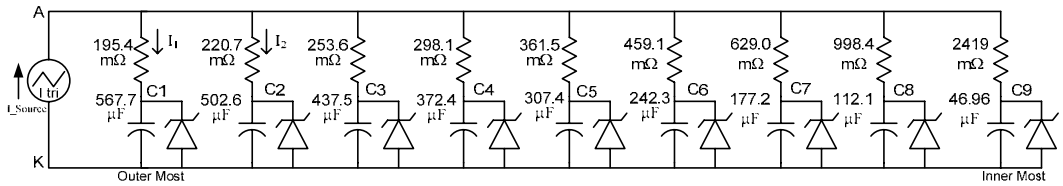


Figure 6.15 Electrolytic capacitor model.

Figure 6.16 shows the effect of reaching '*zener diodes*' voltage-breakdown level almost at the same time in region 2, and also shows that there is no dangerous concentration of current in any layers of the capacitor. This is further verified using the energy per unit volume of the capacitor layer plot in Figure 6.17, which is almost the same for every layer, and causes no harm to the capacitor.

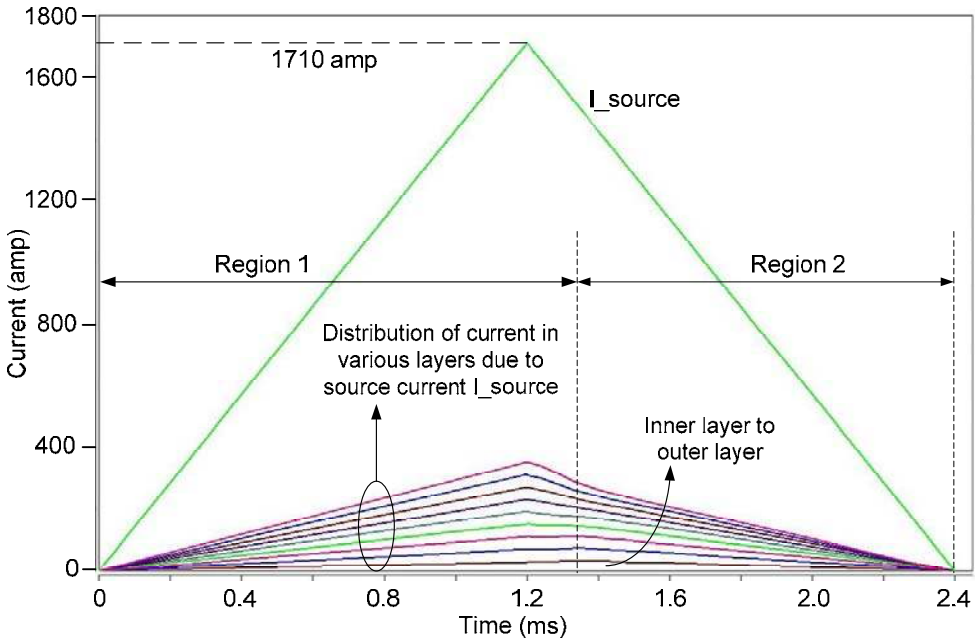


Figure 6.16 Distribution of the capacitor layers' current for successful pulse.

In order to illustrate the failure of the capacitor because of a concentration of current in a small region, the breakdown voltage of one *'zener diode'* is now reduced in the simulation. This may occur because of the manufacturing defect of the capacitor, or it may occur if the amplitude of the current for a successful pulse in Figure 6.16 is high enough to cause partial damage to the capacitor layers. These damaged layers will exhibit

a lower breakdown-voltage compared to the other layers inside the capacitor for a subsequent operation.

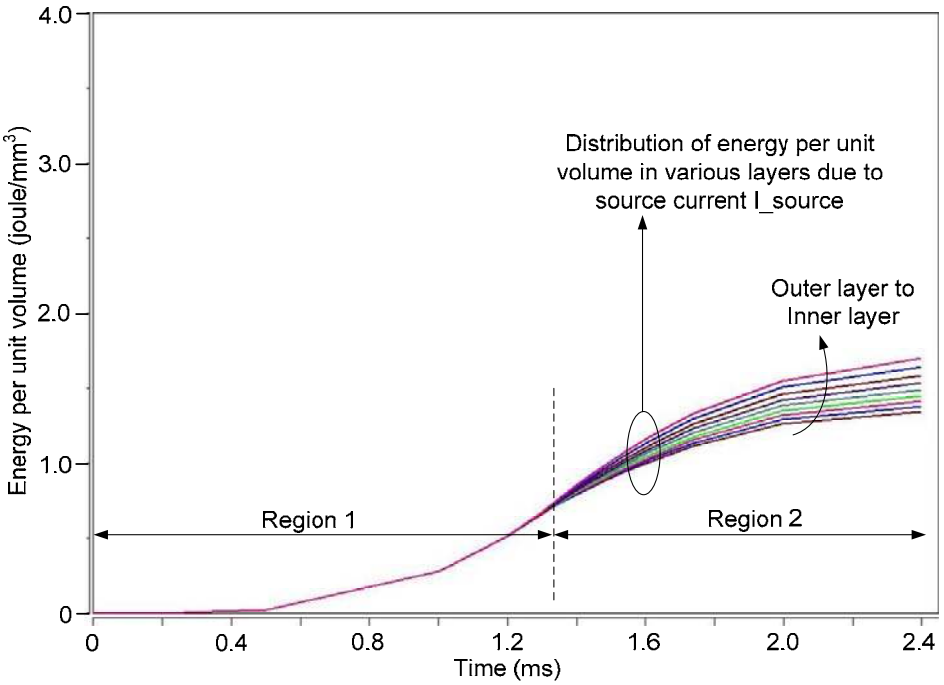


Figure 6.17 Distribution of energy per unit volume for electrolytic capacitor layers for successful pulse.

Further, in order to understand the effect of lower breakdown-voltage of a '*zener diode*', it is assumed that the first capacitor layer (outer most layer) represents the layer with a reduced breakdown-voltage. Region 1 in Figure 6.18 shows the distribution of current through the various capacitor layers follow the ESR values of those layers, when there is no voltage-clamping for any of '*zener diodes*' in Figure 6.15. However, the '*zener diode*' in first layer of the capacitor reaches its breakdown-voltage level ahead of all the other '*zener diodes*'. This results in a dangerous concentration of current in the first capacitor layer. This phenomenon can also be observed in the energy per unit volume plot shown in Figure 6.19, which confirms that the energy density inside the first capacitor layer is much higher compared to the other layers inside the capacitor, and this may damage the capacitor.

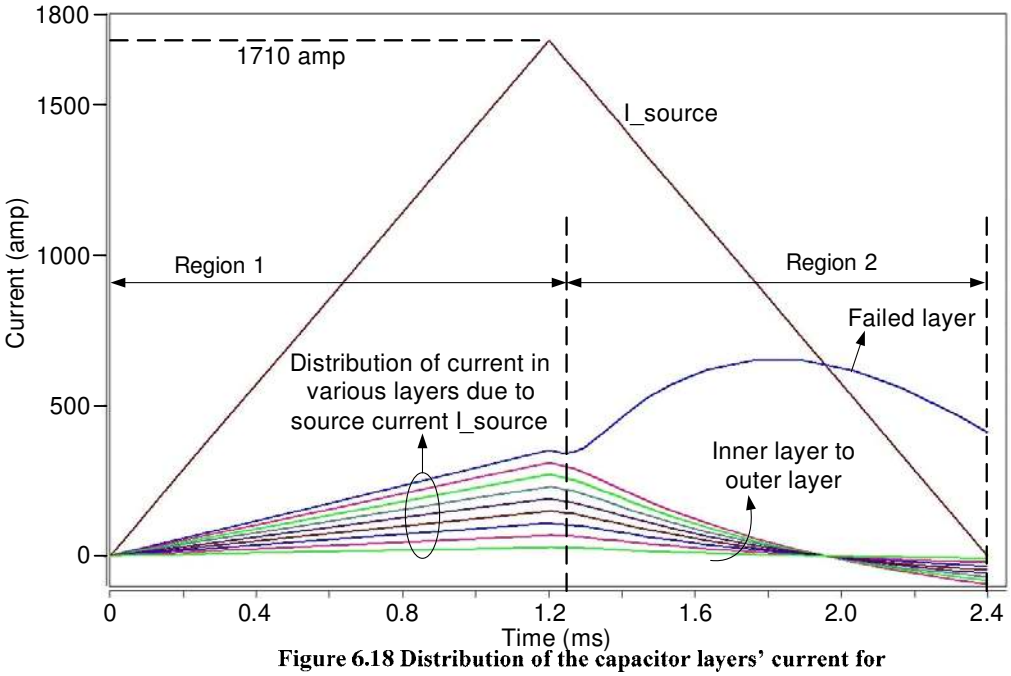


Figure 6.18 Distribution of the capacitor layers' current for unsuccessful pulse.

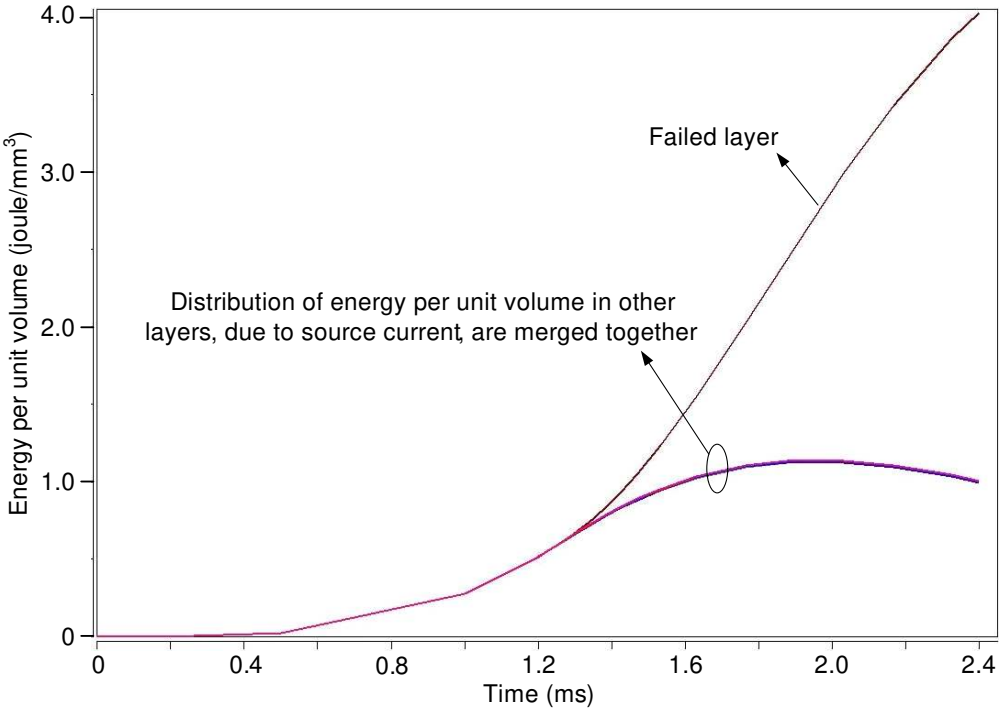


Figure 6.19 Distribution of energy per unit volume for electrolytic capacitor layers for unsuccessful pulse.

The effect of the breakdown of the first capacitor layer on the other capacitor layers, say the second layer, is now investigated further to understand the overall effect of

a capacitor layer breakdown. Suppose, V_{C1K} and V_{C2K} are the voltages across the first and second capacitor layers respectively, and I_1 and I_2 are the corresponding currents shown in Figure 6.15, and V_{AK} is the overall voltage across the capacitor terminal.

Using results from the *Saber* simulation, Figure 6.20 illustrates the effect of breakdown of the first capacitor layer on the second capacitor layer. Breakdown of the first capacitor occurs at the dotted line in Figure 6.20, and the majority of the current starts to flow through the first layer. The voltage across the first capacitor, V_{C1K}, is clamped to the breakdown voltage of the '*zener diode*' in the first capacitor layer. After voltage clamping in the first layer, the current through the second capacitor layer starts to decrease and goes to zero, and reverses the current direction to dump its energy to the first capacitor layer. This phenomenon continues in all other remaining capacitors layers.

Therefore, it can be interpreted that the '*zener diode*' breakdown in only one layer of the capacitor results in a dangerous concentration of a majority of the current at a single layer, and it may lead to a hot spot build up inside the capacitor, which may lead to partial or catastrophic failure of the capacitor. In the next section, experimental results are presented in order to understand the effect of a current surge on the leakage resistance of the capacitor.

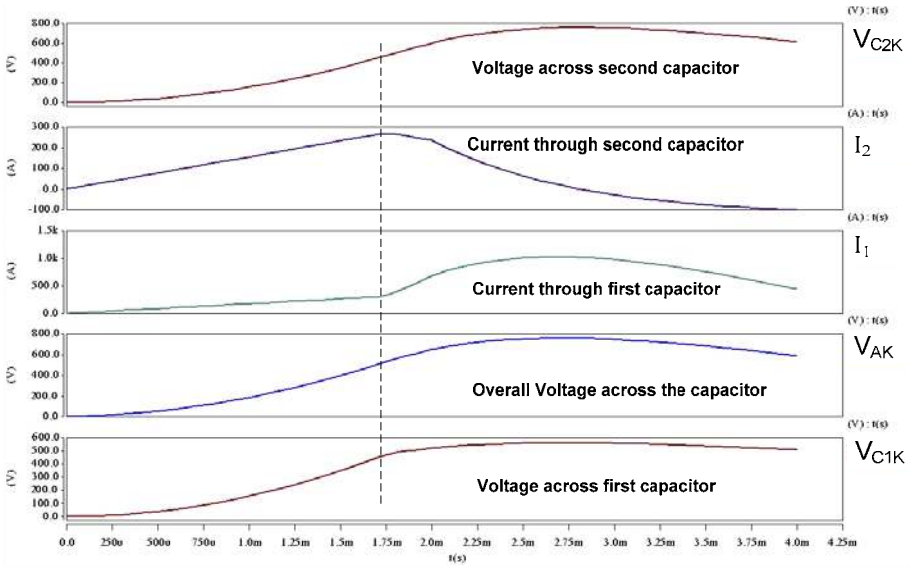


Figure 6.20 Effects of '*Zener diode*' like breakdown.

6.3.3 Experimental results

Figure 6.21 shows an experimental setup to test the effect of current pulses on an electrolytic capacitor. The capacitor bank C_{bank} is charged to a desired voltage by an auto-transformer followed by a bridge-rectifier D_1. Inductor L is used to control the amplitude of the current pulses to the test-capacitor C_{test}. Diode D_2 acts as a freewheeling diode for inductor L. Resistors R_1 and R_2 are potential divider elements to apply a predetermined voltage-bias to the test capacitor C_{test} in a particular test. Diode D_3 is used to prevent the test capacitor C_{test} from discharging through resistor R_2. In addition, a mechanical switch S_{mech} is used to prevent charging of the capacitor C_{test} during the discharge process of the capacitor through its own leakage resistance. IGBT is switched on for a short duration of time in order to generate a current-pulse for a given input voltage across C_{bank} and for a given voltage bias across C_{test}. The gate of the IGBT is connected to an IGBT-driver BG2A by *Powerex,* and the datasheet for BG2A is listed in Appendix D.

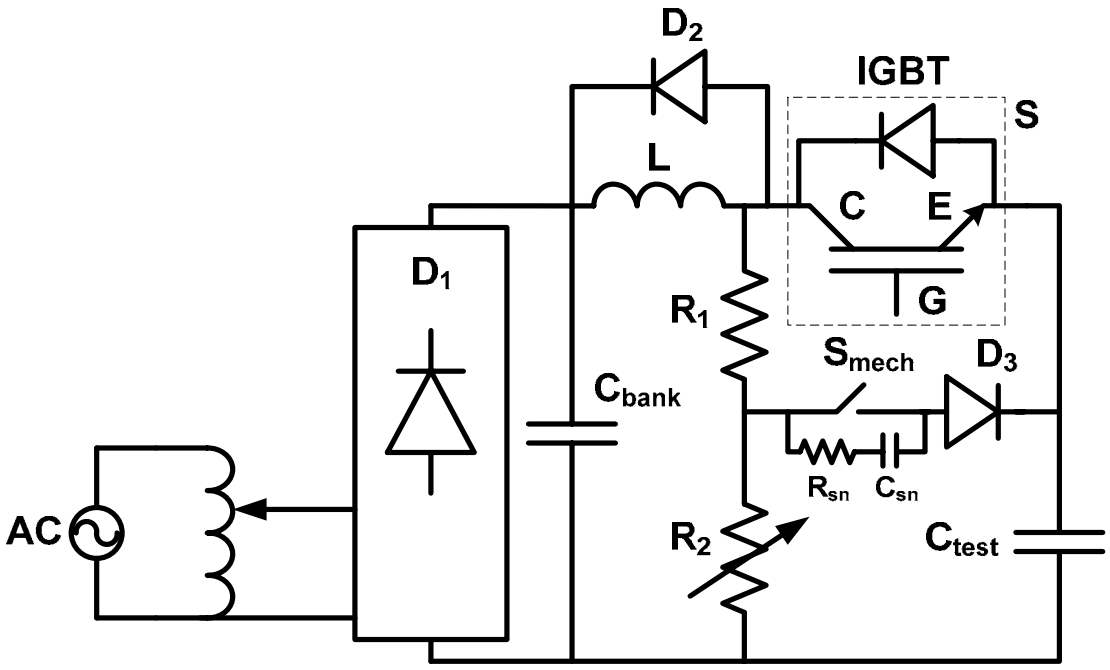


Figure 6.21 Circuit diagram for effects of current-pulses testing.

The primary result is the highest measured voltage level on the capacitor before failure, and secondary result is the largest inrush current (without failure). Figure 6.22 shows an example where the capacitor was able to absorb the pulse without failure, and Figure 6.23 shows an example where the capacitor failed to absorb the pulse. The latter shows that the voltage, instead of remaining at a high level, drops sharply after the failure, and loses the property of a capacitor and the capacitor is considered as damaged.

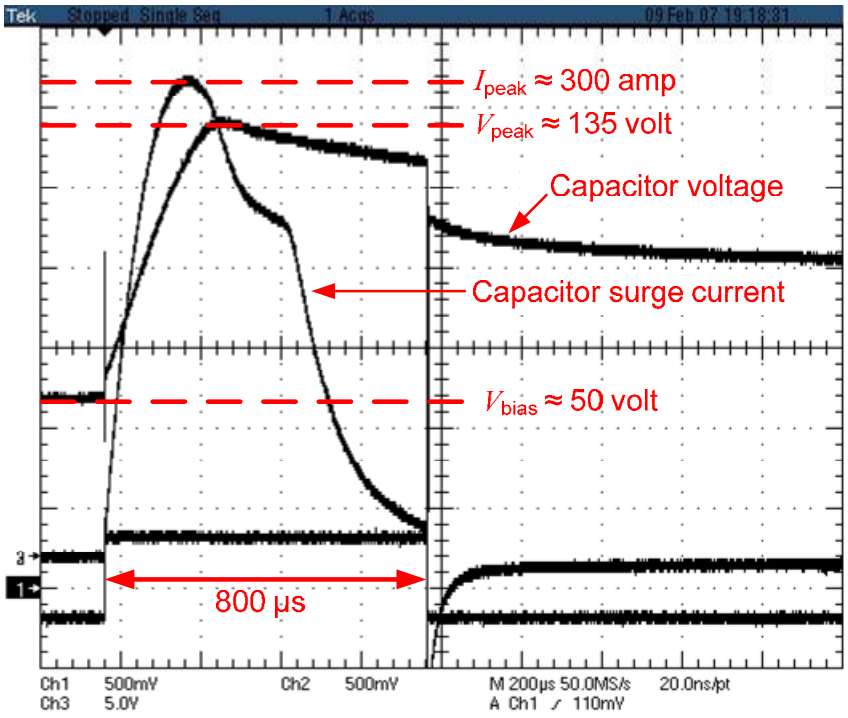


Figure 6.22 Voltage and current plots for a successful current pulse.

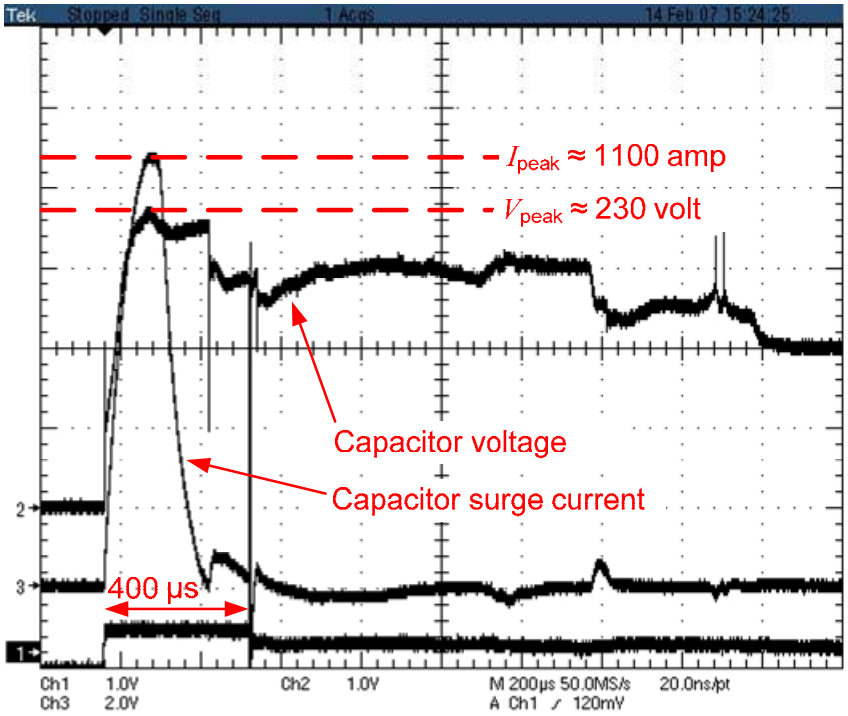


Figure 6.23 Voltage and current plots for an unsuccessful current pulse.

A high bandwidth current sensor by *Pearson Electronics Inc* shown in the experimental setup in Figure 6.24 is used to capture the current pulse waveforms shown in Figures 6.22 and 6.23. The datasheet of the current sensor is given in Appendix E. The capacitor bank C_{bank} and the test capacitor C_{test} are not shown in Figure 6.24, however, the oven shown in Figure 3.4 in Chapter 3 is used to hold C_{bank} and C_{test} in order to prevent any exposure to atmosphere in the event of damage to the capacitors. In addition, the oven is also used to run the experiment with C_{test} at the elevated temperatures. After each pulse, leakage-resistance of the capacitor is calculated by measuring time, $\Delta t = t_2 - t_1$, between two known voltages $v(t_1)$ and $v(t_2)$, while the capacitor is discharging, using equation (6.15)

$$R_{Leakage} = \frac{\tau}{C} = \frac{\Delta t}{C \ln\left(\frac{v(t_1)}{v(t_2)}\right)} \tag{6.15}$$

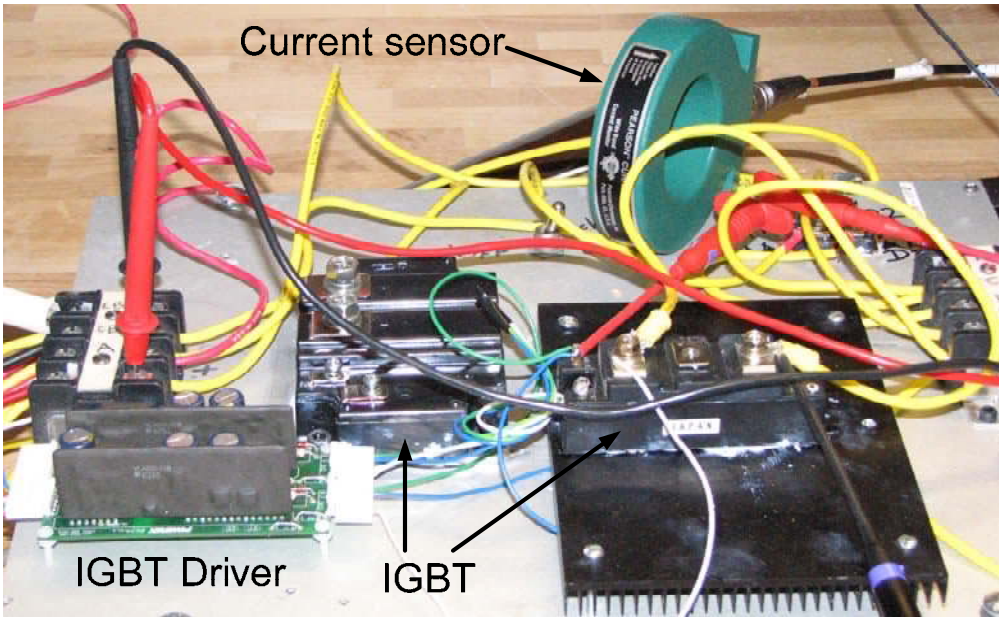


Figure 6.24 Experimental setup for current surge effects.

6.3.3.1 Effect of current pulses with short interval

Figure 6.25 shows the effect of current pulses on leakage-resistance of electrolytic capacitors for three different electrolytic capacitors with the same ratings of 1000 µF, 50 V, 85 ºC by *Panasonic*. Monotonic changes in the leakage resistances for the three capacitors are observed with successive pulses at approximate intervals of around one to 15 minutes depending on the time taken by capacitor in discharging from $v(t_1)$ and $v(t_2)$, and values of leakage-resistances are measured between current pulses. The values of leakage resistances decrease with each current pulse as shown in Figure 6.25.

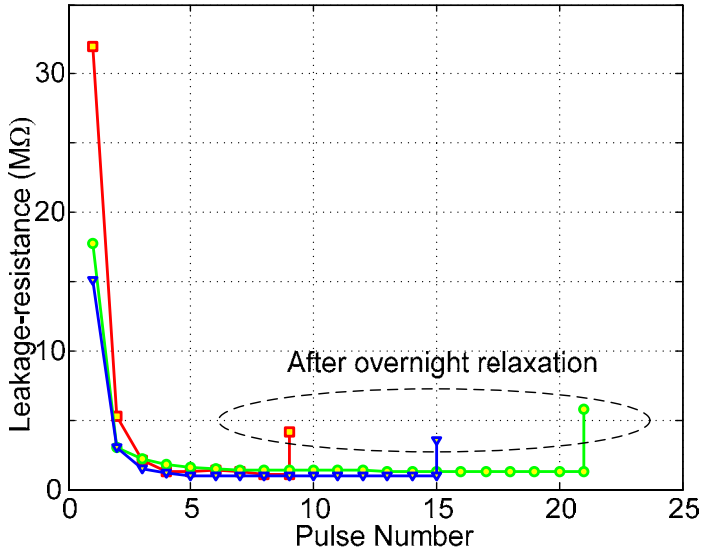


Figure 6.25 Effect of current pulses on electrolytic capacitor leakage resistances.

Figure 6.25 indicates that damage to the capacitors takes place within the first few current pulses. The tested capacitors are left overnight to cool down and the leakage resistances for these capacitors are again measured. The relaxed leakage-resistances do not return to their original values, which indicate that there is permanent physical damage to the capacitor layers.

6.3.3.2 Effect of temperature

In order to understand the effects of temperature on the values of leakage-resistance, a new capacitor and a current pulse weakened capacitor are placed in an oven and values of leakage resistances are plotted over temperatures in Figure 6.26. The leakage resistances decrease with temperature, however, after overnight relaxation, the leakage resistances of these two capacitors return to original values. This suggests that the change in leakage resistances due to temperature is a temporary effect, unlike the permanent effects due to current pulses shown in Figure 6.25. Therefore, it suggests that the short-duration high current pulses generate high temperatures in small-localized regions of the capacitor layers, which result in partial or complete damage to the capacitor layers.

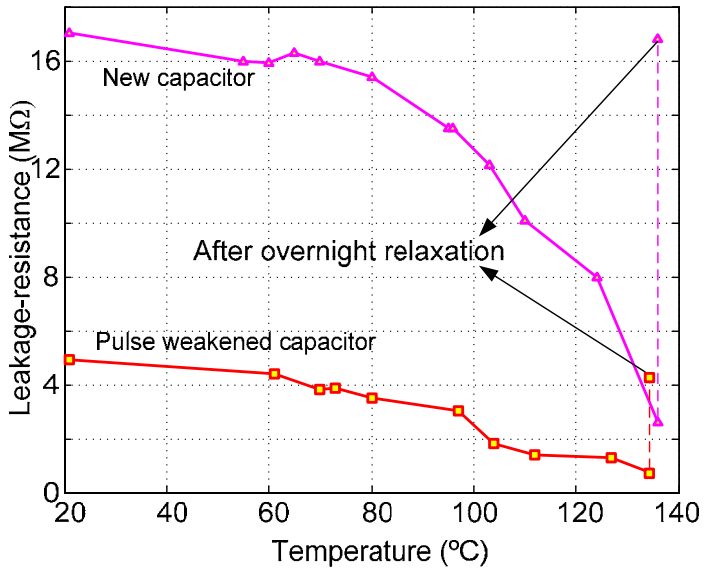


Figure 6.26 Effect on leakage-resistance of temperature on new and current pulse weakened capacitors.

6.3.3.3 Effect of current pulses with a long interval between pulses

Figures 6.27 and 6.28 show the effects of current pulses with 30 to 45 minutes of relaxation after each current pulse with two different capacitors but with the same ratings

of 1000 µF, 50 V, 85 ºC by *Panasonic*. Long time-interval of 35 to 45 minutes is chosen to ensure that capacitor is relaxed before applying next current pulse to the capacitor.

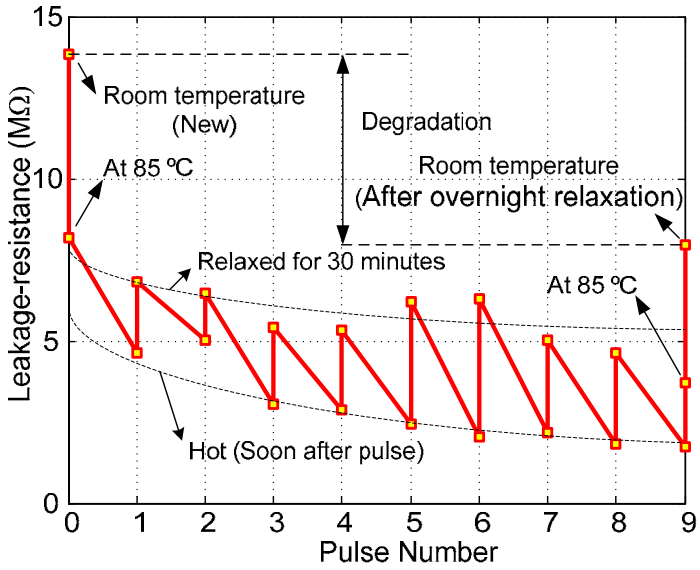


Figure 6.27 Effect of current pulses with relaxation at 85 °C with first capacitor.

Figure 6.27 shows the effect of current pulses at rated ambient temperature of 85 ºC. Each current pulse causes a permanent damage to the capacitor. After the test, capacitor is left at room temperature to relax for overnight, as it can be observed from the Figure 6.27 that the capacitor leakage-resistance is not able to reach its original room-temperature value, and suggests that the current pulses have caused permanent damage to the capacitor.

Similar results are observed for current pulses at room temperature, as shown in Figure 6.28. These results suggest that the each current pulse causes physical damage to the capacitors.

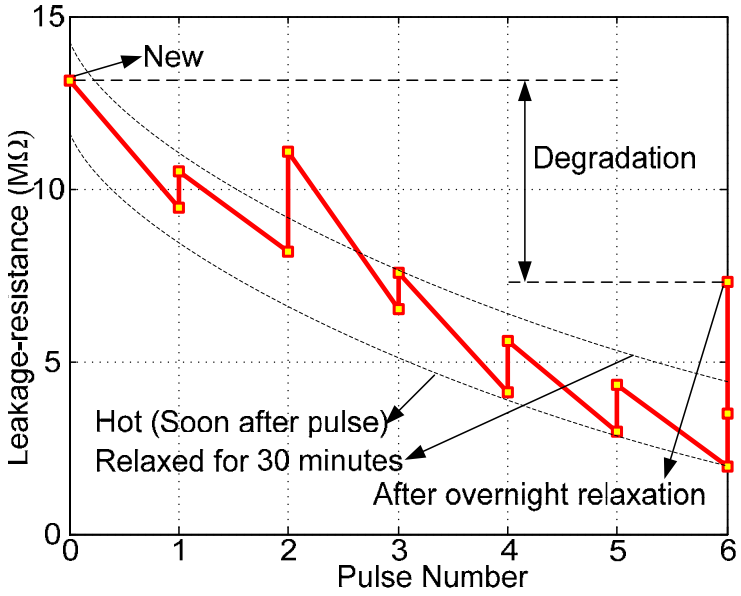


Figure 6.28 Effect of current pulses with relaxation at room temperature with second capacitor.

6.4 Summary

Aluminum electrolytic capacitors are especially sensitive components with respect to current-surges beyond the rated limits, which cause hot-spot regions inside the capacitor. However, it is often impossible to determine the exact maximum current-surge limit, which will never be exceeded in the application, especially when considering short duration transients. The usual solution for the problem is to require a safety margin between the current-surge capability of the capacitor and ripple-current requirement in an application. However, cost optimization requirements tend to drive design engineers to reduce the safety margin as much as possible.

CHAPTER 7

CONCLUSIONS, CONTRIBUTIONS, AND RECOMMENDATIONS

7.1 Summary and conclusions

The purpose of this research is to advance the field of condition monitoring for electrolytic capacitors for power electronics applications. Electrolytic capacitors are responsible for an estimated 60 % of the failures in power electronics circuits [1]. Condition monitoring of electrolytic capacitors is therefore assuming a growing importance in critical high performance applications. Early detection of imminent faults would allow preventive maintenance, and provide sufficient time for the controlled shutdown of the process, thereby reducing the costs of unplanned outage-time and repairs.

7.1.1 Conclusions of research of phase 1: Electrolytic capacitor ripple voltage and current behavior with aging

The fundamentals of an electrolytic capacitor construction, manufacturing process, and the failure modes are presented. A detailed literature survey is presented to summarize the state of the art techniques that are pertinent to the methods proposed in this research. The present research is organized into four sections. The first phase of this

research consists of the study of the effect of capacitor aging on the capacitor ripple voltage and current, assuming these are observable. There exists a direct relation between the aging of the capacitor and the capacitor ripple voltage and ripple current, and it is verified by experimental results. A time-average method is introduced for the condition monitoring of the capacitor using capacitor ripple voltage and current. A monotonic time-average plot is drawn for the capacitor ripple voltage, and a threshold point can be set on the plot to predict the failure of the capacitor. Further, an impedance time-average plot is drawn using capacitor ripple voltage and ripple current, and a similar threshold can be set on the impedance plot to predict the failure of the capacitor. However, the time-average plot for the capacitor ripple voltage is also a function of the variation in the load resistance; therefore, it cannot be used for a converter with varying load. The time-average plot for the impedance therefore gives a more reliable indication of the aging of the capacitor in variable load conditions because it is the ratio of the capacitor ripple voltage and ripple current fundamental. In other words, any change in the capacitor ripple voltage will result in a proportional change in the capacitor ripple current to keep the ratio of these two quantities equal to the impedance of the capacitor at the fundamental switching frequency. Results have showed that an aged capacitor typically has a reduction in capacitance by a factor of 1000, and in ESR by a factor of 11.

7.1.2 Conclusions of research of phase 2: System modeling

The second phase of work is an extension of phase 1. It proposes a method for predicting a fault in the capacitor using the input current of the converter, which is easier to measure than the capacitor ripple voltage. There exists some correlation between the converter input current and the capacitor ripple voltage. Based on this a LMS based

system modeling of the converter is presented to estimate the value of the time-average values of the capacitor ripple voltage. Further, the time-average capacitor ripple voltage is plotted over time for fault monitoring of the capacitor, as described in phase 1, but this would suffer from the drawback during variable load conditions. This gives an alternate method of monitoring the condition of an electrolytic capacitor where capacitor ripple voltage and ripple current are not observable, nevertheless works well for a stationary system.

7.1.3 Conclusions of research of phase 3: Real-time parameter estimation

The third phase of this research proposes a new low cost method to detect the changes in the equivalent series resistor (ESR) and the capacitance value of an electrolytic capacitor in order to realize a real-time condition-monitoring scheme for an electrolytic capacitor. In phase 2, it was demonstrated that effects of changes in the capacitor condition would be reflected in the capacitor ripple voltage and ripple current. However, the work in phase 3 has demonstrated that it is possible to measure the changes in the capacitor parameters directly in order to monitor condition of the capacitor. The main advantages of the proposed method include circuit simplicity, low-cost, and easy implementation. It uses the fact that the there exists three frequency-bands in the Bode-plot of the capacitor where ESR, capacitance, and series inductance of the capacitor are individually dominant. The capacitor ripple voltage and current are processed in the three frequency bands to estimate the parameters of the capacitor. It is important to note that it is not required to remove the capacitor from the converter system, and that it monitors the capacitor parameters in real-time. The proposed method has been demonstrated for a stationary system, in a constant load condition. However, it is possible to use this method

in variable load conditions provided the frequency of load variation is slow. Slow variations in load will ensure that side-bands appear within the band-pass filter response described in Chapter 5.

7.1.4 Conclusions of research of phase 4: Capacitor failure due to inrush current

The fourth phase of this research presents fault characterization of electrolytic capacitors because of inrush current due to supply surge-voltage. Inrush current causes generation of hot spots inside the capacitor volume, and results in a decrease of the capacitor leakage-resistance. In addition, the capacitor may rupture with an explosive sound if the rise in the temperature is too high in the hot-spot regions. These hot-spot regions act as low resistance paths in parallel to the capacitor leakage-resistance and cause quasi-short-circuit conditions, which lead to rupturing of the capacitor. Results show that the leakage resistance decreases typically by a factor, which varies between 2 and 5, depending on the repetitive rate of the pulses. A detailed study of the failure mode due to inrush current along with an electrical circuit model is introduced.

7.2 Contributions

Based on the research presented in Chapters 3 and 4, three papers have been presented in three IEEE conferences. The first paper titled *"Condition Monitoring of Electrolytic Capacitor in Power Electronic Circuits Using Signal Processing Method"* has been presented at the *20th IEEE Annual Applied Power Electronics Conference (APEC)* in March 2005 in Austin, Texas [43]. The second paper titled *"Condition Monitoring of Electrolytic Capacitor in Power Electronic Circuits Using Adaptive Filter Modeling"* has been presented at the *36th IEEE Power Electronics Specialists Conference*

(PESC) in June 2005 in Recife, Brazil [44]. The third paper titled *"LMS Based Condition Monitoring of Electrolytic Capacitors"* has been presented at the *32nd Annual Conference of IEEE Industrial Electronics Society (IECON)* in Nov 2005 in Raleigh, NC [45]; this paper has also been submitted for journal review to the *IEEE Transaction on Industrial Electronics* and reports on the research in Chapter 4 [46].

Based on the research in Chapter 5, a paper titled *"Real-Time Condition Monitoring of Electrolytic Capacitors by Parameter Estimation"* has been presented at the *22nd IEEE Annual Applied Power Electronics Conference (APEC)* in March 2007 in Anaheim, CA [47]. The sixth paper, which is based on the work presented in Chapter 6, has been accepted for IEEE IAS 2007 to be presented during September 23-27 at New Orleans, LA.

The main contributions of this research to the field of electrolytic capacitor condition monitoring are summarized as follows:

- An experimental study has been conducted to evaluate the effect of aging of the electrolytic capacitors on the capacitor ripple voltage and current and concluded that capacitor ripple voltage is a good indicator of aging when loads are relatively constant. For varying loads, the ratio of ripple voltage to ripple current is a good indicator.
- When capacitor ripple voltage and ripple current are not available, an alternative system modeling-based technique has been proposed to estimate the capacitor ripple voltage from the converter input current, and use this estimated ripple voltage as an indicator of aging.

- As another alternative, a new low cost real-time condition monitoring of electrolytic capacitors scheme has been proposed which estimates the ESR and C values in real-time (using a low-cost analog electronic circuit) and which can be used as an indicator of aging.
- Research works listed above are useful to monitor the capacitor failure because of aging. A detailed analysis of the failure of an electrolytic capacitor due to sudden inrush current can has been evaluated to show that local hot spots are created which lead to a decrease in leakage resistance and eventually to quasi-short circuit.

7.3 Recommendations for future research

The purpose of a dissertation is to advance the science in a given field. After this objective is achieved, there is generally still much work remaining to implement this new knowledge into widespread application. Nevertheless, there is still additional work required to poise these new condition-monitoring schemes for application in industries. Some of the works that could initiate interesting research in the future are as follows:

7.3.1 Investigating different kinds of non-stationary operation

Most of the reported works in this dissertation are verified for a stationary system. The reported fault-monitoring scheme using parameter estimation in Chapter 5 can be used for non-stationary systems such as inverters with variable load. As explained in section 7.1.3, parameter estimation technique can be used for variable load conditions provided frequency of load variation is slow. However, further research is needed to classify different non-stationary system frequency-spectrum to develop a comprehensive electrolytic capacitor fault-monitoring scheme. A detailed analysis of non-stationary

system frequency-spectra provides an opportunity to use an inexpensive analog-circuit proposed in Chapter 5 to process the capacitor ripple voltage and ripple current to estimate the parameters of the capacitor in real-time.

7.3.2 Condition monitoring using temperature

The majority of power electronics systems often contain several temperature monitoring devices. One more could be added to monitor the temperature of the capacitor. More research works are needed to investigate further whether there is a direct relationship between the changes in the capacitor ripple voltage and temperature of the capacitor. This will give an opportunity to use the method demonstrated in Chapter 3 using measured temperature instead of capacitor ripple voltage, or a combination of the two.

7.3.3 Relaxation of pulse weakened capacitor with DC bias voltage

As discussed in Chapter 6, the leakage-resistance of the capacitor increases if left for overnight to relax. An electrolytic capacitor has a self-healing property, and it will be interesting to investigate whether this damage in the capacitor is reversible or not, particularly if relaxation is done with a DC bias voltage.

7.3.4 Expansion to other faults in the system

As discussed in Chapter 4, various waveforms in a system are correlated with each other with varying degrees of correlation. Therefore, it may be possible to implement a fault-monitoring scheme that can use an optimal number of signals to monitor the condition of various other components in a system.

APPENDIX A

NI 6036E FAMILY SPECIFICATIONS

This document lists the I/O terminal summary and specifications for the devices that make up the NI 6034E/6035E/6036E family of devices. This family includes the following devices:

- NI PCI-6034E
- NI PCI-6035E
- NI DAQCard-6036E
- NI PCI-6036E

I/O Terminal Summary

Note With NI-DAQmx, National Instruments revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ (Legacy) terminal names and their NI-DAQmx equivalents, refer to *Terminal Name Equivalents* of the *E Series Help*.

Table 1. I/O Terminals

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AI <0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AI SENSE	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AI GND	—	—	—	—	—	—	—
AO 0†	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—
AO 1†	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—
AO GND	—	—	—	—	—	—	—
D GND	—	—	—	—	—	—	—

Table 1. I/O Terminals (Continued)

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
+5 V	—	0.1 Ω	Short-circuit to ground	1 A fused	—	—	—
P0.<0..7>	DIO	—	V_{CC} + 0.5	13 at (V_{CC} – 0.4)	24 at 0.4	1.1	50 kΩ pu
AI HOLD COMP	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
EXT STROBE*	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 0/ (AI START TRIG)	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 1/ (AI REF TRIG)	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 2/(AI CONV CLK)*	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 3/ CTR 1 SOURCE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 4/CTR 1 GATE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 1 OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 5/ (AO SAMP CLK)*	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 6/ (AO START TRIG)	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 7/ (AI SAMP CLK)	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 8/ CTR 0 SOURCE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 9/ CTR 0 GATE	DIO	—	V_{CC} + 0.5	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 0 OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu

Table 1. I/O Terminals (Continued)

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
FREQ OUT	DO	—	—	3.5 at (V_{CC} – 0.4)	5 at 0.4	1.5	50 kΩ pu

* Indicates active low.

† NI 6035E/6036E only.

AI = Analog Input DIO = Digital Input/Output pu = pull-up
AO = Analog Output DO = Digital Output

Note: The tolerance on the 50 kΩ pull-up resistors is large. Actual value might range between 17 kΩ and 100 kΩ.

Specifications

The following specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable per channel)

Type of A/D converter (ADC)..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Max sampling rate ..... 200 kS/s guaranteed

Input signal ranges

Range (Software-Selectable)	Bipolar Input Range
20 V	±10 V
10 V	±5 V
1 V	±500 mV
100 mV	±50 mV

Input coupling ..... DC

Max working voltage (signal + common mode) ..... Each input should remain within ±11 V of ground

Overvoltage protection

Signal	Powered On (V)	Powered Off (V)
AI <0..15>, AI SENSE	±25	±15

FIFO buffer size

NI DAQCard-6036E ..... 1,024 samples (S)
NI 6034E, NI 6035E, NI PCI-6036E ..... 512 S

DMA (PCI only)

Channels..... 1
Data sources/destinations..... Analog input, analog output, counter/timer 0, or counter/timer 1
Data transfers..... Direct memory access (DMA)[1], interrupts, programmed I/O
DMA[1] modes..... Scatter-gather (single transfer, demand transfer)

Configuration memory size..... 512 words

NI 6034E, NI 6035E, NI PCI-6036E

Range 10 to 20 V 0.8

Range 1 V 1.0

Range 100 mV 6.2

Crosstalk ..... DC to 100 kHz

Adjacent channels ..... –75 dB

Other channels ..... –90 dB

Stability

Recommended warm-up time

NI DAQCard-6036E ..... 30 minutes

NI 6034E, NI 6035E, NI PCI-6036E ..... 15 minutes

Offset temperature coefficient

Pregain ..... ±20 µV/°C

Postgain ..... ±175 µV/°C

Gain temperature coefficient ..... ±20 ppm/°C

Analog Output (NI 6035E/6036E Only)

Output Characteristics

Number of channels ..... 2 voltage

Resolution

NI DAQCard-6036E, NI PCI-6036E ..... 16 bits, 1 in 65,536

NI 6035E ..... 12 bits, 1 in 4,096

Max update rate

DMA[1] ..... 10 kHz, system-dependent

Interrupts ..... 1 kHz, system-dependent

Type of D/A converter (DAC) ..... Double buffered, multiplying

FIFO buffer size ..... None

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (single transfer, demand transfer)

Accuracy Information

Device	Nominal Range at Full Scale (V)	Absolute Accuracy					
		% of Reading			Offset (µV)	Temp Drift (%/°C)	Absolute Accuracy at Full Scale (mV)
		24 Hours	90 Days	1 Year			
NI DAQCard-6036E	±10	0.0091	0.0111	0.0133	1.22	0.0005	2.547
NI 6035E	±10	0.18	0.02	0.022	5.93	0.0005	8.127
NI PCI-6036E	±10	0.009	0.011	0.013	1.1	0.0005	2.417

Note: Accuracies are valid for measurements following an internal E Series calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature. NI recommends a one-year calibration interval. The Absolute Accuracy at Full Scale calculations were performed for a maximum range input voltage (for example, 10 V for the ±10 V range) after one year, assuming 100 points of averaged data. Go to `ni.com/info` and enter info code `rdspec` for example calculations.

Figure 2. NI 6035E/6036E Pinout

APPENDIX B

LTC 1968: PRECISION WIDE BANDWIDTH RMS-TO-DC CONVERTER

FEATURES

- **High Linearity:**
  0.02% Linearity Allows Simple System Calibration
- **Wide Input Bandwidth:**
  Bandwidth to 1% Additional Gain Error: 500kHz
  Bandwidth to 0.1% Additional Gain Error: 150kHz
  3dB Bandwidth Independent of Input Voltage Amplitude
- **No-Hassle Simplicity:**
  True RMS-DC Conversion with Only One External Capacitor
  Delta Sigma Conversion Technology
- **Ultralow Shutdown Current:**
  0.1μA
- **Flexible Inputs:**
  Differential or Single Ended
  Rail-to-Rail Common Mode Voltage Range
  Up to $1V_{PEAK}$ Differential Voltage
- **Flexible Output:**
  Rail-to-Rail Output
  Separate Output Reference Pin Allows Level Shifting
- **Small Size:**
  Space Saving 8-Pin MSOP Package

APPLICATIONS

- True RMS Digital Multimeters and Panel Meters
- True RMS AC + DC Measurements

DESCRIPTION

The LTC®1968 is a true RMS-to-DC converter that uses an innovative delta-sigma computational technique. The benefits of the LTC1968 proprietary architecture, when compared to conventional log-antilog RMS-to-DC converters, are higher linearity and accuracy, bandwidth independent of amplitude and improved temperature behavior.

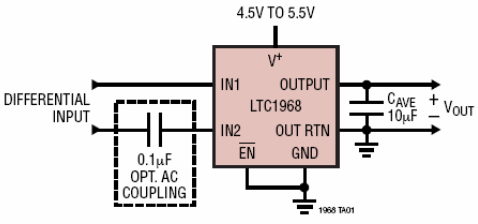
The LTC1968 operates with single-ended or differential input signals and accurately supports crest factors up to 4. Common mode input range is rail-to-rail. Differential input range is $1V_{PEAK}$, and offers unprecedented linearity. The LTC1968 allows hassle-free system calibration at any input voltage.

The LTC1968 has a rail-to-rail output with a separate output reference pin providing flexible level shifting; it operates on a single power supply from 4.5V to 5.5V. A low power shutdown mode reduces supply current to 0.1μA.

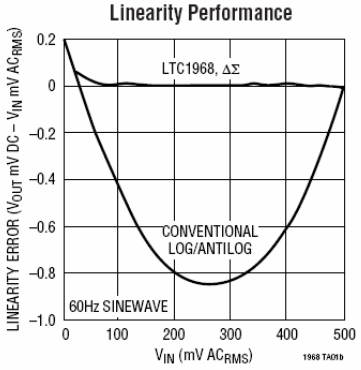
The LTC1968 is packaged in the space-saving MSOP package, which is ideal for portable applications.

TYPICAL APPLICATION

Single Supply RMS-to-DC Converter



Linearity Performance

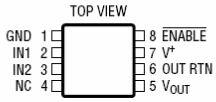


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
  V^+ to GND 6V
Input Currents (Note 2) ..... ±10mA
Output Current (Note 3) ..... ±10mA
$\overline{\text{ENABLE}}$ Voltage ..... –0.3V to 6V
OUT RTN Voltage ..... –0.3V to V^+
Operating Temperature Range (Note 4)
  LTC1968C/LTC1968I ..... –40°C to 85°C
Specified Temperature Range (Note 5)
  LTC1968C/LTC1968I ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 220°C/ W

ORDER PART NUMBER
LTC1968CMS8 LTC1968IMS8
MS8 PART MARKING
LTAFG

Consult LTC Marketing for parts specified with wider operating temperature ranges. The temperature grade (I or C) is indicated on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V_{OUTRTN} = 2.5V, C_{AVE} = 10µF, V_{IN} = 200mV_{RMS}, $V_{\overline{ENABLE}}$ = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Accuracy							
G_{ERR}	Low Frequency Gain Error	50Hz to 20kHz Input (Notes 6, 7)	 ●		±0.1	±0.3 ±0.4	% %
V_{OOS}	Output Offset Voltage	(Notes 6, 7)			0.2	0.75	mV
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Drift	(Note 11)	●		2	10	µV/°C
LIN_{ERR}	Linearity Error	50mV to 350mV (Notes 7, 8)	●		±0.02	±0.15	%
PSRRG	Power Supply Rejection	(Note 9)	 ●		±0.02	±0.20 ±0.25	%/V %/V
V_{IOS}	Input Offset Voltage	(Notes 6, 7, 10)			0.4	1.5	mV
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Drift	(Note 11)	●		2	10	µV/°C
Additional Error vs Crest Factor (CF)							
	CF = 3	60Hz Fundamental, 200mV_{RMS}	●		0.2		mV
	CF = 5	60Hz Fundamental, 200mV_{RMS}	●		5		mV
Input Characteristics							
V_{IMAX}	Maximum Peak Input Swing	Accuracy = 1% (Note 14)	●	1	1.05		V
I_{VR}	Input Voltage Range		●	0		V^+	V
Z_{IN}	Input Impedance	Average, Differential (Note 12) Average, Common Mode (Note 12)			1.2 100		MΩ MΩ
CMRRI	Input Common Mode Rejection	(Note 13)	●		50	400	µV/V
V_{IMIN}	Minimum RMS Input		●			5	mV
PSRRI	Power Supply Rejection	(Note 9)	●		250	700	µV/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V⁺ = 5V, V_{OUTRTN} = 2.5V, C_{AVE} = 10µF, V_{IN} = 200mV_{RMS}, $V_{\overline{ENABLE}}$ = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Characteristics							
OVR	Output Voltage Range		●	0		V⁺	V
Z_{OUT}	Output Impedance	(Note 12)	●	10	12.5	16	kΩ
CMRRO	Output Common Mode Rejection	(Note 13)	●		50	250	µV/V
V_{OMAX}	Maximum Differential Output Swing	Accuracy = 1%, DC Input (Note 14)	 ●	1.0 0.9	1.05		V V
PSRRO	Power Supply Rejection	(Note 9)	●		250	1000	µV/V
Frequency Response							
f_{1P}	1% Additional Gain Error (Note 15)				500		kHz
f_{-3dB}	±3dB Frequency (Note 15)				15		MHz
Power Supplies							
V⁺	Supply Voltage		●	4.5		5.5	V
I_S	Supply Current	IN1 = 20mV, IN2 = 0V IN1 = 200mV, IN2 = 0V	●		2.3 2.4	2.7	mA mA
Shutdown Characteristics							
I_{SS}	Supply Current	$V_{\overline{ENABLE}}$ = 4.5V	●		0.1	10	µA
I_{IH}	$\overline{ENABLE}$ Pin Current High	$V_{\overline{ENABLE}}$ = 4.5V	●	–1	–0.1		µA
I_{IL}	$\overline{ENABLE}$ Pin Current Low	$V_{\overline{ENABLE}}$ = 0.5V	●	–3	–0.5	–0.1	µA
V_{TH}	$\overline{ENABLE}$ Threshold Voltage				2.1		V
V_{HYS}	$\overline{ENABLE}$ Threshold Hysteresis				0.1		V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs (IN1, IN2) are protected by shunt diodes to GND and V⁺. If the inputs are driven beyond the rails, the current should be limited to less than 10mA.

Note 3: The LTC1968 output (V_{OUT}) is high impedance and can be overdriven, either sinking or sourcing current, to the limits stated.

Note 4: The LTC1968C/LTC1968I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LTC1968C is guaranteed to meet specified performance from 0°C to 70°C. The LTC1968C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested nor QA sampled at these temperatures. The LTC1968I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: High speed automatic testing cannot be performed with C_{AVE} = 10µF. The LTC1968 is 100% tested with C_{AVE} = 47nF.

Note 7: The LTC1968 is 100% tested with DC and 10kHz input signals. Measurements with DC inputs from 50mV to 350mV are used to calculate the four parameters: G_{ERR}, V_{OOS}, V_{IOS} and linearity error. Correlation tests have shown that the performance limits can be guaranteed with the additional testing being performed to guarantee proper operation of all internal circuitry.

Note 8: The LTC1968 is inherently very linear. Unlike older log/antilog circuits, its behavior is the same with DC and AC inputs, and DC inputs are used for high speed testing.

Note 9: The power supply rejections of the LTC1968 are measured with DC inputs from 50mV to 350mV. The change in accuracy from V⁺ = 4.5V to V⁺ = 5.5V is divided by 1V.

Note 10: Previous generation RMS-to-DC converters required nonlinear input stages as well as a nonlinear core. Some parts specify a "DC reversal error," combining the effects of input nonlinearity and input offset voltage. The LTC1968 behavior is simpler to characterize and the input offset voltage is the only significant source of "DC reversal error."

Note 11: Guaranteed by design.

Note 12: The LTC1968 is a switched capacitor device and the input/output impedance is an average impedance over many clock cycles. The input impedance will not necessarily lead to an attenuation of the input signal measured. Refer to the Applications Information section titled "Input Impedance" for more information.

Note 13: The common mode rejection ratios of the LTC1968 are measured with DC inputs from 50mV to 350mV. The input CMRR is defined as the change in V_{IOS} measured with the input common mode voltage at 0V and V⁺, divided by V⁺. The output CMRR is defined as the change in V_{OOS} measured with OUT RTN = 0V and OUT RTN = V⁺ – 350mV divided by V⁺ – 350mV.

Note 14: The LTC1968 input and output voltage swings are limited by internal clipping. However, its ΔΣ topology is relatively tolerant of momentary internal clipping.

Note 15: The LTC1968 exploits oversampling and noise shaping to reduce the quantization noise of internal 1-bit analog-to-digital conversions. At higher input frequencies, increasingly large portions of this noise are aliased down to DC. Because the noise is shifted in frequency, it becomes a low frequency rumble and is only filtered at the expense of increasingly long settling times. The LTC1968 is inherently wideband, but the output accuracy is degraded by this aliased noise.

APPENDIX C

WIDE BANDWIDTH PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ACCURACY
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

APPLICATIONS

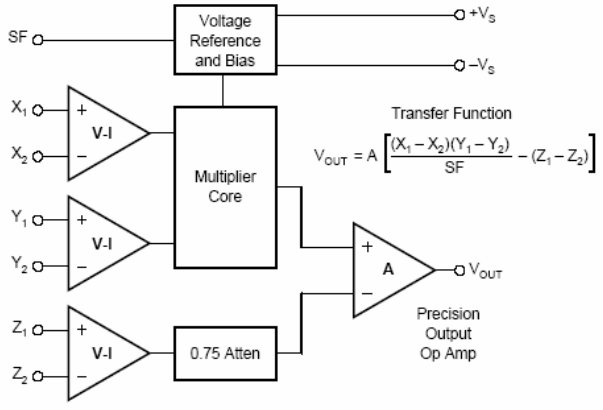
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC, unless otherwise noted.

MODEL	MPY634KP/KU MIN	MPY634KP/KU TYP	MPY634KP/KU MAX	MPY634AM OBSOLETE MIN	MPY634AM OBSOLETE TYP	MPY634AM OBSOLETE MAX	MPY634BM OBSOLETE MIN	MPY634BM OBSOLETE TYP	MPY634BM OBSOLETE MAX	MPY634SM OBSOLETE MIN	MPY634SM OBSOLETE TYP	MPY634SM OBSOLETE MAX	UNITS
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			*			*		
Total Error[1]													
(–10V ≤ X, Y ≤ +10V)			±2.0			±1.0			±0.5			*	%
T_A = min to max		±2.5			±1.5			±1.0				±2.0	%
Total Error vs Temperature		±0.03			±0.022			±0.015				±0.02	%/°C
Scale Factor Error													
(SF = 10.000V Nominal)[2]		±0.25			±0.1			*			*		%
Temperature Coefficient of													
Scaling Voltage		±0.02			±0.01			±0.01			*		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			*			*		%
Nonlinearity													
X (X = 20Vp-p, Y = 10V)		±0.4			±0.4			0.2	±0.3		*		%
Y (Y = 20Vp-p, X = 10V)		±0.01			±0.01			*	±0.1		*		%
Feedthrough[3]													
X (Y Nulled, X = 20Vp-p, 50Hz)		±0.3			±0.3			±0.15	±0.3		*		%
Y (X Nulled, Y = 20Vp-p, 50Hz)		±0.01			±0.01			*	±0.1		*		%
Both Inputs (500kHz, 1Vrms)													
Unnulled	40	50		45	55		*	60		*	*		dB
Nulled	55	60		55	65		60	70		*	*		dB
Output Offset Voltage		±50	±100		±5	±30		*	±15		*	*	mV
Output Offset Voltage Drift		*			±200			±100			*	±500	µV/°C
DYNAMICS													
Small Signal BW,													
(V_{OUT} = 0.1Vrms)	6	10		8	10		*	*		6	*		MHz
1% Amplitude Error													
(C_{LOAD} = 1000pF)		100			100			*			*		kHz
Slew Rate (V_{OUT} = 20Vp-p)		20			20			*			*		V/µs
Settling Time													
(to 1%, ΔV_{OUT} = 20V)		2			2			*			*		µs
NOISE													
Noise Spectral Density:													
SF = 10V		0.8			0.8			*			*		µV/√Hz
Wideband Noise:													
f = 10Hz to 5MHz		1			1			*			*		mVrms
f = 10Hz to 10kHz		90			90			*			*		µVrms
OUTPUT													
Output Voltage Swing	±11			±11			*			*			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			*			*		Ω
Output Short Circuit Current													
(R_L = 0, T_A = min to max)		30			30			*			*		mA
Amplifier Open Loop Gain													
(f = 50Hz)		85			85			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} (V_{CM} = 0)		±12			±12			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0)		±10			±10			*			*		V
(see Typical Performance Curves)													
Offset Voltage X, Y		±25	±100		±5	±20		±2	±10		*	*	mV
Offset Voltage Drift X, Y		200			100			50			*		µV/°C
Offset Voltage Z		±25	±100		±5	±30		±2	±15		*	*	mV
Offset Voltage Drift Z		200			200			100				500	µV/°C
CMRR	60	80		60	80		70	90		*	*		dB
Bias Current		0.8	2.0		0.8	2.0		*	*		*	*	µA
Offset Current		0.1			0.1			*			*	2.0	µA
Differential Resistance		10			10			*			*		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*			*		
Total Error[1] untrimmed													
(X = 10V, –10V ≤ Z ≤ +10V)		1.5			±0.75			±0.35			±0.75		%
(X = 1V, –1V ≤ Z ≤ +1V)		4.0			±2.0			±1.0			*		%
(0.1V≤ X ≤ 10V, –10V ≤ Z ≤ 10V)		5.0			±2.5			±1.0			*		%
SQUARE PERFORMANCE													
Transfer Function		$\frac{(X_1 - X_2)^2}{10V} + Z_2$			$\frac{(X_1 - X_2)^2}{10V} + Z_2$			*			*		
Total Error (–10V ≤ X ≤ 10V)		±1.2			±0.6			±0.3			*		%

SPECIFICATIONS (CONT)

ELECTRICAL

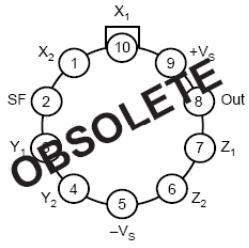
At T_A = +25°C and V_S = ±15VDC, unless otherwise noted.

MODEL	MPY634KP/KU MIN	MPY634KP/KU TYP	MPY634KP/KU MAX	MPY634AM OBSOLETE MIN	MPY634AM OBSOLETE TYP	MPY634AM OBSOLETE MAX	MPY634BM OBSOLETE MIN	MPY634BM OBSOLETE TYP	MPY634BM OBSOLETE MAX	MPY634SM OBSOLETE MIN	MPY634SM OBSOLETE TYP	MPY634SM OBSOLETE MAX	UNITS
SQUARE-ROOTER PERFORMANCE		$\sqrt{10V\ (Z_2 - Z_1)} + X_2$			$\sqrt{10V\ (Z_2 - Z_1)} + X_2$								
Transfer Function ($Z_1 \le Z_2$)								*			*		
Total Error[1] (1V ≤ Z ≤ 10V)		±2.0			±1.0			±0.5			*		%
POWER SUPPLY													
Supply Voltage:													
Rated Performance		±15			±15			*			*		VDC
Operating	±8		±18	±8		±18	*		*	*		±20	VDC
Supply Current, Quiescent		4	6		4	6		*	*		*	*	mA
TEMPERATURE RANGE													
Specification	–40		+85	–25		+85	*		*	–55		+125	°C
Storage	–40		+85	–65		+150	*		*	*		*	°C

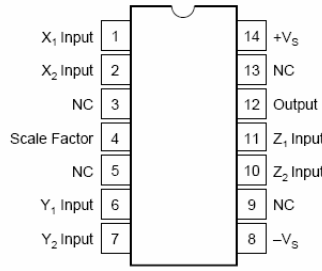
* Specification same as for MPY634AM.
Gray indicates obsolete parts.
NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

PIN CONFIGURATIONS

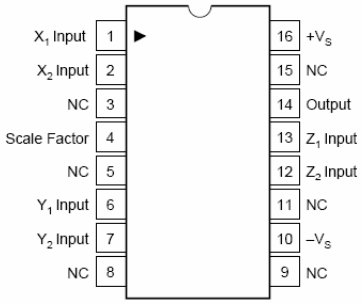
Top View



TO-100: MPY634AM/BM/SM



DIP: MPY634KP



SOIC: MPY634KU

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY634AM/BM OBSOLETE	MPY634KP/KU	MPY634SM OBSOLETE
Power Supply Voltage	±18	*	±20
Power Dissipation	500mW	*	*
Output Short-Circuit to Ground	Indefinite	*	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*	*
Temperature Range:			
Operating	–25°C/+85°C	–40°C/+85°C	–55°C/+125°C
Storage	–65°C/+150°C	–40°C/+85°C	*
Lead Temperature (soldering, 10s)	+300°C	*	*
SOIC 'KU' Package		+260°C	

* Specification same as for MPY634AM/BM.
NOTE: Gray indicates obsolete parts.

ORDERING INFORMATION

MPY634 ( ) ( )

Basic Model Number
Performance Grade[1]
K: U: –40°C to +85°C
Package Code
P: Plastic 14-pin DIP
U: 16-pin SOIC

NOTE: (1) Performance grade identifier may not be marked on the SOIC package; a blank denotes "K" grade.

PACKAGE INFORMATION[1]

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER
MPY634KP	14-Pin PDIP	010
MPY634KU	16-Pin SOIC	211

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

APPENDIX D

BG2A: UNIVERSAL GATE DRIVE PROTOTYPE BOARD

Application NOTES:

Second Release: December 23, 20

BG2A – Universal Gate Drive Prototype Board

Description: BG2A is a fully isolated two channel gate drive circuit designed for use with dual IGBT modules. The BG2A utilizes Powerex VLA500-01 or VLA502-01 hybrid gate drivers to provide efficient switching of modules rated up to 1400A. The hybrid gate drivers also provide protection against unexpected short circuit conditions using desaturation detection. The VLA500-01 and VLA502-01 hybrid gate drivers have an integrated DC to DC converter with 2500VRMS isolation to provide isolated gate drive power. Control signals are isolated using high speed opto couplers with 15KV/us common mode noise immunity. The BG2A provides an isolated fault feedback signal if a short circuit condition is detected.

Features:

- Up to 12A Peak Output Current
- 2500VRMS isolation for control power and signals
- Standard AMP MTA .100" Connectors
- Operates from a single 15VDC supply
- Wide output voltage swing +15V/-8V
- Compact Size 4" x 2.1" (101mm x 53mm)

Applications:

BG2A is designed for use with all Powerex NF, A and NFH series IGBT modules.

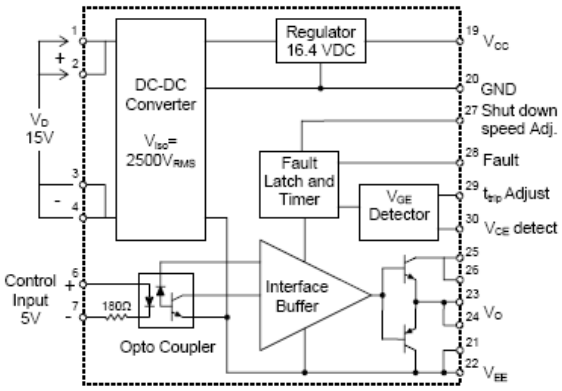
- **Use VLA500-01 hybrid gate drivers for Powerex NF and A Series IGBT modules**
- **Use VLA502-01 hybrid gate drivers for Powerex NFH Series IGBT modules**

Ordering Information: **BG2A-NF** is a kit that includes a bare PCB with two VLA500-01 gate drivers (For use with NF-Series and A-Series IGBT modules)
BG2A-NFH is a kit that includes a bare PCB with two VLA502-01 gate drivers (For use with NFH-Series IGBT modules)
BG2A is a bare PCB only

Circuit Explanation: The BG2A is a basic two channel gate driver designed around the recommended application circuit for the Powerex VLA500-01 and VLA502-01 hybrid gate drivers. A functional block diagram of the VLA500/502 hybrid gate driver is shown for reference in Figure 1. The VLA500-01 uses a standard high speed open collector type opto-coupler with a maximum turn-off propagation delay of 1.3us. This makes it suitable for industrial applications with operating frequencies of up to 20KHz. The VLA500-01 is recommended

for use with Powerex NF-Series and A-Series IGBT modules. The VLA502-01 uses a high speed buffered output type opto-coupler which provides a maximum propagation delay of 0.7us. This makes it suitable for use in high frequency applications operating at more than 20KHz. The VLA502-01 is recommended for use with Powerex NFH-Series IGBT modules. For additional detailed information on the operation of the hybrid gate drivers please see the individual data sheets.

Figure 1: VLA500-01/VLA502-01 Block Diagram



A complete schematic and component selection guide for the BG2A is shown in Figure 2. The board will normally be operated with two input voltage sources. A 5V logic source (+V_L) provides drive for the high speed opto-couplers inside the hybrid gate drivers and pull-up voltage for the fault signal isolation optos OP1 and OP2. A 15V power supply (+V_S) provides power for the gate driver and is connected to the primary side of the hybrid gate driver's built in DC to DC converter at pins 1,2 and 3,4. The +15V source is decoupled with the low impedance electrolytic capacitor C1. In the BG2A circuit a 1000uF capacitor was selected for C1 so that the same capacitor could be used for C1, C2, C3, C5 and C6. In most applications this will be much larger than necessary to support the drivers ripple current. Typical applications will be able to use 100uF or less depending on the load current and the distance from the main 15V supply filter capacitors. The hybrid's built in DC to DC converter provides isolated gate drive power which consists of +16.4V (V_{CC}) at pin 19 and -9V (V_{EE}) at pins 21 and 22. These supplies share a common ground at pin 20. The gate drive power supplies are decoupled using the low impedance electrolytic capacitors C2, C3, C5 and C6. It is very important that these capacitors have low enough impedance and sufficient ripple current capability to provide the required high current gate drive pulses. The 1000uF capacitors used on the BG2A are sized to supply 12A gate pulses at a 20KHz rate. If the application is operating at lower frequency or lower peak current it may be possible to reduce the size of these capacitors. Consult the hybrid gate driver individual data sheets for details on selecting the decoupling capacitors.

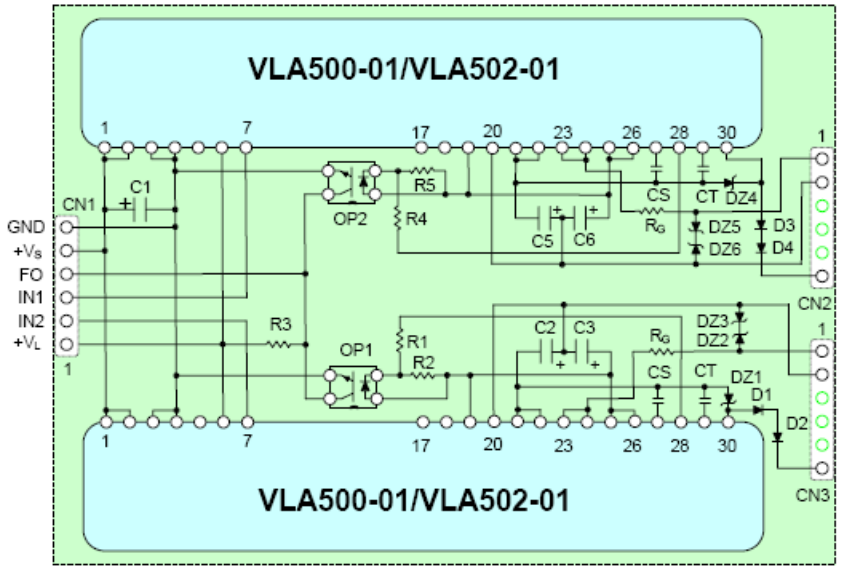
The V_{EE} and V_{CC} supplies are connected to the drivers output stage to produce gate drive at pins 23 and 24. The gate drive current is adjusted by selecting the appropriate series gate resistance (R_G). R_G will normally be adjusted to provide suitable drive for the module being used. For more information see Powerex IGBT module application notes. Protection against gate voltage surges is provided by DZ2, DZ3, DZ5, and DZ6. These zener diodes also help to control short circuit currents by shunting miller current away from the gate.

Short circuit protection is provided by means of desaturation detection. For details on the operation of this circuit consult the VLA500/VLA502 data sheets. The collector voltage of each IGBT is detected through the series connected high voltage blocking diodes D1, D2 and D3, D4. The combined blocking voltage of the series connected diodes must be equal to or greater than the V_{CES} rating of the IGBT. For applications using lower voltage devices it may be possible to use a single detection diode. DZ1 and DZ4 protect the gate driver's detect input (Pin 30) from voltage surges during reverse recovery of the high voltage blocking diodes. The CS and CT capacitors are used to adjust the drivers protection circuit trip time and slow shut-down speed. The driver's default settings are sufficient for many applications and therefore these capacitors can be omitted. For details on the use of CT and CS consult the VLA500/VLA502 data sheets.

If the gate driver's short circuit protection is activated it immediately shuts down the gate drive and pulls pin 28 low to indicate a fault. Current flows from Vcc (pin 19) through the LED in fault isolation opto (OP1, OP2) to pin 28. The transistor in the fault isolation opto turns on and pulls the fault signal line (FO) at pin 4 of CN1 low. This opto isolated signal can now be used by the controller to detect the fault condition.

Interface Circuit Requirements: A typical interface circuit for the BG2A is shown in Figure 3. A single +15V control power supply (+V_S) is connected to pin 5 of CN1 with its ground at pin 6. This supply provides all of the gate drive power for both channels via the hybrid gate drivers' built in DC to DC converters. The current drawn from the 15V supply will vary from less than 200mA to more than 1A depending on the switching frequency and size of IGBT being driven. Consult the hybrid gate driver individual data sheets for details on determining the

Figure 2: BG2A Schematic and Component Selection Guide



Component Selection:

Designation	Typical Value	Description	Example: Mfg./PN
D1,D2,D3,D4	0.5 A, 1000V	V_{CE} detection diode – ultra fast recovery	ON Semi/MUR1100E
DZ2, DZ3, DZ5, DZ6	16V, 1W	Gate Voltage Surge Protection	1N4745
DZ1, DZ4	30V, 1W	Detect input pin surge voltage protection	1N4751
C1, C2, C3. C5, C6	1000 µF, 35V	Power supply filter – Electrolytic, low Impedance	Panasonic EEU-FC1V102
CS	0-1000 pF	Adj. soft shutdown – Multilayer ceramic or film**	EPCOS B37979---------
CT	0-200 pF	Adj. trip time - Multilayer ceramic or film**	EPCOS B37979---------
R1, R4	4.7kΩ, 0.25W	Fault sink current limiting resistor	
R2, R5	3.3kΩ, 0.25W	Fault signal noise suppression resistor	
R3	4.7KΩ, 0.25W	Fault feedback pull-up resistor	
OP1, OP2	NEC PS2501	Opto-coupler for fault signal isolation	NEC/ PS2501
CN1, CN2, CN3	MTA .100"	Input and gate drive connectors*	AMP 641216-6

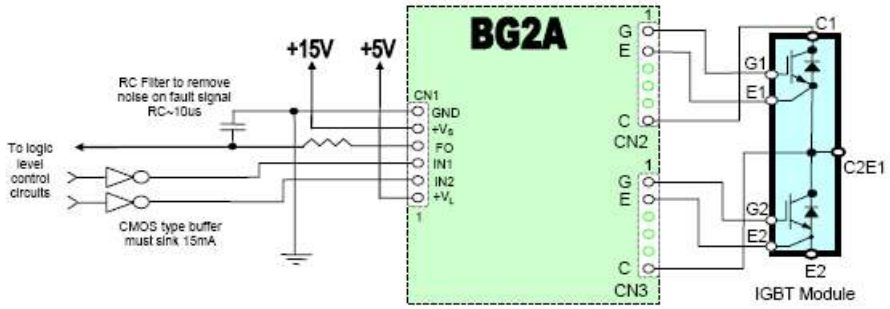
* Remove the three unused pins on CN2 and CN3 to maintain appropriate high voltage spacing.
Recommended mating connector AMP CST-100 Housing P/N 770602-6 with crimp contact 770666-2.
** CS, CT are only required in certain special applications. Please see VLA500/VLA502 application notes for details.

required supply current. A 5V logic supply is connected at pin 1 of CN1 and shares the same common ground at pin 6 of CN1 as the 15V control supply. The 5V supply is directly connected to pin 6 of the hybrid gate driver which is internally connected to the anode of the LED in the high speed opto coupler. The 5V supply is also used to pull the output side of the fault isolation opto couplers high.

The control signal interface is designed for use with standard 5V CMOS logic. The control input signals at pins 2 an 3 of connector CN1 are used to turn the IGBTs on and off. These signals are active low which means that the gate driver output will be high (IGBT on) when they are pulled low. These control pins are connected directly to pin 7 of the hybrid gate driver which is connected internally through a limiting resistor to the cathode of the LED in the high speed opto coupler (see figure 1). When the control signal is pulled low current flows from the 5V logic supply through the LED to turn the gate driver's output on. The control pins must be pulled low with a buffer that is capable of sinking 15mA in order to turn on the high speed opto coupler inside the VLA500/502. A CMOS buffer that actively pulls its output high is recommended for maintaining good common mode noise immunity in the off state. Open collector type drive is not recommended.

The fault signal line on pin 4 of CN1 is active low which means that a fault condition will be indicated by a low level signal. During normal operation pin 4 is pulled high to the +5V supply ($+V_L$) by the 4.7K resistor R3.

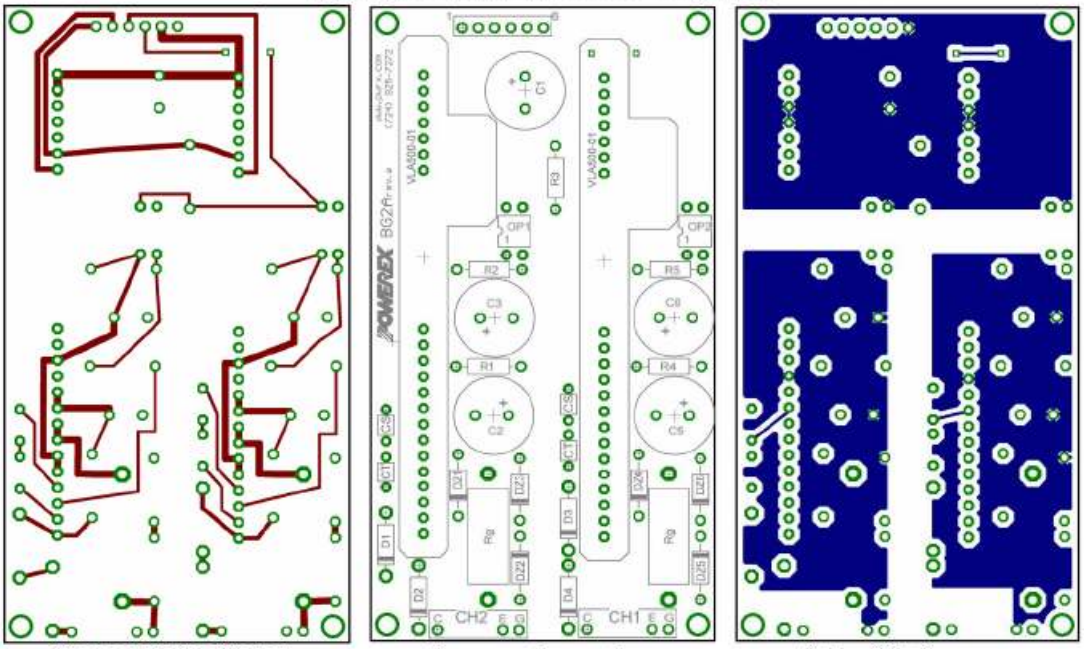
Figure 3: BG2A External Wiring Diagram



If either of the VLA500/502 gate drivers detects a short circuit condition the fault isolation optos (OP1, OP2) turn on and pull pin 4 of CN1 low. When a fault is detected the hybrid gate drivers disable the output and produce a fault signal for a minimum of 1ms. Any signal on the fault line that is significantly shorter than 1ms can not be a legitimate fault so it should be ignored. Therefore, for a robust noise immune design, it is recommended that an RC filter with a time constant of approximately 10us be added between pin 4 and the controller as shown in figure 3.

Printed Circuit Layout: Figure 4 shows the layout of the BG2A two channel gate driver board. The compact 2" x 4" circuit board with only 24 components clearly demonstrates the advantage of using the VLA500/502 hybrid gate drivers. One important feature is the use of three ground plane islands for the regions of the PCB having high voltage differences. Two of the islands are tied to the emitter/circuit common (Pin 20) of each output channel. The third island is connected to logic interface common at pin 6 of CN1. This layout prevents undesirable coupling of noise between the control side and the gate drive channels.

Figure 4: BG2A Printed Circuit Board Layout



Component Side Copper | Component Legend | Solder Side Copper

APPENDIX E

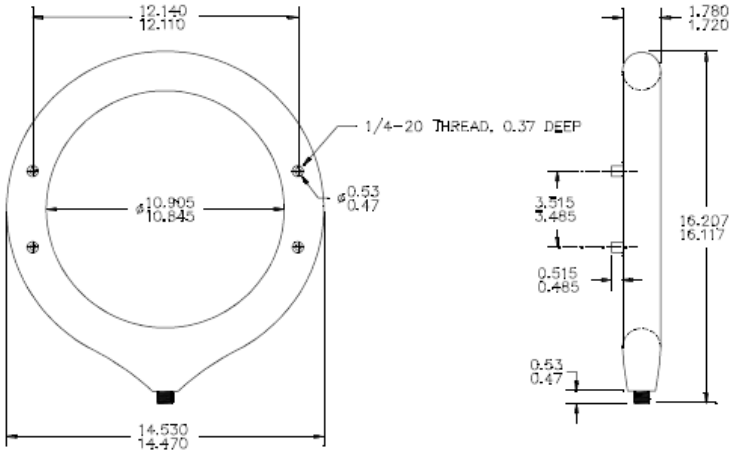
PEARSON CURRENT MONITOR

PEARSON ELECTRONICS, INC.

PEARSON™ CURRENT MONITOR MODEL 1010

Sensitivity	0.1 Volt/Ampere +1/-0%
Output resistance	50 Ohm
Maximum peak current	5,000 Amperes
Maximum rms current	120 Amperes
Droop rate	0.25 %/microsecond
Useable rise time	50 nanoseconds
Current time product	0.7 Ampere-second*
Low frequency 3dB cut-off	400 Hz (approximate)
High frequency 3dB cut-off	7 MHz (approximate)
I/f figure	4.4 peak Amperes/Hz
Output connector	UHF (SO-239)
Shielding	Double
Operating temperature	0 to 65 ºC
Weight	12.5 pounds

* Maximum current-time product can be obtained by using core-reset bias as described in the *Application Notes*. 0.25 Ampere-second is typical without bias.



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