Conduction and trapping mechanisms in SiO_2 films grown near room temperature by multipolar electron cyclotron resonance plasma enhanced chemical vapor deposition

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Silicon dioxide layers with stoichiometric composition and excellent electrical properties were deposited at a substrate temperature of 60 °C with an electron cyclotron resonance plasma source. This work is focused on determining the electrical conduction and trapping mechanisms of the deposited films. From the temperature dependence of current density–electric field characteristics, Fowler–Nordheim tunneling was found to be the dominant conduction mechanism in SiO_2 films obtained with low silane flow and at low pressure. For layers deposited with higher silane flows and higher pressures, the current at low biases is highly dependent on temperature. Positive charge was measured at the Si/SiO_2 interface during low electric stress, while electrons were trapped at the interface for electric fields higher than 7 MV/cm. Constant current stress measurements confirmed that low silane flow and low total pressure are suitable deposition conditions for obtaining a film comparable to thermally grown oxide from the reliability point of view. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1736645]

I. INTRODUCTION

The demand for high-quality gate dielectrics manufactured at low-temperature for semiconductor devices is increasing. An example of such devices is thin film transistors (TFTs) fabricated with polysilicon or large grain single crystalline silicon.[1] These low temperature devices can be used for circuit integration on large area substrates such as glass, in high density displays and imagers. For these applications, the TFTs require not only high mobility silicon but also high quality gate dielectrics with good interface and bulk properties. It is known, however, that a low deposition temperature degrades the films properties.

Electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR PECVD) has proved to be successful in obtaining silicon oxide (SiO_2) layers at room temperature, with high breakdown strength and good interface properties, similar to those of thermal oxide grown at 1000 °C.[2] However, the fixed oxide charge and interface trap density are larger in the case of plasma deposited dielectrics, due to plasma damage and undesired hydrogen bonds.[3]

In order to become suitable as gate dielectrics for thin film transistors, the low temperature SiO_2 layers have to exhibit not only high breakdown field and low interface trap density, but also high oxide integrity, resistance to electrical stress, and low trapping probability. Reliability problems and electrical transport for SiO_2 films obtained by ECR PECVD at room temperature have not got much attention until now. Only one paper dealing with the dielectric behavior under high electric stresses of ECR PECVD layers deposited at 300 °C has been published.[4]

We have chosen for deposition a distinct ECR discharge configuration, called *multipolar* ECR.[5] This technique has been shown to reduce the hydrogen contamination down to 0.2 at. % and to improve the dielectric strength of the obtained films.[6] Multipolar ECR PECVD has certain advantages such as the magnetic field in parallel to the substrate, which minimizes the plasma damage, a tunable microwave cavity, and a quartz dome that reduces the metal contamination. Electrical properties were not explored in detail for *multipolar* ECR PECVD silicon oxide layers, despite their excellent chemical composition.

Previous work[7] has shown that multipolar ECR PECVD can deliver high-quality SiO_2 with breakdown field of 10 MV/cm, resistivity of 10^{16} Ω cm and oxide charge in the order of 10^{11} cm^{-2} without substrate heating at low SiH_4 flow rate and low deposition pressure.

The purpose of this article is to determine the conduction mechanism, the interface stability to electrical stress, and the reliability of multipolar ECR PECVD SiO_2, for different SiH_4 flow rates and deposition pressures. In Sec. III A the main conduction mechanism is established by studying the temperature dependence of current–voltage ($I-V$) characteristics, first for superior layers obtained at low pressure and low SiH_4 flow and then for leaky dielectrics obtained at high pressure and high SiH_4 flow. For these layers, a model describing the electronic transport is proposed. Section III B deals with the trap charging phenomena during the electric stress by measuring capacitance–voltage ($C-V$) characteristics of $Al/SiO_2/Si$ capacitors for different level of stress and various periods of time. The final Sec. III C describes the influence of the deposition conditions on the charge-to-breakdown values, confirming the high-quality of SiO_2

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layers obtained at low SiH_4 flow rate and low deposition pressure.

II. EXPERIMENT

The deposition system consisting of a microwave plasma disk reactor (MPDR-300) comparable with the one described by Asmussen[5] has been described elsewhere.[8] Electronic pure nitrous oxide (N_2O) and 2% silane (SiH_4) diluted in helium were used as the gas precursors. The base pressure in the reaction chamber was 3×10^{-6} Torr.

The SiO_2 films were deposited near room temperature, without external heating. Due to plasma heating, the temperature of the substrate measured by a thermocouple bonded inside the sample holder reached a maximum of 60 °C. During the experiments, the flow rate of N_2O was maintained at a constant value of 20 sccm and the microwave power was set to 400 W. The total pressure was in the range of 4–20 mTorr and the flow rate of 2% SiH_4-in-helium varied between 5 and 15 sccm. TFTs with large grain silicon[1] require thinner gate dielectric than amorphous TFTs (a few hundred nanometers). Therefore, the thickness of the deposited silicon oxide films was chosen to be around 50 nm. Thinner films with similar electrical properties can also be deposited with this technique.[9] For comparison purposes, a reference thermally grown SiO_2 layer of 25 nm was grown on a silicon wafer with dry O_2, at 950 °C.

3 in. (100)-oriented *n*-type standard silicon wafers obtained by the Czochralski method, doped with phosphorous and with a resistivity of 1–10 Ω cm were used for the experiments. The wafer preparation included a standard cleaning procedure[8] followed by a 1% HF etch in order to remove the native oxide. Postdeposition anneal (PDA) in a wet nitrogen (N_2) ambient (N_2 bubbled through de-ionized water at room temperature) has been performed for 60 min, at a temperature of 500 °C, for all the films. The effect of the PDA upon the film electric properties was studied subsequently and presented in another publication;[10] it has been found that the PDA had no observable improvement on electrical properties.

Metal–oxide–semiconductor (MOS) capacitors were manufactured by sputtering a 1-μm-thick aluminum (Al) layer on the front and the backside of the wafer. By means of lithography and etching, 0.1 and 0.01 mm^2 Al-gate capacitors were formed. All samples were subjected to postmetallization annealing (PMA) for 5 min, at 400 °C in wet N_2 ambient. PMA has little or no influence upon the current behavior, improving only the interface trap density.[10]

A Hewlett-Packard 4156 parameter analyzer was used for $I-V$ and constant current stress (CCS) measurements. Positive voltages were applied on the metal gate. The substrate temperature was controlled by a Temptronic thermochuck. High frequency (10 kHz) and quasistatic $C-V$ measurements were carried out before and after electrical stress with a Hewlett-Packard 4275A multifrequency meter and a Hewlett-Packard 4140B pA meter at a bias sweep rate of 0.1 V/s.

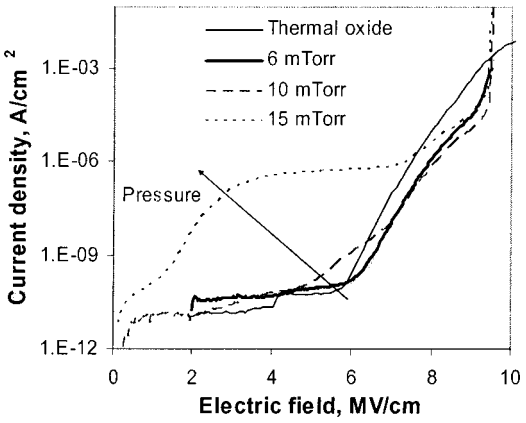

FIG. 1. Current density vs electric field for ECR films deposited with 20 sccm N_2O and 5 sccm SiH_4 at 400 W and various pressures (6, 10, and 15 mTorr) and for thermally grown oxide.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The SiO_2 films deposited with the multipolar ECR plasma source at room temperature exhibited high electrical quality with breakdown fields of 10 MV/cm, resistivities of 10^{16} Ω cm, net oxide charges in the order of 10^{11} cm^{-2} and interface trap densities of 10^{10} eV^{-1} cm^{-2}.[7] In order to optimize further the deposition parameters and to determine the electrical integrity of these layers, we investigated their conduction mechanism and charge-to-breakdown versus the pressure and the SiH_4 flow.

A. Conduction mechanism

1. Experimental I–V characteristics

It can be observed in Figs. 1 and 2 that the $I-V$ characteristics of the deposited SiO_2 layers are similar with that of thermally grown oxide only if the total pressure and silane flow are lower than 6 mTorr and 7.5 sccm, respectively. It also appears that for higher deposition pressures and flows the $I-V$ curves have a different shape and the leakage current increases substantially, despite the constant breakdown

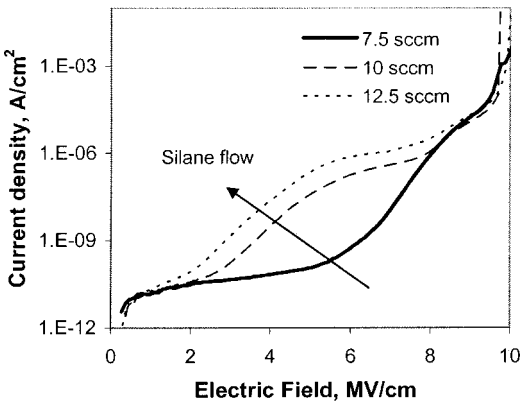

FIG. 2. Current density vs electric field for films deposited with 20 sccm N_2O, at 400 W, 12 mTorr, and various SiH_4/He flows (7.5, 10, and 12.5 sccm).

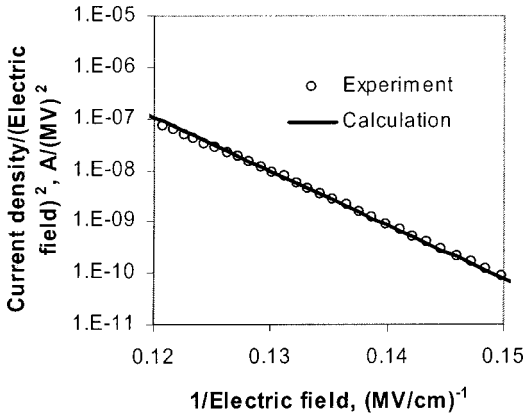

FIG. 3. Fowler–Nordheim plot for a film deposited with 5 sccm SiH_4/He and 20 sccm N_2O at 400 W and 4 mTorr, $q\phi=3$ eV.

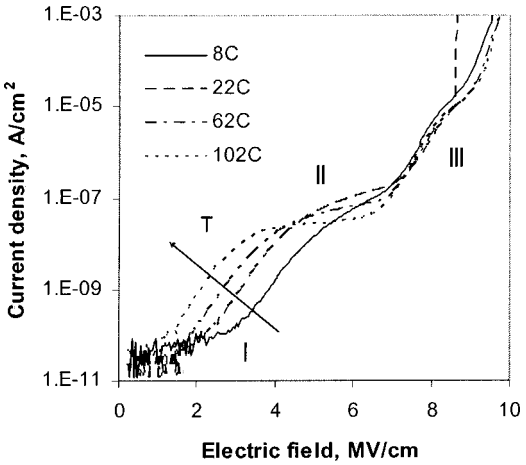

FIG. 4. Current density vs electric field for a film deposited with 12.5 sccm SiH_4/He and 20 sccm N_2O at 400 W and 12 mTorr measured at various temperatures.

field. This effect was explained in a previous article[7] as the result of composition deviation from the stoichiometric SiO_2 due to (1) hydrogen contamination in case of high pressure and (2) silicon excess in case of high silane flow rate.

Because all the inferior dielectrics exhibited $I-V$ curves with similar shape, but different slopes and magnitude, we decided to investigate separately the mechanisms of electrical transport in the superior and inferior layers.

2. Superior oxides conduction mechanism

In order to determine the conduction mechanism, the dependency of current density–electric field ($J-E$) curves on temperature for the high-quality samples formed at low pressures (4 and 6 mTorr) was studied by modifying the wafer temperature from 8 to 102 °C. There is negligible change in the $J-E$ curves with varying the temperature, the shape of the curves is similar with the one presented in Fig. 1 for the film obtained at 6 mTorr. The current measured at electric fields higher than 6 MV/cm is practically independent of the chuck temperature. This indicates that the electron transport through the oxide layer obeys the Fowler–Nordheim tunneling,[11] which is given by the expression

$$J_{\mathrm{FN}}=[q^2m_0/(8\pi h\phi m_e)] \times E^2\exp[-8\pi(2m_e q\phi^3)^{1/2}/(3hE)], \quad (1)$$

where E is the electric field, q is the electron charge, h is Planck's constant, m_0 is the free electron mass, m_e ($=0.49\times m_0$)[12] the effective mass of an electron in silicon, and ϕ is the barrier height for electrons in silicon. In order to confirm this hypothesis, the Fowler–Nordheim plot [$\ln(J/E^2)$ vs E^{-1}] is shown in Fig. 3. As one can see, the experimental data could be fitted with a straight line and from the slope, the energy barrier was extracted: $\phi=3$ V. This value is comparable to the barrier height estimated for thermally grown oxide.[13] From these results we can conclude that the dominant conduction mechanism in the high-quality layers obtained at low pressure and low silane flow is the Fowler–Nordheim tunneling.

3. Nonstoichiometric oxides conduction mechanism

a. Temperature influence. Next, the behavior of an oxide deposited at a higher SiH_4 flow with higher leakage current was studied at different temperatures (Fig. 4) in order to determine the main conduction mechanism. Three different regions can be distinguished in the plot. In region I, at low biases the current depends highly on temperature, while in region III, at electric fields higher than 8 MV/cm, no dependency on temperature is detected.

In region II, the current increases very slowly with the applied voltage. This ''quasisaturation'' of the current is caused by charge trapping in the dielectric. As a result, an internal electric field, opposed to the external electric field is produced and the increase of the carrier flow with increasing the external field is suppressed.[14,15]

The noise observed for low currents and biases in Fig. 4 is caused by the heating element which controls the wafer temperature. Apparently, the measurement of very low currents is influenced by the functioning of the Temptronic thermochuck. The noise was not observed for measurements performed with the heater turned off.

b. Model proposal. To verify the trap-charging hypothesis, we measured the $I-V$ characteristics until 8.5 MV/cm, twice without delay (Fig. 5). The electric field is reduced due to charge trapping during the first sweep and consequently the current is lower for the second sweep in regions I and II. Because the silicon wafer is n-doped and positive gate voltage is applied, we assume that substrate injection of electrons is mainly responsible for the conduction process.[16] Consequently, the charge stored in the oxide is also negative and this impedes the subsequent electron movement from the silicon toward the gate. It cannot be excluded that trapped holes or fixed positive charge also exist in the oxide provided that its density is much lower than that of negative charge.

In region I, before saturation, the current for the first and second measurement can both be fitted with a straight line if represented in the Pool–Frenkel representation. The main conduction mechanism in these layers at low biases is most

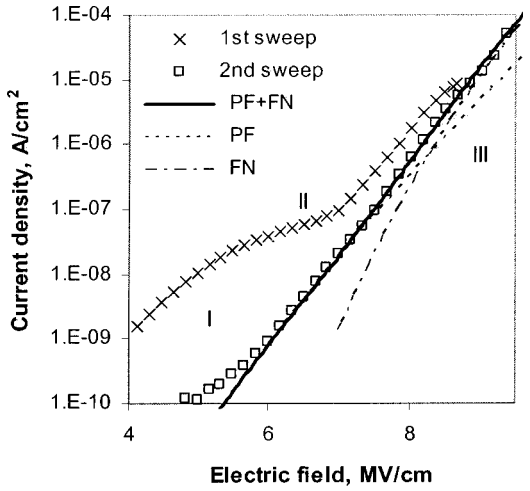

FIG. 5. Two consecutive measurements of current density vs electric field for the same capacitor made with a film deposited with 10 sccm SiH_4/He and 20 sccm N_2O at 400 W and 12 mTorr; theoretical Poole–Frenkel (PF), Fowler–Nordheim (FN), and the sum of PF and FN currents.

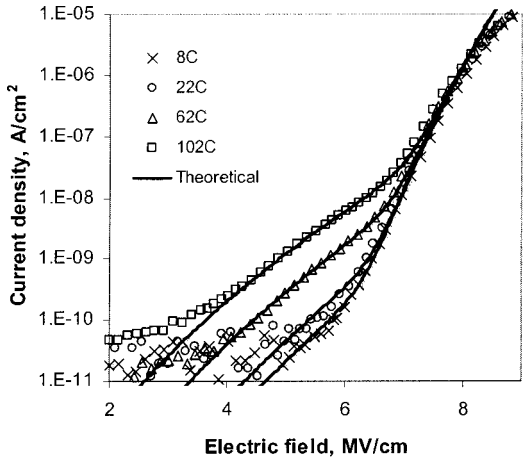

FIG. 6. Current density vs electric field for a film deposited with 7.5 sccm SiH_4/He and 20 sccm N_2O at 400 W and 12 mTorr measured at 8, 22, 62, and 102 °C; theoretical current as a sum of Poole–Frenkel current and Fowler–Nordheim current, $q\phi_T = 0.87$ eV, $q\phi = 3$ eV.

probably the Poole–Frenkel effect,[17] expressed by

$$J_{\mathrm{PF}} = CE \exp[-q\phi_T/(kT)] \times \exp[E^{1/2}\sqrt{q^3/(\pi\varepsilon_0\varepsilon_R)}/(rkT)], \quad (2)$$

where ϕ_T denotes the barrier height of the trap, k is the Boltzmann's constant, ε_R is the dielectric constant of the SiO_2, and C and r are constants. Since the Poole–Frenkel effect is the *thermal emission* of charge carriers from traps,[18] the high dependence of current on temperature in region I is, hence, explained. Also it is known that the probability of the Poole–Frenkel emission is increased when a high density of shallow traps exists in the bandgap, which was confirmed by the remeasurement of the $I-V$ characteristics.

Because the first measurement is transient, we concentrated upon determining the conduction mechanism for the second sweep. As it can be seen in Fig. 5, the shoulder in region II disappears in the second $I-V$ measurement, thus regions I and II become one region, where the current is still dependent on temperature (Fig. 6). In region III, no significant modification appears between the first and the second $I-V$ curve (Fig. 5), and the temperature has no significant effect upon the current even for the second measurement (Fig. 6). Due to this dual temperature dependence, we propose to write the current measured in the second sweep as a sum of the Poole–Frenkel current (dominant at low voltages) and Fowler–Nordheim tunneling current (dominant at high biases)

$$J = J_{\mathrm{PF}} + J_{\mathrm{FN}}. \quad (3)$$

As it is shown in Fig. 5, the theoretical expression fitted very well the measured current. The band diagram showing the conduction mechanisms detected in the MOS structures is presented in Fig. 7.

c. Model verification. In order to verify this model, we measured the second sweep current for four different temperatures: 8, 22, 62, and 102 °C and compared them with the calculated current, written as in Eq. (3) for these temperatures. In Fig. 6 a good fitting for all the temperatures was obtained for a trap energy ($q\phi_T$) of 0.87 eV and a barrier height energy ($q\phi$) of 3 eV (see also Fig. 7 for graphic representation of ϕ_T and ϕ).

The same conduction processes were found in all the films deposited at high pressure and high silane flow, with different ϕ_T and ϕ. Moreover, the leakage current and the electric field shift increased with both silane flow and total pressure (Figs. 1 and 2), indicating an increase in trap density.[19] In the case of oxides deposited with high silane flow, it is believed that the traps are a result of silicon dangling bonds.[20] For high deposition pressure, the efficiency of energy transfer from the plasma toward the depositing film is lower.[21] Consequently, there is insufficient energy for particles to migrate on the film surface, for hydrogen desorption and for creation of strong chemical bonds.[6] Therefore, the density of weak bonds, especially hydrogen bonds increases, as measured in the infrared spectra[8] and more traps participate in the low-field conduction process.

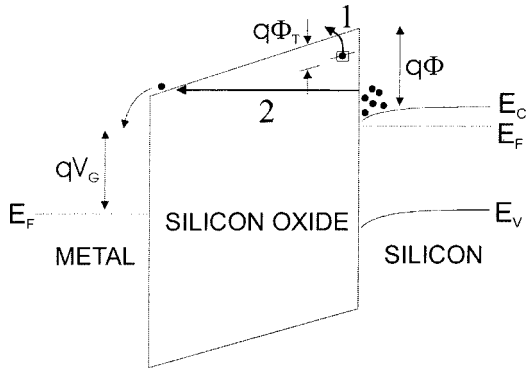

FIG. 7. Simplified energy diagram for an Al/SiO_2/Si structure with leaky oxide. For low biases the Poole–Frenkel effect (1) is dominant, while at high V_G, Fowler–Nordheim tunneling (2) appears.

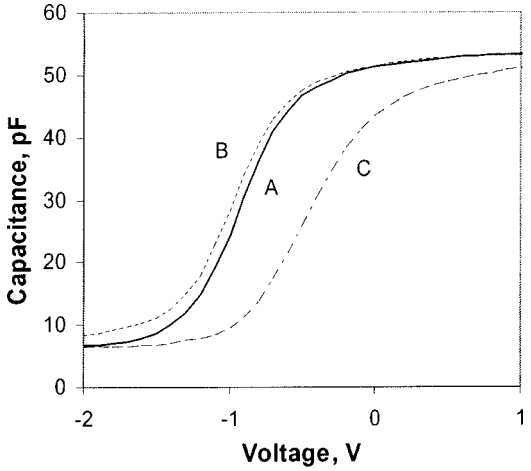

FIG. 8. High frequency $C-V$ characteristics for a film deposited with 7.5 sccm SiH_4/He and 20 sccm N_2O, at 400 W and 12 mTorr: (a) before bias-stress, (b) after a bias-stress of 6 MV/cm for 36 s, and (c) after a bias-stress 8 MV/cm for 36 s.

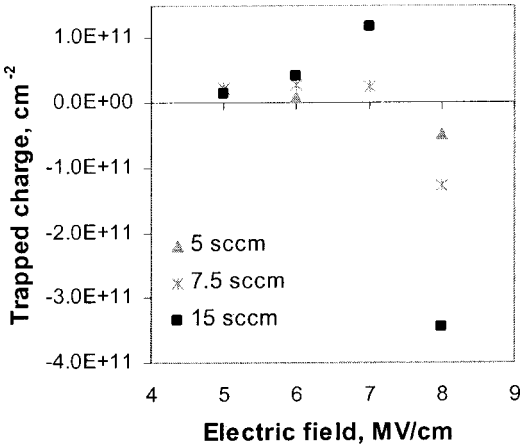

FIG. 9. Variation in trapped charge vs electric field stress (during 36 s) for the films deposited with 20 sccm N_2O at 400 W, 12 mTorr, and various SiH_4/He flows (5, 7.5, and 15 sccm).

For either high total pressure or high silane flow, an increase in SiH_4 partial pressure occurs, thus also the deposition rate is increased. The higher the growth rate, the smaller the probability that strong chemical bonds are formed and that hydrogen is desorbed, hence inferior dielectrics will be produced.

In summary, it has been observed that ECR plasma enhanced deposition at pressures lower than 10 mTorr can provide silicon oxide layers with a Fowler–Nordheim tunneling conduction mechanism, as in the case of thermally grown oxide. With increasing either the pressure, or the silane flow, the conduction mechanism in the layer is modified, becoming the Poole–Frenkel emission for low electric fields.

B. Charge trapping during electric stress

For a better understanding of trapping phenomena at the Si/SiO_2 interface, electric fields of 5, 6, 7, and 8 MV/cm were applied to MOS capacitors of 0.1 mm^2 in condition of substrate accumulation. The bias was applied for three periods of time of 36, 54, and 72 s and $C-V$ measurements were performed after each stress period. Figure 8 shows the high-frequency $C-V$ curves before and after stressing the oxide with 6 and 8 MV/cm for 36 s.

As it can be observed in Fig. 8, the $C-V$ curve shifts toward negative voltages during a low electric field stress, indicating an increase in positive charge. The curve shifts towards positive voltages for fields higher than 8 MV/cm due to an increase in negative charge trapped at the interface. The same effect was registered for all ECR deposited layers, dense or porous, and also for the reference layer, a thermally grown SiO_2 layer. Only the magnitude of the shift in the flatband voltage varied with the deposition parameters, as it can be observed in Fig. 9, where the trapped charge, extracted from the flatband voltage, is presented for different deposition conditions. We can identify the positive bias of 8 MV/cm as the onset of electron trap generation at the interface.

The differences in net oxide charge were presented also versus the stress time in Fig. 10 for layers obtained with different silane flow. We notice that the positive charge density created by applying an electric field of 6 MV/cm is much smaller than the negative charge trapped during an 8 MV/cm electric stress. With increasing the silane flow, from both Figs. 9 and 10, it can be observed that the charge trapped during stress increases, which is an indication that the layers deposited at higher silane flow possess more dangling or weak bonds. A similar behavior was observed for layers obtained at higher pressure.

The sign of the trapping charge ("+" for low biases and "−" for high biases) could not be correlated with the conduction mechanism; all oxides began to trap electrons at the interface at 8 MV/cm. However, for poorer dielectrics the charge value and the ratio between the charge and interface trap density (Table I) were higher. The oxide fabricated at 4 mTorr and 5 sccm SiH_4 exhibited an increase of 7×10^9 cm^{-2} in positive charge during the 36 s stress of 6 MV/cm, and trapped 4×10^{10} cm^{-2} negative charge in case of an electric field of 8 MV/cm. These values are comparable with the ones for thermally grown oxide.

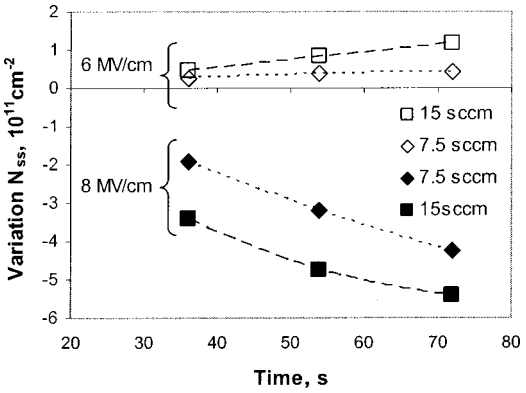

FIG. 10. Variation in trapped charge vs stress time for two films deposited with 20 sccm N_2O at 400 W, 12 mTorr, and various SiH_4/He flows (7.5 and 15 sccm).

TABLE I. Ratio between generated oxide charge and interface trap density after a positive electric stress of 6 MV/cm was applied on the gate of MOS capacitors with various oxide layers.

N_{ss}/D_{it}	36 s	54 s	72 s
Thermal oxide	1.58	2.26	0.75
5 sccm SiH_4/He 4 mTorr	0.35	0.6	0.88
5 sccm SiH_4/He 10 mTorr	1.62	1.66	1.87
5 sccm SiH_4/He 15 mTorr	*10.23*	*10.87*	*9.06*
7.5 sccm SiH_4/He 12 mTorr	0.57	1.12	1.03
15 sccm SiH_4/He 12 mTorr	*29.09*	*28.48*	*20.31*

The changes in flatband voltage cannot be explained in terms of mobile ion drift, because the mobile ion density, measured by bias temperature stress (BTS) has very low values, lower than 10^9 cm^{-2}, thus we can consider the oxide free of mobile ions.

Experiments performed with thermally grown oxide by DiMaria[22] have shown the same trend of capturing holes for low injected charge and trapping electrons at the interface for high injected charge. However, in the case of the referred experiment, the applied fields were higher than 8 MV/cm and the current increases during electric stress, not decreases, as it can be seen for our films, in Fig. 11. The phenomenon was explained by DiMaria in terms of trapped holes, which were created by hot electrons that arrive at the aluminum gate by the Fowler–Nordheim tunneling. However, in our case the Fowler–Nordheim tunneling is rather small at 5–6 MV/cm for superior oxides.

The shoulder in the $J-E$ curves presented in the previous section indicated that electrons are trapped in the dielectric bulk even at low electric fields of 5 MV/cm in the inferior oxides. Furthermore, the $I-t$ curves measured during stressing superior oxides and presented in Fig. 11, indicate also that negative charge is trapped in the oxide, decreasing the total current. Nevertheless, the charge present at the interface calculated from $C-V$ characteristics is positive for low biases and negative only for high biases of 8 MV/cm. Other experiments with plasma deposited SiO_2 layers[23,24] have shown the same trapping characteristics during electric stress, i.e., positive charge shown by the $C-V$ characteristics and negative charge revealed by the current behavior. Because the flatband voltage is sensitive only to the charge trapped close to the Si/SiO_2 interface, the electrons can be trapped in the bulk or at the metal/SiO_2 interface, as shown in experiments performed with nonstoichiometric layers,[4,24] and their charge is not reflected in the $C-V$ characteristics, appearing only in the $I-V$ characteristics. For low electric fields the positive charge situated at the interface exceeds the charge of electrons trapped at the interface. With increasing the electric field, however, more electron traps are created and filled at the Si/SiO_2 interface and the $C-V$ curves shift toward positive voltage.

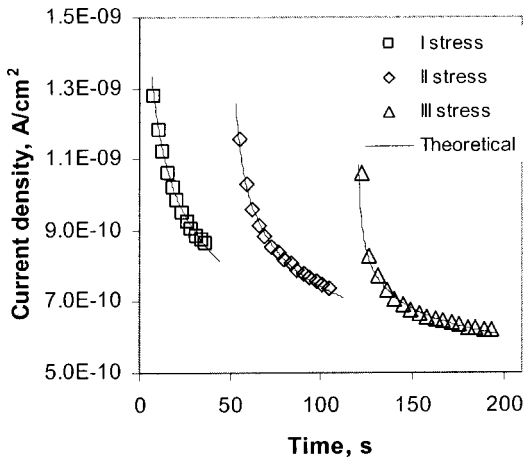

FIG. 11. Current density vs stress time for a film deposited with 5 sccm SiH_4/He, 20 sccm N_2O at 400 W and 4 mTorr, while stressed by 6 MV/cm.

By applying a negative bias to the metal gate, we observed a larger shift in the flatband voltage toward negative voltages than in the case of low positive bias stress. This phenomenon is already known in literature,[25] for lower biases (2–4 MV/cm) and higher temperatures (200 °C), from comparing the damage caused by negative bias temperature stress (NBTS) with the effects of positive bias temperature stress (PBTS). The degradation process of thermally grown SiO_2 was described by a chemical reaction proposed by Jeppson and Svensson[25] and applied also in the case of radio frequency-PECVD layers,[26] which takes place with destruction of silicon-hydrogen bonds and removal of electrons, as in

$$\text{Si–H} + \text{Si-O} \rightarrow \text{Si–OH} + \text{Si}^+ + \text{e}^-. \quad (4)$$

This degradation process can be the source of positive charge that appears in our layers at low biases. Furthermore, the destruction of Si–H bonds can explain the severe degradation in case of dielectrics obtained at high pressure and with high silane flow. The presence of high concentration of Si–H bonds in the inferior oxides, may lead to increased flux of electrons towards the metal gate, raising the value of current with the applied voltage as it can be seen in Figs. 1 and 2.

Furthermore, we calculated the interface trap density (D_{it}) by Castagne method[27] after a stress of 6 MV/cm, and we presented the ratio between the additional oxide charge (N_{ss}) and D_{it} in Table I after applying an electric stress for different periods of time. It can be observed that N_{ss}/D_{it} ratios exhibit values around unity for the dense oxides and the thermally grown oxide, and 10–30 times higher for the porous and nonstoichiometric layers deposited with high silane flow and at high pressure. The increased positive charge confirms the destruction of hydrogen bonds which are present in high concentrations in these layers, and creation of positive silicon ions.

The current passing through the oxide decreases during the stress, as shown in Fig. 11. The current density recovers between the measurements (Fig. 11), indicating that some of the trapped electrons were detrapped during the subsequent

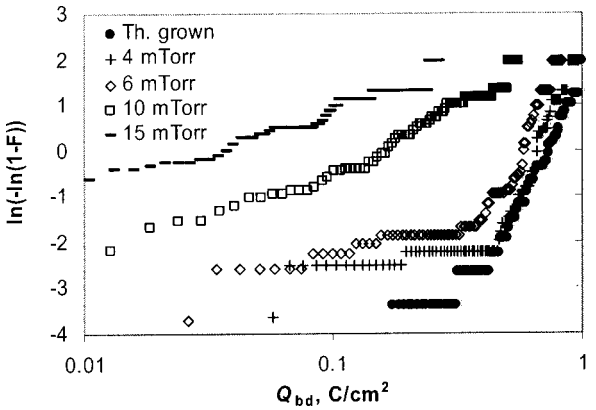

FIG. 12. Weibull plot for films deposited with 5 sccm SiH_4/He and 20 sccm N_2O at 400 W and various pressures (4, 6, 10, and 15 mTorr) and for a thermally grown oxide.

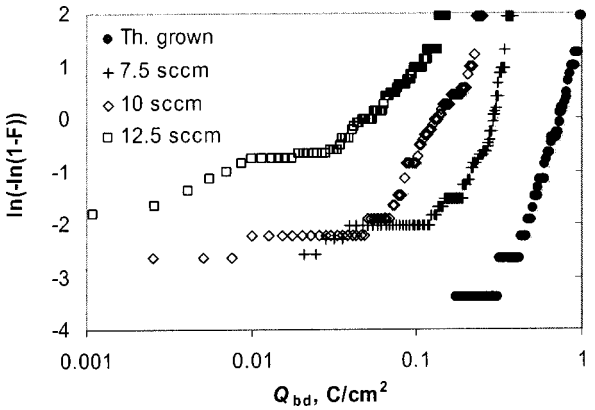

FIG. 13. Weibull plot for films deposited with 20 sccm N_2O, at 400 W and 12 mTorr and various SiH_4/He flow (7.5, 10 and 12.5 sccm) and for a thermally grown oxide.

$C-V$ measurement. The recovery of the current was also dependent on deposition conditions. For inferior dielectrics obtained at high silane flow or high pressure, the traps were deeper and the current at the beginning of the second stress had values similar to the ones measured at the end of the first stress.

The transient current is well described by a power-law dependence on time similar to the one predicted by the trap-assisted tunneling model[28]

$$J = J_0 t^a, \quad a < 0, \tag{5}$$

where a was found to take values between -1 and -0.1. Apparently, a saturation of the trapped charges appears in time and only a higher field can induce more defects in the dielectric.

C. Oxide integrity

For further understanding of the oxide integrity in case of strong electric stress, CCS measurements were performed. A constant current of 5×10^{-3} A/cm^2 was forced through the oxide by applying positive voltage on the gate. Electrons were injected from the substrate. In Fig. 12, the charge-to-breakdown distributions (Weibull plot)[29] of ECR oxides deposited at different pressure and thermally grown oxide are presented. Each curve is the result of 50 measurements, carried out on Al-gate capacitors with an area of 0.01 mm^2.

The films deposited at lower pressure (4 and 6 mTorr) have high values for the charge-to-breakdown (Q_{50} $\sim$0.7 C/cm^2).[30] The Weibull plot for the oxide deposited at 4 mTorr is similar with the one for the 25 nm reference SiO_2 film grown at 1000 °C.

On the contrary, the layers deposited at higher pressure feature a smaller charge-to-breakdown and a larger distribution of extrinsic breakdowns. This indicates a higher density of traps in the bulk of the dielectrics deposited at higher pressure. It is confirmed once again that multipolar ECR PECVD is an excellent deposition system for very low pressures.

The effect of SiH_4 flow rate upon the oxide reliability was studied next (Fig. 13). Low values for the charge-to-breakdown and large distributions of defect-related breakdowns can be observed for the films deposited with high SiH_4 flow, probably due to an increased number of silicon unsaturated bonds.

While stressing the dielectrics with constant current, an increase in the required voltage was measured, due to charge trapping and the appearance of an internal electric field. From the voltage variation, the bulk trap density was calculated (after Ref. 19) to be 10^{17} cm^{-3}. The experiments presented in this section demonstrate that oxides with good reliability can be deposited at near room temperature for optimal conditions.

IV. CONCLUSIONS

We have identified the main conduction mechanisms in the ECR PECVD SiO_2. For the films obtained at lower pressure and lower silane flow, the conduction mechanism detected was Fowler–Nordheim tunneling. For films deposited at higher flows or higher total pressures, the conduction mechanism is trap related for low applied biases. The leakage current increases with increasing these two deposition parameters, indicating a higher trap density. The $I-V$ characteristics are transient, the current after stressing can be written as a sum of Poole–Frenkel and Fowler–Nordheim current, for various temperatures.

Electrons were trapped in the oxide bulk during electric stress, while positive and negative charge was measured to be present at the interface, depending on the electric field. The oxide degradation process, which is related to the trap density, was also influenced by deposition conditions.

The constant current stress measurements confirmed that decreasing the silane flow and pressure can improve the oxide integrity. The best films have charge-to-breakdown values comparable to the ones for thermally grown oxide.

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