Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs

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***Abstract*—Silicon nanowire transistors with Schottky-barrier contacts exhibit both n-type and p-type characteristics under different bias conditions. Polarity controllability of silicon nanowire transistors has been further demonstrated by using an additional polarity gate. The device can be configured as n-type or p-type by controlling the polarity gate voltage. This paper extends this approach by using three independent gates and shows its interest to implement dual-threshold-voltage configurable circuits. Polarity and threshold voltage of uncommitted devices are determined by applying different bias patterns to the three gates. Uncommitted logic gates can thus be configured to implement different logic functions, targeting either high-performance or low-leakage applications. Dual-threshold-voltage design is thereby achievable through the use of a wiring scheme on an uncommitted pattern. With the polarity controllability of the three-independent-gate device, a range of logic functions is also obtained by replacing V_{DD} and GND by complementary input signals. Synthesis results of ISCAS'85 and VTR sequential benchmark circuits with these devices show, before place and route, comparable performance and 51% reduction of leakage power consumption compared to 22-nm low-standby-power FinFET technology.**

***Index Terms*—Ambipolar, configurable, dual-threshold-voltage, silicon nanowire.**

I. INTRODUCTION

LEAKAGE power consumption has become an important issue in circuit design with around 30% to 50% of the current *S*ystem-*O*n-*C*hip (SOC) power consumption [1]. In CMOS technology, multi-threshold-voltage (multi-V_t) design is widely used to reduce the overall leakage power consumption of circuits [2]. Low-V_t devices are used in the critical paths to meet timing constraints, while high-V_t devices with low leakage are used in slack paths. However, the implementation of multi-V_t circuits requires extra technological steps to build devices with different threshold voltages, which affect the layout regularity and increase the process costs compared to single-V_t design [3]. Adaptive body biasing is another popular technique to mitigate the increasing leakage power consumption, but separate body biasing for tuning threshold voltage of each transistor is hard to achieve due to the area overhead of additional circuits and routing resources [4].

In order to achieve better electrostatic control and reduce short channel effects, FinFETs have been successfully used for the 22-nm technology node [5], [6]. Leakage in FinFETs is significantly reduced as compared to planar devices. To achieve an even better electrostatic control, *Si*licon *N*ano*W*ire *FETs* (SiNWFETs) with gate-all-around control have shown to be a natural extension of FinFETs [7]. Furthermore, the use of metal contacts in the source and drain regions creates Schottky barriers that can be electrically trimmed to take advantage of the inherent ambipolar behavior, i.e., the simultaneous n-type and p-type characteristics.

This ambipolar phenomenon is directly exploited within vertically-stacked *D*ouble-*G*ate (DG) SiNWFET [8]. By using a double-independent-gate structure, the polarity of the device (i.e., type of carriers) can be selected electrically. Ambipolar DG SiNWFETs are desirable for the development of new logic architectures, which are intrinsically not implementable with CMOS in a compact form [9]. Moreover, their leakage current can be further reduced by efficiently controlling Schottky barriers [10].

In this paper, we present the vertically-stacked *T*hree-*I*ndependent-*G*ate (TIG) SiNWFET. A preliminary version of this work has been presented in [11]. The proposed TIG SiNWFET exploits and controls its ambipolar behavior to enable a dynamic control of the device polarity, as well as a tuning of its threshold voltage. Dual-V_t configurable circuits are achievable by applying different connection schemes to uncommitted devices.

Due to the absence of D-flip-flop, the early work [11] focused on combinational logic circuits. In this paper, we give more information on the fabrication technology of TIG SiNWFET and its performance estimated by TCAD simulation at 22-nm technology. The operation modes of TIG SiNWFET under different bias conditions are presented in detail. Based on these configurations, logic gates are mapped onto an uncommitted pattern towards high-performance and low-leakage applications. With the flexibility of TIG SiNWFET, we also propose an unconventional way to implement a range of logic functions by replacing V_{DD} and GND with complementary input signals. Along with a compact true-single-phase-clock D-flip-flop, the new set of functions with TIG SiNWFETs are able to benchmark both combinational and sequential circuits. Synthesis of benchmark circuits onto TIG SiNWFETs before place and route shows comparable performance and 51% reduction of leakage

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power consumption compared to *L*ow-*ST*andby-*P*ower (LSTP) FinFET counterpart.

The remaining parts of this paper are organized as follows. In Section II, we introduce the background of multi-V_t design and ambipolar SiNWFETs. In Section III, we present the vertically-stacked TIG SiNWFET technology, its operation modes and performance estimation. In Section IV, we map logic gates onto an uncommitted pattern with both low-V_t and high-V_t configurations. Performance of logic gates and benchmark circuits with TIG SiNWFETs is compared with LSTP FinFET technology in Section V followed by a discussion of challenges and opportunities in Section VI and conclusions in Section VII.

II. Background

In this section, we briefly review the conventional multi-threshold-voltage technology, and introduce the electrostatic control in state-of-the-art ambipolar silicon nanowire FETs.

A. Conventional Multi-Threshold-Voltage Technology

For a given technology node, devices with low V_t normally show larger ($\sim 1.5\times$) I_{on} but also much larger ($\sim 30\times$) I_{off} when compared to high-V_t devices [5], [12]. Low-V_t devices with larger I_{on} are used in the critical paths to reduce delay and meet timing constraints. In non-critical paths, leakage power consumption becomes the main constraint. Then, high-V_t devices with lower I_{off} are preferred. The mix of different threshold voltages is called multi-V_t design, and is a common technique to reduce the overall leakage power consumption, without degrading the performance of circuits.

In multi-V_t design, devices with different threshold voltages can be obtained in different ways. A straightforward method is the use of different gate materials to tune the gate workfunction, thereby modifying the threshold voltage of the device [3], [13]. Similar as tuning the gate oxide thickness and channel doping concentration to modify V_t, this method requires extra process steps, which affects the layout regularity and increases the process costs compared to single-V_t design.

Adaptive body biasing is another approach to achieve multi-V_t design. Due to the body effect of MOSFETs, the threshold voltage of a device is modulated by separately biasing its source and body terminals [14], [15]. Nevertheless, separately tuning threshold voltage of each transistor is hard to achieve with this approach due to the isolation restriction and the area overhead of additional circuits and routing resources [4].

Compared to bulk MOSFETs, *F*ully-*D*epleted *SOI* (FDSOI) technology provides more flexibility to utilize the body effect. The threshold voltage of the FDSOI device can be also tuned by properly doping a ground plane layer below the buried oxide [13]. However, this method also requires extra process steps.

Table I summarizes the limitations of these conventional multi-V_t technologies. Either extra process steps or group tuning is required to implement the multi-V_t design. These technologies cannot perfectly avoid all the limitations.

To overcome these limitations, we propose in this paper a new device, which can realize dual-V_t circuits with a unified process for all the devices. The threshold voltage of pre-defined devices is tuned by applying different biases on extra gate terminals. This voltage biasing is decided individually by applying different connection schemes.

TABLE I
LIMITATIONS OF CONVENTIONAL MULTI-VT TECHNOLOGY

Limitations	Gate workfuntion engineering	Adaptive body biasing	Ground plane doping
Extra process	Yes	No	Yes
Group tuning	No	Yes	No
FDSOI only	No	No	Yes

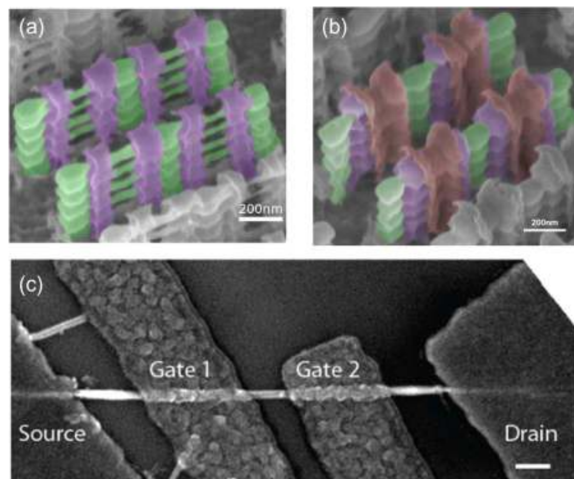

Fig. 1. SEM pictures of state-of-the-art ambipolar SiNWFETs, (a) Vertically stacked SiNWFET with only polarity gate, (b) and with both polarity gate and control gate [8], (c) Single SiNWFET with two independent gates ($\text{scale bar} = 200\ \text{nm}$) [10].

B. Electrostatic Control in Schottky-Barrier SiNWFETs

In order to improve the electrostatic control in short channel devices, FinFETs with a tri-gate structure have been successfully used for 22-nm technology node [5], [6]. Beyond FinFETs, silicon nanowire FETs with a gate-all-around structure are expected to achieve an even better electrostatic control.

On the other hand, metal source/drain technology has been investigated to reduce the contact resistance and to overcome the issues in heavily doped source/drain technology [16]. The metal-silicon contacts create Schottky barriers at source and drain. Schottky-barrier FETs show simultaneous *n*-type and *p*-type characteristics, since metal can provide the conduction of both electrons and holes. With efficient control of an additional polarity gate, Schottky barriers in SiNWFETs can be electrically trimmed. Electrons or holes are then selectively injected into the channel, and the polarity of the device is thereby determined.

Polarity control in a vertically stacked SiNWFET has been demonstrated with three gate regions in [8]. The structure is shown in Fig. 1(a), (b). The two gates close to source and drain are connected together and named as *P*olarity *G*ate (PG) (Fig. 1(a)). The other gate in the inner region is called as *C*ontrol *G*ate (CG) (Fig. 1(b)). The fabricated device exhibits both *n*-type and *p*-type characteristics depending on the polarity gate bias. Moreover, this device with gate-all-around structure shows <70 mV/dec subthreshold slope, which is approaching the theoretical limit.

Another approach to control the polarity consists of a single SiNWFET with two independent gate regions as shown in Fig. 1(c) [10]. The two gates independently modulate the Schottky

TABLE II
TWO FABRICATED SINWFETS WITH POLARITY CONTROLLABILITY

Device Structure	Channel Length	I_{on}/I_{off}	I_{off}	SS [mV/dec]
[8] Stacked NWs "PG-CG-PG"	$350nm$	$10^7(n)$ $10^6(p)$	$< 1pA$	$64(n)$ $70(p)$
[10] Single NW "PG-CG"	$680nm$	$10^7(n)$ $10^9(p)$	$< 4fA$	$220(n)$ $90(p)$

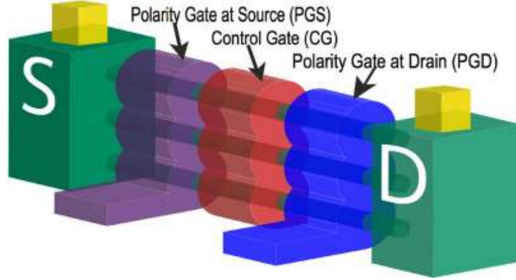

Fig. 2. Structure of a vertically-stacked three-independent-gate SiNWFET.

barriers at source and drain. Therefore, at OFF state, by drastically suppressing the tunneling at both source and drain, this device shows a very low leakage current, below 4 fA.

Table II summarizes the structure and performance of the two state-of-the-art ambipolar devices, including I_{on}/I_{off} ratio, leakage current and *S*ubthreshold *S*lope (SS). Although the channel length of these two devices is much longer than state-of-the-art CMOS devices, the principle of polarity control and leakage suppression still holds even with shrunk channel.

The two ambipolar SiNWFETs show either ideal subthreshold slope or ultra-low leakage current. Trade off between performance and leakage power consumption can thus be achievable by combining the two kinds of characteristics.

III. THREE-INDEPENDENT-GATE SILICON NANOWIRE FET

In this section, vertically-stacked TIG SiNWFET is introduced. Instead of using two different structures as discribed in Section II, the high-performance and low-leakage characteristics can be exploited in a unified structure. Polarizability and leakage control of the device are then discussed. TCAD simulation validates the dual-V_t ambipolar characteristic of the device, and also predicts its performance at state-of-the-art technology node.

A. Structure of TIG SiNWFET

Fig. 2 illustrates a vertically-stacked SiNWFET with three independent gate-all-around gate regions. This TIG structure enables all operations of the previous two devices. With this vertically-stacked structure, the driving strength is determined by the number of stacked nanowires, without any impact on area. Three nanowires are stacked in Fig. 2.

Vertically-stacked TIG SiNWFET can be fabricated with the same top-down process of vertically-stacked DG SiNWFET described in [8]. First, the stack of nanowires is obtained by a single *D*eep *R*eactive *I*on *E*tching (DRIE) Bosch process. Then the polarity gates are patterned and followed by a self-aligned patterning of control gate. After the formation of the gates, silicon nitride spacers are used to isolate the structures. A nickel layer is deposited and annealed to produce NiSi at source/drain and gate contacts. Finally, the unreacted nickel is removed by a selective etching of nickel over NiSi. This top-down approach enables large-scale fabrication of arrays of vertical stacks of nanowires, compared to the bottom-top approach which requires transfer procedures of grown nanowires on a final substrate [10], [17].

As opposed to DG-SiNWFETs, *P*olarity *G*ate at *S*ource (PGS) and *P*olarity *G*ate at *D*rain (PGD) are independent and modulate the Schottky barrier thickness to tune respectively the tunneling of electrons and holes. The *C*ontrol *G*ate (CG) in the inner region is used to switch the channel conduction as in conventional MOSFETs. With this novel structure, TIG SiNWFET is able to implement all operations of the previous two devices [8], [10], and thereby introduces tunable high performance and low leakage characteristics.

B. Operation of TIG SiNWFET

By independently biasing the three gates to either GND (‘0’) or V_{DD} (‘1’), 8 operation modes of this device are divided into 4 groups. We can identify two ON states, two standard OFF states, two low-leakage OFF states, and two uncertain states which will not be used. Fig. 3 illustrates the six most important operation modes and their corresponding band diagrams when $V_{DS} = V_{DD}$ (i.e., S = ‘0' and D = ‘1').

1) ***ON states***: As shown in Fig. 3(a), (b), when $\text{PGS} = \text{PGD} = \text{CG}$, one of the Schottky barriers is thin enough to allow hole tunneling from drain (*p*-type) or electron tunneling from source (*n*-type), and there is no barrier in the channel. Thus, majority carriers flow through the device easily.
2) ***OFF states***: Current is shut off due to the barrier induced by opposite biasing of control gate and polarity gates as shown in Fig. 3(c), (d). Nevertheless, small number of carriers are still tunneling through the thin barrier into the channel. This mode is similar to DG SiNWFET [8].
3) ***Low-leakage OFF states***: When $\text{PGS} = \text{S}$ and $\text{PGD} = \text{D}$ in Fig. 3(e), (f), thick barriers prevent carriers from tunneling at both source and drain and ensure minimum leakage in the device. This mode corresponds to the two-gate SiNWFET [10].
4) ***Uncertain states***: When $\text{PGS} =$ ‘1' and $\text{PGD} =$ ‘0', barriers are thin enough for tunneling. However, this condition may also create an unexpected barrier in the inner region that will block the current flow, and cause signal degradation. Hence, the uncertain states should be prohibited by always fixing $\text{PGD} =$ ‘1' ($\text{PGS} =$ ‘0') for *n*FET (*p*FET), or using PGD=PGS.

A symbol of TIG SiNWFET is shown in Fig. 4(a), with all five terminals. According to the transition between ON and OFF states, four configurations of TIG SiNWFET are also depicted in Fig. 4, including Low-V_t (LVT) *n*FET/*p*FET and High-V_t (HVT) *n*FET/*p*FET. The uncertain states are naturally avoided in these configurations.

1) ***Low-V_t pFET*** (Fig. 4(b)): PGS and PGD are biased to GND. The voltage sweep on CG makes a transition between *p*-type ON (Fig. 3(a)) and standard OFF states (Fig. 3(c)).
2) ***Low-V_t nFET*** (Fig. 4(c)): PGS and PGD are biased to V_{DD}. The voltage sweep on CG makes a transition be-

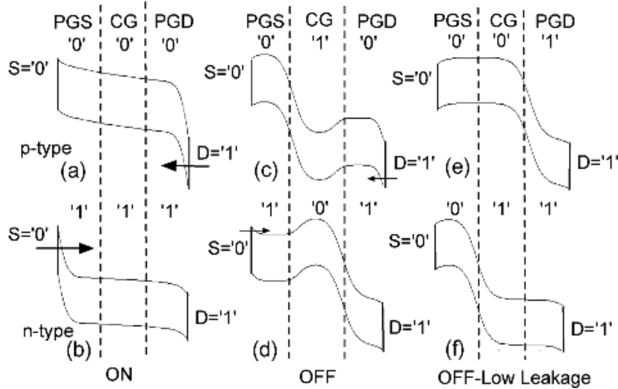

Fig. 3. ON, OFF and low-leakage OFF operation modes and their corresponding band diagrams.

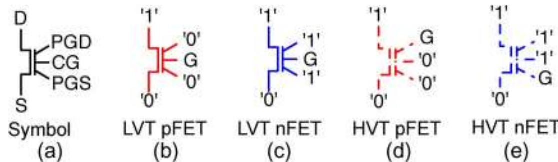

Fig. 4. Bias configurations of TIG SiNWFET with a single input.

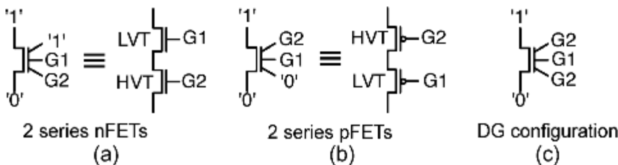

Fig. 5. Bias configurations of TIG SiNWFET for two inputs.

tween n-type ON (Fig. 3(b)) and standard OFF states (Fig. 3(d)).

3) ***High*-V_t *pFET*** (Fig. 4(d)): GND is applied to CG and PGS, and a voltage sweep is applied on PGD. In this configuration, the device switches between p-type ON (Fig. 3(a)) and low-leakage OFF states (Fig. 3(e))
4) ***High*-V_t *nFET*** (Fig. 4(e)): V_{DD} is applied to CG and PGD, and a voltage sweep is applied on PGS. In this configuration, the device switches between n-type ON (Fig. 3(b)) and low-leakage OFF states (Fig. 3(f)).

The configuration of TIG SiNWFET can be further extended for two inputs by combining the bias configurations for a single input in Fig. 4.

1) ***2 series nFETs*** (Fig. 5(a)): By combining the LVT and HVT nFET configurations, two inputs on CG and PGS implement the function of 2 series nFETs.
2) ***2 series pFETs*** (Fig. 5(b)): Similarly, the configuration of 2 series pFETs is obtained by combining the LVT and HVT pFET configurations.
3) ***DG configuration*** (Fig. 5(c)): The TIG SiNWFET can also work as a DG SiNWFET demonstrated in [8]. In this configuration, the device is ON when $G1 = G2$. Thus, this configuration is efficient for implementation of XOR function [18].

Even though a specified gate is used for polarization in TIG SiNWFETs, these two-inputs configurations efficiently utilize the extra gates without source/drain region between two inputs, thereby mitigating the area overhead compared to conventional CMOS devices. In addition, the internal node capacitance between two inputs does not exist in TIG SiNWFETs. This helps to reduce the delay of circuits.

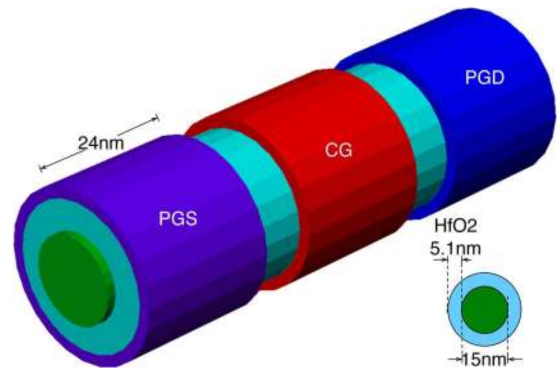

Fig. 6. Schematic of simulated 22-nm TIG SiNWFET.

C. Performance Estimation by TCAD

In order to estimate device performance at advanced technology node, a single TIG SiNWFET is simulated by using *Synopsys Sentaurus* [19]. Schematic of the device is shown in Fig. 6. Diameter of the lightly p-type doped silicon nanowire is 15 nm. Three 24-nm metal gates with mid-gap workfunction are placed on 5.1 nm HfO_2 high-κ dielectric layer $(\text{Equivalent Oxide Thickness} = 0.8\ \text{nm})$. *S*chottky *B*arrier *H*eight (SBH) for electrons is set to 0.35 eV in the simulation to get nearly symmetric n-type and p-type characteristics. This barrier height is achievable in actual process by using barrier height modulation technology [20], [21]. The symmetric n-type and p-type characteristics have also been observed in ambipolar SiNWFETs by applying radially compressive strain [22]. In our simulation, $V_{DD} = 1.2$ V is applied. The requirement of larger V_{DD} than conventional MOSFET is due to the presence of Schottky barriers and the longer channel length.

This TIG SiNWFET is simulated with the four configurations in Fig. 4. Dual-V_t characteristic of TIG SiNWFET is depicted in Fig. 7 in both linear and logarithmic scales. Solid lines indicate the low-V_t configurations, and dash lines indicate the high-V_t configurations. The threshold difference between the low-V_t and the high-V_t configurations is about 0.3 V.

In conventional dual-V_t technology, the high-V_t devices achieve lower leakage current but also reduce I_{on} compared to low-V_t devices. However, with TIG SiNWFET, I_{on} of both low-V_t and high-V_t configurations keep the same value since they share the same ON states shown in Fig. 3(a), (b). Thus, despite the degraded subthreshold slope (29% increase in simulation), the use of high-V_t devices reduces the leakage power consumption (by 86% in simulation) without significantly degrading the speed of circuits. This is a natural advantage of the dual-V_t technology based on TIG SiNWFETs. Since velocity saturation has been taken into account in the simulation, the characteristics above threshold voltage in LVT configurations are approximately linear in Fig. 7(a) [23]. With even higher/lower V_{CG} in LVT nFET/pFET configurations, the drain current saturates due to the limitation of source injection from the Schottky barrier.

The performance of simulated TIG SiNWFET with different configurations is listed in Table III. The subthreshold slopes were extracted at the lowest point following the methodology in [24]. Considering the carrier transport in LVT and HVT configurations, the control of the barrier height in the channel from CG is more efficient than the Schottky barrier thickness modulation from polarity gates [25]. Therefore, LVT configurations

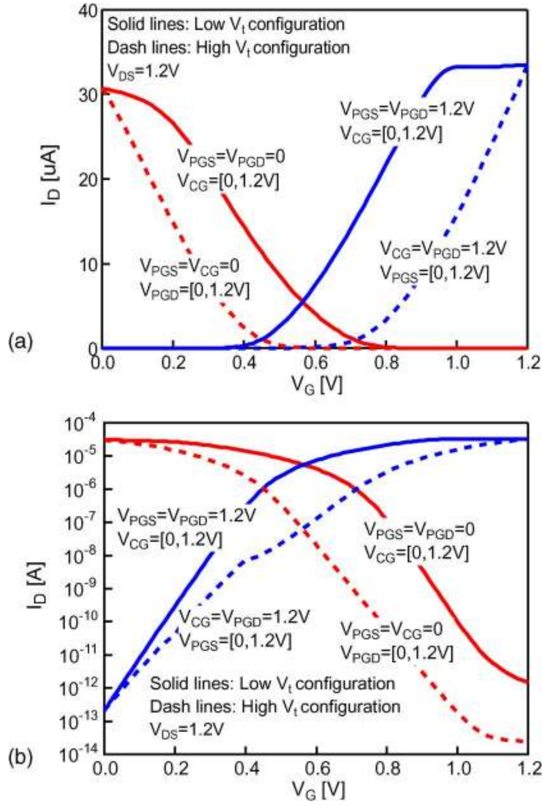

Fig. 7. Transfer characteristic of a single TIG SiNWFET illustrating the dual-V_t property—(a) linear scale (b) logarithmic scale.

TABLE III
PERFORMANCE OF SIMULATED 22-NM TIG SINWFET

Configuration	I_{on}/I_{off}	I_{off} [pA]	SS [mV/dec]
LVT nFET	10^8	0.21	64
LVT pFET	10^7	1.5	64
HVT nFET	10^8	0.21	86
HVT pFET	10^9	0.025	79

demonstrate better subthreshold slope than HVT configurations. The simulation result also shows that the leakage current of *p*FET can be significantly reduced by effectively modulating the Schottky barrier thickness with HVT configuration. In contrast, HVT and LVT *n*FET configurations demonstrate the same leakage current. The reason for this is that, SBH for electrons is relatively low in our simulation and the leakage current is dominated by thermionic current. Differently from tunneling current, thermionic current mainly depends on the barrier height, not the barrier thickness. Therefore, the leakage suppression in HVT *n*FET configuration can be improved by applying higher SBH for electrons.

IV. PHYSICAL DESIGN OF DUAL-V_t CIRCUITS

In this section, a physical design approach for dual-V_t circuits is proposed in order to fully exploit the flexibility of TIG SiNWFETs. An uncommitted logic gate pattern is introduced and basic logic functions are mapped onto it. By using both low-V_t and high-V_t configurations, logic gates towards either high performance or low leakage applications are implemented using different connection schemes. A compact implementation of a range of logic functions is also proposed.

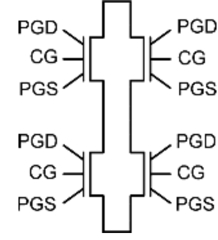

Fig. 8. Uncommitted logic gate pattern.

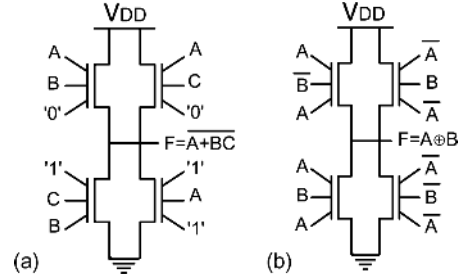

Fig. 9. (a) AOI gate and (b) XOR gate mapped onto proposed gate pattern.

A. Uncommitted Logic Gate Pattern

Regularity is one of the key features to increase the yield of integrated circuits at advanced technology nodes [26]. If logic functions can be mapped onto an uncommitted pattern, the layout regularity will be consequently improved.

An uncommitted logic gate pattern built with four TIG SiNWFETs is proposed in Fig. 8. There are two pull-up paths and two pull-down paths. Each path consists of only one transistor. Even though this pattern is very simple, a large range of functions can be mapped onto it with different configurations of TIG SiNWFETs. The implementation of unate and binate logic functions and D-flip-flop will be shown in the following part.

B. Logic Implementation

With different configurations of TIG SiNWFETs, we can map both combinational and sequential elements in logic circuits onto the proposed uncommitted gate pattern.

1) Combinational Elements: Fig. 9(a) presents an example of an AOI gate. Its functionality is obtained by applying the configurations of 2 series *p*FETs/*n*FETs and LVT *n*FET. Thus, only 4 transistors are needed for this AOI gate, instead of 6 conventional MOSFETs. In Fig. 9(b), an XOR gate is mapped onto this pattern. In this XOR circuit, the DG configuration of TIG SiNWFET is applied, which is efficient to implement binate logic functions.

*2) Sequential Elements: T*rue-*S*ingle-*P*hase-*C*lock *D*-*F*lip-*F*lop (TSPC DFF) is an efficient implementation of storage element in synchronous circuits [27], [28]. Based on the configurations of TIG SiNWFET for 1-input and 2-input conditions, a TSPC DFF is mapped onto the proposed gate pattern with 8 transistors, as compared to 11 transistors in conventional CMOS circuit (Fig. 10(a)). The equivalent logic structure is given in Fig. 10(b). This rising-edge triggered DFF is composed of 4 stages: a CLK-low enabled inverter at the first stage, a dynamic inverter at the second stage, and a CLK-high enabled inverter at the third stage, followed by a static inverter.

Although a single TIG SiNWFET is larger than a conventional MOSFET, the area gap of circuits between the two technologies is reduced thanks to the lower transistor count. More-

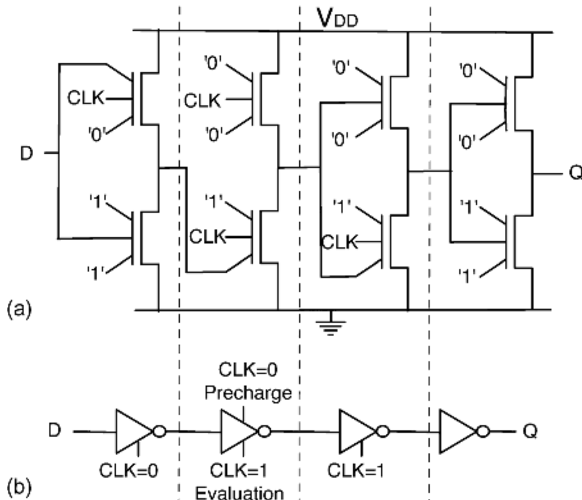

Fig. 10. TSPC DFF (a) mapped onto the proposed gated pattern, (b) equivalent gate-level circuit.

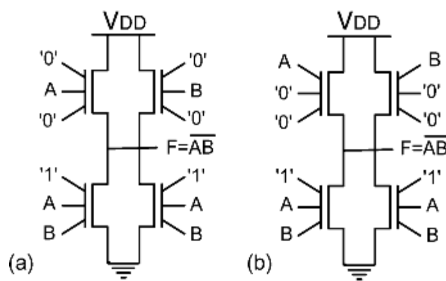

Fig. 11. Mapping of NAND gate towards (a) high performance and (b) low leakage application.

over, in the proposed gate pattern, each pull-up and pull-down path has only one series transistor. There is no internal node capacitance which needs to be charged or discharged. The speed of circuits is consequently improved.

C. Dual-V_t Design With TIG SiNWFETs

Delay and leakage of logic gates can be tuned by applying LVT and HVT configurations of TIG SiNWFET. For example, Fig. 11 illustrates two different mapping schemes of NAND gate for *H*igh *P*erformance (HP) and *L*ow *L*eakage (LL) applications. In Fig. 11(a), the HP gate is obtained by connecting inputs to the CGs of *p*FETs. Thus, the performance for pulling the logic gate up is improved by applying the LVT configuration of the devices. In contrast, the LL gate (Fig. 11(b)) is obtained by controlling the *p*FETs from the PGDs. Leakage power is thereby reduced by forcing the devices into HVT operation. In both HP and LL gates, PGSs and CGs of *n*FETs are connected to input signals to realize the logic function.

In a circuit, the signals A and B usually have different constraints. Since the CG of *n*FET shows low-V_t capability, while the PGS of *n*FET shows high-V_t capability (as shown in Fig. 5(a)), we can map the signals in critical paths onto the CG and the signals belonging to non-critical paths onto PGS. This method is also applicable for the pull-up path. Thus, the delay and leakage of the NAND gates can be even better tuned with more mapping schemes. Fine-grained dual-V_t design is thereby achievable with TIG SiNWFETs.

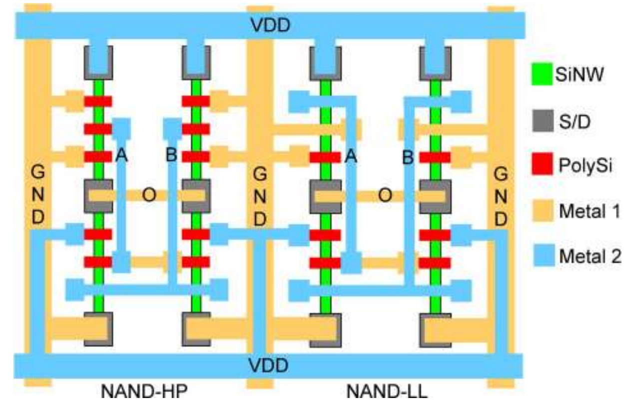

Fig. 12. Connection schemes of NAND gate towards high performance and low leakage application.

D. Connection Schemes for Uncommitted Gate Pattern

According to the presented mapping schemes, wiring on the uncommitted gate pattern can implement different functions with fine-grained tuning of delay and leakage of circuits. In order to maintain the layout regularity, the TIG SiNWFETs and contacts are pre-fabricated according to the uncommitted pattern proposed previously. It is worth pointing out that all the devices are identical as their properties are tuned electrically, therefore uniformizing the technology.

As observed previously, most of the TIG SiNWFET access gates have a fixed polarity. Hence, power and ground signals are spread all over the proposed logic gate pattern. In order to minimize the routing effort for power lines, the power distribution network is consequently optimized. A grid network is built with a mesh of power and ground lines. Based on this novel power distribution grid, logic gates implementing different functions towards HP and LL applications are obtained by wiring metal lines on the pre-fabricated gate pattern. For example, different connection schemes of NAND gate are demonstrated in Fig. 12, corresponding to the HP and the LL configurations shown in Fig. 11, respectively.

E. Compact Implementation of Logic Functions

In conventional CMOS circuits, *p*FETs can only efficiently transmit ‘1’ and *n*FETs can only efficiently transmit ‘0’. Due to the restriction of the full swing of output signal, the *P*ull*U*p *N*etwork (PUN) with *p*FETs can only be connected to V_{DD} and *P*ull-*D*own *N*etwork (PDN) with *n*FETs can only be connected to GND. This is the conventional implementation of the static CMOS circuits (Fig. 13(a)). When transmitting a variable, CMOS transmission gate is necessary, which consists of complementary transistors. With transmission gates, *p*FET and *n*FET are both ON to avoid output signal degradation (Fig. 13(b)).

In contrast, an ambipolar device is able to switch its polarity. This property enables the design of other transmission gates corresponding to different logic functions. Fig. 14(a) shows an XOR-based transmission gate, which is very efficient for binate logic function implementations [18]. This property can be extended to the transmission of variables using a single device. Indeed, by selecting the device polarity according to the transmitted variable, it is possible to use a unique device. Since *C*

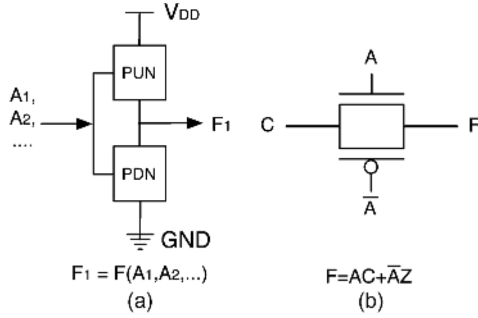

Fig. 13. (a) Static CMOS logic function, (b) Conventional CMOS transmission gate. Z is the high-resistivity state.

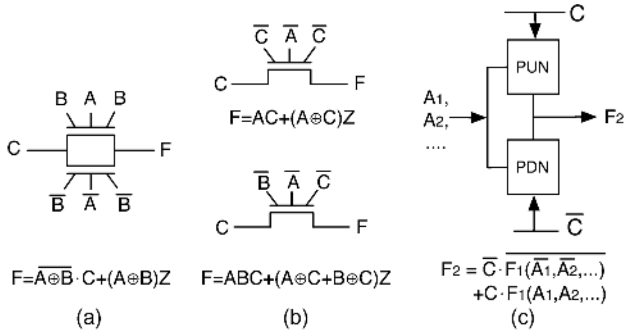

Fig. 14. (a) XOR-based transmission gate, (b) Transmission gate with single ambipolar device. Z is the high-resistivity state. (c) Compact implementation of logic functions with ambipolar devices.

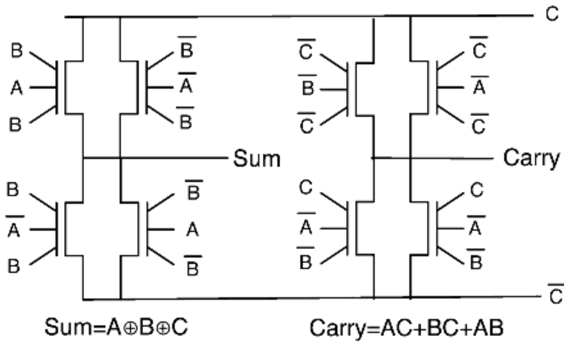

Fig. 15. Compact implementation of 1-bit full adder.

determines the device polarity in Fig. 14(b), single-input and two-input configurations of TIG SiNWFET (see Fig. 4 and Fig. 5) can be applied to obtain two novel transmission gates, respectively. By using this property, we can then extend the standard PUN/PDN to transmit a variable. Therefore, the fixed V_{DD} and GND in original design are extended to any complementary signals (Fig. 14(c)). More complex functions are thereby derived from original functions without any additional transistors, with a compact form intrinsically not implementable with conventional static CMOS logic or CMOS transmission gates.

To illustrate this compact implementation in detail, an example of 1-bit full adder is illustrated in Fig. 15. It is realized in a very compact form and mapped onto the proposed gate pattern.

The relationship between the original function and derived new function is shown in Fig. 14(c). It is found that the sum and carry of 1-bit full adder can be directly derived from 2-input XNOR and NAND functions. In the sum function, the two devices in either PUN or PDN have complementary polarities, and

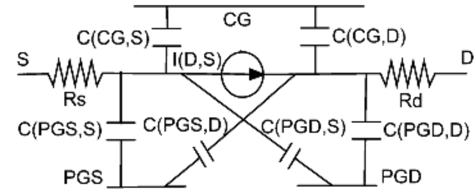

Fig. 16. Equivalent circuit model of TIG SiNWFET.

hence transmit the third input C or $\overline{C}$ without signal degradation. This also refers to the XOR transmission gate (Fig. 14(a)). In the carry function, the polarities of all devices are determined by the complementary signals C and $\overline{C}$. Each device can be considered as a transmission gate shown in Fig. 14(b). When C = '1', it is the NAND gate as shown in Fig. 11(a). When C = '0', it becomes a NOR gate. This is exactly the expected carry function.

V. Architectural Benchmarking

In this section, the effect of performance tuning and leakage power reduction by applying the physical design approach for dual-V_t configurable circuits is discussed for logic gates and benchmark circuits.

A. Methodology

A simple model for the proposed TIG SiNWFET is written in Verilog-A to enable circuit-level simulations. The equivalent circuit of a single TIG SiNWFET is shown in Fig. 16. The current source is described by a table model extracted from TCAD simulation. Access resistances are estimated according to the device geometry. Each capacitance is extracted from TCAD simulation as an average value under all possible bias conditions. The coupling capacitances between the gates are much smaller than the total capacitance of the device, and therefore neglected in the model. According to the capability of vertically-stacked silicon nanowire technology, we assume that there are four nanowires per stack. The stack is modeled by parallel arrangement of single TIG SiNWFET model.

A logic cell library is characterized using *Cadence Encounter Library Characterizer (ELC)*. The library consists of combinational logic cells INV, NAND, NOR, XOR, XNOR, AOI, OAI in both HP and LL configurations. More than these basic cells, the library also consists of the sum and carry functions implemented as in Fig. 15. To simulate sequential circuits, a TSPC DFF with asynchronous set/reset is also characterized. All the cells in the library are built from the uncommitted gate pattern described in Section IV. The area estimation of these cells is done according to the 22-nm design rules [5]. The impact of proposed connection scheme is considered in cell area estimation. A wire-load model is applied to take into account the capacitance and resistance of the interconnections. The supply voltage of vertically-stacked TIG SiNWFET library is 1.2 V.

Since we are demonstrating a physical design approach to implement dual-V_t circuits for standby power reduction, a counterpart library with supply voltage of 0.9 V is built with *P*redictive *T*echnology *M*odel (PTM) 20-nm *L*ow-*ST*andby-*P*ower (LSTP) FinFET model [29]. The LSTP FinFET library consists of all basic combinational cells and a TSPC DFF as in the TIG SiNWFET library. Considering that the sum and carry functions cannot be implemented with FinFET in such a compact form as with TIG SiNWFET, these

TABLE IV
PERFORMANCE OF GATES WITH TIG SINWFET AND LSTP FINFET

Logic Gates		HP TIGNW	LL TIGNW	LSTP FinFET
INV	Delay [ps]	22.2	25.3	20.5
	Leakage [pW]	4.02	0.56	6.43
	Area [μm^2]	0.166	0.166	0.109
NAND	Delay [ps]	25.7	29.3	25.5
	Leakage [pW]	7.17	1.11	6.88
	Area [μm^2]	0.332	0.332	0.218
XOR	Delay [ps]	33.5	36.7	40.0
	Leakage [pW]	15.23	6.15	41.36
	Area [μm^2]	0.664	0.664	0.654
AOI	Delay [ps]	26.4	28.8	30.4
	Leakage [pW]	7.19	4.60	7.06
	Area [μm^2]	0.332	0.332	0.327
DFF	Delay [ps]	41.5	43.5	47.4
	Leakage [pW]	239.7	176.7	257.4
	Area [μm^2]	0.996	0.996	1.036

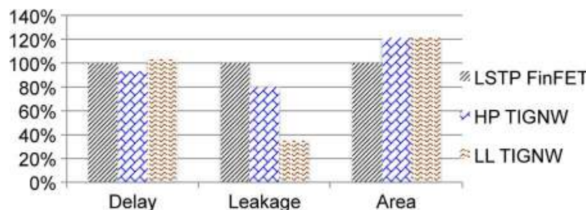

Fig. 17. Comparison results of logic gates with TIG SiNWFET and FinFET.

functions are not included in the FinFET library. The area of a FinFET is also estimated according to the 22-nm design rules.

With both TIG SiNWFET and LSTP FinFET libraries, combinational and sequential benchmark circuits are synthesized by *Synopsys Design Compiler*. Circuit-level performances results are extracted from the post-synthesis reports.

B. Gate Level Characterization

Table IV lists the maximum delay under a load of four INV $\times$ 1 gates, leakage power and area of some logic gates. These gates are built with different configurations using the different V_t modes of TIG SiNWFETs. The traditional CMOS counterparts are realized with LSTP FinFETs. The average comparison results are depicted in Fig. 17.

The LL TIG SiNWFET gates demonstrate a leakage power reduction of 65% compared to LSTP FinFET gates, at a cost of a 4% increase in delay. The low-leakage property stems from the good control of the thick Schottky barriers in the device that prevents carriers from tunneling into the channel during OFF state.

The HP TIG SiNWFET gates demonstrate a slight 6% reduction in delay as compared to LSTP FinFET gates. Among HP gates, AOI and XOR gates and DFF show 15% gain in performance and comparable area than FinFET, while INV and NAND gates show larger delay and area. While INV and NAND gates have the same implementation as in CMOS and suffer from the use of larger transistors, AOI and XOR gates and DFF are implemented on the proposed uncommitted logic gate pattern in a very different way. Indeed, the gates have only one transistor in each pull-up and pull-down path that is consequently of benefit to the different metrics.

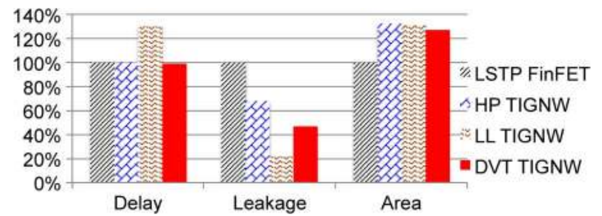

Fig. 18. Average comparison results of ISCAS'85 benchmark circuits with Dual-V_t TIG SiNWFET and LSTP FinFET.

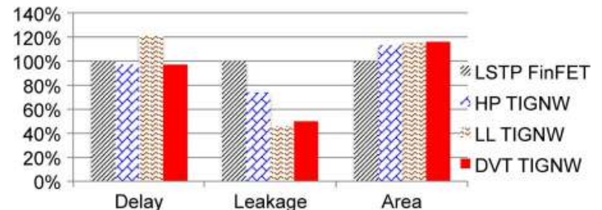

Fig. 19. Average comparison results of VTR benchmark circuits with Dual-V_t TIG SiNWFET and LSTP FinFET.

Noise margins were also characterized for the inverters. The HP inverter demonstrates noise margins of 0.52 V for '1' and 0.35 V for '0'. In contrast, noise margins of LL inverter are 0.60 V for '1' and 0.51 V for '0'. These results show 13% improvement compared to FinFET (0.38 V for '1' and 0.36 V for '0') when normalized to the supply voltages.

C. Circuit Level Results

The performance and leakage power consumption with TIG SiNWFETs and LSTP FinFETs are evaluated for both combinational and sequential circuits.

1) Combinational Circuits Results: Critical path delay, leakage power, and area of ISCAS'85 benchmark circuits are reported for HP, LL, dual-V_t TIG SiNWFET and LSTP FinFET libraries in Table V. Fig. 18 shows the average comparison results.

HP library demonstrates comparable performance with 32% leakage power reduction compared to FinFET library. While LL library shows a leakage power reduction of 78%, but with a 32% increase in delay. In contrast, by applying HP gates in critical path and LL gates in non-critical path, dual-V_t circuits with TIG SiNWFET keep comparable performances but reduce the leakage power consumption by 53% compared to LSTP FinFET circuits. An additional area cost of 28% is due to the larger size of three-independent-gate devices.

2) Sequential Circuits Results: To compare the performance of sequential circuits built with TIG SiNWFETs and LSTP FinFET, the *V*erilog-*T*o-*R*outing (VTR) sequential benchmark circuits are synthesized [30]. Results are shown in Table VI and Fig. 19.

Benchmark circuits with dual-V_t TIG SiNWFET gates show the same performance as with HP TIG SiNWFET gates, and also the same leakage power consumption as with LL TIG SiNWFET gates. Thus, comparable performance with 51% leakage power reduction are achieved with dual-V_t TIG SiNWFET compared to LSTP FinFETs despite an additional area cost of 16%.

VI. CHALLENGES AND OPPORTUNITIES

In this section, we highlight the challenges and opportunities in the TIG SiNWFET technology, physical design, CAD tools, and architechture.

TABLE V
DELAY, LEAKAGE, AND AREA OF ISCAS'85 BENCHMARK CIRCUITS WITH DUAL-V_t TIG SINWFET AND LSTP FINFET

Circuits	HP TIG SiNWFET			LL TIG SiNWFET			Dual-V_t TIG SiNWFET			LSTP FinFET		
	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]
c432	0.30	1.87	100.89	0.38	0.60	102.55	0.31	1.28	95.75	0.31	2.54	81.89
c499	0.28	3.66	188.41	0.37	1.33	208.45	0.25	2.51	190.80	0.25	7.56	154.09
c880	0.24	4.04	219.42	0.29	1.19	202.67	0.24	2.34	192.76	0.24	5.36	166.63
c1355	0.29	3.34	166.87	0.38	1.12	190.53	0.26	2.47	184.02	0.25	7.29	148.40
c1908	0.33	3.75	207.20	0.45	1.11	182.49	0.36	2.67	187.13	0.36	6.36	153.14
c2670	0.22	4.94	269.68	0.29	1.68	264.43	0.22	3.48	289.45	0.23	8.05	221.74
c3540	0.42	9.32	515.74	0.55	3.25	519.76	0.43	6.65	502.85	0.45	10.95	354.35
c5315	0.31	12.02	662.60	0.41	4.49	703.15	0.30	8.57	668.80	0.31	17.07	490.89
c6288	1.08	32.92	1814.34	1.40	9.64	1672.77	1.10	22.55	1546.86	1.15	32.77	1070.82
c7552	0.27	15.94	852.10	0.37	4.60	783.79	0.28	11.04	790.70	0.27	25.56	647.23

TABLE VI
DELAY, LEAKAGE, AND AREA OF VTR BENCHMARK CIRCUITS WITH DUAL-V_t TIG SINWFET AND LSTP FINFET

Circuits	HP TIG SiNWFET			LL TIG SiNWFET			Dual-V_t TIG SiNWFET			LSTP FinFET		
	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]
diffeq1	1.90	145.77	5869.4	2.43	74.51	6011.9	1.90	107.03	6034.2	1.94	244.72	5228.6
diffeq2	2.30	113.59	5264.4	2.75	54.07	5349.8	2.30	70.77	5345.7	2.44	204.16	4654.3
or1200	2.25	315.36	8576.6	2.81	190.33	8786.1	2.25	208.78	9139.5	2.25	416.62	7343.0
bgm	1.62	2924.70	96260.5	2.06	1664.3	100521.8	1.63	1837.6	98219.7	1.63	3569.90	78945.1
blob_merge	1.37	346.35	12717.3	1.65	193.06	12667.4	1.38	195.64	13165.2	1.38	516.00	11179.0
sha	0.76	263.58	3801.2	0.98	180.99	3841.7	0.76	185.36	3807.0	0.88	301.95	3400.2
boundtop	0.49	530.80	6842.8	0.62	372.03	6721.8	0.50	379.93	6830.9	0.50	590.06	5824.8
raygentop	1.12	503.56	12118.1	1.36	320.07	12625.4	1.13	350.19	12561.1	1.13	723.81	11193.9
stereovision1	0.68	3793.20	56869.9	0.83	2544.1	58099.5	0.69	2621.3	57874.0	0.69	4796.80	54338.3
stereovision2	1.31	5666.80	98028.1	1.72	3713.5	97402.9	1.32	3793.9	100068.9	1.38	7177.90	87749.9

A. Technology

There are many challenges in the fabrication of vertically-stacked TIG SiNWFET. In order to yield energy efficient circuits with a single type of transistor, symmetric *n*-type and *p*-type characteristics of ambipolar SiNWFETs are required [22]. Therefore, metallic source/drain with near mid-gap workfunction is preferred to achieve this symmetry. Unfortunately, such a high Schottky barrier height limits the ON-state current of device, and the circuit speed is consequently limited. To overcome this issue, larger supply voltage is required to improve the tunneling at a cost of increased power consumption. A solution consists of using semiconductors with narrower band gap for the nanowires, like germanium. Nevertheless, lower barrier height will result in larger leakage current and degraded $I_{\rm on}/I_{\rm off}$ ratio. Alternatively, radially compressive strain is applied in the ambipolar SiNWFET technology in recent research, and ideal symmetry of *n*-type and *p*-type characteristics is observed [22].

B. Physical Design

In the presented technology, the intrinsic gate capacitance $C_{\rm gate}$ and the leakage current $I_{\rm off}$ are proportional to the number of nanowires per stack, while the interconnection capacitance $C_{\rm wire}$ keeps constant. Delay and leakage power are estimated for a given number of stacked nanowires *N* as

$$Delay \approx \frac{NC_{\rm gate,1NW} + C_{\rm wire}}{NI_{\rm on,1NW}V_{\rm DD}}$$

$$Leakage\ Power \approx NI_{\rm off,1NW}V_{\rm DD}$$

For a small *N*, a single stack of nanowires cannot drive a heavy wire load. Thus, a set of stacks have to be used to reduce the delay, which comes at a cost in area. In contrast, by increasing the number of stacked nanowires *N*, delay of the circuits will decrease, but limited by intrinsic gate delay, at cost of a linear increase in leakage power consumption. A trade-off number of nanowires per stack needs to be carefully investigated to optimize the delay and leakage power consumption according to circuit design constraints.

C. CAD Tools

State-of-the-art logic synthesis tools are efficient for unate logic functions. In contrast, TIG SiNWFET is efficient at implementing both unate and binate logic functions. Hence, it is expected to obtain even better performance of TIG SiNWFET based circuits thanks to novel logic synthesis tools exploiting a large class of functions [31].

In TIG SiNWFET technology, the delay and leakage of circuits are fine tuned according to the performance requirement.

An optimal mapping scheme yields to the fine-grained tuning at transistor level for each circuit as presented in Section IV. With the mapping result, direct routing on the prefabricated devices is desired. However, a single TIG SiNWFET has 5 terminals in a compact area. Thus, routing on these devices is challenging. To mitigate routing efforts, a regular layout technique called sea-of-tiles could be applied, which has shown the potential on routing and area utilization with DG SiNWFETs [9].

D. Architecture

Polarity control of SiNWFET creates a new way to implement logic functions. Besides the demonstrated functions in this work, circuits with ambipolar SiNWFETs are able to implement more novel functions, such as the power-gated differential logic [32].

In the presented physical design, dual-V_t circuits are achievable by wiring metal lines on prefabricated uncommitted patterns. With the same approach as building structured ASICs, only metal/via layers are customized to realize these designs. Therefore, the fine-grained dual-V_t design is achievable in structured ASICs with TIG SiNWFET technology.

In addition, desired logic functions can be obtained by assigning inputs to proper terminals on the proposed uncommitted pattern. Thus, with programable connection between inputs and terminals, we can also envisage using the presented pattern to efficiently build novel FPGAs logic blocks.

VII. Conclusions

In this work, an efficient approach to implement dual-V_t configurable circuits with a novel three-independent-gate silicon nanowire FETs is presented. This device can be electrically configured in terms of polarity and threshold voltage. Logic gates using these devices can thus be realized to either fit high performance or low leakage applications, simply by wiring of an uncommitted gate structure. A range of logic functions are realized in a very compact form by utilizing the polarity and threshold controllability of TIG SiNWFETs. Benchmarking results show that, before place and route, comparable performance can be achieved with a 51% reduction of leakage power consumption for circuits based on TIG SiNWFET compared to low-standby-power FinFET technology, at a limited 16% increase in area.

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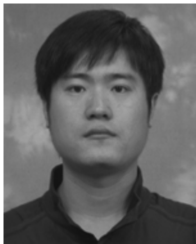

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