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Connecting Chips With More Than 100 GHz Bandwidth

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ABSTRACT Connecting chips within a module is a basic requirement in transforming MMIC performance to system functionality. More and more applications demand for operation at high mm-wave frequencies or with ultra-large bandwidth. While semiconductor devices have seen tremendous progress in terms of their frequency limits, the chip interconnects lag behind and often form the bottleneck in realizing such systems. This paper reviews the broadband potential of the most common interconnect types in use and their performance demonstrated so far, covering wirebonding, approaches with chips embedded in a substrate, and flip-chip. Additionally, as an intermediate solution between system-on-chip and system-in-a-package, semiconductor hetero-integration on the chip-level is included. As is discussed, bond wire interconnects are most limited in bandwidth among the four types and reach the 100 GHz band only at the expense of narrowband characteristics. Dedicated embedded-chip packaging techniques show significantly better performance, bandwidths in the order of 100 GHz have been shown in the literature. Flip-chip has clearly the highest potential, interconnects covering the range from DC to 500 GHz have been demonstrated and are presented in the paper. Hetero-integration on the chip proves to allow for very broadband interconnects between elements and circuits on the compound chip as well: For an InP-on-BiCMOS process 325 GHz bandwidth were achieved and even higher values seem to be feasible.

INDEX TERMS Packaging, interconnects, mm-waves, wirebonding, flip-chip, hetero-integration, multi-chip modules, MCM-D.

I. INTRODUCTION

The frequency limits of semiconductor technologies have seen a continuous improvement over the past decades. Operation frequencies in the 300 GHz range are now accessible with several technologies, from RFCMOS and SiGe-BiCMOS to InP technologies, and even GaN is entering this arena. The increased high-frequency performance has advanced broadband capabilities as well. Bandwidths in excess of 100 GHz are within easy reach, meeting the demands for ultra-wide band operation in high-speed optical communications, non-destructive testing, broadband measurements (single-sweep 220 GHz VNAs are on the market), spectroscopy, and others [1], [2]. Also, radar-based imaging instruments demand for solutions well above 100 GHz, with bandwidths of 60 GHz up to even 100 GHz [3], [4].

However, the development of packaging has not kept pace with the progress in semiconductor technology and the interconnects between different chips have become a major obstacle in realizing the high-frequency and broadband systems targeted [5]. The basic reason is that on-chip and off-chip structures follow different scaling rules. While on the chip down-scaling of the characteristic transistor dimensions

proved to be a very successful approach, which has reached the ultimate limits of lithography, for off-chip structures much coarser dimensional limits apply, which are determined by hybrid fabrication technologies and by the large dimensions involved in packaging, both in lateral dimension and volume.

Commercial electronic in mm-wave and THz systems today still use mostly single-chip hollow waveguide-housed components which are realized in split-block technology. While performing well in terms of loss and bandwidth, the split-block packages are bulky and costly to manufacture, and difficult to scale to MIMO or phased-array configurations.

In order to circumvent this bottleneck in packaging, system-on-chip (SoC) solutions have been applied, combining the entire high-frequency part of a system on a single chip, thus avoiding any critical off-chip connection. However, this requires a semiconductor process with universal capabilities for all transmit and receive functionalities, including antennas and optical components, for instance. III-V compound semiconductor processes provide ultimate performance and the availability of optical components on-chip, but are limited in IC complexity, while CMOS and BiCMOS technologies offer best complexity while giving rise to trade-off in performance [6]. Usually, the required set of specifications is difficult to fulfill with a single technology and, therefore, the availability of chip interconnects with high bandwidth remains an essential requirement in many applications.

This is the basic motivation for this paper. Its purpose is to review the state-of-the-art solutions for ultra-broadband interconnects and to report on our own research results in this field. In order to limit the scope, we will focus on truly broadband approaches, with a bandwidth of 100 GHz and more, such as required for next-generation high-data-rate fiber-based optical communications, for instance. Further emerging applications involving electronic chips with wideband performance are edge computing, imaging sensors [7], mm-wave point-to-point radio links [8]–[10], and mm-wave radar [11].

The paper is organized as follows: Section II starts with considerations in assessing the bandwidth potential of an interconnect in general. In the following sections, the state of the art in the most common approaches will be presented and their bandwidth potential discussed. This includes relevant own results using flip-chip technology and hetero-integration on chip level. The conclusions then summarize the outcome and identify general trends.

II. BANDWIDTH LIMITATION OF AN INTERCONNECT: BASIC CONSIDERATIONS

The basic equivalent-circuit description of a chip interconnect is shown in Fig. 1. Note that the π-topology is treated here while its T-counterpart is equally important but the conclusions to be drawn do not differ. On the left-hand side, one has a first chip or the board, represented by the voltage source with internal impedance Z_L, on the right-hand side the second chip is located, with the matched input impedance Z_L. The interconnect itself is described by the parasitic reactances, the inductance L and the capacitances C_1 and C_2. For the sake of simplicity, losses in the interconnect are neglected, which, of course, can make a significant difference at high frequencies.

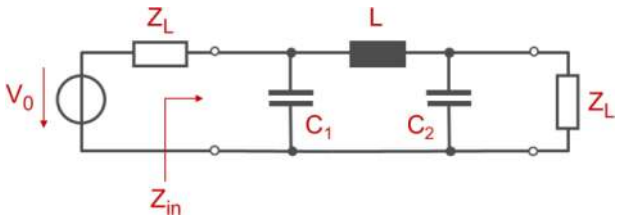

FIGURE 1. Basic equivalent circuit of an interconnect in an environment with characteristic impedance Z_L.

As can be seen easily, in the low frequency limit $\omega \to 0$ the reactance ωL and the susceptances ωC_i become negligible compared to Z_L. As a consequence, Z_{in} is equal to Z_L, the reflections vanish ($S_{11} = 0$) and the transmission reaches unity ($S_{21} = 1$). This is the fully transparent interconnect, the ultimate target for any type of interconnect. With growing frequency, the influence of the parasitic elements L and C_i increases and the transmission properties of the interconnect degrade, i.e., the magnitude of S_{11} increases, as does insertion loss. There are two basic approaches to ensure the desired low-reflective and low-insertion loss properties also at higher frequencies:

- L and C_i usually scale with the dimensions of the interconnect. Therefore, miniaturizing the interconnect geometry maintains its transparent features from zero up to higher frequencies. More precisely, also the dielectric and magnetic properties play a role, which is the reason why the term electrical length should be used instead of the pure physical dimensions.
- If the electrical length cannot be kept small enough, there is only one alternative: Dimensioning L and C_i in a way that they are compensating each other, either forming a short transmission line of characteristic impedance Z_L (i.e., sqrt(L/($C_1 + C_2$)) = Z_L) or adding further elements so that a filter is realized with a thru-band at the desired frequency. However, these measures always introduce bandwidth restrictions and work properly only within a given frequency range. Simply speaking, one trades good transmission within a certain band by worse behavior outside this band. Hence, while this approach is very popular for narrow-band applications (e.g., when using wirebonding), its applicability in the broadband case studied here is limited.

These simple considerations reveal already the fundamental recipe to achieve broadband performance: Keep the physical and the electrical dimensions of an interconnect as small as possible and search for a packaging approach that allows you to do so. This is a key criterion when evaluating the broadband capabilities of a packaging technique.

One should emphasize at this point that it is not only the interconnect itself which needs to be considered because its size is largely determined by the dimensions of the interfaces, i.e., the pads and their minimum pitch, on the chip and on

the board. Usually the board fabrication technology is the one with the largest dimensions and thus the one which puts constraints on interconnect size. Therefore, the choice of the appropriate board technology is essential for achieving maximum bandwidth. An example is the MCM-D approach (e.g., [12], [13]), which allows for much smaller pad size and pitch than the common printed circuit boards, though at higher cost. See [14] for a more comprehensive overview on the board technologies.

In the following sections, we will refer to these basic considerations when briefly discussing the most popular interconnect concepts in use for high-frequency and broadband applications.

III. WIREBONDING

Historically, bond wire transitions (see Fig. 2(a)) were among the first interconnects used for microwave frequencies and until today they represent the most widespread interconnect approach, applied for frequencies from DC to beyond 100 GHz (see, e.g., [15]). However, they suffer from the fact that the two chips to be connected, or the chip and the board, have to be placed side-by-side, which limits downscaling of dimensions. Critical parameters in this regard are the gap g between the chips (see Fig. 2(a)), the shape of the wire loop, and possibly a difference in chip/board thicknesses. An additional impact originates from the distance of the pads on chip or board to the edge of the chip or board. Altogether, this restricts minimum bond wire length to around 100 μm, bond wires shorter than 50 μm are very difficult to achieve using classical technologies.

Thus, the bond wire causes significant parasitic inductance. It can be somewhat mitigated by using multiple bond wires. But, at mm-wave frequencies, the compensation technique has to be applied (see Section II) and, therefore, these transitions are all of the bandpass or lowpass type and narrowband in nature, so that it is very difficult to reach the full 100 GHz bandwidth range targeted here (see, e.g., [16]–[18]), at least not with decent insertion loss values and reflection levels. It can be accomplished only for special structures and non-standard packaging methods (e.g., [19]), which can be used for prototyping but are not compatible with higher volume fabrication.

IV. EMBEDDING CHIPS

In order to reduce the problems associated with the wire bond inductance, packaging approaches were developed that allow embedding of the chips in cavities of the substrate or in a multi-layer structure. Accordingly, this approach is referred to as 'embedded chips' in this paper. Fig. 2(b) illustrates the principal arrangement. It leads to a planarized surface for chip and board so that the interconnects can be realized as planar structures on top of the chips. This allows interconnect sections that can be tailored with regard to their size and characteristic impedance. Moreover, depending on the process used, the dimensions of the interconnect can be decreased to values much smaller than those possible for wirebonding. All this is beneficial for interconnect high-frequency performance.

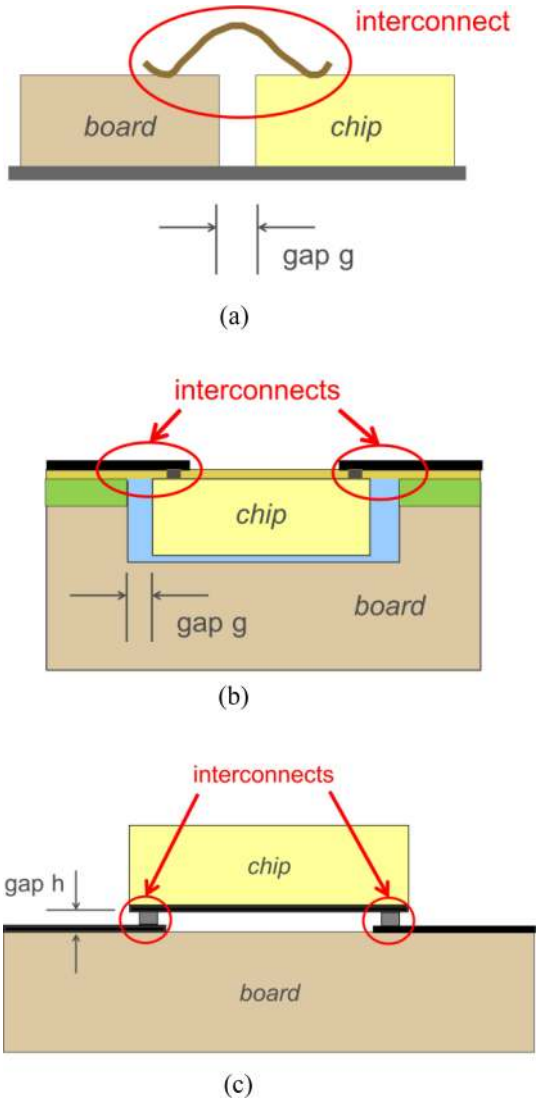

FIGURE 2. The three most common approaches to package a chip and connect it: Wirebonding, embedded chip, and flip-chip. (a) Wirebonding. (b) Example for the embedded-chip approach: chip mounted in a cavity in a multi-layer board and connected by transmission-line interconnects bridging the lateral gap around the chip. (c) Flip-chip.

A few examples are to illustrate the variety of approaches which fall into this category. One way is to etch cavities into a substrate and use BCB to planarize the surface and support the interconnect structures [20], [21]. If a multi-layer structure is used as the substrate, the chips can be embedded even more easily (see, e.g., [14], [22]). Regarding bandwidth, values up to 170 GHz have been published [21].

A further development related to this approach is the so-called eWLB method [23], which forms a molded substrate around the chip and realizes a redistribution layer on its surface which not only connects to the chip pads but also serves as the interface between the fine dimensions on the chip and the larger ones used to connect to the board, e.g.,

by using ball grid arrays. The eWLB-type approaches are in widespread use nowadays and being optimized continuously [24]. Frequencies beyond 200 GHz and bandwidths of more than 50 GHz have been shown (e.g., [25] states a frequency range from 200 …300 GHz for the interconnect).

Strictly speaking, the common eWLB packages do not fully belong to the embedded chip approaches since the molded chip with the redistribution layer is flipped and mounted to the board by a ball-grid array. Thus, eWLB is more a combination of the embedded-chip technique with the flip-chip one. Accordingly, the bandwidth is limited primarily by the ball-grid array with its coarse dimensions and not the embedded-chip interconnect itself.

Another solution for high-bandwidth interconnects that is somewhat related to chip embedding is the QUILT approach [26], which employs an edge-to-edge coupling between chips. A quite impressive bandwidth of 200 GHz was demonstrated.

Summarizing one can state that embedding the chips is a versatile approach, which after thorough optimization definitely can reach bandwidths in the 100 GHz range and above and still is compatible with volume fabrication.

V. FLIP-CHIP

A. CONCEPT AND OVERVIEW

The flip-chip concept is shown in Fig. 2(c). It differs from the ones in Fig. 2(a) and (b) significantly because the chip is flipped and mounted on top of the board. This allows further shrinking of the interconnect dimensions, which is limited now only by the available process technologies on the chip and the board and the minimum gap h between chip and board. These dimensions are much smaller than those that can be achieved with wirebonding and the embedded-chip techniques, if an appropriate fabrication process for the board is applied. Hence, the flip-chip concept inherently offers the best bandwidth potential of the three versions shown in Fig. 2.

The flip-chip interconnects are formed by small metallic pillars called bumps. One should note that reducing the gap h, which corresponds to the bump height, yields smaller interconnects but also increases proximity effects between chip and board, which show up as a detuning of the chip, i.e., a change in the high-frequency behavior of the circuit on the chip. Also, due to the sandwich structure a mismatch between the thermal expansion coefficients of chip and motherboard will cause mechanical stress on the interconnects, which may require an underfiller to distribute the forces and stabilize the structure under thermal cycling. Finally, because the backside of the chip is thermally not connected, heatsinking may become an issue and requires additional measures such as so-called thermal bumps, which do not serve any electrical function but only ensure proper heat transfer from the chip down to the board.

The excellent bandwidth capabilities of the flip-chip approach are supported by the published data. An overview of the work on flip-chip at mm-wave frequencies until the early 2000 years can be found in [27], demonstrating bandwidths up to 100 GHz (e.g., [28]). Further examples for flip-chip realizations in the mm-wave range present W-band modules for point-to-point communications [29] and on organic substrate [30], solutions for 0 …67 GHz [31], [32] and those for the full band up to 110 GHz [33], [34]. In [35], a transceiver module for imaging applications with 220 GHz bandwidth is presented. The publications include work on lead-free bumps [33] and underfiller [29], [32]. Also, on a liquid crystal polymer substrate (see [30]), 170 GHz bandwidth have been achieved [36]. Having a more detailed look at the results one finds in many cases relatively flat frequency characteristics without a cut-off at the higher frequency band so that one could expect even wider bandwidths than reported (e.g., for [32]–[34]).

All these works apply one or both of the two design strategies explained in Section II, i.e., miniaturizing the bump interconnect and using compensation techniques to further reduce influence of the parasitics [29], [32], [34].

B. RECENT RESULTS

More recently, the authors have pushed further the bandwidth to the 500 GHz range (see [37]–[39]). The key strategy was to follow the successful path described above, shrinking bump dimensions to a few μm (2 μm diameter and 10 …30 μm pitch) and performing a systematic design in reducing parasitics and then compensating the remaining reactive effects.

Another important aspect at frequencies beyond 100 GHz is the potential excitation of higher-order or radiating modes at the transition. In principle, any transition forms a discontinuity for wave propagation and hence leads to creation of higher-order modes. This may lead to power loss due to radiation, to coupling into substrate modes in both chip and carrier, or to signal reflections and hence standing waves. Therefore, it is essential when designing chip transitions to consider radiation and mode coupling in the design procedure.

Both the interconnect itself and the transmission-line-types connected to it need to be chosen properly to suppress radiation as far as possible. For this reason, although the coplanar waveguide provides best geometrical fit to the bump transition, the thin-film microstrip line was employed on the chip and the strip line on the board, in order to ensure almost radiation-free performance of the transmission lines on the chip and the board up to highest frequencies. In both cases, the lines were realized by embedding highly conductive gold lines in multi-layer BCB structures.

Figs. 3(a), (b), and (c) illustrate the entire arrangement and the core part of the resulting transition. Despite the scaling described earlier, such a structure is still no longer electrically short at the higher end of the frequency band. Therefore, for design, the transition was broken into different sub-parts and the impedance in each ‘partially uniform’ section was first locally optimized to be close to 50 ohm. Then, a global optimization was used to account for the interactions between the different sections. This strategy tries to mimic the transition by a cascade of matched transmission lines.

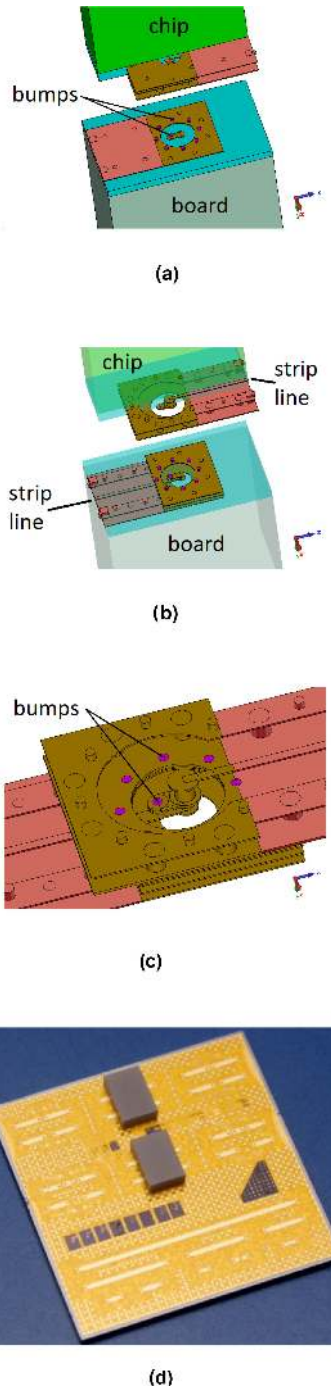

FIGURE 3. **The 500 GHz flip-chip interconnect and the test structures fabricated. (a) The flip-chip transition structure (chip lifted, front half blanked). (b) View as in Fig. 3(a), but upper metallization on chip blanked and strip line section on board opened. (c) View as in Fig. 3(b), but chip mounted, only metallizations shown. (d) Fabricated flip-chip modules.**

A second challenge was the pad capacitance. Again, scaling reduces this quantity, but it is still not negligible at the higher frequencies. Our strategy was to introduce ground cuts to reduce this capacitance further, in order to achieve widest bandwidth but accept some radiative coupling into parasitic modes of the board and chip substrate. Overall, a total of 16

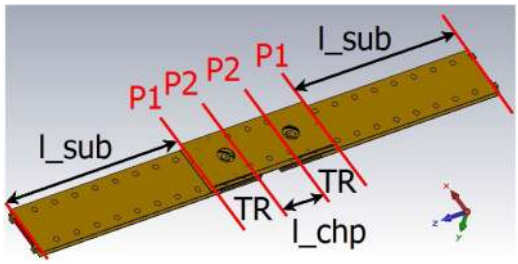

FIGURE 4. **Simplified view of the back-to-back structure (only metallization structures shown), with reference planes P1 …P4 for deembedding S-parameters.**

dimensions needed to be optimized by repeated em simulations to develop this interconnect.

For experimental verification, back-to-back test structures for on-wafer measurements were designed and realized with AlN chips on a Si carrier substrate (referred to as board). They consist of a thru line on the chip, two flip-chip transitions according to Fig. 3(a) and two connecting lines on the board. Fig. 3(d) presents a photo of the module with the chips mounted. Fig. 4 adds information on the back-to-back line structure, including the reference planes. Only the metallizations are plotted, one can distinguish the two connection lines on the board (l_sub) as well as the transmission-line section on the chip (l_chp) and the two interconnects. All transmission lines are strip lines. Their behavior was extracted by calibration elements on the board and realizing back-to-back structures with three different line lengths on the chip. In this way, the loss contributions of the two interconnects could be separated from the remaining parts of the structure.

Fig. 5 presents the measured S-parameters for three samples, each with a different line length on the chip. In Fig. 5(a), the reflection magnitude is plotted against frequency for the range from DC to 500 GHz (since this has to be performed over several bands with different probes, there are some small gaps in the curve). The reflections for the two consecutive transitions remain below −15 dB up to 500 GHz.

Fig. 5(b) adds the corresponding data for the transmission magnitude. An insertion loss of less than 1.8 dB is observed within the entire frequency range, which means less than 0.9 dB per transition from DC to 500 GHz. In order to assess the loss mechanisms responsible, the figure includes simulation results for the structure with lossless materials (so that only radiation exists) and with lossy materials (which should describe the measurement case). As can be seen, at lower frequencies material losses (conductor, dielectric) are the main contributors to insertion loss. At 500 GHz, however, the situation is reversed, where the radiation into parasitic modes dominates.

Fig. 5(c) shows the electrical length of the two consecutive transitions. One finds that a single transition at 500 GHz provides around 180 degree phase shift. The linear phase behavior of the transition over the entire DC to 500 GHz bandwidth means it essentially acts as an additional piece of transmission line.

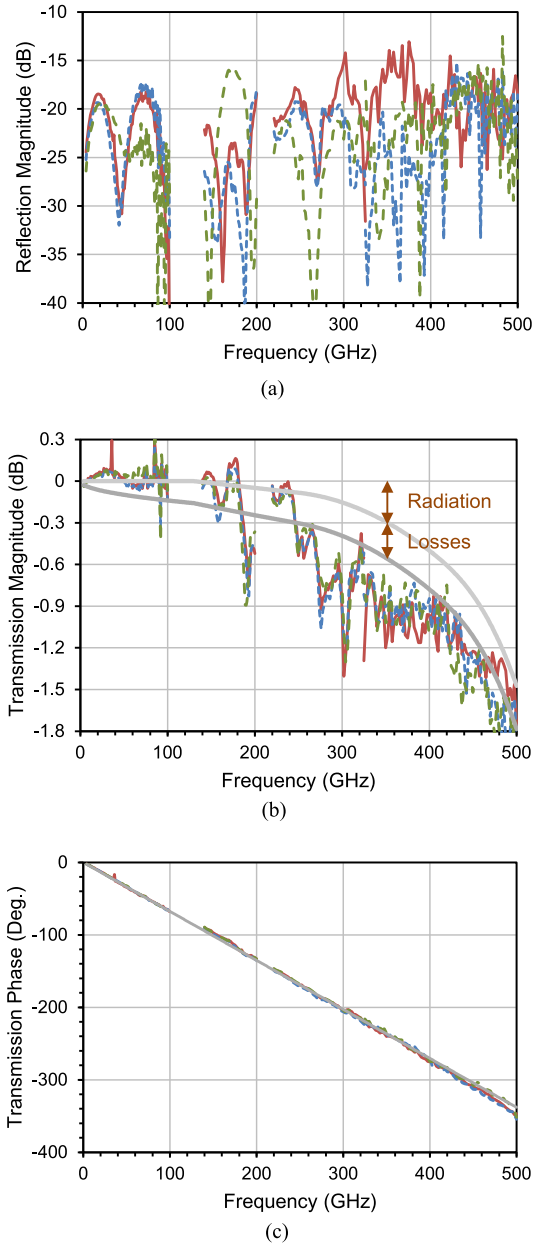

FIGURE 5. Measured S parameters of the back-to-back structure according to Fig. 4 (the three colors refer to structures with different line lengths on the chip of 160 …640 μm); from [38]. (a) Reflections (magnitude) as a function of frequency. (b) Transmission magnitude against frequency (line losses of connecting lines and chip section deembedded; grey curves denote simulation results w/o and with material losses, indicating the contribution of radiation and material losses, respectively). (c) Transmission phase of the 2 interconnects; contributions of connecting lines and chip section deembedded, grey line denotes simulation data.

It is interesting to discuss whether and how the interconnect can be further scaled to frequencies beyond 500 GHz. As stated above, radiation loss is the dominant loss phenomenon in this range. Therefore, the openings in the ground metal layers must be shrinked to avoid prohibitively high radiative loss, which eventually will make the excess capacitances the most dominant parasitics phenomenon.

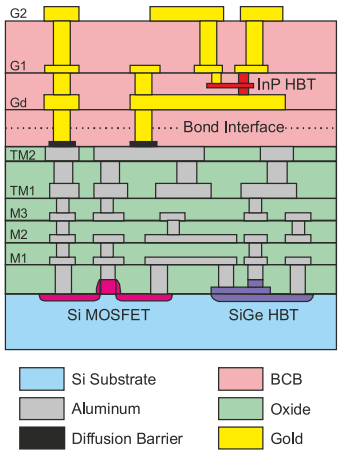

FIGURE 6. Layer stack of the InP-on-SiGe-BiCMOS technology [41], [42], M1 …TM2 refers to the BiCMOS stack, Gd …G2 contain the InP circuit parts (from [42]).

VI. HETEROGENEOUS INTEGRATION ON CHIP-LEVEL

A. OVERVIEW ACTIVITIES

As mentioned in the Introduction, the system-on-a-chip (SoC) approach is attractive because it almost eliminates the interconnect problems. However, it requires all subcircuits to be realized in the same technology, in most cases (Bi)CMOS. This can significantly compromise performance, mainly output power and noise figure, since III-V technologies like InP offer here values significantly better than BiCMOS. So, the ideal solution would be to have hetero-integrated chips, which combine elements and circuits of different technologies and their specific advantages on a single chip. In the US, DARPA has been pushing this through various programs in the last years (see [40]), covering a broad circuit spectrum and starting from high-speed AD converters. In Europe, a much smaller activity, as a joint project of two German research institutes (FBH and IHP), is targeting the same field but focusing on the combination of InP with SiGe-BiCMOS and application-wise on mm-wave circuits only (see [41], [42]). This work forms the background of the interconnect results presented in the following subsection.

B. INTERCONNECT RESULTS

In the course of the development of the InP-on-BiCMOS hetero-integration process [41] the authors had to deal with the interconnect issue in great detail. The basic idea behind the integration was to combine InP-HBT based subcircuits for special mm-wave functions with the BiCMOS circuitry providing the remaining functionalities. This is realized by BCB wafer bonding, which yields a hetero-integrated chip that contains the InP circuits in the top layers and the full BiCMOS stack below. Fig. 6 illustrates the resulting layer stack. From this graph it is clear that the realization of a high-performance (vertical) transition between the InP and the BiCMOS circuits within the hetero-integrated chips was a key issue in achieving the target of a technology-transparent

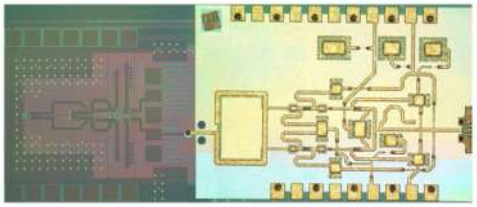

FIGURE 7. Chip photograph of 328 GHz hetero-integrated oscillator realized in InP-on-BiCMOS technology.

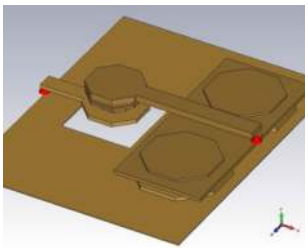

FIGURE 8. Transition core for the hetero-integration interconnect (only metals shown, other material blanked). The port on the left-hand side refers to the BiCMOS part (TM2-M2), on the right-hand side to the InP-BCB part (GD-G2) – for layer definition see Fig. 6.

solution. Fig. 7 shows a chip photograph of a hetero-integrated 328 GHz oscillator [43], which combines an 82 GHz VCO in SiGe-BiCMOS with a quadrupler realized as InP DHBT circuit. On the left-hand side of the photo the SiGe VCO can be seen, which is covered by the BCB-InP stack. The InP quadrupler is on the right-hand side and both are connected via an interconnect in the center.

Fig. 8 illustrates the geometry of this transition. The port on the left side is a buried microstrip between the TM2-M2 layers of the BiCMOS stack, whereas the one on the right forms a thin-film microstrip between the G2-GD layers of the InP part (for layer definitions see Fig. 6). The transition was designed for frequencies up to 300 GHz. Due to the small dimensions, radiation losses are negligible for these frequencies. Accordingly, in contrast to the 500 GHz version of Section V.B, extensive ground shielding around the signal via stack was not needed in this case. The ground connection between the two chips is simply a stack of level-raising vias which can be seen on the right-hand side. The pad on the BiCMOS side causes significant capacitance to ground and, therefore, a ground cut was introduced to reduce this effect. The size of the pad cannot be scaled down further because it must accommodate misalignment of the two wafers due to the wafer-bonding process.

The fabrication of the InP-BiCMOS interconnect has been verified for potential misalignment and connection errors using a test structure with a chain of 10 transitions (see Fig. 9). The structures were characterized from 0 to 325 GHz, the reference planes are shown in Fig. 9. Fig. 10 presents the measured insertion loss (S_{21}) as well as reflection co-efficient (S_{11}) data of the test structure. In order to obtain the insertion loss

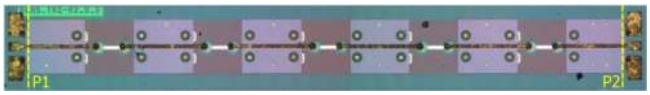

FIGURE 9. Test structure with 10 consecutive back-to-back transitions for characterization of electrical performance and process robustness (darker regions refer to the BiCMOS sections); P1 and P2 indicate the reference planes used for on-wafer calibration of measurements.

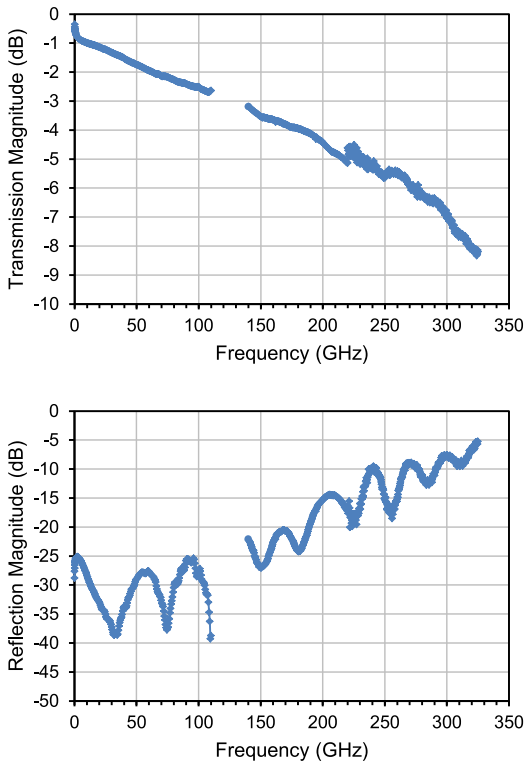

FIGURE 10. Measured transmission and reflection parameters of the structure in Fig. 9 as a function of frequency.

(IL) per transition, it is necessary to subtract the losses of the transmission line and to divide by the number of transitions. This leads to a measured IL of less than 0.5 dB per transition from 0 to 325 GHz. Regarding the reflection data it is more difficult to extract the S_{11} of a single transition from that of the entire chain but the overall characteristics and the value of -5 dB at 325 GHz indicate that the excellent behavior of the insertion loss applies to the reflections as well. A detailed analysis of the InP-BiCMOS interconnect can be found in [44].

As can be concluded from this data, the potential of this interconnect has not been fully exploited and a bandwidth up to 500 GHz and even more is within reach. This corresponds with the fact that hetero-integration on the chip level probably allows for the smallest interconnect dimensions: very dense hetero-interconnects with 5 μm pitch have been demonstrated [45]. Therefore, this approach is expected to yield the highest bandwidth performance among the interconnects studied in this paper.

VII. CONCLUSION

Ultra-broadband interconnects to and from chips with bandwidths up to 500 GHz are a reality today. This is achieved by employing packaging schemes that minimize interconnect dimensions and their electrical length. A prerequisite is to employ a board technology which allows for pad sizes and pitch small enough. Then, among the common techniques, the flip-chip concept offers the best bandwidth potential and has set the pace. Hetero-integration approaches combining several semiconductor technologies on the same chip can achieve similar and better performance for the intra-chip connections. For bandwidths in the 100 GHz range, the various packaging concepts using chip embedding are viable when adapted appropriately while common wire bonding techniques are restricted to lower bandwidths.

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