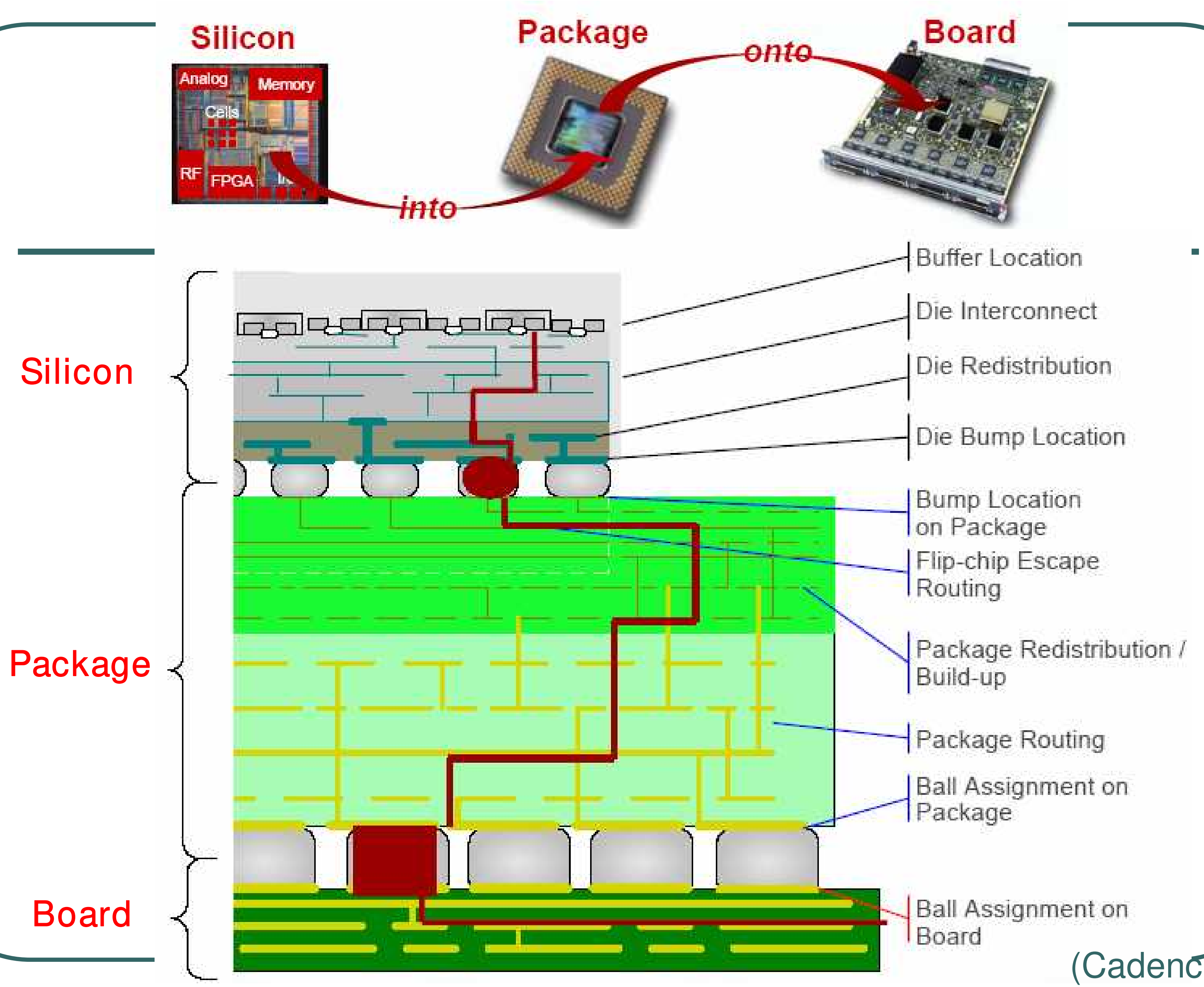
Constraint Driven I/O Planning and Placement for Chip-package Co-design

Jinjun Xiong, Yiuchung Wong, Egino Sarto, Lei He

University of California, Los Angeles
Rio Design Automation, Inc.

Agenda

- Motivation
- Overview of our approach
- Chip-package aware design constraints
- CIOP: constraint-driven I/O placement problem formulation
- Multi-step CIOP algorithm
- Experiment results
- Conclusion



Silicon
Analog
Memory
Cells
RF
FPGA
into
Package
onto
Board
Silicon
Package
Board
Buffer Location
Die Interconnect
Die Redistribution
Die Bump Location
Bump Location on Package
Flip-chip Escape Routing
Package Redistribution / Build-up
Package Routing
Ball Assignment on Package
Ball Assignment on Board

(Cadence)

I/O Placement for Flip-chip

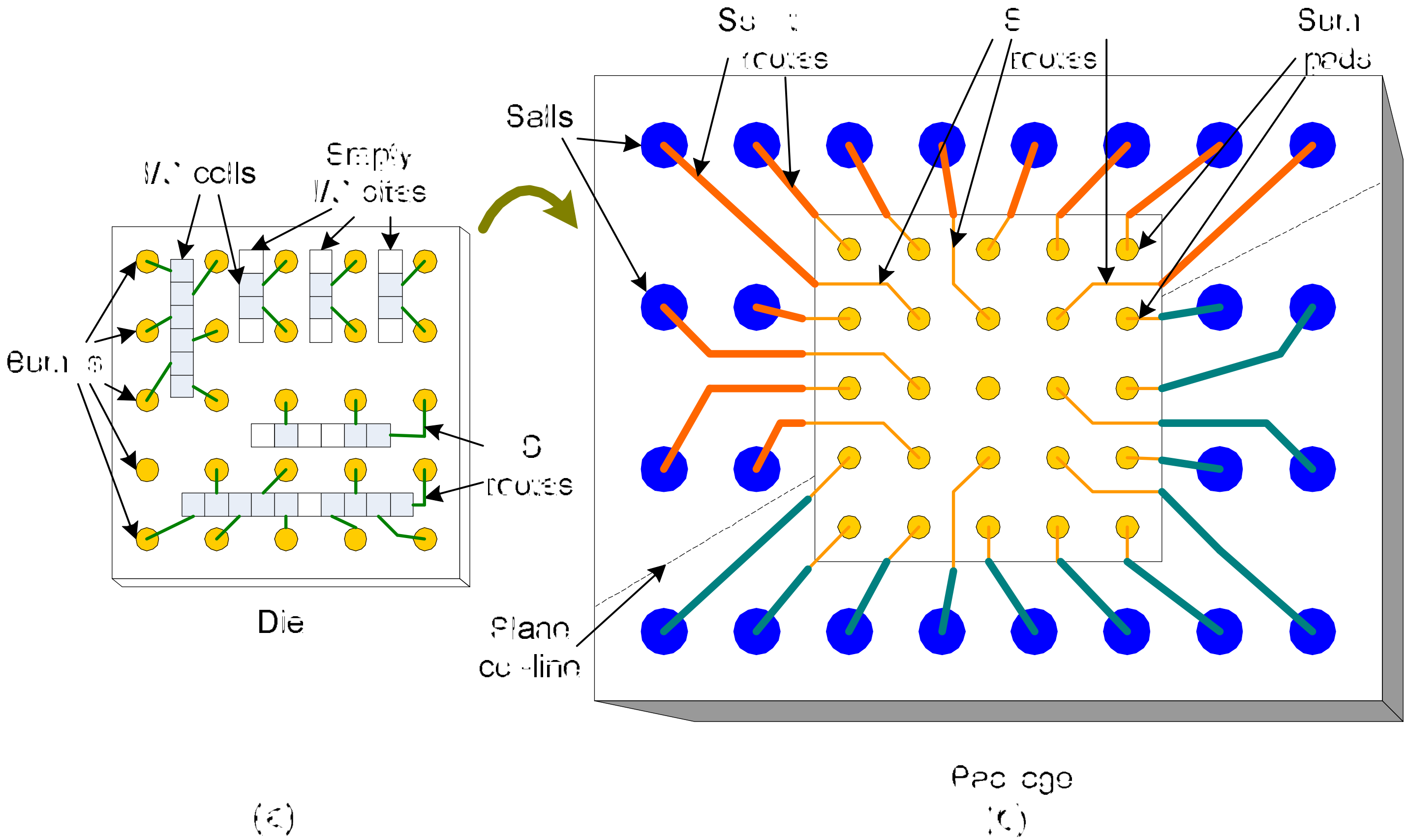
- I/O placement is the key to chip and package co-design

- It faces the following challenges
  - I/O cells placed anywhere on the die
  - Consider the bump locations on the package
  - Timing closure
  - Signal integrity (SI)
  - Power integrity

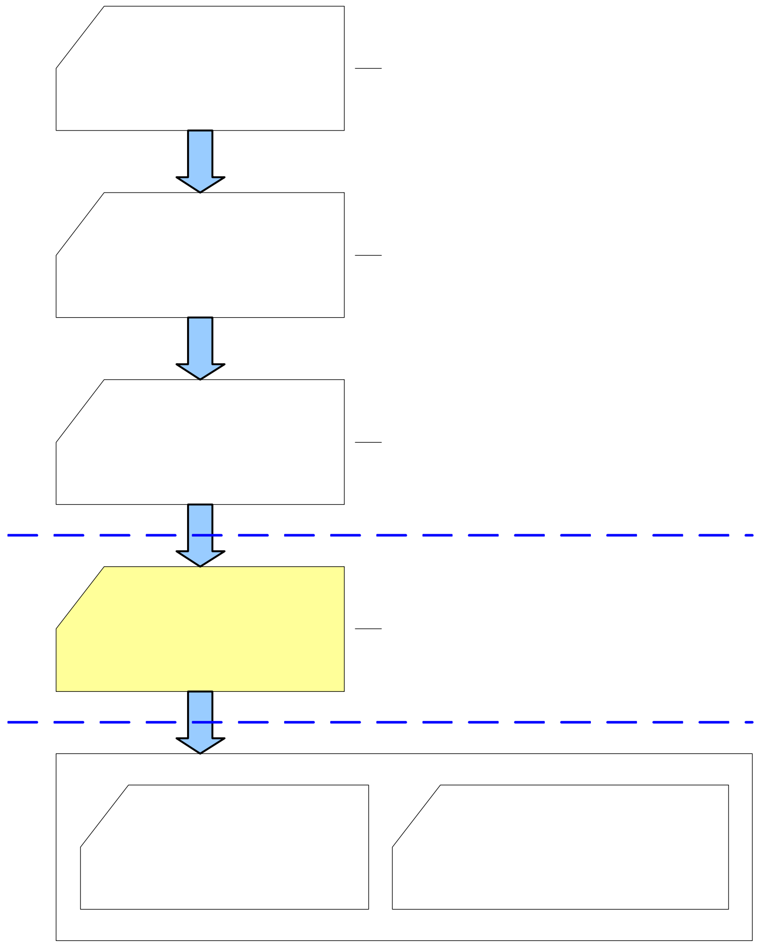
Major Contributions

- A design flow with respect to a set of design constraints
- A new formulation of constraint-driven I/O placement
- An effective multi-step design methodology for chip-package co-design

IO Design Hierarchy



Co-design Methodology



- Global I/O and core co-placement
- Bump array placement
  - Areas for bump pads
- I/O site definition
  - Areas for I/O cells
- Constraint driven detailed I/O placement
- I/O placement consists of three essential sub-problems
  - Placement of bump arrays
  - Placement of I/O sites
  - Placement of I/O cells

Power Integrity Constraints

- Power domain constraint
  - I/O cell voltage specification
  - Cells from same domain prefer physically closer
- Minimize power plane cut lines in the package
  - Provide proper power reference plane for traces
  - Depend on physical locations of I/O cells
- Proper signal-power-ground (SPG) ratio
  - Primary and secondary P/G driver cells
  - Minimize voltage drop and Ldi/dt noise

Timing Constraints

- Substrate routes in package varies significantly
  - Length spans from 1mm to 21mm
  - Timing varies more than 70ps for SSTL_2
- I/O cells with critical timing constraints shall take this into account
  - Differential pair prefer to escape in parallel

I/O Standard Related Constraints

- High-speed design → high-speed I/O
- I/O standard requirements
  - Relative timing requirements on signals
  - Likely to be connected to the same interface at other chips, so prefer to keep relative order to ease routing
- Closeness constraint
- Bump assignment feasibility constraint

Floorplan Induced Region Constraints

- Top-down design flow
  - PCB floorplan
- Bottom-up design
  - Chip floorplan
- I/O cells have region preference
  - Which side?
  - What location?

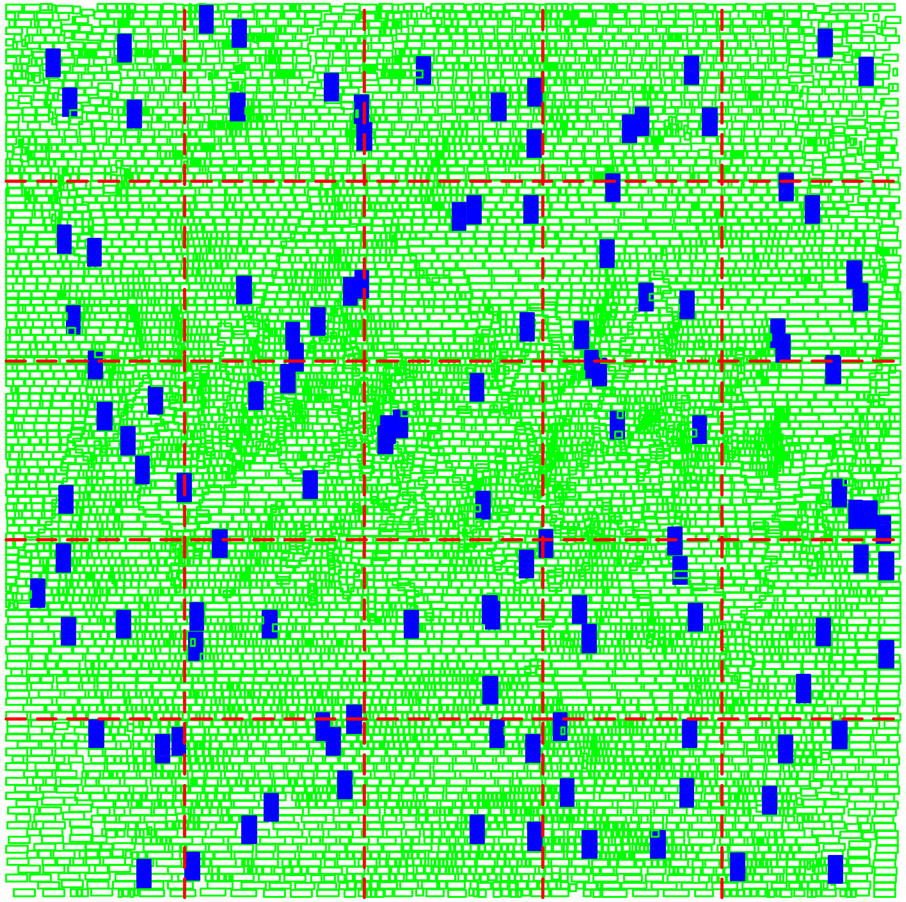
CIOP Problem Formulation

- Given: a fixed die size, a net-list with I/O cells, a set of design constraints
- Find:
  - Placement of bump arrays
  - Placement of I/O site
  - Legal placement of I/O cells
- Such that: all design constraints are satisfied
  - Wire length is also minimized

Agenda

- Motivation
- Overview of our approach
- Chip-package aware design constraints
- CIOP: constraint-driven I/O placement problem formulation
- Multi-step CIOP algorithm
  - Constraint-driven global I/O planning
  - Constraint-driven detailed I/O placement
- Experiment results
- Conclusion

Global I/O and Core Co-placement

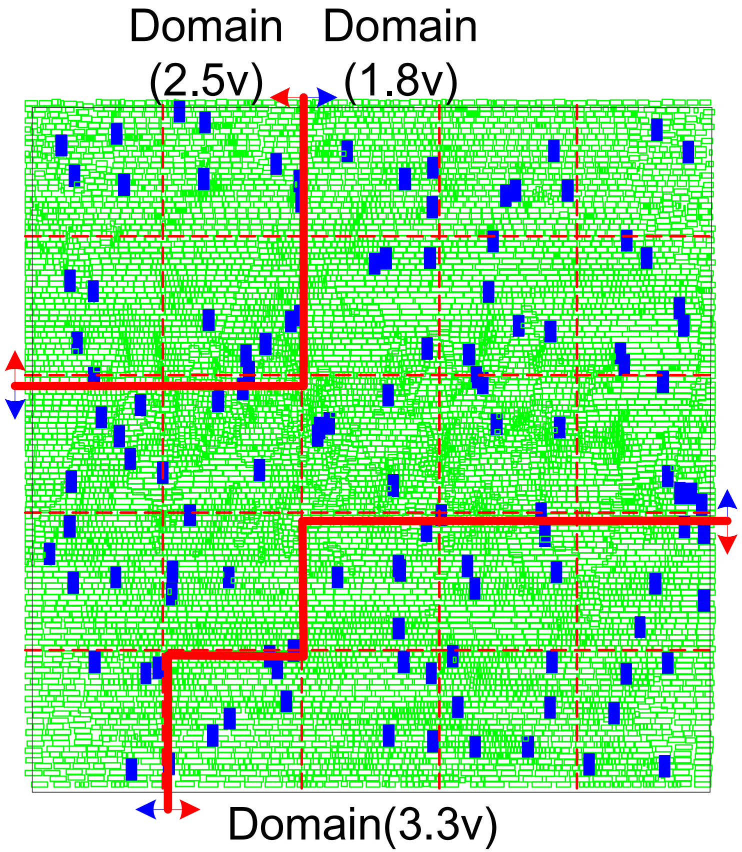


- Wire-length driven
- Constraint driven
  - Minimize power domain slicing on the package planes
- Grid-based
  - Uniformity
- No restriction on a particular global placement engine
  - Force-directed
  - Partition-based
  - Analytic-based

Global I/O and Core Co-placement

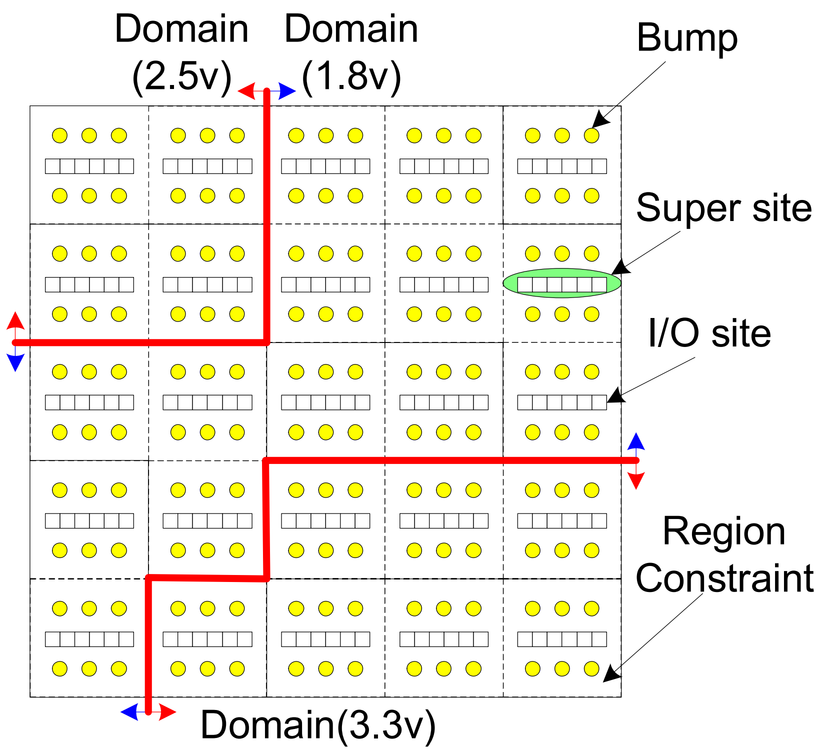
- Additional components to cost function
  - Region constraint: quadratic penalty functions
  - SI constraints and escapability constraints→ bin capacity constraints
    - High level abstraction for efficiency consideration
- Power domain constraints: I/O cells from the same power domain closer to each other
  - Add a virtual net to connect I/O cells belonging to the same domain
  - Each bin is assigned to at most one power domain
    - Decided by the majority I/O cells' power domain property
  - Adjacent bins of the same domain are merged
  - If one power domain is too fragmented, the corresponding virtual net will be given a higher weight in the next placement run

Global I/O and Core Co-placement



- Power domain definition
  - Majority I/O cells location
  - Modeled in global placement
- Translated to region constraints for I/O cells for the following steps

Bump and Site Definition



- Regular bump pattern is preferred
  - Escapability analysis
- Regular I/O site is preferred
  - I/O proximity
  - RDL planar routability analysis
- I/O sites more than I/O cells
  - SPG ratio consideration
  - Flexibility for later bump assignment
- I/O super site: a cluster of I/O sites

Agenda

- Motivation
- Overview of our approach
- Chip-package aware design constraints
- CIOP: constraint-driven I/O placement problem formulation
- Multi-step CIOP algorithm
  - Constraint-driven global I/O planning
  - Constraint-driven detailed I/O placement
- Experiment results
- Conclusion

ILP Feasibility Problem for Super Site Assignment

$$\sum x_{i,j} \le \overline{p_j}, \quad \forall S_j \qquad (2)$$

$$\sum (x_{i0,j} + x_{i1,j}) \le \overline{d_j}, \quad \forall S_j \qquad (3)$$

$$x_{k,j} = 0, \quad \forall c_k \in C_i^R, \forall S_j \notin R_i \qquad (4)$$

$$x_{i0,j} = x_{i1,j}, \quad \forall D_i, \forall S_j \qquad (5)$$

- One I/O cell to one I/O site
- I/O site capacity const
- Differential pair capacity
- Region constr.
- Differential pair const.

ILP Feasibility Problem for Super Site Assignment

$$
\begin{aligned}
l_{i,x}^{min} \le a_j \cdot x_{k,j} + u_R \cdot (1 - x_{k,j}), &\quad \forall c_k \in C_i^L, \forall L_i, \forall S_j \\
a_j \cdot x_{k,j} + u_L \cdot (1 - x_{k,j}) \le l_{i,x}^{max}, &\quad \forall c_k \in C_i^L, \forall L_i, \forall S_j \\
l_{i,x}^{max} - l_{i,x}^{min} \le \overline{l_{i,x}}, &\quad \forall L_i \\
l_{i,y}^{min} \le b_j \cdot x_{k,j} + u_T \cdot (1 - x_{k,j}), &\quad \forall c_k \in C_i^L, \forall L_i, \forall S_j \\
b_j \cdot x_{k,j} + u_B \cdot (1 - x_{k,j}) \le l_{i,y}^{max}, &\quad \forall c_k \in C_i^L, \forall L_i, \forall S_j \\
l_{i,y}^{max} - l_{i,y}^{min} \le \overline{l_{i,y}}, &\quad \forall L_i
\end{aligned}
$$

- Captures clustering constraints (L_i, C_i^L)

Legal Assignment of I/O Cells to I/O Sites

- Solved on a per super site basis
- Min-cost-max-flow problem
  - A bipartite graph G(V1,V2,E)
  - V1: the set of I/O cells assigned to the super site
  - V2: the set of I/O cells within the super site
  - E: the feasible connection between V1 and V2
    - Query bumps escape layer properties
    - Query substrate route characteristics: e.g., impedance, route length
    - Determine whether or not an I/O cell is allowed to be assigned to an I/O site
  - Cost of E: preference in assignment
    - RDL wire length from I/O cells to I/O sites
    - Constraint violation

Experiment Results

Design	# Signal I/O	# Power Domain	# Constraints
d1	1221	4	1801
d2	504	6	814
d3	450	4	934
d4	641	25	1433

- Real industrial designs
- Constraints not include the ones that are generated internally

Experiment Results

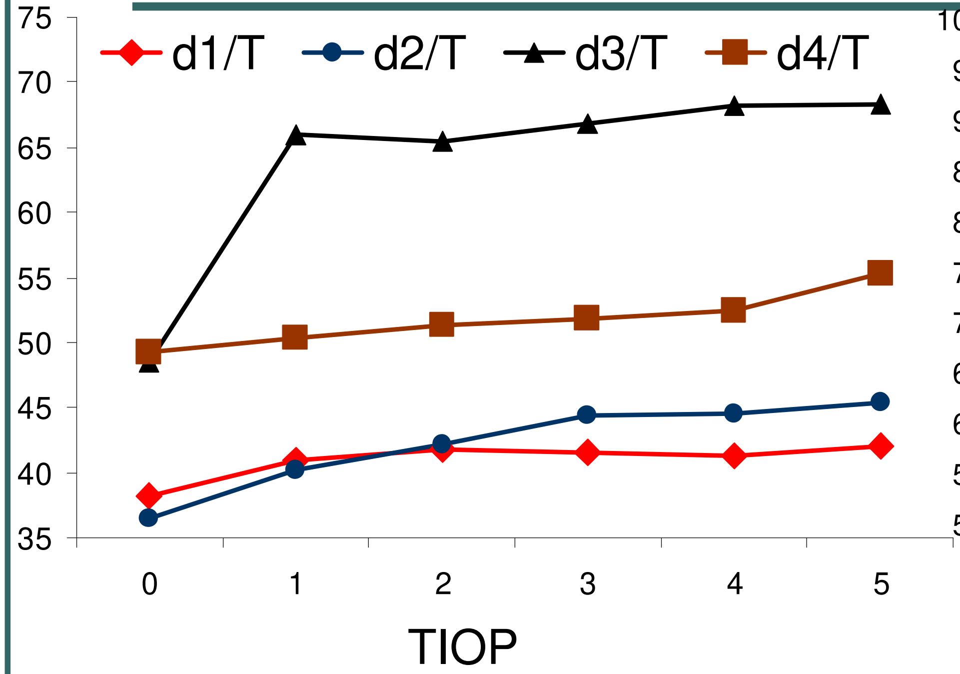
Design	Bumps	Domains	P/G Cells	CSR	Runtime(s)
d1	1560	6	328	100%	538
d2	963	12	445	100%	177
d3	906	6	453	100%	132
d4	1187	71	459	100%	81

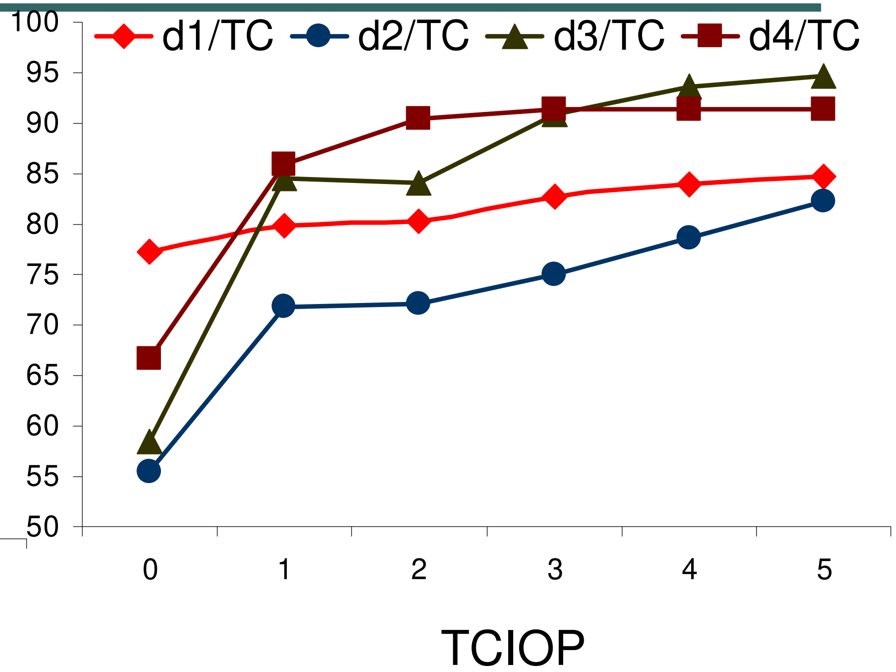
- CSR: Constraint Satisfaction Ratio
- Our algorithm can satisfy all design constraints in one iteration
- Runtime is very promising

Comparison Study

- Two base-line algorithms are studied
  - TIOP: conventional constraint-oblivious approach
  - TCIOP: Constraint-driven global I/O planning + conventional constraint-oblivious I/O placement
  - Both may not satisfy all design constraints in one iteration
- Iterative local refinement procedure follows to further improve CSR
  - Swapping, shifting, relocating

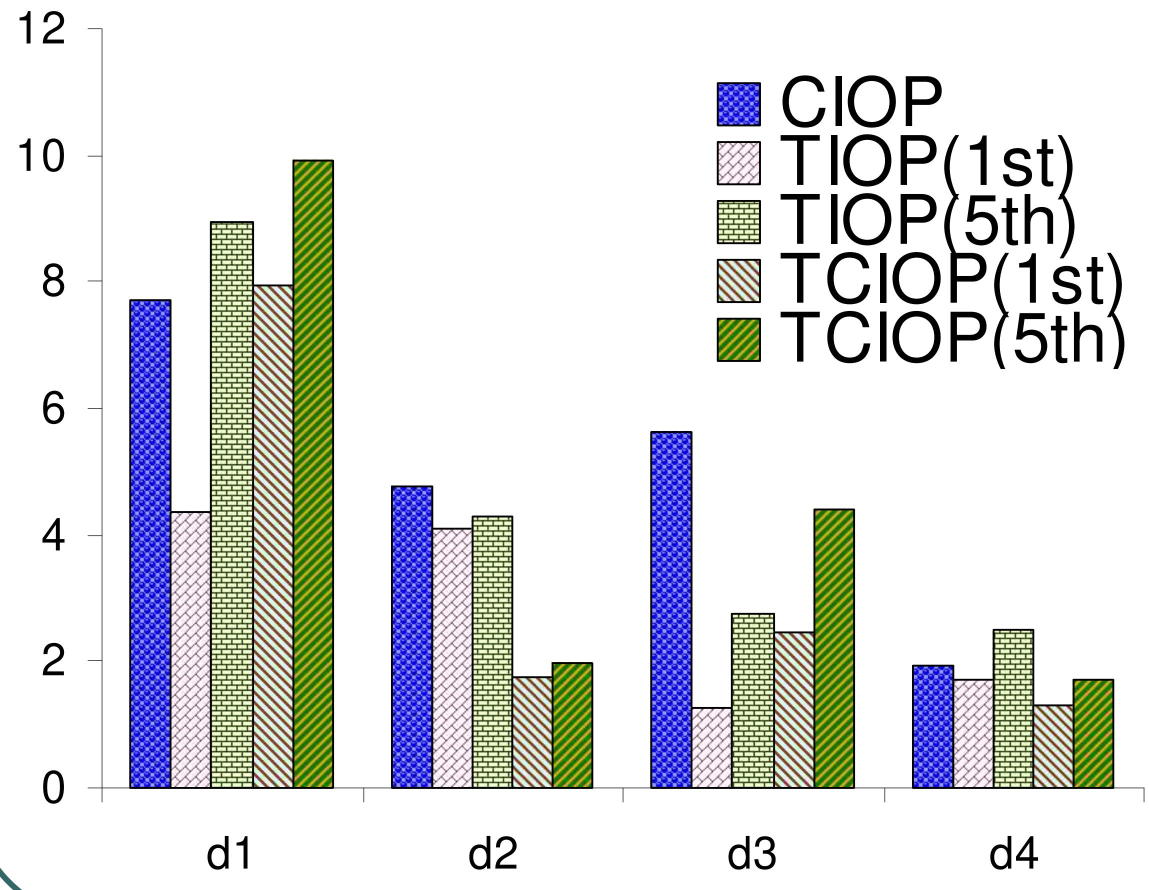
Comparison on CSR





- X-axis: iteration number
- Y-axis: CSR in percentage
- Recall: our CIOP's CSR = 100% using one iteration

Comparison on Wire Length



- Normalize wire length w.r.t. that of TIOP's zeroth iteration
- Wire length increase in percentage

Agenda

- Motivation
- Overview of our approach
- Chip-package aware design constraints
- CIOP: constraint-driven I/O placement problem formulation
- Multi-step CIOP algorithm
- Experiment results
- Conclusion

Conclusion

- Formally defined a set of common design constraints for chip-package co-design
- Formulated a detailed constraint-driven I/O placement problem (CIOP)
- Solved CIOP via an effective multi-step algorithm