Continuity of Thresholded Mode-Switched ODEs and Digital Circuit Delay Models

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ABSTRACT

Thresholded mode-switched ODEs are restricted dynamical systems that switch ODEs depending on digital input signals only, and produce a digital output signal by thresholding some internal signal. Such systems arise in recent digital circuit delay models, where the analog signals within a gate are governed by ODEs that change depending on the digital inputs.

We prove the continuity of the mapping from digital input signals to digital output signals for a large class of thresholded mode-switched ODEs. This continuity property is known to be instrumental for ensuring the faithfulness of the model w.r.t. propagating short pulses. We apply our result to several instances of such digital delay models, thereby proving them to be faithful.

KEYWORDS

mode-switched ordinary differential equations; thresholding operator; continuity; circuit delay models; faithfulness

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1 INTRODUCTION

A natural class of hybrid systems can be described by the dynamics of a continuous process, which is controlled by externally supplied digital mode switch signals, and provides a digital output based on whether some internal signal crosses a threshold, see Fig. 1 for an illustration. Examples are digitally controlled thermodynamic processes, hydrodynamic systems, and, in particular, digital integrated circuits. The continuous dynamics of these systems are described by *Ordinary Differential Equations* (ODEs) for the temperature, the pipe's pressures and fill-levels, or the gate's currents and voltages over time. Digital mode switches are used to switch between ODE systems, e.g., by turning on a heater, closing a valve, or applying an input transition to a gate's input. The environment of the hybrid system is only notified if the temperature or fill-level crosses a threshold, or, in the case of a digital gate, is said to produce an output transition when some internal voltage crosses a threshold.

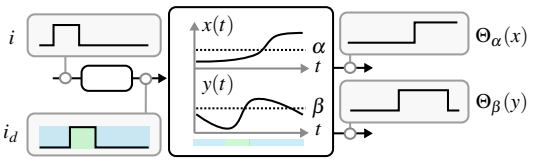

Figure 1: Thresholded mode-switched ODE with a single mode input i, the delayed input i_d, two continuous states x, y, and two thresholded outputs $\Theta_\alpha(x)$ and $\Theta_\beta(y)$.

In this work, we consider the composition of such hybrid systems in a circuit, where digital threshold signals of one component drive mode switch signals of a downstream component. We give conditions that ensure the continuity of the outputs of such circuits with respect to their inputs and provide two application examples in the context of circuit delay models. The proven continuity property shows that small variations of the inputs lead to small variations of the output signal, a property that is necessary for digital circuit models to be consistent with physical analog ODE models.

Digital circuits, continuity, and faithful delay models. Analog simulations of digital circuits are time-consuming and are thus replaced by digital simulations whenever possible. Typical application domains that require simulation of precise circuit transition times are particularly timing-critical, asynchronous parts of a circuit, e.g., inter-neuron links using time-based encoding in hardware-implemented spiking neural networks [2], where the worst-case

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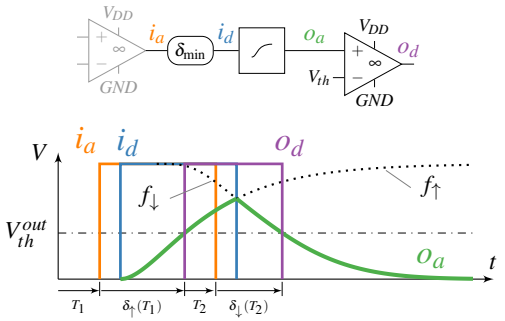


Figure 2: Hybrid involution delay channel model (upper part) with a sample execution (bottom part). Adapted from [8].

delay estimates provided by static timing analysis techniques are not sufficient for ensuring correct operation.

A mandatory prerequisite for dynamic timing analysis are digital delay models, which allow to accurately determine the input-to-output delay of every constituent gate in a circuit. Suitable models must also account for the fact that the delay of an individual signal transition usually depends on the previous transition(s), in particular, when they were close. The simplest class of such models are *single-history delay models* [1, 7, 8], where the input-to-output delay $\delta(T)$ of a gate depends on the previous-output-to-input delay T.

It has been proved by Függer et al. [8] that a certain continuity property of single-history models is mandatory for the digital abstraction to faithfully model the analog reality. In particular, the predicted output transitions must not be substantially affected by arbitrarily short input glitches. For example, the constant-low input signal and an arbitrarily short low-high-low pulse must produce arbitrary close gate output signals. So far, the only delay model known to ensure this continuity property is the *involution delay model* (IDM) [8], which consists of zero-time Boolean gates interconnected by single-input single-output involution delay channels. An IDM channel is characterized by a delay function δ, which is a negative involution, i.e., $-\delta(-\delta(T)) = T$. In its generalized version, different delay functions $\delta_\uparrow$ resp. $\delta_\downarrow$ are assumed for rising resp. falling transitions, requiring $-\delta_\uparrow(-\delta_\downarrow(T)) = T$. Unlike all other existing delay models, the IDM has been proved to faithfully model glitch propagation for the so-called short-pulse filtration problem [8], and is hence the only candidate for a faithful delay model known so far [7].

It has also been shown [8] that involution delay functions arise naturally in a 2-state thresholded hybrid channel model, which consists of a pure delay component, a slew-rate limiter with a rising and falling switching waveform, and an ideal comparator (Fig. 2): The binary-valued input i_a is delayed by $\delta_{\min} > 0$, which assures causality of channels, i.e., $\delta_{\uparrow/\downarrow}(0) > 0$. For every transition on i_d, the generalized slew-rate limiter switches to the corresponding waveform ($f_\downarrow/f_\uparrow$ for a falling/rising transition). The essential property here is that the analog output voltage o_a is a *continuous* (but not necessarily smooth) function of time. Finally, the comparator generates the output o_d by digitizing o_a w.r.t. the discretization threshold voltage V_{th}.

Whereas the accuracy of IDM predictions for single-input, single-output circuits like inverter chains or clock trees turned out to be very good, this is less so for circuits involving multi-input gates [14]. It has been revealed by Ferdowsi et al. [4] that this is primarily due to the IDM's inherent lack of properly covering output delay variations caused by *multiple input switching* (MIS) in close temporal proximity [3], also known as the *Charlie effect*: compared to the *single input switching* case, output transitions are sped up/slowed down with decreasing transition separation time on different inputs. Single-input, single-output delay channels like IDM cannot exhibit such a behavior.

To capture MIS effects in a 2-input NOR gate, Ferdowsi et al. [4] hence proposed an alternative digital delay model based on a 4-state hybrid gate model. It has been obtained by replacing the 4 transistors in the RC-model of a CMOS NOR gate by ideal zero-time switches, which results in one mode per possible digital state of the inputs $(A, B) \in \{(0,0), (0,1), (1,0), (1,1)\}$. In each mode, the voltage of the the output signal and an internal node are governed by constant-coefficient first order ODEs. When an input signal changes its state, the system switches to the new mode and its corresponding ODEs.

Albeit digitizing this hybrid gate model, using a comparator with a suitable threshold voltage V_{th} as in Fig. 2, leads to a quite accurate digital delay model, it turned out to still fail to capture the MIS delay for a rising output transition. In a follow-up paper [5], Ferdowsi et. al. hence introduced a refined gate delay model, where the switching-on of the pMOS transistors is not instantaneous, but rather governed by a simple time evolution function $\sim 1/t$, inspired by the Shichman-Hodges transistor model [12]. The resulting 4-state hybrid model consists of a single not-constant-coefficient first-order ODE per mode, and has been shown to accurately model MIS effects.

Whereas the experimental evaluation of the modeling accuracy of the hybrid models discussed above shows that they outperform the simple IDM model [14], it is not clear whether they are also *faithful* digital delay models. What would be needed here is a proof that the digital delay models obtained by digitizing hybrid models satisfy the continuity property required for faithfulness.

Contributions. Our paper answers this question in the affirmative. More generally, we prove that any thresholded hybrid model like the one shown in Fig. 1 that satisfies some mild conditions on their ODEs results in a continuous digitized hybrid model. We then show that the above hybrid gate models fall into this category, and that the proven continuity implies faithful short-pulse propagation of any such model. Since the square of a signal is (proportional to) its power, this also implies a continuity property from the input signal power to the output signal power. Consequently, these delay models are indeed promising candidates for the correct and timing+power-accurate simulation of digital circuits. In more detail:

(1) We show that any hybrid model, where mode m is governed by a system of first-order ODEs $\frac{dx}{dt} = f_m(t, x)$, leads to a continuous digital delay model, provided all the f_m are continuous in t and Lipschitz continuous in x, with a common Lipschitz constant for every $t > 0$ and m.
(2) We prove that the parallel composition of finitely many digitized hybrid gates in a circuit result in a unique and Zeno-free execution, under some mild conditions regarding causality. In conjunction with our continuity result, we prove that

the resulting model is faithful w.r.t. solving the canonical short-pulse filtration problem.
(3) We demonstrate that the hybrid gate models proposed in [4, 5] satisfy these properties, and are hence continuous and thus faithful.

Paper organization. In Section 2, we instantiate our general continuity result (Theorem 5). Section 3 presents our main continuity result for hybrid gate models (Theorem 6 and Theorem 7), and Section 4 deals with circuit composition. In Section 5, we provide examples for the hybrid models considered in this work: a simple heater from literature [9], the simple hybrid gate model [4], and the advanced gate model [5]. Some conclusions and directions of future research are provided in Section 6.

2 THRESHOLDED MODE-SWITCHED ODES

In this section, we provide a generic proof that every hybrid model that adheres to some mild conditions on its ODEs leads to a continuous digital delay model. We start with proving continuity in the analog domain and then establish continuity of the digitized signal obtained by feeding a continuous real-valued signal into a threshold voltage comparator. Combining those results will allow us to assert the continuity of digital delay channels like the one shown in Fig. 2.

2.1 Continuity of ODE mode switching

For a vector $x \in \mathbb{R}^n$, denote by $\|x\|$ its Euclidean norm. For a piecewise continuous function $f : [a, b] \to \mathbb{R}^n$, we write $\|f\|_1 = \int_a^b \|f(t)\|\, dt$ for its 1-norm and $\|f\|_\infty = \sup_{t\in[a,b]} \|f(t)\|$ for its supremum norm. The projection function of a vector in $\mathbb{R}^n$ onto its k^{th} component, for $1 \le k \le n$, is denoted by $\pi_k : \mathbb{R}^n \to \mathbb{R}$.

In this section, we will consider non-autonomous first-order ODEs of the form $\frac{d}{dt}\, x(t) = f(t, x(t))$, where the non-negative $t \in \mathbb{R}_+$ represents the time parameter, $x(t) \in U$ for some arbitrary open set $U \subseteq \mathbb{R}^n$, $x_0 \in U$ is some initial value, and $f : \mathbb{R}_+ \times U \to \mathbb{R}^n$ is chosen from a set F of bounded functions that are continuous for $(t, x) \in [0, T] \times U$, where $0 < T < \infty$, and Lipschitz continuous in U with a common Lipschitz constant for all $t \in [0, T]$ and all choices of $f \in F$. It is well-known that every such ODE has a unique solution $x(t)$ with $x(0) = x_0$ that satisfies $x(t) \in U$ for $t \in [0, T]$, is continuous in $[0, T]$, and differentiable in $(0, T)$.

The following lemma shows the continuous dependence of the solutions of such ODEs on their initial values. To be more explicit, the exponential dependence of the Lipschitz constant on the time parameter allows temporal composition of the bound. The proof can be found in standard textbooks on ODEs [13, Theorem 2.8].

Lemma 1. *Let $U \subseteq \mathbb{R}^n$ be an open set and let $f : \mathbb{R} \times U \to \mathbb{R}^n$ be Lipschitz continuous with Lipschitz constant K for $t \in [0, T]$ with $T > 0$, and let $x, y : [0, T] \to U$ be continuous functions that are differentiable on $(0, T)$ such that $\frac{d}{dt}\, x(t) = f(t, x(t))$ and $\frac{d}{dt}\, y(t) = f(t, y(t))$ for all $t \in (0, T)$. Then, $\|x(t) - y(t)\| \le e^{tK}\|x(0) - y(0)\|$ for all $t \in [0, T]$.*

A *step function* $s : \mathbb{R}_+ \to \{0, 1\}$ is a right-continuous function with left limits, i.e., $\lim_{t\to t_0^+} s(t) = s(t_0)$ and $\lim_{t\to t_0^-} s(t)$ exists for all $t_0 \in \mathbb{R}_+$. A *binary signal* s is a step function $s : [0, T] \to \{0, 1\}$, a *mode-switch signal* a is a step function $a : [0, T] \to F$, $t \mapsto a_t$.

Given a mode-switch signal a, a *matching output signal* for a is a function $x_a : [0, T] \to U$ that satisfies

(i) $x_a(0) = x_0$,
(ii) the function x_a is continuous,
(iii) for all $t \in (0, T)$, if a is continuous at t, then x_a is differentiable at t and $\frac{d}{dt}\, x_a(t) = a_t(t, x_a(t))$.

For (iii), recall that the domain of a is F.

Lemma 2.1 (Existence and uniqueness of matching output signal). *Given a mode-switch signal a, the matching output signal x_a for a exists and is unique.*

Proof. x_a can be constructed inductively, by pasting together the solutions x_{t_j} of $\frac{d}{dt}\, x_{t_j}(t) = a_{t_j}(t, x_{t_j}(t))$, where $t_0 = 0$ and $t_1 < t_2 < \dots$ are a's switching times in S_a: For the induction basis $j = 0$, we define $x_a(t) := x_{t_0}(t)$ with initial value $x_{t_0} = x_{t_0}(t_0) := x_0$ for $t \in [0, t_1]$. Obviously, (i) holds by construction, and the continuity and differentiability of $x_{t_0}(t)$ at other times ensures (ii) and (iii).

For the induction step $j \to j + 1$, we assume that we have constructed $x_a(t)$ already for $0 \le t \le t_j$. For $t \in [t_j, t_{j+1}]$, we define $x_a(t) := x_{t_{j+1}}(t)$ with initial value $x_{t_{j+1}} = x_{t_{j+1}} := x_a(t_j) = x_{t_j}(t_j)$. Continuity of $x_a(t)$ at $t = t_j$ follows by construction, and the continuity and differentiability of $x_{t_{j+1}}(t)$ again ensures (ii) and (iii). □

Given two mode-switch signals a, b, we define their distance as

$$d_T(a, b) = \lambda\big(\{t \in [0, T] \mid a_t \ne b_t\}\big) \tag{1}$$

where λ is the Lebesgue measure on $\mathbb{R}$. The distance function d_T is a metric on the set of mode-switch signals.

The following Theorem 2 shows that the mapping $a \mapsto x_a$ is continuous.

Theorem 2. *Let $K \ge 1$ be a common Lipschitz constant for all functions in F and let M be a real number such that $\|f(t, x(t))\| \le M$ for all $f \in F$, all $x \in U$, and all $t \in [0, T]$. Then, for all mode-switch signals a and b, if x_a is the output signal for a and x_b is the output signal for b, then $\|x_a - x_b\|_\infty \le 2Me^{TK} d_T(a, b)$. Consequently, the mapping $a \mapsto x_a$ is continuous.*

Proof. Let $S = \{t \in (0, T) \mid a \text{ or } b \text{ is discontinuous at } t\} \cup \{0, T\}$ be the set of switching times of a and b. The set S must be finite, since both a and b are right-continuous on a compact interval. Let $0 = s_0 < s_1 < s_2 < \cdots < s_m = T$ be the increasing enumeration of S.

We show by induction on k that

$$\forall t \in [0, s_k]: \quad \|x_a(t) - x_b(t)\| \le 2Me^{tK} d_t(a, b) \tag{2}$$

for all $k \in \{0, 1, 2, \dots, m\}$. The base case $k = 0$ is trivial. For the induction step $k \mapsto k + 1$, we distinguish the two cases $a_{s_k} = b_{s_k}$ and $a_{s_k} \ne b_{s_k}$.

If $a_{s_k} = b_{s_k}$, then we have $a_t = b_t$ for all $t \in [s_k, s_{k+1})$ and hence $d_t(a, b) = d_{s_k}(a, b)$ for all $t \in [s_k, s_{k+1}]$. Moreover, we can apply Lemma 1 and obtain

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_a(t) - x_b(t)\| \le e^{(t-s_k)K} \|x_a(s_k) - x_b(s_k)\| \ . \tag{3}$$

Plugging in (2) for $t = s_k$ reveals that (2) holds for all $t \in [s_k, s_{k+1}]$ as well.

If $a_{s_k} \neq b_{s_k}$, then x_a and x_b follow different differential equations in the interval $t \in [s_k, s_{k+1}]$. We can, however, use the mean-value theorem for vector-valued functions [11, Theorem 5.19] to obtain

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_a(t) - x_a(s_k)\| \leq M(t - s_k) \text{ and} \tag{4}$$

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_b(t) - x_b(s_k)\| \leq M(t - s_k). \tag{5}$$

This, combined with the induction hypothesis, the equality $d_t(a,b) = d_{s_k}(a,b) + (t - s_k)$, and the inequalities $1 \leq e^{tK}$ and $e^{s_k K} \leq e^{tK}$, implies

$$\begin{aligned}
\|x_a(t) - x_b(t)\| &\leq \|x_a(t) - x_a(s_k)\| \\
&\quad + \|x_a(s_k) - x_b(s_k)\| + \|x_b(s_k) - x_b(t)\| \\
&\leq 2M(t - s_k) + 2Me^{s_k K} d_{s_k}(a,b) \\
&\leq 2Me^{tK}(t - s_k) + 2Me^{tK} d_{s_k}(a,b) \\
&= 2Me^{tK}\big(d_t(a,b) - d_{s_k}(a,b)\big) + 2Me^{tK} d_{s_k}(a,b) \\
&= 2Me^{tK} d_t(a,b)
\end{aligned}$$

for all $t \in [s_k, s_{k+1}]$. This concludes the proof. □

We conclude this section with the remark that the (proof of the) continuity property of Theorem 2 is very different from the standard (proof of the) continuity property of controlled variables in closed thresholded hybrid systems. Mode switches in such systems are caused by the time evolution of the system itself, e.g., when some controlled variable exceeds some value. Consequently, such systems can be described by means of a *single* ODE system with discontinuous righthand side [6].

By contrast, in our hybrid systems, the mode switches are solely caused by changes of digital inputs that are *externally* controlled: For every possible pattern of the digital inputs, there is a dedicated ODE system that controls the analog output. Consequently, the time evolution of the output now also depends on the time evolution of the inputs. Proving the continuity of the (discretized) output w.r.t. different (but close, w.r.t. some metric) digital input signals requires relating the output of *different* ODE systems.

2.2 Continuity of thresholding

For a real number $\xi \in \mathbb{R}$ and a function $x : [a,b] \to \mathbb{R}$, denote by $\Theta_\xi(x)$ the thresholded version of x defined by

$$\Theta_\xi(x) : [a,b] \to \{0,1\}, \quad \Theta_\xi(x)(t) = \begin{cases} 0 & \text{if } x(t) \leq \xi, \\ 1 & \text{if } x(t) > \xi. \end{cases} \tag{6}$$

Lemma 3. *Let $\xi \in \mathbb{R}$ and let $x : [a,b] \to \mathbb{R}$ be a continuous strictly monotonic function with $x(b) = \xi$. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that, for every continuous function $y : [a,b] \to \mathbb{R}$, the condition $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$.*

Proof. We show the lemma for the case that x is strictly increasing. The proof for strictly decreasing x is analogous.

Set $\chi = x(a)$. Since x is bijective onto the interval $[\chi, \xi]$, it has an inverse function $x^{-1} : [\chi, \xi] \to [a,b]$. The inverse function x^{-1} is continuous because the domain $[a,b]$ is compact [11, Theorem 4.17].

The relation $t \leq x^{-1}(\xi - \delta)$ implies $x(t) + \delta \leq \xi$. Hence, if $\|x - y\|_\infty < \delta$, then $y(t) \leq x(t) + \delta \leq \xi$ for all $t \leq x^{-1}(\xi - \delta)$. This means that $\Theta_\xi(y)(t) = 0$ for all $t \leq x^{-1}(\xi - \delta)$, so $t > x^{-1}(\xi - \delta)$ for every $t \in [a,b]$ where $\Theta_\xi(y)(t) = 1$.

By assumption, we have $\Theta_\xi(x)(t) = 0$ for all $t \in [a,b]$. Thus,

$$\begin{aligned}
\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 &= \lambda\big(\{t \in [0,T] \mid \Theta_\xi(y) = 1\}\big) \\
&= \lambda\big(\{t \in [0,T] \mid y(t) > \xi\}\big) \\
&\leq b - x^{-1}(\xi - \delta).
\end{aligned} \tag{7}$$

Note that continuity of y is sufficient to ensure that the set in Eq. (7) is measurable. Since x^{-1} is continuous, we have $x^{-1}(\xi - \delta) \to x^{-1}(\xi) = b$ as $\delta \to 0$. In particular, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $b - x^{-1}(\xi - \delta) < \varepsilon$. This concludes the proof. □

The following Lemma 4 shows that we can drop the assumption $x(b) = \xi$ in Lemma 3:

Lemma 4. *Let $\xi \in \mathbb{R}$ and let $x, y : [a,b] \to \mathbb{R}$ be two continuous functions where x is strictly monotonic. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$.*

Proof. We again show the lemma for the case that x is strictly increasing. The proof for strictly decreasing x is analogous.

Let $\varepsilon > 0$. We distinguish three cases:

(i) If $x(b) < \xi$, then we have $\Theta_\xi(x)(t) = 0$ for all $t \in [a,b]$. Choosing $\delta = \xi - x(b)$, we deduce $y(t) < x(t) + \delta \leq x(b) + \xi - x(b) = \xi$ for all $t \in [a,b]$ whenever $\|x - y\|_\infty < \delta$. Hence, we get $\Theta_\xi(y)(t) = 0$ for all $t \in [a,b]$ and thus $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = 0 < \varepsilon$.

(ii) If $x(a) > \xi$, then we can choose $\delta = x(a) - \xi$ and get $\Theta_\xi(y)(t) = \Theta_\xi(x)(t) = 1$ for all $t \in [a,b]$ whenever $\|x - y\|_\infty < \delta$. In particular, $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = 0 < \varepsilon$.

(iii) If $x(a) \leq \xi \leq x(b)$, then there exists a unique $c \in [a,b]$ with $x(c) = \xi$. Applying Lemma 3 on the restriction of x on the interval $[a,c]$, we get the existence of a $\delta_1 > 0$ such that $\|x - y\|_{[a,c],\infty} < \delta_1$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,c],1} < \varepsilon/2$; herein, $\|\cdot\|_{[a,c],\infty}$ and $\|\cdot\|_{[a,c],1}$ denote the supremum-norm and the 1-norm on the interval $[a,c]$, respectively. Applying Lemma 3 on the restriction of x on the interval $[c,b]$ after the coordinate transformation $t \mapsto -t$ yields the existence of a $\delta_2 > 0$ such that $\|x - y\|_{[c,b],\infty} < \delta_2$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[c,b],1} < \varepsilon/2$. Setting $\delta = \min\{\delta_1, \delta_2\}$, we thus get $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,b],1} = \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,c],1} + \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[c,b],1} < \varepsilon/2 + \varepsilon/2 = \varepsilon$ whenever $\|x - y\|_{[a,b],\infty} < \delta$. □

The following Theorem 5 shows that the mapping $x \mapsto \Theta_\xi(x)$ is continuous for a given function x, provided that x has only finitely many local optima, i.e., points where $x'(t) = 0$:

Theorem 5. *Let $\xi \in \mathbb{R}$ and let $x, y : [0,T] \to \mathbb{R}$ be two differentiable functions. Assume that x has only finitely many local optima. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$. Consequently, the mapping $x \mapsto \Theta_\xi(x)$ is continuous.*

Proof. Let $\mathcal{N} = \{t \in [0,T] \mid x \text{ has a local optimum at } t\} \cup \{0, T\}$, which is finite by assumption, and $t_0 < t_1 < t_2 < \cdots < t_m$ be the increasing enumeration of $\mathcal{N}$. By the mean-value theorem, the function x is strictly monotonic in every interval $[t_k, t_{k+1}]$ for $k \in \{0, 1, 2, \ldots, m-1\}$.

Let $\varepsilon > 0$. Applying Lemma 4 to the restriction of x on each of the intervals $[t_k, t_{k+1}]$, we get the existence of $\delta_k > 0$ such that $\|x - y\|_{[t_k,t_{k+1}],\infty} < \delta_k$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[t_k,t_{k+1}],1} < \varepsilon/m$ for

each $k \in \{0, 1, 2, \ldots, m-1\}$. Setting $\delta = \min\{\delta_0, \delta_1, \delta_2, \ldots, \delta_{m-1}\}$, we thus obtain

$$\begin{aligned} \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[0,T],1} &= \sum_{k=0}^{m-1} \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[t_k,t_{k+1}],1} \\ &< \sum_{k=0}^{m-1} \varepsilon/m = \varepsilon \end{aligned} \tag{8}$$

whenever $\|x - y\|_{[0,T],\infty} < \delta$. □

3 CONTINUITY OF DIGITIZED HYBRID GATE

To prepare for our general result about the continuity of hybrid gate models, we will first (re)prove the continuity of IDM channels as shown in Fig. 2, which has been established by a quite tedious direct proof in [8]. In our notation, an IDM channel consists of:

- A nonnegative minimum delay $\delta_{\min} \geq 0$ and a delay function $\Delta_{\delta_{\min}}(s)$ that maps the binary input signal i_a, augmented with the left-sided limit $i_a(0-)$ as the *initial value*[1] that can be different from $i_a(0)$, to the binary signal $i_d = \Delta_{\delta_{\min}}(i_a)$, defined by

$$\Delta_{\delta_{\min}}(i_a)(t) = \begin{cases} i_a(0-) & \text{if } t < \delta_{\min} \\ i_a(t - \delta_{\min}) & \text{if } t \geq \delta_{\min} \end{cases}. \tag{9}$$

- An open set $U \subseteq \mathbb{R}^n$, where $\pi_1[U]$ represents the analog output signal and $\pi_k[U]$, $k = \{2, 3, \ldots, n\}$, specifies the internal state variables of the model. In this fashion,[2] we presume that $\pi_1[U] = (0, 1)$, i.e., the range of output signals is contained in the interval $(0, 1)$.
- Two bounded functions $f_\uparrow, f_\downarrow : \mathbb{R} \times U \to \mathbb{R}^n$ with the following properties:
  - $f_\uparrow, f_\downarrow$ are continuous for $(t, x) \in [0, T] \times U$, for any $0 < T < \infty$, and Lipschitz continuous in U, which entails that every trajectory x of the ODEs $\frac{d}{dt}\, x(t) = f_\uparrow(t, x(t))$ and $\frac{d}{dt}\, x(t) = f_\downarrow(t, x(t))$ with any initial value $x(0) \in U$ satisfies $x(t) \in U$ for all $t \in [0, T]$, recall Section 2.1.
  - for no trajectory x of the ODEs $\frac{d}{dt}\, x(t) = f_\uparrow(t, x(t))$ and $\frac{d}{dt}\, x(t) = f_\downarrow(t, x(t))$ with initial value $x(0) \in U$ does $\pi_1 \circ x$ have infinitely many local optima, i.e., critical points with $(\pi_1 \circ x)'(t) = 0$.
- An initial value $x_0 \in U$, with $x_0 = f_\uparrow$ if $i_a(0-) = 1$ and $x_0 = f_\downarrow$ if $i_a(0-) = 0$.
- A mode-switch signal $a : [0, T] \to \{f_\uparrow, f_\downarrow\}$ defined by setting $a(t) = f_\uparrow$ if $i_d(t) = 1$ and $a(t) = f_\downarrow$ if $i_d(t) = 0$.
- The analog output signal $o_a = x_a$, i.e., the output signal for a and initial value x_0.
- A threshold voltage $\xi = V_{th} \in (0, 1)$ for the comparator that finally produces the binary output signal $o_d = \Theta_\xi(o_a)$.

By combining the results from Section 2.1 and 2.2, we obtain:

Theorem 6. *The channel function of an IDM channel, which maps from the input signal i_a to the output signal o_d, is continuous with respect to the* 1*-norm on the interval* $[0, T]$.

[1] In [8], this initial value of a signal was encoded by extending the time domain to the whole $\mathbb{R}$ and using $i_a(-\infty)$.

[2] In real circuits, the interval $(0, 1)$ typically needs to be replaced by $(0, V_{DD})$.

Proof. The mapping from i_a to o_d is continuous as the concatenation of continuous mappings:

- The mapping from $i_a \mapsto i_d$ is continuous since $\Delta_{\delta_{\min}}$ is trivially continuous for input and output binary signals with the 1-norm.
- The mapping $i_d \mapsto a$ is a continuous mapping from the set of signals equipped with the 1-norm to the set of mode-switch signals equipped with the metric d_T, since the points of discontinuity of a are the points where i_d is discontinuous.
- By Theorem 2, the mapping $a \mapsto x_a$ is a continuous mapping from the set of mode-switch signals equipped with the metric d_T to the set of piecewise differentiable functions $[0, T] \to U$ equipped with the supremum-norm.
- The mapping $x_a \mapsto \pi_1 \circ x_a$ is a continuous mapping from the set of piecewise differentiable functions $[0, T] \to U$ equipped with the supremum-norm to the set of piecewise differentiable functions $[0, T] \to (0, 1)$ equipped with the supremum-norm. Since $\|(x_1, \ldots, x_n)\|_1 = \|x_1\|_1 + \cdots + \|x_n\|_1$ for every $x \in U$, this follows from $\|\pi_1(x)\|_1 \leq \|x\|_1$.
- By Theorem 5, the mapping $\pi_1 \circ x_a \mapsto \Theta_\xi(\pi_1 \circ x_a)$ is a continuous mapping from the set of piecewise differentiable functions $[0, T] \to (0, 1)$ equipped with the supremum-norm to the set of binary signals equipped with the 1-norm. □

General digitized hybrid gates have $c \geq 1$ binary input signals $i_a = (i_a^1, \ldots, i_a^c)$, augmented with *initial values* $(i_a^1(0-), \ldots, i_a^c(0-))$, and a single binary output signal o_d, and are specified as follows:

Definition 3.1 (Digitized hybrid gate). A digitized hybrid gate with c inputs consists of:

- c delay functions $\Delta_{\delta_j}(s)$ with $\delta_j \geq 0$, $1 \leq j \leq c$, that map the binary input signal i_a^j with initial value $i_a^j(0-)$ to the binary signal $i_d^j = \Delta_{\delta_j}(i_a^j)$, defined by

$$\Delta_{\delta_j}(i_a^j)(t) = \begin{cases} i_a^j(0-) & \text{if } t < \delta_j \\ i_a^j(t - \delta_j) & \text{if } t \geq \delta_j \end{cases}. \tag{10}$$

- An open set $U \subseteq \mathbb{R}^n$, where $\pi_1[U]$ represents the analog output signal and $\pi_k[U]$, $k = \{2, 3, \ldots, n\}$, specifies the internal state variables of the model.
- A set F of bounded functions $f^\ell : \mathbb{R} \times U \to \mathbb{R}^n$, with the following properties:
  - f^ℓ is continuous for $(t, x) \in [0, T] \times U$, for any $0 < T < \infty$, and Lipschitz continuous in U, with a common Lipschitz constant, which entails that every trajectory x of the ODE $\frac{d}{dt}\, x(t) = f^\ell(t, x(t))$ with any initial value $x(0) \in U$ satisfies $x(t) \in U$ for all $t \in [0, T]$.
  - for no trajectory x of the ODEs $\frac{d}{dt}\, x(t) = f^\ell(t, x(t))$ with initial value $x(0) \in U$ does $\pi_1 \circ x$ have infinitely many local optima, i.e., critical points with $(\pi_1 \circ x)'(t) = 0$.
- A mode-switch signal $a : [0, T] \to F$, which obtained by a continuous choice function a_c acting on $i_d^1(t), \ldots, i_d^c(t)$, i.e., $a(t) = a_c(i_d^1(t), \ldots, i_d^c(t))$.
- An initial value $x_0 \in U$, which must correspond to the mode selected by $a_c(i_a^1(0-), \ldots, i_a^c(0-))$.
- The analog output signal $o_a = x_a$, i.e., the output signal for a and initial value x_0.

- A threshold voltage $\xi = V_{th} \in (0, 1)$ for the comparator that finally produces the binary output signal $o_d = \Theta_\xi(o_a)$.

By essentially the same proof as for Theorem 6, we obtain:

Theorem 7. *The gate function of a digitized hybrid gate with c inputs, which maps from the vector of input signals $i_a = (i_a^1, \ldots, i_a^c)$ to the output signal o_d, is continuous with respect to the* 1*-norm on the interval* $[0, T]$.

4 COMPOSING GATES IN CIRCUITS

In this section, we will first compose digital circuits from digitized hybrid gates and reason about their executions. More specifically, it will turn out that, under certain conditions ensuring the causality of every composed gate, the resulting circuit will exhibit a unique execution, for every given execution of its inputs. This uniqueness is mandatory for building digital dynamic timing simulation tools.

Moreover, we adapt the proof that no circuit with IDM channels can solve the bounded SPF problem utilized in [8] to our setting: Using the continuity result of Theorem 7, we will prove that no circuit with digitized hybrid gates can solve bounded SPF. Since unbounded SPF can be solved with IDM channels, which are simple instances of digitized hybrid gate models, faithfulness follows.

4.1 Executions of circuits

Circuits. Circuits are obtained by interconnecting a set of input ports and a set of output ports, forming the external interface of a circuit, and a finite set of digitized hybrid gates. We constrain the way components are interconnected in a natural way, by requiring that any gate input, channel input and output port is attached to only one input port, gate output or channel output, respectively. Formally, a *circuit* is described by a directed graph where:

C1) A vertex Γ can be either a *circuit input port*, a *circuit output port*, or a digitized hybrid *gate*.
C2) The *edge* (Γ, I, Γ') represents a 0-delay connection from the output of Γ to a fixed input I of Γ'.
C3) Circuit input ports have no incoming edges.
C4) Circuit output ports have exactly one incoming edge and no outgoing one.
C5) A c-ary gate G has a single output and c inputs $I_1, \ldots, I_c$, in a fixed order, fed by incoming edges from exactly one gate output or input port.

Executions. An *execution* of a circuit C is a collection of binary signals s_Γ defined on $[0, \infty)$ for all vertices Γ of C that respects all the gate functions and input port signals. Formally, the following properties must hold:

E1) If i is a circuit input port, there are no restrictions on s_i.
E2) If o is a circuit output port, then $s_o = s_G$, where G is the unique gate output connected to o.
E3) If vertex G is a gate with c inputs $I_1, \ldots, I_c$, ordered according to the fixed order condition C5), and gate function f_G, then $s_G = f_G(s_{\Gamma_1}, \ldots, s_{\Gamma_c})$, where $\Gamma_1, \ldots, \Gamma_c$ are the vertices the inputs $I_1, \ldots, I_c$ of C are connected to via edges $(\Gamma_1, I_1, G), \cdots, (\Gamma_d, I_c, G)$.

The above definition of an execution of a circuit is "existential", in the sense that it only allows checking for a given collection of signals whether it is an execution or not: For every hybrid gate in the circuit, it specifies the gate output signal, given a *fixed* vector of input signals, all defined on the time domain $t \in [0, \infty)$. A priori, this does not give an algorithm to construct executions of circuits, in particular, when they contain feedback loops. Indeed, the parallel composition of general hybrid automata may lead to non-unique executions and bizarre timing behaviors known as *Zeno*, where an infinite number of transitions may occur in finite time [10].

To avoid such behaviors in our setting, we require all discretized hybrid gates in a circuit to be *strictly causal*:

Definition 4.1 (Strict causality). A digitized hybrid gate G with c inputs is strictly causal, if the pure delays δ_j for every $1 \le j \le c$ are positive. Let $\delta^C_{\min} > 0$ be the minimal pure delay of any input of any gate in circuit C.

We proceed with defining input-output causality for gates, which is based on signal transitions. Every binary signal can equivalently be described by a sequence of transitions: A *falling transition* at time t is the pair $(t, 0)$, a *rising transition* at time t is the pair $(t, 1)$.

Definition 4.2 (Input-output causality). The output transition $(t, .) \in s_G$ of a gate G *is caused* by the transition $(t', .) \in s_G^j$ on input I_j of G, if $(t, .)$ occurs in the mode $a_c(i_d^1(t^+), \ldots, i_d^c(t^+))$, where $i_d^j(t^+)$ is the pure-delay shifted input signal at input I_j at the last mode switching time $t^+ \le t$ (see Eq. (10)) and $(t', .)$ is the last transition in s_G^j before or at time $t^+ - \delta_j$, i.e., $\nexists (t'', .) \in s_G^j$ for $t' < t'' \le t^+ - \delta_j$.

We also assume that the output transition $(t, .) \in s_G$ *causally depends* on every transition in s_G^j before or at time $t^+ - \delta_j$.

Strictly causal gates satisfy the following obvious property:

Lemma 4.3. *If some output transition $(t, .) \in s_G$ of a strictly causal digitized hybrid gate G in a circuit C causally depends on its input transition $(t', .) \in s_G^j$, then $t - t' \ge \delta_j$.*

The following Theorem 4.4 shows that every circuit made up of strictly causal gates has a unique execution, defined for $t \in [0, \infty)$.

Theorem 4.4 (Unique execution). *Every circuit C made up of finitely many strictly causal digitized hybrid gates has a unique execution, which either consists of finitely many transitions only or else requires $[0, \infty)$ as its time domain.*

Proof. We will inductively construct this unique execution by a sequence of iterations $\ell \ge 1$ of a simple deterministic simulation algorithm, which determines the prefix of the sought execution up to time t_ℓ. Iteration ℓ deals with transitions occurring at time t_ℓ, starting with $t_1 = 0$. To every transition e generated throughout its iterations, we also assign a *causal depth* $d(e)$ that gives the maximum causal distance to an input port: $d(e) = 0$ if e is a transition at some input port, and $d(e)$ is the maximum of $1 + d(e^j)$, $1 \le j \le c$, for every transition added at the output of a c-ary gate caused by transitions e^j at its inputs.

Induction basis $\ell = 1$: At the beginning of iteration 1, which deals with all transitions occurring at time $t_1 = 0$, all gates are in their initial mode, which is determined by the initial values of their inputs. They are either connected to input ports, in which case $s_i(0-)$ is used, or to the output port of some gate G, in which case

$s_G(0)$ (determined by the initial mode of G) is used. Depending on whether $s_i(0-) = s_i(0)$ or not, there is also an input transition $(0, s_i(0)) \in s_i$ or not. All transitions in the so generated execution prefix $[0, t_1] = [0, 0]$ have a causal depth of 0.

Still, the transitions that have happened by time t_1 may cause additional *potential future transitions*. They are called future transitions, because they occur only after t_1, and potential because they need not occur in the final execution. In particular, if there is an input transition $(0, s_i(0)) \in s_i$, it may cause a mode switch of every gate G that is connected to the input port i. Due to Lemma 4.3, however, such a mode switch, and hence each of the output transitions e that may occur during that new mode (which all are assigned a causal depth $d(e) = 1$), of G can only happen at or after time $t_1 + \delta^C_{\min}$. In addition, the initial mode of any gate G that is not mode switched may also cause output transitions e at arbitrary times $t > 0$, which are assigned a causal depth $d(e) = 0$. Since at most finitely many critical points may exist for every mode's trajectory, it follows that at most *finitely* many such future potential transitions could be generated in each of the finitely many gates in the circuit. Let $t_2 > t_1$ denote the time of the closest transition among all input port transitions and all the potential future transitions just introduced.

Induction step $\ell \to \ell + 1$: Assume that the execution prefix for $[0, t_\ell]$ has already been constructed in iterations $1, \ldots, \ell$, with at most finitely many potential future transitions occurring after t_ℓ. If the latter set is empty, then the execution of the circuit has already been determined completely. Otherwise, let $t_{\ell+1} > t_\ell$ be the closest future transition time.

During iteration $\ell + 1$, all transitions occurring at time $t_{\ell+1}$ are dealt with, exactly as in the base case: Any transition e, with causal depth $d(e)$, happening at $t_{\ell+1}$ at a gate output or at some input port may cause a mode switch of every gate G that is connected to it. Due to Lemma 4.3, such a mode switch, and hence each of the at most finitely many output transitions e' occurring during that new mode (which all are assigned a causal depth $d(e') = d(e) + 1$), of G can only happen at or after time $t_{\ell+1} + \delta^C_{\min}$. In addition, the at most finitely many potential future transitions w.r.t. t_ℓ of all gates that have not been mode-switched and actually occur at times greater than $t_{\ell+1}$ are retained, along with their assigned causal depth, as potential future transitions w.r.t. $t_{\ell+1}$. Overall, we again end up with at most finitely many potential future transitions, which completes the induction step.

To complete our proof, we only need to argue that $\lim_{\ell\to\infty} t_\ell = \infty$ for the case where the iterations do not stop at some finite ℓ. This follows immediately from the fact that, for every $k \geq 1$, there must be some iteration $\ell \geq 1$ such that $t_\ell \geq k\delta^C_{\min}$. If this was not the case, there must be some iteration after which no further mode switch of any gate takes place. This would cause the set of potential future transitions to shrink in every subsequent iteration, however, and thus the simulation algorithm to stop, which provides the required contradiction. □

From the execution construction, we also immediately get:

Lemma 4.5. *For all $\ell \geq 1$, (a) the simulation algorithm never assigns a causal depth larger than ℓ to a transition generated in iteration ℓ, and (b) at the end of iteration ℓ the sequence of causal depths of transitions in s_Γ for $t \in [0, t_\ell]$ is nondecreasing for all components Γ.*

4.2 Impossibility of short-pulse filtration

The results of the previous subsection allow us to adapt the impossibility proof of [8] to our setting. We start with the the definition of the SPF problem:

Short-Pulse Filtration. A signal *contains a pulse* of length Δ at time T_0, if it contains a rising transition at time T_0, a falling transition at time $T_0 + \Delta$, and no transition in between. The *zero signal* has the initial value 0 and does not contain any transition. A circuit *solves Short-Pulse Filtration (SPF)*, if it fulfills all of:

- F1) The circuit has exactly one input port and exactly one output port. *(Well-formedness)*
- F2) If the input signal is the zero signal, then so is the output signal. *(No generation)*
- F3) There exists an input pulse such that the output signal is not the zero signal. *(Nontriviality)*
- F4) There exists an $\varepsilon > 0$ such that for every input pulse the output signal never contains a pulse of length less than or equal to ε. *(No short pulses)*

We allow the circuit to behave arbitrarily if the input signal is not a single pulse or the zero signal.

A circuit *solves bounded SPF* if additionally:

- F5) There exists a $K > 0$ such that for every input pulse the last output transition is before time $T_0 + \Delta + K$, where T_0 is the time of the first input transition. *(Bounded stabilization time)*

A circuit is called a *forward circuit* if its graph is acyclic. Forward circuits are exactly those circuits that do not contain feedback loops. Equipped with the continuity of digitized hybrid gates and the fact that the composition of continuous functions is continuous, it is not too difficult to prove that the inherently discontinuous SPF problem cannot be solved with forward circuits.

Theorem 4.6. *No forward circuit solves bounded SPF.*

Proof. Suppose that there exists a forward circuit that solves bounded SPF with stabilization time bound K. Denote by s_Δ its output signal when feeding it a Δ-pulse at time 0 as the input. Because s_Δ in forward circuits is a finite composition of continuous functions by Theorem 7, $\|s_\Delta\|_{[0,T],1}$ depends continuously on Δ, for any T.

By the nontriviality condition (F3) of the SPF problem, there exists some Δ_0 such that s_{Δ_0} is not the zero signal. Set $T = 2\Delta_0 + K$.

Let $\varepsilon > 0$ be smaller than both Δ_0 and $\|s_{\Delta_0}\|_{[0,T],1}$. We show a contradiction by finding some Δ such that s_Δ either contains a pulse of length less than ε (contradiction to the no short pulses condition (F4)) or contains a transition after time $\Delta + K$ (contradicting the bounded stabilization time condition (F5)).

Since $\|s_\Delta\|_{[0,T],1} \to 0$ as $\Delta \to 0$ by the no generation condition (F2) of SPF, there exists a $\Delta_1 < \Delta_0$ such that $\|s_{\Delta_1}\|_{[0,T],1} = \varepsilon$ by the intermediate value property of continuity. By the bounded stabilization time condition (F5), there are no transitions in s_{Δ_1} after time $\Delta_1 + K$. Hence, s_{Δ_1} is 0 after this time because otherwise it is 1 for the remaining duration $T - (\Delta_1 + K) > \Delta_0 > \varepsilon$, which would mean that $\|s_{\Delta_1}\|_{[0,T],1} > \varepsilon$. Consequently, there exists a pulse in s_{Δ_1} before time $\Delta_1 + K$. But any such pulse is of length at most ε because

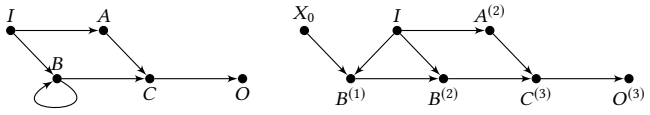


Figure 3: Circuit C (left) and $C_3(O)$ (right) under the assumption that the gate B has initial value 0. It is $z(X_0) = 0$, $z(I) = z(A^{(2)}) = \infty$, $z(B^{(1)}) = 1$, $z(B^{(2)}) = 2$, $z(C^{(3)}) = 3$, and $z(O^{(3)}) = 3$.

$\|s_{\Delta_1}\|_{[0,\Delta_1+K],1} \leq \|s_{\Delta_1}\|_{[0,T],1} = \varepsilon$. This is a contradiction to the no short pulses condition (F4). □

We next show how to simulate (part of) an execution of an arbitrary circuit C by a forward circuit C' generated from C by the unrolling of feedback loops. Intuitively, the deeper the unrolling, the longer the time C' behaves as C.

Definition 4.7. Let C be a circuit, V a vertex of C, and $k \geq 0$. We define the *k-unrolling of C from V*, denoted by $C_k(V)$, to be a directed acyclic graph with a single sink, constructed as follows:

The unrolling $C_k(I)$ from input port I is just a copy of that input port. The unrolling $C_k(O)$ from output port O with incoming channel C and predecessor V comprises a copy of the output port $O^{(k)}$ and the unrolled circuit $C_k(V)$ with its sink connected to $O^{(k)}$ by an edge.

The 0-unrolling $C_0(B)$ from hybrid gate B is a trivial Boolean gate X_v without inputs and the constant output value v equal to B's initial digitized output value. For $k > 0$, the k-unrolling $C_k(B)$ from gate B comprises an exact copy of that gate $B^{(k)}$. Additionally, for every incoming edge of B from V in C, it contains the circuit $C_{k-1}(V)$ with its sink connected to $B^{(k)}$. Note that all copies of the same input port are considered to be the same.

To each component Γ in $C_k(V)$, we assign a value $z(\Gamma) \in \mathbb{N}_0 \cup \{\infty\}$ as follows: $z(\Gamma) = \infty$ if Γ has no predecessor (in particular, is an input port) and $\Gamma \notin \{X_0, X_1\}$. Moreover, $z(X_0) = z(X_1) = 0$, $z(V) = z(U)$ if V is an output port connected by an edge to U, and $z(B) = \min_{c \in E^B}\{1 + z(c)\}$ if B is a gate with its inputs connected to the components in the set E^B. Fig. 3 shows an example of a circuit and an unrolled circuit with its z values.

Noting that, for every component Γ in $C_k(V)$, $z(\Gamma)$ is the number of gates on the shortest path from an X_v node to Γ, or $z(\Gamma) = \infty$ if no such path exists, we immediately get:

Lemma 4.8. *The z-value assigned to the sink vertex $V^{(k)}$ of a k-unrolling $C_k(V)$ of C from V satisfies $z(V^{(k)}) \geq k$.*

Recalling the causal depths assigned to transitions during the execution construction in Theorem 4.4, we are now in the position to prove the result for a circuit simulated by an unrolled circuit.

Theorem 4.9. *Let C be a circuit with input port I and output port O that solves bounded SPF. Let $C_k(O)$ be an unrolling of C, Γ a component in C, and Γ' a copy of Γ in $C_k(O)$. For all input signals s_I on I, if a transition e is generated for Γ by the execution construction algorithm run on circuit C with input signal s_I and $d(e) \leq z(\Gamma')$, then e is also generated for Γ' by the algorithm run on circuit $C_k(O)$ with input signal s_I; and vice versa.*

Proof. Assume that e is the first transition violating the theorem. The input signal is the same for both circuits, and the initial digitized values of gates in C and both their copies in $C_k(O)$ and the X_v gates resulting from their 0-unrolling are equal as well. Hence, e cannot be any such transition (added in iteration 1 only).

If e was added to the output of a gate B in either circuit, the transition e' resp. e'' at one of its inputs that caused e in C resp. $C_k(V)$ must have been different. These transitions e' resp. e'' must come from the output of some other gate B_1, and causally precede e. Hence, by Definition 4.2, $d(e) = d(e') + 1$, and by Lemma 4.5, $d(e) \geq d(e'')$. Also by definition, $z(B) = z(B_1) + 1$ in $C_k(O)$. Since $d(e) \leq z(B)$ by assumption, we find $d(e') \leq z(B_1)$ and $d(e'') \leq z(B)$, so applying our theorem to e' and e'' yields a contradiction to e being the first violating transition. □

We can finally prove that bounded SPF is not solvable, even with non-forward circuits.

Theorem 4.10. *No circuit solves bounded SPF.*

Proof. We first note that the impossibility of bounded SPF also implies the impossibility of bounded SPF when restricting pulse lengths to be at most some $\Delta_0 > 0$.

Since all transitions generated in the execution construction Theorem 4.4 up to any bounded time t_ℓ have bounded causal depth, let ζ be an upper bound on the causal depth of transitions up to the SPF stabilization time bound $\Delta_0 + K$. Then, by Theorem 4.9 and Lemma 4.8, the ζ-unrolled circuit $C_\zeta(O)$ has the same output transitions as the original circuit C up to time $\Delta_0 + K$, and hence, by definition of bounded SPF, the same transitions for all times. But since $C_\zeta(O)$ is a forward circuit, it cannot solve bounded SPF by Theorem 4.6, i.e., neither can C. □

5 APPLICATIONS

We next discuss three examples of thresholded mode-switched ODE systems. For all non-closed systems, the proven continuity shows that similar digital inputs lead to similar digital outputs.

We start with an introductory example from control theory, the bang-bang heating controller for thermodynamic systems. Following [9], let $x(t)$ be the system's temperature at time t and $h(t)$ be the mode of the binary heating signal that can be off (0) or on (1). With a pure delay $\delta > 0$ for the heating to take effect, we assume that the heat flow is described as

$$\dot{x} = \begin{cases} -0.1x(t) & \text{if } h(t-\delta) = 0 \\ 5 - 0.1x(t) & \text{if } h(t-\delta) = 1 \end{cases} \tag{11}$$

for the heating being off or on, respectively: the temperature falls to 0 in the former case and approaches 50 degrees in the latter.

The heating signal is controlled by a bang-bang controller (with hysteresis) with two threshold temperatures, 19 and 20 degrees. It could be implemented by an ideal SR-latch, with pure delay δ, where the Set port (S) is driven by the inverted $\neg\Theta_{19}(x)$, the reset port (R) is driven by $\Theta_{21}(x)$, and the output of the latch controlling the heating mode signal h.

In fact, digital circuits are a particularly rich and interesting source of application examples in general. We will demonstrate this by means of two hybrid gate models for a CMOS NOR gate (see Fig. 4 for the schematics), namely, the simple model proposed in [4] (as

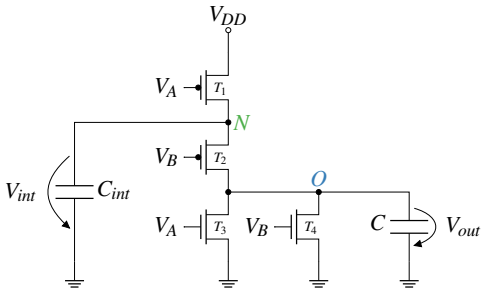


Figure 4: Transistor level implementation of the NOR gate.

an instance of an autonomous ODE model) and the advanced model presented in [5] (as an instance of a non-autonomous ODE model). The SR-latch from the previous example can be implemented via two cross-coupled NOR gates.

5.1 Simple Hybrid Model

The *simple hybrid gate model* proposed in [4] replaces all transistors in Fig. 4 by ideal zero-time switches, which are switched on and off at the relevant input threshold voltage $V_{th} = V_{DD}/2$ crossing times. More precisely, depending on whether the corresponding input is 1 or 0, every pMOS transistor is removed ($R = \infty$) resp. replaced by a fixed resistor $R < \infty$, and vice versa for an nMOS transistor. This leads to the following system of coupled autonomous first-order ODEs governing the analog trajectories of the gate's output in the respective mode:

- System $(1,1)$: $V_A = 1$, $V_B = 1$: If inputs A and B are 1, both nMOS transistors are conducting and thus replaced by resistors, causing the output O to be discharged in parallel. By contrast, N is completely isolated and keeps its value. This leads to the following ODEs:

$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} f_1(V_{int}(t), V_{out}(t)) \\ f_2(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} 0 \\ -\left(\frac{1}{CR_3} + \frac{1}{CR_4}\right) V_{out}(t) \end{pmatrix}$$

- System $(1,0)$: $V_A = 1$, $V_B = 0$: Since T_1 and T_4 are open, node N is connected to O, and O to *GND*. Both capacitors have to be discharged over resistor R_3, resulting in less current that is available for discharging C. One obtains:

$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} f_3(V_{int}(t), V_{out}(t)) \\ f_4(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\frac{V_{int}(t)}{C_{int}R_2} + \frac{V_{out}(t)}{C_{int}R_2} \\ \frac{V_{int}(t)}{CR_2} - \left(\frac{1}{CR_2} + \frac{1}{CR_3}\right) V_{out}(t) \end{pmatrix}$$

- System $(0,1)$: $V_A = 0$, $V_B = 1$: Opening transistors T_2 and T_3 again decouples the nodes N and O. We thus get

$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} f_5(V_{int}(t), V_{out}(t)) \\ f_6(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\frac{V_{int}(t)}{C_{int}R_1} + \frac{V_{DD}}{C_{int}R_1} \\ -\frac{V_{out}(t)}{CR_4} \end{pmatrix}$$

- System $(0,0)$: $V_A = 0$, $V_B = 0$: Closing both pMOS transistors causes both capacitors to be charged over the same resistor R_1, similarly to system $(1,0)$. Thus

$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} f_7(V_{int}(t), V_{out}(t)) \\ f_8(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\left(\frac{1}{C_{int}(t)R_1} + \frac{1}{C_{int}(t)R_2}\right) V_{int} + \frac{V_{out}(t)}{C_{int}R_2} + \frac{V_{DD}}{C_{int}R_1} \\ \frac{V_{int}(t)}{CR_2} - \frac{V_{out}(t)}{CR_2} \end{pmatrix}$$

Every f_i, $i \in \{1, \ldots, 8\}$, is a mapping from $U = (0,1)^2 \subseteq \mathbb{R}^2$ to $\mathbb{R}$, whereat U is the vector of the voltages at the nodes N and O in Fig. 4. Solving the above ODEs provides analytic expressions for these voltage trajectories, which can even be inverted to obtain the relevant gate delays. As it turned out in [4], although the model perfectly covers the MIS effects in the case of falling output transitions, it fails to do so in the rising output transitions case. Nevertheless, despite this accuracy shortcoming, the results of the present paper imply that the model is faithful. More specifically, we obtain the following theorem:

Theorem 5.1. *For any $i \in \{1, \ldots, 8\}$, the mapping f_i, defined above, is Lipschitz continuous.*

Consequently, we can instantiate Definition 3.1 with

$$a_c(i_d^A, i_d^B) = \begin{cases} \begin{pmatrix} f_1(V_{int}(t), V_{out}(t)) \\ f_2(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i_d^A, i_d^B) = (1,1) \\ \begin{pmatrix} f_3(V_{int}(t), V_{out}(t)) \\ f_4(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i_d^A, i_d^B) = (1,0) \\ \begin{pmatrix} f_5(V_{int}(t), V_{out}(t)) \\ f_6(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i_d^A, i_d^B) = (0,1) \\ \begin{pmatrix} f_7(V_{int}(t), V_{out}(t)) \\ f_8(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i_d^A, i_d^B) = (0,0) \end{cases}$$

5.2 Advanced Hybrid Model

Unlike the simple hybrid model [4] outlined in the previous section, the *advanced hybrid gate model* proposed in [5] covers all MIS delay behaviors properly. It can be viewed as a generalization of the simple model, in which switching-on the pMOS transistors is not instantaneous but instead governed by a simple time evolution function representing the Shichman-Hodges transistor model [12]. To be more specific, the idea is to replace the transistors with time-variant resistors (see Fig. 5b), so that the values of $R_i(t)$, $i \in \{1, \ldots, 4\}$, vary between some fixed on-resistance R_i and the off-resistance ∞, according to the following functions:

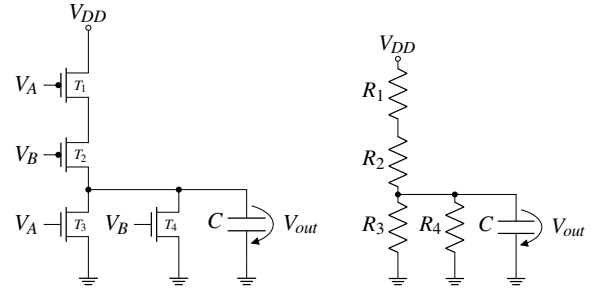
$$R_i^{on}(t) = \frac{\alpha_i}{t - t^{on}} + R_i;\ t \geq t^{on}, \tag{12}$$

$$R_i^{off}(t) = \infty;\ t \geq t^{off}. \tag{13}$$

Herein, α_i [Ω s] and on-resistance R_i [Ω] are constant slope parameters; t^{on} resp. t^{off} represent the time when the respective transistor is switched on resp. off. The switching-on of the nMOS transistors happens instantaneously also here, so $\alpha_3 = \alpha_4 = 0$.

Applying Kirchhoff's rules to Fig. 5b leads to $C\frac{\mathrm{d}V_{out}}{\mathrm{d}t} = \frac{V_{DD} - V_{out}}{R_1(t) + R_2(t)} - \frac{V_{out}}{R_3(t) \,||\, R_4(t)}$, which can be transformed into the non-homogeneous non-autonomous ODE with non-constant coefficients

$$\frac{\mathrm{d}V_{out}}{\mathrm{d}t} = f(t, V_{out}(t)) = -\frac{V_{out}(t)}{C\,R_g(t)} + U(t), \tag{14}$$



(a) Transistor level without taking the parasitic capacitance into account

(b) Advanced Hybrid Model configuration

Figure 5: Implementations of a CMOS NOR gate.

Table 1: $f(t, V_{out}(t))$ for each state transition.

State transition	$f(t, V_{out}(t))$
$(0,0) \to (1,0)$	$f_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nA}}$
$(1,1) \to (1,0)$	$f_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nA}}$
$(0,1) \to (1,0)$	$f_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nA}}$
$(0,0) \to (0,1)$	$f_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nB}}$
$(1,1) \to (0,1)$	$f_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nB}}$
$(1,0) \to (0,1)$	$f_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{CR_{nB}}$
$(1,0) \to (0,0)$	$f_3(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)}{C(\frac{\alpha_1}{t}+\frac{\alpha_2}{t+\Delta}+2R)}$
$(0,1) \to (0,0)$	$f_4(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)}{C(\frac{\alpha_1}{t+\Delta}+\frac{\alpha_2}{t}+2R)}$
$(1,1) \to (0,0)$	$f_5(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)t}{C(2Rt+\alpha_1+\alpha_2)}$
$(1,0) \to (1,1)$	$f_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$
$(0,1) \to (1,1)$	$f_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$
$(0,0) \to (1,1)$	$f_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$

where $\frac{1}{R_g(t)} = \frac{1}{R_1(t)+R_2(t)} + \frac{1}{R_3(t)} + \frac{1}{R_4(t)}$ and $U(t) = \frac{V_{DD}}{C(R_1(t)+R_2(t))}$.

As comprehensively described in [5], depending on each particular resistor's mode in each input state transition, different expressions for $R_g(t), U(t)$ and thus for $f(t, V_{out}(t))$ are obtained. They are summarized in Table 1. Note that we have used the notation $R_1 = R_{p_A}, R_2 = R_{p_B}$ with abbreviations $2R = R_{p_A} + R_{p_B}$, $R_3 = R_{n_A}$, and $R_4 = R_{n_B}$ for the two nMOS transistors T_3 and T_4. Due to the symmetry, we end up with only six different functions.

The following theorem shows that they are continuous in the first argument and Lipschitz continuous in the second argument.

Theorem 5.2. *Let $F = \{f_1, \ldots, f_6 : \mathbb{R} \times (0,1) \to \mathbb{R}\}$ be the set of all functions described in Table 1, modulo symmetry. Every $f_i \in F$, where $i \in \{1, \ldots, 6\}$, is continuous and Lipschitz continuous in the second argument $V_{out}(t)$.*

Defining $s(t) = (i_d^A(t^+), i_d^B(t^+))$ and $s_p(t) = (i_d^A(t), i_d^B(t))$, we can again instantiate Definition 3.1 by the choice function

$$a_c(s(t)) = \begin{cases} f_1(t, V_{out}(t)) & s(t) = (1,0) \\ f_2(t, V_{out}(t)) & s(t) = (0,1) \\ f_3(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (1,0) \\ f_4(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (0,1) \\ f_5(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (1,1) \\ f_6(t, V_{out}(t)) & s(t) = (1,1) \end{cases}$$

which, according to Eq. (14), results in $dV_{out}(t)/dt$ being

$$\begin{cases} \frac{-V_{out}(t)}{CR_{nA}} & s(t) = (1,0) \\ \frac{-V_{out}(t)}{CR_{nB}} & s(t) = (0,1) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t(t+\Delta_t)}{C\left(2Rt^2+(\alpha_1+\alpha_2+2\Delta_t R)t+\alpha_1\Delta_t\right)} & s(t) = (0,0), s_p(t) = (1,0) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t(t+\Delta_t)}{C\left(2Rt^2+(\alpha_1+\alpha_2+2\Delta_t R)t+\alpha_2\Delta_t\right)} & s(t) = (0,0), s_p(t) = (0,1) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t}{C(2Rt+\alpha_1+\alpha_2)} & s(t) = (0,0), s_p(t) = (1,1) \\ \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}}) & s(t) = (1,1). \end{cases}$$

6 CONCLUSIONS

We presented a general continuity proof for a broad class of first-order thresholded hybrid models, as they arise naturally in digital circuits. We showed that, under mild conditions regarding causality, digitized hybrid gates could be composed to form circuits with unique and well-behaved executions. We concluded with concrete gate model instantiations of our model.

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A ADDITIONAL DETAILS FOR SECTION 5 (APPLICATIONS)

Theorem 5.1. *For any $i \in \{1, \ldots, 8\}$, the mapping f_i, defined above, is Lipschitz continuous.*

Proof. Albeit the proof is evident, we elaborate it for f_7; similar arguments apply to the other cases. Let $K = max\{(\frac{1}{C_{int}R_1} + \frac{1}{C_{int}R_2}), \frac{1}{C_{int}R_2}\}$. For any voltages of $V_{int}(t)^{(1)}, V_{int}(t)^{(2)}, V_{out}(t)^{(1)}$, and $V_{out}(t)^{(2)}$ belonging to $(0, 1)$, we find

$$\begin{aligned}
&\left\|f_7(V_{int}(t)^{(1)}, V_{out}(t)^{(1)}) - f_7(V_{int}(t)^{(2)}, V_{out}(t)^{(2)})\right\| = \\
&\Big\|-\big(\frac{1}{C_{int}R_1} + \frac{1}{C_{int}R_2}\big)(V_{int}(t)^{(1)} - V_{int}(t)^{(2)}) + \\
&\quad \frac{1}{C_{int}R_2}\big(V_{out}(t)^{(1)} - V_{out}(t)^{(2)}\big)\Big\| \leq \\
&K\Big\|(V_{int}(t)^{(1)} - V_{int}(t)^{(2)}) + (V_{out}(t)^{(1)} - V_{out}(t)^{(2)})\Big\|.
\end{aligned}$$

□

Theorem 5.2. *Let $F = \{f_1, \ldots, f_6 : \mathbb{R} \times (0, 1) \to \mathbb{R}\}$ be the set of all functions described in Table 1, modulo symmetry. Every $f_i \in F$, where $i \in \{1, \ldots, 6\}$, is continuous and Lipschitz continuous in the second argument $V_{out}(t)$.*

Proof. The proof is clear for functions f_1, f_2, and f_6. It is also straightforward for f_5: Let $g(t) \doteq \frac{t}{C(2Rt+\alpha_1+\alpha_2)}$. Since $t \in [0, T]$, $g(t)$ takes its supremum value in the interval, which we denote by K (i.e., $sup_{t\in[0,T]}g(t) = K$). We observe

$$\begin{aligned}
&\|f_5(t, V^1_{out}(t)) - f_5(t, V^2_{out}(t))\| = \\
&\left\|\frac{\big(-V^1_{out}(t) + V_{DD}\big)t}{C(2Rt + \alpha_1 + \alpha_2)} - \frac{\big(-V^2_{out}(t) + V_{DD}\big)t}{C(2Rt + \alpha_1 + \alpha_2)}\right\| = \\
&\left\|\frac{-t}{C(2Rt + \alpha_1 + \alpha_2)} \cdot (V^1_{out}(t) - V^2_{out}(t))\right\| \leq |K|\left\|(V^1_{out}(t) - V^2_{out}(t))\right\|,
\end{aligned}$$

which concludes the proof for f_5. The proof for f_3 and f_4 follows the same route; we only sketch the proof of the Lipschitz continuity for f_3. We can write

$$\|f_3(t, V^1_{out}(t)) - f_3(t, V^2_{out}(t))\| = \quad \left\|\frac{-(V^1_{out}(t) - V^2_{out}(t))}{\frac{\alpha_1}{t+\Delta} + \frac{\alpha_2}{t} + 2R}\right\|.$$

The fact that t and Δ both belong to the closed interval $[0, T]$ provides us with a Lipschitz constant L, which is independent of t. Consequently,

$$\|f_3(t, V^1_{out}(t)) - f_3(t, V^2_{out}(t))\| \leq L \cdot \|\big(V^1_{out}(t) - V^2_{out}(t)\big)\|,$$

which completes the proof. □