Continuous-Time Delta-Sigma A/D Converters for High Speed Applications

by

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Abstract

This is a thesis about implementation of a ΔΣ modulator with continuous-time techniques. A methodology to obtain proper continuous-time (*s*-domain) transfer functions for a continuous-time ΔΣ modulator has been presented. Different classes of continuous-time modulators based on the DAC waveform in the ΔΣ loop and the number of digital delays in the feedback loop have been recognized and analyzed. A new structure for the LC-based ΔΣ modulators has been proposed. A fourth-order transconductor-*C* modulator has been implemented in a 0.8μm BiCMOS technology. Advantages and drawbacks of continuous-time modulators particularly with transconductor-*C* technique have been investigated. A new transconductor-*C* filter and further work are recommended to improve the performance of the current modulator.

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List of Symbols

A list of the major symbols, notations and abbreviations with their definitions are as follows:

$\lvert\ \rvert$	Absolute value
$\lVert\ \rVert_1$	One-norm
$\lVert\ \rVert_\infty$	Infinity-norm
$\boldsymbol{A}_c$	An $N \times N$ state space matrix for a continuous-time modulator
$\boldsymbol{A}_d$	An $N \times N$ state space matrix for a discrete-time modulator
A_{dc}	The DC gain of an amplifier
$A(K)$	Noise amplification factor which demonstrates a stability check for a $\Delta\Sigma$ modulator
A/D	Analog-to-digital
ADC	Analog-to-digital converter
a_k	A residue of a discrete-time $\Delta\Sigma$ loop transfer function
$\hat{a}_k$	A residue in a continuous-time $\Delta\Sigma$ loop filter
B	Bandwidths in Hz
$\boldsymbol{b_c}$	An $N \times 1$ vector defining the state space parameter of a continuous-time modulator
$\boldsymbol{b_d}$	An $N \times 1$ vector defining the state space parameter of a discrete-time modulator
C	Capacitor
CMRR	Common-mode rejection ratio
C_{ox}	Oxide capacitance of the gate-to-body per unit area
$\boldsymbol{c_c}$	An $N \times 1$ vector defining the state space parameter of a continuous-time modulator
$\boldsymbol{c_d}$	An $N \times 1$ vector defining the state space parameter of a discrete-time modulator
ΔT	A fraction of one clock period in a continuous-time $\Delta\Sigma$ modulator as an extra loop delay
D/A	Digital-to-analog
DAC	Digital-to-analog converter

d_c	a scaler defining the state space parameter of a continuous-time modulator
d_d	a scaler defining the state space parameter of a discrete-time modulator
$\Delta\Sigma$	Delta-Sigma
$e(k)$	Additive White noise modeling the $\Delta\Sigma$ quantization noise
$\mathrm{F_i}$	Noise figure of the ith stage amplifier
$F_{aa}(\omega)$	Implicit anti-alias filtering frequency response in a continuous-time modulator
$\varphi_i(\omega)$	Phase frequency response of a transconductor circuit
f	Frequency in Hz
f_{bp}	A frequency in a bandpass region (like $f_s/4$) in Hz
f_{lp}	A frequency in a low pass region around DC in Hz
f_s	Sampling frequency in Hz
G	Gain
G_i	Gain of the *i*th stage amplifier
$G(z)$	Transfer function of the feedforward filter in a discrete-time modulator
$\hat{G}(j\omega)$	Frequency response of the feedforward filter in a continuous-time $\Delta\Sigma$ modulator
$G_i(\omega)$	Amplitude frequency response of a transconductor circuit
G_m	Transconductance representation of an OTA in its model
G_m-C	Transconductor-capacitor circuit
G_o	Output conductance representation of an OTA in its model
g_{ds}	Drain-source conductance
g_m	Transconductor element
g_{mb}	Body-effect transconductance
g_{mbi}	*i*th transconductance element in the feedforward path of a transconductor-*C* filter used in the feedback loop of a $\Delta\Sigma$ modulator
g_{mai}	*i*th transconductance element in the feedforward path of a transconductor-*C* filter used in the feedforward path of a $\Delta\Sigma$ modulator
g_{mf}	One of two transconductance elements in a resonator configuration
g_{mx}	One of two transconductance elements in a resonator configuration
g_{oX}	The output conductance of the transconductor called *X*
$H(z)$	Open-loop transfer function of a $\Delta\Sigma$ modulator

HD_i	ith harmonic distortion in dB
$H_{LC}(s)$	A simple transfer function of an LC resonator
$H(z, m)$	Open-loop modified z-transfer function of a $\Delta\Sigma$ modulator with extra loop delay
$H(e^{j\omega T})$	Loop frequency response of a discrete-time modulator
$\hat{H}(s)$	Open-loop transfer function of a continuous-time $\Delta\Sigma$ loop filter
$h(n)$	The entire $\Delta\Sigma$ open-loop impulse response
$\hat{h}(t)$	The $\Delta\Sigma$ loop filter impulse response
I	DC current in a transistor
I_D	Drain current in a MOSFET
I_E	Emitter current in a bipolar transistor
IIP_3	Third-order intermodulation intercept point in dBm
IM_3	Third-order intermodulation product referred to the fundamental tone level in dBc
I_m	Peak current swing in a transistor
$I_n(x)$	Modified Bessel function of the first kind, of order n
I_S	Constant saturation current in a bipolar transistor
$\overline{i_n^2}$	Current noise spectral density in A^2/Hz
i	Small signal current in a transistor
$\overline{i(t)}$	Average DC value of $i(t)$
k	Boltzmann's constant
K	Loop gain a $\Delta\Sigma$ modulator
K_x	A quasi linear gain defined for a $\Delta\Sigma$ modulator related to the input signal
K_n	A quasi linear gain defined for a $\Delta\Sigma$ modulator related to quantization noise
k_{hz}	Half delayed return to zero coefficient in an LC modulator
k_{nz}	Non return to zero coefficient in an LC modulator
k_{rz}	Return to zero coefficient in an LC modulator
L	Length of A CMOS channel
LC	Inductance-capacitance tank circuit
LHP	Left half plane in the S-plane
MSA	Maximum amplitude signal at which the modulator results in the maximum SNR

μ_n	Electron mobility in the induced *n* channel
NEF	noise excess factor
NF	Noise figure of entire circuit
N_q	In-band quantization noise
NRZ	Non-return-to-zero pulse waveform
N_t	Input referred thermal noise voltage integrated over a certain bandwidth
$NTF(z)$	Noise transfer function of a ΔΣ modulator
$NTF_K(z)$	Noise transfer function of a modulator as a function of loop gain *K*
$NTF_m(z)$	Noise transfer function obtained from the modified *z*-transform of the modulator loop
OSR	Oversampling ratio
pdf	probability density function
p_i	*i*th pole of a circuit
Q	Quality factor of a filter
R	Resistor
R	Sampling rate to the twice of the maximum input signal frequency ratio in a bandpass modulator
RHP	Right half plane in the *S*-plane
$R_{HZ}(t)$	A RZ pulse waveform with a half delay
$R_i(t)$	An arbitrary DAC pulse waveform
$R_{NZ}(t)$	NRZ pulse waveform
$R_p(t)$	A pulse waveform with *p* sec aperture
R_{ph}	The resistive model for the NMOS transistor in series with Miller capacitor
$R_{RZ}(t)$	RZ pulse waveform
R_z	The resistor in series with Miller integrating capacitor
RZ	Return-to-zero pulse waveform
r_b	Base region resistance in a bipolar transistor
r_{ds}	MOS drain-to-source small signal output resistance
$\sum$	Sum over all parts from *i* to *k*
$S(K)$	One-norm of a ΔΣ modulator's noise transfer function as a function of loop gain *i.e.* $NTF_K(z)$
SFDR	Spurious free dynamic range

S_i/N_i	Signal-to-noise ratio at the input of an amplifier
S_o/N_o	Signal-to-noise ratio at the output of an amplifier
$STF(z)$	Signal transfer function of a ΔΣ modulator
$STF_c(\omega)$	Signal frequency response in a continuous-time ΔΣ modulator
s	Complex frequency in S-plane
$\hat{s}_k$	A pole in a continuous-time ΔΣ loop filter
sgn(x)	Sign function
T	Absolute temperature
T	A clock period
TC-amp	Transconductor-capacitor-amplifier circuit
TIMD	Total intermodulation distortion in dB
$T(s)$	Voltage transfer function of a transconductor circuit
V_{BE}	Base-Emitter junction voltage drop in a bipolar transistor
V_{DS}	MOS drain-to-source voltage
V_{GS}	MOS gate-to-source voltage
V_{freq}	Control voltage to tune the center frequency of a filter
V_f	Shorter form used for V_{freq}
V_{on}	The so-called on voltage in a MOSFET
V_{phase}	Control voltage to cancel the excess phase and so the Q of a filter
V_{ph}	Shorter form used for V_{phase}
V_{th} or V_t	MOS threshold voltage
$\frac{V_T}{2}$	Thermal voltage in a bipolar transistor
v_n^2	Voltage noise spectral density in V^2/Hz
W	Width of a CMOS channel
ω	Frequency in rad/s
ω_o	Center frequency of a bandpass filter in rad/s
ω_o	Unity bandwidth of an op-amp in rad/s
ω_s	Sampling frequency in rad/s
$\hat{X}(j\omega)$	Spectrum of an input signal to a continuous-time modulator
$\hat{x}(t)$	Input signal to a continuous-time modulator
$Y(e^{j\omega T})$	Spectrum of an output signal in a continuous-time or discrete-time modulator

$\mathcal{Z}$	Ordinary z-transform
$\mathcal{Z}_m$	Modified z-transform
ZOH	Zero order hold
z	Complex frequency in Z-plane
z_k	A pole of a discrete-time $\Delta\Sigma$ loop transfer function
z_i	ith zero of a circuit

Chapter 1

Introduction

1.1 Analog-to-Digital Conversion

It is not exaggerating to say that data converters are key components of almost any electronic system. Since the real world is inherently analog and the trend in telecommunication, voice, video, instrument, computer and many other applications is to get a digital form of the analog signal to make use of robust, flexible and reliable signal processing, the analog-digital interfaces become critical paths. In terms of complexity data converters are composed of many analog building blocks such as op-amps, sample (track)-and-holds and comparators which makes their design very challenging especially when a system is put on a chip. In a data converter designers often have to mix analog and digital techniques and acquire a very good knowledge in both analog and signal processing areas. Sometimes even dealing with some abstract theories such as nonlinear phenomena and stability becomes unavoidable. In this sense, perhaps the most interesting class of data converters is Delta-Sigma ($\Delta\Sigma$) analog-to-digital (A/D) converters which are sometimes referred to as oversampling, interpolative or noise-shaping converters. A $\Delta\Sigma$ A/D converter usually consists of an analog part called a $\Delta\Sigma$ modulator producing an oversampled bit stream followed by a digital part implementing decimation and digital filtering to complete the A/D conversion.

Depending on the application of an A/D converter the trade-off among speed, resolution and power is made given the specifications and the process. In [Snel92] a comparison among several analog-to-digital converters (ADC) has been made and the resultant plots demonstrate very useful relations. Regarding speed and accuracy it was found that the best converters had $2^N f_s = 100\text{GHz}$, where N is the converter's resolution in bits and

f_s the sampling frequency. For eight-bit converters a wide range of $1\text{mW}-10\,\text{mW/MHz}$ has been found as a relationship between power and sampling rate while the best 8-bit part was consuming $2.5\,\text{mW/MHz}$. This means that in a state-of-the art converter one can expect to get an 8-bit ADC with $100\,\text{MHz}$ sampling frequency consuming $250\,\text{mW}$. A survey among some of the most recent ADCs in the literature verified the preceding information. For example, an 8-bit $150\,\text{MHz}$ sampling ADC with $350\,\text{mW}$ power consumption was reported in 1995 [Mor95]. However, most ADCs were consuming higher power in the order of 1W at high sampling rates [Kim93] or higher resolution (10 bits) [Col93].

As mentioned, Delta-Sigma ($\Delta\Sigma$) converters form a popular class of analog-to-digital converters. However, they have been mostly developed for high precision voice applications using switched-*C* techniques. For video applications such as digital-TV, HDTV or direct satellite broadcast systems usually a moderate dynamic range between 7 to 10 bits is enough but a fairly high clock rate in order of $100\,\text{MHz}$ is required. So far, flash [Rey94] or half-flash [Lon93], pipeline and/or sub-ranging [Con93], [Lin90], [Nis95] A/D converters have been developed for the video applications.

This thesis studies the feasibility of a $\Delta\Sigma$ modulator for high-speed high-bandwidth applications such as video. Since it is well known that continuous-time techniques such as transconductor-*C* filters can be faster than their switched-*C* counterparts in the same process, the motivation for this thesis was the development of a method for implementing continuous-time $\Delta\Sigma$ modulators with special stress on transconductor-*C* realization. Although one can not expect to achieve a very high dynamic range performance from transconductor-*C* circuits due to their known non-linearity problems, it seems that for the medium dynamic range applications such as video, these circuits are suitable.

Another motivation for studying the transconductor-*C* approach for $\Delta\Sigma$ modulation was the new trend for moving analog/digital interface closer to the signal source which necessitates higher ADC sampling rates. Perhaps, talking about analog-to-digital conversion for radio frequencies (RF) in GHz range seems to be a bit unrealistic today. However, conversion of analog signals at an intermediate frequency (IF) is quite

achievable. A ΔΣ modulator for converting an IF signal at up to 10.7 MHz [Sing94] has been already reported using switched-*C* techniques. This thesis investigates the possibility of analog-to-digital conversion of an analog signal at higher IF frequencies. This thesis demonstrates a fourth-order ΔΣ transconductor-*C* circuit implementation. It also shows some practical advantages and drawbacks of a continuous-time ΔΣ implementation which have been supported by analysis and simulations and practically verified by experiments. It studies the problems associated with the LC realizations [Gail89], [Thu91], [Tro93] and introduces a new structure for an LC ΔΣ modulator.

1.2 Contributions

The contributions made in this thesis to the study and implementation of a continuous-time ΔΣ modulator are as follows:

1) It gives a methodology to obtain a continuous-time loop filter transfer function from a switched-*C* counterpart given the waveform(s) of the digital-to-analog converter(s) (DAC) in the ΔΣ feedback loop. The loop filter transfer functions for some important modulators have been explicitly presented.

2) It develops two different classes of equivalent continuous-time modulators for every switched-*C* modulator which has at least two loop delays: *i*) a zero-delay modulator and *ii*) a modulator with one or more digital loop delays.

3) It analyzes the effects of the extra loop delays or propagation delay times of the components in a continuous-time ΔΣ modulator such as those in the comparator, latch or D-flip flop, DAC and parasitic interconnects by the modified z-transform method. It explicitly derives the modified noise transfer functions $NTF_m(z)$ for two popular bandpass modulators as well.

4) It analytically proves the anti-alias filtering property of continuous-time modulators which is then verified by simulations and real circuit experiments.

5) It introduces a novel architecture for LC type ΔΣ modulators which provides enough degrees of freedom to produce an arbitrary ΔΣ loop impulse response.

6) It employes a master-slave tuning algorithm to control the notch center frequency and the Q of noise-shaping in a second-order transconductor-*C* ΔΣ modulator. Such a method has been already used for tuning of the transconductor-*C* filters but to the author's knowledge not for tuning of ΔΣ modulator parameters.

7) It demonstrates the design and implementation of a fully monolithic fourth-order transconductor-*C* ΔΣ modulator along with a master biquadratic (biquad) filter in a 0.8μm BiCMOS process. It gives the experimental results of the realized chips. It clearly explains the causes of the discrepancies between simulations and experiments and suggests a new design for a future implementation.

1.3 Organization of the Thesis

Chapter 2 introduces the concepts of a continuous-time ΔΣ as well as a bandpass ΔΣ modulator. Stability criteria in a ΔΣ modulator are critically reviewed and a mixture of one-, two- and infinity-norm constraints given in [Risb94] are compared to some previous stability criteria.

Chapter 3 proposes a systematic method to obtain a proper *s*-domain transfer function for a continuous-time modulator from an original discrete-time (switched-*C*) equivalent. It shows how different DACs in a modulator loop such as non-return-to-zero (NRZ), return-to-zero (RZ) and so on would lead to different continuous-time loop filters. It discusses the sensitivity of continuous-time modulators to the extra loop delays. It culminates by proving the anti-alias filtering property of continuous-time modulators.

Chapter 4 introduces a new pulse-shaping architecture for LC continuous-time modulators. It shows how the overall loop impulse response of an LC modulator can be fixed to coincide with that of an ideal discrete-time equivalent by providing two degrees

of freedom at the input of each LC resonator in DAC feedback paths.

Chapter 5 develops a BiCMOS transconductor-*C*-amplifier (TC-amp) filter for a fourth-order ΔΣ modulator. It studies the sensitivity of a general transconductor-*C* modulator to its loop filter parameters (Q and center frequency). It gives an analysis with simulation support to show how the Q of a TC-amp filter can be adjusted using cancellation of excess phase in each resonator (integrator) by tuning resistors in series with the Miller integrating capacitors. It demonstrates a small-signal and non-linearity analysis for the proposed TC-amp integrator. It concludes with the simulation results of the entire transconductor-*C*-amplifier ΔΣ modulator circuit.

Chapter 6 shows the implementation of a second-order transconductor-*C* ΔΣ modulator with a master-slave automatic tuning scheme. It discusses the linearity of the modulator and the matching between the master and the slave parts. It proves the anti-alias filtering property of transconductor-*C* modulators experimentally.

Chapter 7 investigates the speed, tunablity, noise and power trade-offs in the proposed class of triode-mode BiCMOS transconductor-*C* modulators. It shows how the dynamic range of a transconductor-*C* modulator can be improved by optimizing the transconductor-*C* circuits with respect to their input-referred noise. It shows that this improvement sacrifices the modulator's speed and tunablity while the power consumption is slightly lowered. It concludes with the introduction of a regular transconductor-*C* modulator architecture as opposed to the designed TC-amp modulators.

Chapter 8 demonstrates the experimental results of two fourth-order bandpass TC-amp ΔΣ modulators along with their master biquad filters implemented in a 0.8μm BiCMOS process. It shows the experimental noise-shaping spectrums of both chips. It investigates disagreements between the chips' noise-shaping spectra and simulation results. It diagnoses some important causes and proposes a complete new design for a future implementation.

Chapter 2

Overview of Delta-Sigma Modulator

Delta-Sigma (ΔΣ) modulation refers to a class of noise-shaping linear encoders (typically one-bit) which transforms an analog (continuous-time) signal to an oversampled bit stream. A general diagram of a ΔΣ modulator is shown in Fig. 2.1. Oversampling of the continuous-time signal before quantization reduces the quantization noise density by the factor of the oversampling ratio OSR which is defined as the ratio of the sampling rate to twice the signal bandwidth (Nyquist rate). The in-band quantization noise is reduced by 3 dB (0.5 bit) for every doubling of the oversampling ratio. The linear system in the modulator loop shapes the quantization noise by placing nulls in the quantization noise spectrum at the band of interest which in turn enhances the output bit stream signal-to-quantization noise ratio further. Delta-Sigma modulators have been of outstanding interest at low-speed high-resolution applications. However, they have not been very successful in high-speed high-bandwidth applications. The explanation is that the high performance of ΔΣ modulators can typically be exploited at high oversampling ratios. For high bandwidth applications this requires a very high sampling rate which makes the real implementation very difficult.

Switched-*C* techniques have been the dominant approach for implementing the ΔΣ loop filters. One can achieve very good matching and linearity with a switched-*C* technique; however, the clock speed is a limiting factor. The reasons are the opamp speed (bandwidth) and non-ideal effects in the switches like nonzero "on"-resistance and clock feedthrough. It is shown [Greg86] that in order to have a negligible error at a switched-*C* integrator with a two-phase clock scheme, the unity-gain bandwidth of the opamp ω_o should be (at least) five times as large as the clock frequency f_s *i.e.* $f_o \approx 5 f_s$. Recently, a

continuous-time technique [Gail89], [Thu91], [Tro93] for bandpass LC-based modulators has been introduced as an alternative for the switched-*C* (discrete-time) approach. The continuous-time modulators can also make use of some other continuous-time techniques such as the transconductor-*C* (G_m-*C*) approach. Since a transconductor-*C* integrator operates at its unity-gain frequency ω_o, so one can estimate that within the same technology a typical continuous-time filter can be five times faster than a typical switched-*C* one.

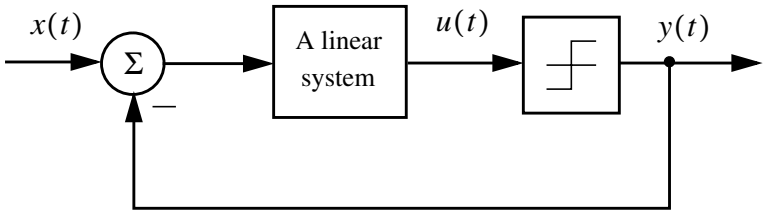

Figure 2.1 : A general ΔΣ modulator.

The higher-order ΔΣ modulators can alleviate the high-speed clock requirement somewhat. That's why many researchers have developed some higher-order ΔΣ topologies [Lee87b], [Ada91], [Cha90]. Unfortunately, modulator structures (order > 2) are prone to instability. So, the stability analysis continue to be a central research issue for these modulators [Risb94].

In this chapter an overview on continuous-time modulators will be given. Then, bandpass ΔΣ modulators are reviewed. A survey of ΔΣ stability analyses will conclude the chapter.

2.1 Continuous-time Delta-Sigma Modulator

Delta-Sigma modulation was proposed in 1962 [Ino62] by Inose *et. al.* as a modification of Delta modulation, which couldn't fulfill the requirements of digital transmission of analog signals. The same authors in 1963 [Ino63] presented an analysis for signal-to-noise characteristics of a ΔΣ modulator along with a real circuit implementation. Their modulator loop filter was an integrator composed of the discrete-component continuous-time circuits. Fig. 2.2 shows a block diagram of the lowpass filters used in [Ino63],

where G represents the loop DC-gain implemented by a transistor. Later on in [Bra69] it was shown that since the modulator feedback signals are sampled, the loop behavior including the continuous-time feedback loop filter can be described by a z-domain transfer function. The general analysis given in [Bra69] was correct, however, the z-domain transfer functions proposed for a simple integrator $1/(s+\alpha)$ and a double integrator $(s+\beta)/s^2$ were wrong. Candy [Can74] used the same idea to make an 8-bit A/D converter intended for 1-MHz signal bandwidths. He used a continuous-time single-stage integrator for the modulator loop similar to that in [Ino62]. His analysis showed again despite the fact that the loop filter is continuous-time, because of the presence of a sampler (quantizer) inside the modulator loop, the loop function can be expressed by a z-domain transfer function. Ignoring aliasing effects he gave representation for the baseband spectrum of the output signal for the first-order modulator. In [Can85] an extended analysis of [Can74] was given which related a

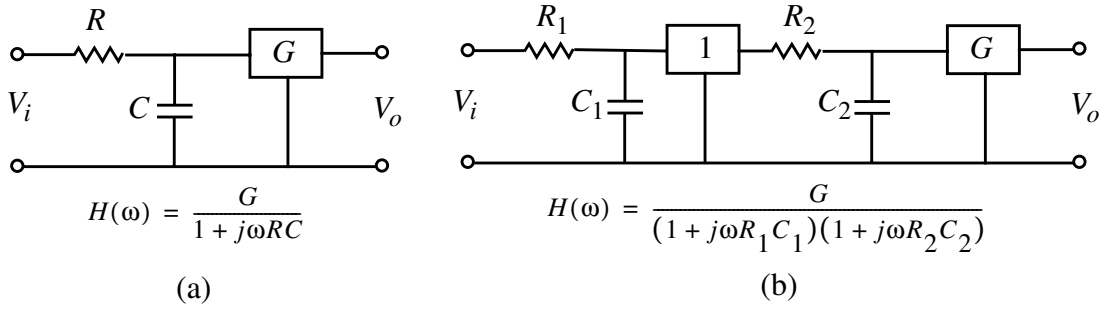

Figure 2.2 : The modulator loop filters used in [Ino63] with their transfer functions, (a) single-integrator, and (b) double-integrator.

modulator with a second-order continuous-time filter to its discrete-time equivalent. This was a correct z-domain loop transfer function representing a loop including a continuous-time double integrator and a D/A with a non-return to zero (NRZ) feedback pulse:

$$\frac{2z-1}{(z-1)^2} \leftrightarrow \frac{1+1.5sT}{(sT)^2} \qquad (2.1)$$

where T is the sampling period.

With the advent of switched-C filters most integrated-circuit $\Delta\Sigma$ A/D converters became

switched-C based [Ada91], [AD92]. There have been some exceptions in which a mixed continuous-time discrete-time scheme has been chosen. For example in [Sig90] the fourth-order integrated circuit modulator loop filter consists of a continuous-time chopper-stabilized front end integrator followed by a third-order switched-C circuit. The primary reason for using a continuous-time front-end integrator instead of discrete-time one in [Sig90] was noise. For a switched-C integrator, the noise is determined by thermal noise sampled on the input capacitors: kT/C. To suppress the sampled noise in a discrete-time loop for a very high resolution A/D like the one reported in [Sig90], an input capacitor in order of several hundred picofarads is required. This large capacitor is undesirable for integration and could cause some nonlinear settling of analog input and nonlinear sampling in the input switches too. Since the input signal is not sampled in the continuous-time integrator the above errors are eliminated. Besides, the continuous-time integrator provided a *sinc*-shaped anti-alias filtering for the modulator [Can85].
Shortly after introduction of the bandpass $\Delta\Sigma$ modulator [Sch89], [Gail89] continuous-time modulators attracted more attention [Thu91], [Tro93]. The main reason was the higher speed capability of continuous-time filters compared to their switched-C counterparts. Especially for bandpass modulators, the speed of the loop filter is the major limitation on the center IF frequency of the modulator. The continuous-time bandpass modulators used in [Gail89], [Thu91], [Tro93] were discrete-LC-type filters. Unfortunately, as will be shown in Ch. 4 they didn't produce a proper loop transfer function, so their modulators were susceptible to instability and didn't give the maximum achievable *SNR* for the given order.

2.2 Bandpass Delta-Sigma Modulator

As mentioned the modulator loop filter puts nulls in the quantization noise across the band of interest. In a lowpass $\Delta\Sigma$ modulator the zeros of the quantization noise are near DC. One can extend this principle to bandpass by moving nulls into some non-DC frequencies which produces a band-reject noise-shaping property instead. This can be expressed by a linear model of the modulator shown in Fig. 2.3 in which the quantizer is substituted by an additive white noise $e(k)$. From this linear model one can define noise transfer function $NTF(z)$ and signal transfer function $STF(z)$ as follows:

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$
$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.2)$$

By using a linear model with given specifications such as *SNR*, bandwidth (BW) and oversampling ratio (OSR) the required $NTF(z)$ can be obtained, and consequently from (2.2) the loop filter $H(z)$ is derived. For a bandpass design one can first meet the *SNR*-BW/OSR requirement for a given sampling frequency with a lowpass modulator assuming that the input signal is centered at zero IF. The resulting lowpass modulator

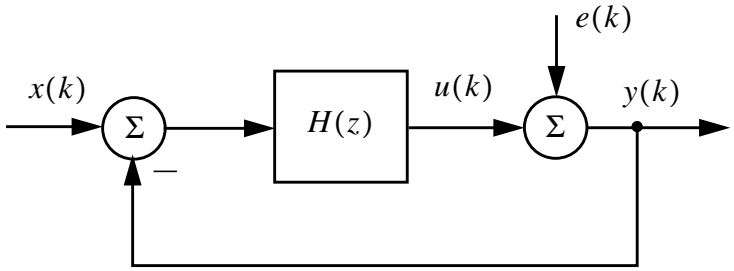

Figure 2.3 : The general linear model for a ΔΣ modulator.

would consist of a lowpass loop filter $H(z)$ and produce a highpass $NTF(z)$. Then the $NTF(z)$ can be transformed to a bandreject filter by a lowpass to bandpass transformation [Opp75], say:

$$z^{-1} \rightarrow -z^{-1}\frac{z^{-1}-\alpha}{1-\alpha z^{-1}} \quad , \text{ where } -1<\alpha<1 \qquad (2.3)$$

which in turn produces a bandpass loop filter $H(z)$. It is apparent from (2.3) that the order of the obtained bandpass modulator is twice as high as that of the original lowpass and one intuitively can expect to get the same *SNR* for a given bandwidth. Selecting the sampling frequency f_s, 2^n times faster than the modulator center frequency f_o, where n is an integer, reduces the complexity of the decimation filter [Sch89]. One good choice is at $f_s = 4f_o$ which corresponds to the $z^{-1} \rightarrow -z^{-2}$ lowpass to bandpass transformation, the special case in (2.3) when $\alpha = 0$. In frequency domain this means

$$-j2\pi f_{lp} \rightarrow e^{j(\pm 2\pi f_s/2 - 4\pi f_{bp})} \Rightarrow f_{bp} = \pm f_s/4 + \frac{f_{lp}}{2} \qquad (2.4)$$

where f_{bp} is the mapped bandpass and f_{lp} the original lowpass frequencies and as is apparent from (2.4) the prototype lowpass *NTF* zeros at DC are mapped to $\pm f_s/4$. This frequency band transformation is shown in Fig. 2.4. As shown in Fig. 2.4 the OSR and the positive or negative bandwidths *B* in both bandpass and lowpass modulators are the same; however, the distances between the spread zeros on the unit circle in the bandpass are half those in the lowpass. The latter can be observed from (2.4) too. The transformation $z^{-1} \rightarrow -z^{-2}$ doesn't change the dynamics of the lowpass prototype, so a stable lowpass modulator produces a stable bandpass one.

The preservation of stability is not always true for a general transformation given in (2.3). Therefore, one can use an optimization algorithm [Sch93], [Risb94] or some computer filter approximator [Ous90] to design an arbitrary bandreject *NTF*(*z*) at a desired center frequency considering some modulator stability constraints. It should be noted that the optimized *NTF*(*z*) maximizes the *SNR* at a certain bandwidth or OSR. So, usually these kind of modulators are application specific and don't result in the optimum performance as a general purpose A/D modulator say for different bandwidths and/or variant OSRs.

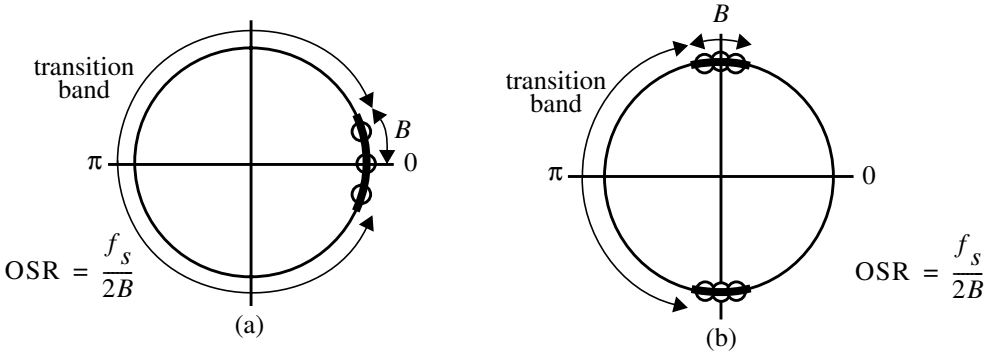

Figure 2.4 : The frequency mapping produced by the $z^{-1} \rightarrow -z^{-2}$ transformation, the *NTF* zeros and the band of interest *B* in (a) lowpass and (b) bandpass modulators.

The maximum sampling frequency is usually determined by the technology limit and the bandwidth is known from the application, so the order and type of the modulator loop filter and the band location have to be selected for achieving the required *SNR*. One

consideration for the band selection in a switched-*C* modulator is making the transition band (shown in Fig. 2.4) wider, say by placing the center frequency closer to DC *i.e.* having a higher f_s/f_c. This relaxes the requirements on the anti-aliasing filter. Therefore, the $f_s/4$ center frequency might not always be a good choice. Consequently, a lower center frequency like $f_s/8$ may be required which makes the decimation process a bit more complex than the simple $f_s/4$ case too. For a continuous-time modulator, however, due to its inherent anti-alias filtering property which will be shown in Sec. 3.2 this is not an issue. So, for a continuous-time modulator, $f_s/4$ is probably the best choice for the center frequency; it simplifies the decimation process and lets a designer use the $z^{-1} \rightarrow -z^{-2}$ transformation too.

2.3 Stability in a Delta-Sigma Modulator

The design of a ΔΣ modulator is not complete unless a robust stability condition is achieved. Many investigators have tried to come up to a reliable criterion for the stability of a ΔΣ modulator. Although several stability criteria exist, they either give no guarantee whatsoever or are over conservative. The main reason for this problem is that a ΔΣ modulator is a highly non-linear system because of the presence of a quantizer, usually one bit, in the forward path. Analysis of a non-linear closed loop system has always been a big problem for control engineers [Tha62]. They usually need to make a linear approximation to reach a solution which can predict the response of the non-linear system up to some extent. Furthermore, in a ΔΣ modulator the behavior of the signals at the input of quantizer and quantization noise are stochastic. The latter fact even restricts the use of the ordinary non-linear control theory in ΔΣ modulators and would require an analysis of a non-linear system with a random process excitation.

Besides, the most often used linear model of a ΔΣ modulator shown in Fig. 2.3 substituting the quantizer with a gain of one and an additive independent white noise as the quantization error can not explain some dynamic characteristics of the modulator like noise spectrum dependency on the input signal.

2.3.1 Quasi-linear Loop Gain

Ardalan and Paulos [Ard87] proposed a comprehensive closed form quasi-linear

solution which replaces the quantizer with two linearized gains based on a mean square error criterion. They assumed that the input signal to the quantizer is composed of a part related to the modulator input signal and a zero mean random component. A block diagram of these interlocked linear systems are shown in Fig. 2.5. They assumed a Gaussian distribution for the input signal to the quantizer. In order to obtain the linearized loop gains one can run simulations for getting the variance and the mean value (statistics) of the signal $e(t)$ at the input of quantizer or solve a set of simultaneous equations numerically.

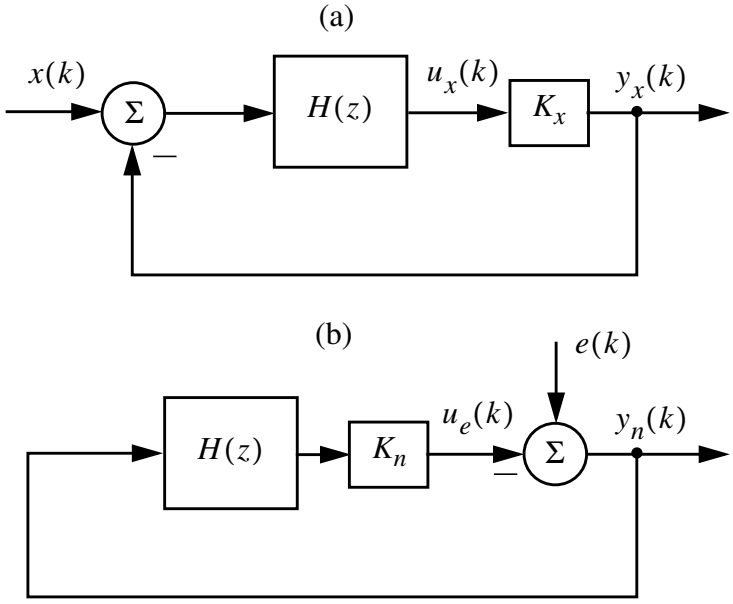

Figure 2.5 : (a) Linearized system for the input signal to modulator, (b) equivalent system for quantization noise.

Knowing the loop gain, one can write the noise transfer function from the block diagram in Fig. 2.5 as:

$$NTF_K(z) = \frac{1}{1 + K_n H(z)} \qquad (2.5)$$

Clearly the shaping of the noise spectra by the loop gain K_n is apparent from (2.5) and since the loop gain K_n is a function of the input amplitude the noise transfer function dependency on the input signal is justified. It was shown that increase of the input amplitude (DC in lowpass modulators) would reduce the loop gain and consequently

shape the noise spectrum, producing more in-band noise. This way one can use linear control tools like root locus, Nyquist plot, etc. to investigate the modulator stability against the loop gain (input amplitude). In [Ard87] it was shown that for DC input at high input amplitude values K_n is much lower than K_x, so for a stability test the noise equivalent system shown in Fig. 2.5b and represented in (2.5) should be used.

The excellent theoretical work in [Ard87] has not received much attention due to its complexity and again not offering a certain stability guarantee for different class of modulators. Later, in [Wol88], [Ada91] the stability of a ΔΣ modulator was analyzed by replacing the quantizer with a linear gain which was defined by the ratio between the mean values of the quantizer output and input.

2.3.2 BIBO or One-norm Criterion

In [Sch92] the bounded input bounded output (BIBO) criterion which is based on the worst case assumption was improved by using modulator invariance behavior to positive scaling of the feedback filter $H(z)$. This is shown from Fig. 2.6 in which a positive gain $K > 0$ is placed in front of the quantizer. Obviously since $\text{sgn}(kx) = \text{sgn}(x)$ this won't alter the behavior of the modulator. However, it does change the noise and signal transfer

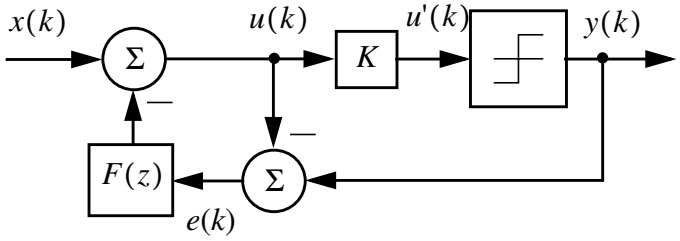

Figure 2.6 : A ΔΣ modulator with a positive gain element in front of the quantizer.

functions. One can show that for $K = 1$: $F(z) = 1 - NTF(z) = \dfrac{H(z)}{1 + H(z)}$ where $NTF(z)$ is the noise transfer function and $H(z)$ the loop filter. Placing a gain factor K in front of the quantizer in Fig. 2.6 is like scaling the loop filter $H(z)$ in Fig. 2.3. In order to get different $F(z)$ in Fig. 2.6 resulting in exactly the same modulator with exactly the same stability properties:

$$F_K(z) = \frac{K \cdot H(z)}{1 + K \cdot H(z)} = 1 - NTF_K(z) \tag{2.6}$$

where $NTF_K(z)$ was given in (2.5).

For BIBO stability in one-bit quantizer (±1 output) in Fig. 2.6 we need to ensure $|e(n)| \le 1$. With this assumption one can write the following inequality:

$$\begin{aligned} |u(n)| &\le |x(n)| + \left| \sum_{i=0}^{\infty} f_K(i) e(n-i) \right| \\ &\le \|x\|_\infty + \left| \sum_{i=0}^{\infty} f_K(i) e(n-i) \right| \\ &\le \|x\|_\infty + \left| \sum_{i=0}^{\infty} f_K(i) \right| \\ &\le \|x\|_\infty + \|f_K\|_1 \end{aligned} \tag{2.7}$$

where $\| \ \|_\infty$ and $\| \ \|_1$ are the infinity and one-norm of a sequence. Assuming $|u(n)| \le 2$ guarantees that $|e(n)| \le 1$, so the BIBO condition for stability is

$$\|f_K\|_1 \le 2 - \|x\|_\infty \tag{2.8}$$

The one-norm of $NTF_K(z)$ is defined as $S(K)$ in [Risb94]:

$$S(K) = \|ntf_K\|_1 = \sum_n |ntf_K(n)| \tag{2.9}$$

where $ntf_K(n) = \mathcal{Z}^{-1}[NTF_K(z)]$. Since $ntf_K(0) = 1$ to ensure causality, which means the modulator loop is not delay free, from (2.6) and (2.9): $\|f_K\|_1 = S(K) - 1$. Therefore the BIBO condition shown in (2.8) can be expressed as

$$\|x\|_\infty \le 3 - S_{min} \tag{2.10}$$

where S_{min} is the global minimum of $S(K)$.

It has been shown [Sch89] that the one-norm condition is conservative for second order lowpass modulators, for example the standard second-order modulator fails the one-norm test.

2.3.3 Two-norm Criterion

Recently Risbo [Risb94] modified the mean square error criterion introduced in [Ard87]

and came up with a very interesting stability criterion. This stability test uses a two-norm of $NTF_K(z)$ which can be written from the general linearized model shown in Fig. 2.3 as:

$$\begin{aligned} A(K) &= \sum \left| ntf_K(n) \right|^2 = \left\| ntf_K \right\|_2^2 \\ &= \int_0^1 \left| NTF_K(e^{j2\pi f}) \right|^2 df \end{aligned} \tag{2.11}$$

where recall $NTF_K(z) = \dfrac{1}{1 + K \cdot H(z)}$.

Now since the transfer function between quantization noise $e(k)$ and $y(k)$ is known,

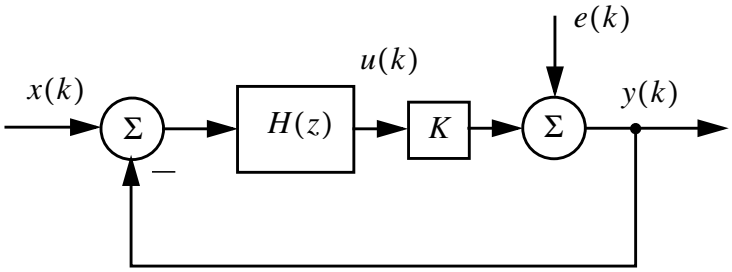

Figure 2.7 : A general ΔΣ modulator with linearized quantizer model.

assuming $e(k)$ a zero mean white stochastic noise, the output variance can be expressed as:

$$\begin{aligned} V\{y(n)\} &= \sigma_e^2 \cdot A(K) \\ &= E\{y^2(n)\} - E^2\{y(n)\} = 1 - m_y^2 \end{aligned} \tag{2.12}$$

where m_y is the output DC (mean value). The second line in (2.12) is based on the fact that ± 1 $y(n)$ sequence has fixed unity output power. Equation (2.12) shows why $A(K)$ is called *noise amplification factor* [Risb94].

From (2.12) making use of the result for Gaussian pdf of signal at input of the quantizer [Ard87]:

$$A(K) = \frac{1 - m_y^2}{1 - m_y^2 - \frac{2}{\pi}\exp\left(-2(erf^{-1}(m_y))^2\right)} \quad . \tag{2.13}$$

Fig. 2.8 shows the modulator's noise amplification A respect to the output mean value with Gaussian pdf assumption. As shown the maximum value of A (A_{min}) is 2.75 for the zero input case. Risbo [Risb94] distinguished A for chaotic[1] and every high order

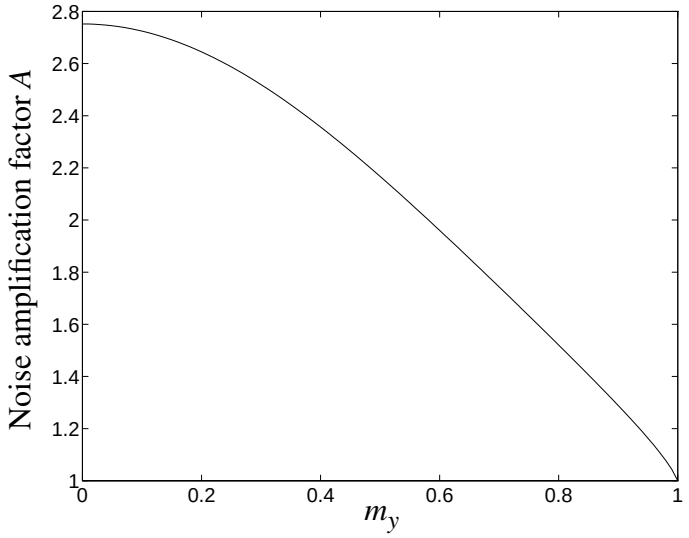

Figure 2.8 : Noise amplification factor A against m_y.

modulator (N > 2) which are convex with a global minimum somewhere in the middle of the stable K-interval and A becomes infinite at the endpoints of the stable K-interval. $A(K)$ for a third-order multiple-pole lowpass modulator is shown in Fig. 2.9a. The infinite values of A at endpoints of stable K-interval can be related to the root locus of the NTF_K of the modulator versus K variation. As shown in Fig. 2.9b, from the linear analysis, the modulator can be stable only in $K \in$ [0.5 1.15] interval.

It is shown [Risb94] that the Gaussian pdf assumption doesn't hold for many modulators. For example, in the preceding third-order multiple-pole A_{min} = 9.34 which is much higher than 2.75 predicted by the Gaussian pdf assumption for zero input shown

1. So called chaotic modulator refers to one in which some of the loop filter's poles are outside unit circle.

in Fig. 2.8.

Although the two norm criterion combined with root locus stability test (or any other conventional method) is approximate, one can get enough information to improve designs and compare them. For example, for a third-order design the following two systems have been studied:

1) a modified multiple-pole third-order modulator with $\alpha_1 = 0.35$, $\alpha_2 = 0.7$ and $\alpha_3 = 1$ [Bai94], where α coefficients are the gains of three integrators in third-order loop.

2) a spread-pole third-order modulator in which the loop filter pole frequencies obtained by a *NTF* optimization [Sch93]:

$$f_i \in \left\{0, \pm\sqrt{\frac{3}{5}} \cdot f_b\right\} \tag{2.14}$$

and the loop filter zeros for OSR = 64 are given in [Risb94] to ensure a good stability condition:

$$z_{1,2} = 0.7752 \pm j\sqrt{0.0663} \tag{2.15}$$

The *A* and root locus of these systems are shown in Fig. 2.10. As shown in Fig. 2.10a the

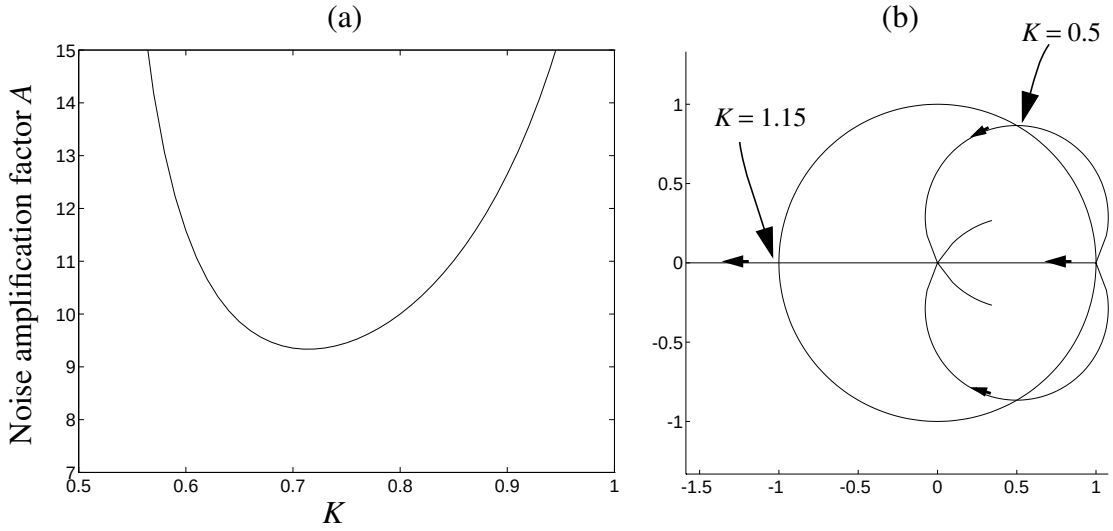

Figure 2.9 : (a) Noise amplification factor *A* versus *K* for a third-order multiple-pole lowpass modulator, (b) $NTF_K(z)$ root locus versus *K*.

modified multiple-pole third-order system has A_{min} = 4.04 which is lower than the one shown in Fig. 2.9. The spread-pole system as shown in Fig. 2.10a produces an A_{min} = 2.31, lower than 2.75 for Gaussian pdf assumption. Its root locus *i.e.* the inner curve shown in Fig. 2.10b exits the unit circle for lower K value (0.5 as opposed to 1.0 in the multiple-pole system). The lower gain is more desirable since higher input signal levels can be accommodated before reaching an unstable situation.

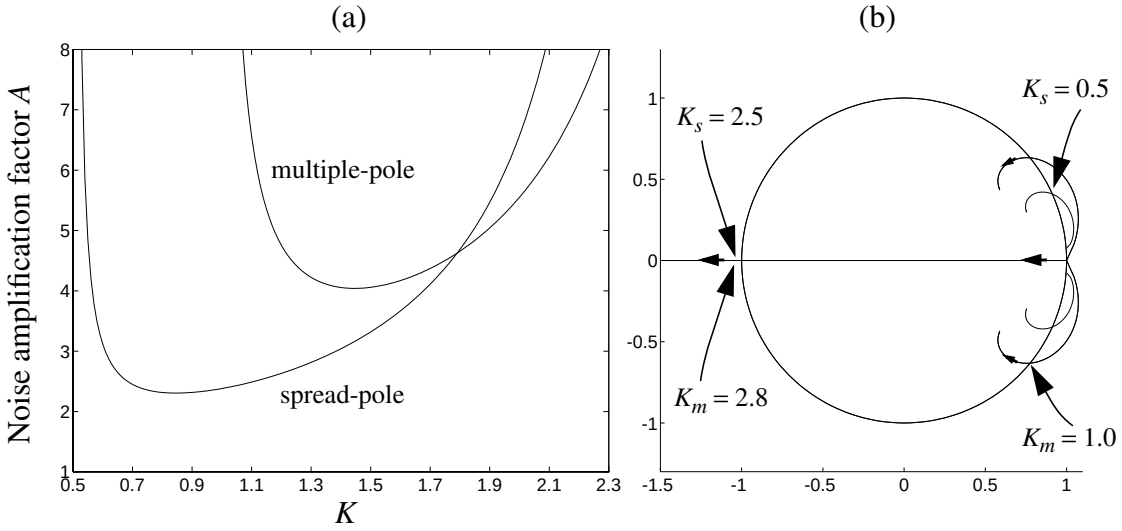

Figure 2.10 : (a) Noise amplification factor A versus K for a modified third-order multiple-pole lowpass modulator and a spread-pole design, (b) $NTF_K(z)$ root locus versus K, where K_m stands for

From the global minimum of A *i.e.* A_{min} which only depends on the loop filter the maximum stable amplitude (MSA) can be achieved by making use of (2.13) [Risb94]:

$$A_{\text{Gauss}}(\text{MSA}) = A_{min} \qquad (2.16)$$

The empirical results have shown that the MSA derived on the assumption of Gaussian pdf are very accurate [Risb94] for high-order modulators.

However, Risbo reported [Risb94] that the two-norm criterion by itself didn't predict the reliability of a high order modulator very well. He has proposed an optimization strategy which is based on a mixture of one-, two- and infinity-norm constraints. The latter had been mentioned before by Lee [Lee87a] which constraints the gain of the noise transfer function at every frequency to be less than 2. Risbo made use of the poles of the loop filter-prototypes presented in [Sch93] and optimized the loop filter zeros to achieve the

most reliable and stable condition.

The author believes the stability criteria presented to date would help a designer to come up to a modulator as a good starting point. However, to ensure a robust stability giving the desired *SNR*, simulations are the most reliable method.

2.4 Summary

The idea of continuous-time ΔΣ modulators and bandpass modulators have been reviewed. The second part of the chapter was devoted to the stability issue in a ΔΣ modulator as a major concern in any ΔΣ modulator design. One-norm, two-norm and infinity-norm constraints as some interesting checks for a ΔΣ stability have been reviewed. At the end a recent method which makes use of all mentioned stability constraints was discussed.

Chapter 3

Continuous-Time Delta-Sigma Modulator Transfer Function Design

Early designs of continuous-time ΔΣ modulators were approximate, guided by the intuition that the general continuous-time integrators *i.e.* ω_o/s should work for lowpass modulators and correspondingly the continuous-time resonators $\omega_o s/(s^2+\omega_o^2)$ for bandpass modulators. However, this simple assumption leads to implementation of an incorrect loop transfer function for a ΔΣ modulator. In this chapter it is shown that a continuous-time ΔΣ loop filter has to be designed according to the digital-to-analog converter (DAC) output waveform in the feedback path of the modulator. A simple explanation is that the continuous-time filters respond to an input signal continuously, unlike the switched-*C* filters in which an analog charge is supplied to the filter at a clock phase ϕ and the output analog voltage is ready at a clock phase $\overline{\phi}$. So, a switched-*C* filter doesn't see the variations of the input signal during the clock period ϕ and $\overline{\phi}$. On the other hand, from the linear system theory the output of a continuous-time filter is the result of convolution of the filter response with the input signal in the time interval $t \in [-\infty, \infty]$. Several continuous-time ΔΣ loop filters associated with different DAC pulse waveforms have been studied in this chapter.

3.1 Transformation of a Discrete-Time Delta-Sigma Modulator to a Continuous-Time Delta-Sigma Modulator

A block diagram of a continuous-time ΔΣ modulator is shown in Fig. 3.1. Because of the

presence of a sampler inside the loop (the quantizer is clocked, making for implicit sampling) the overall loop transfer function in a continuous-time modulator is really a discrete-time transfer function! In other words as shown in Fig. 3.2 the loop transfer

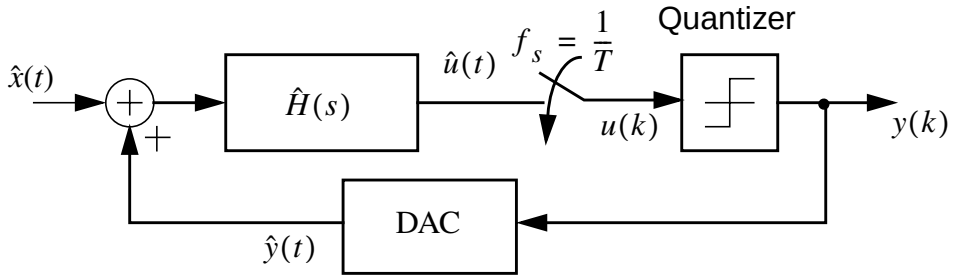

Figure 3.1 : A continuous-time ΔΣ modulator.

function from the output of quantizer back to its input has an exact equivalent z-domain transfer function $H(z)$. This doesn't mean that the waveforms inside the loop are

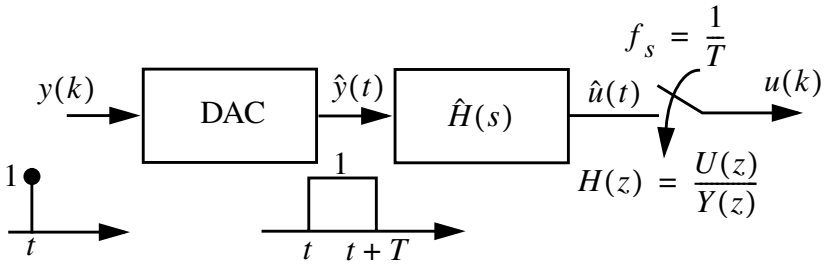

Figure 3.2 : ΔΣ open loop block diagram.

sampled-data like the ones in a switched-C (discrete-time) modulator. However, the sample values of the continuous-time waveform at the input of the quantizer at the sample times define an exact discrete-time impulse response for the continuous-time loop. In order to clarify this statement two examples of a second-order lowpass and a second-order bandpass ΔΣ modulators with loop transfer functions of $z^{-1}(2-z^{-1})/(1-z^{-1})^2$ and $z^{-2}/(1+z^{-2})$ are given here briefly. The loop impulse responses of these discrete-time systems and their corresponding continuous-time

counterparts are shown in Fig. 3.3 and Fig. 3.4 respectively. As shown in these figures

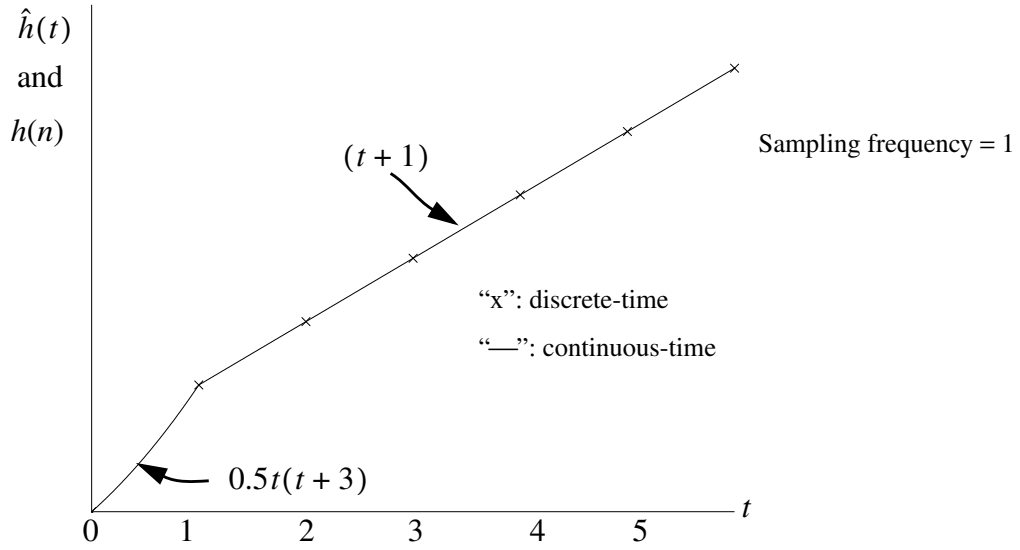

Figure 3.3 : Open-loop impulse response of the second-order lowpass modulator.

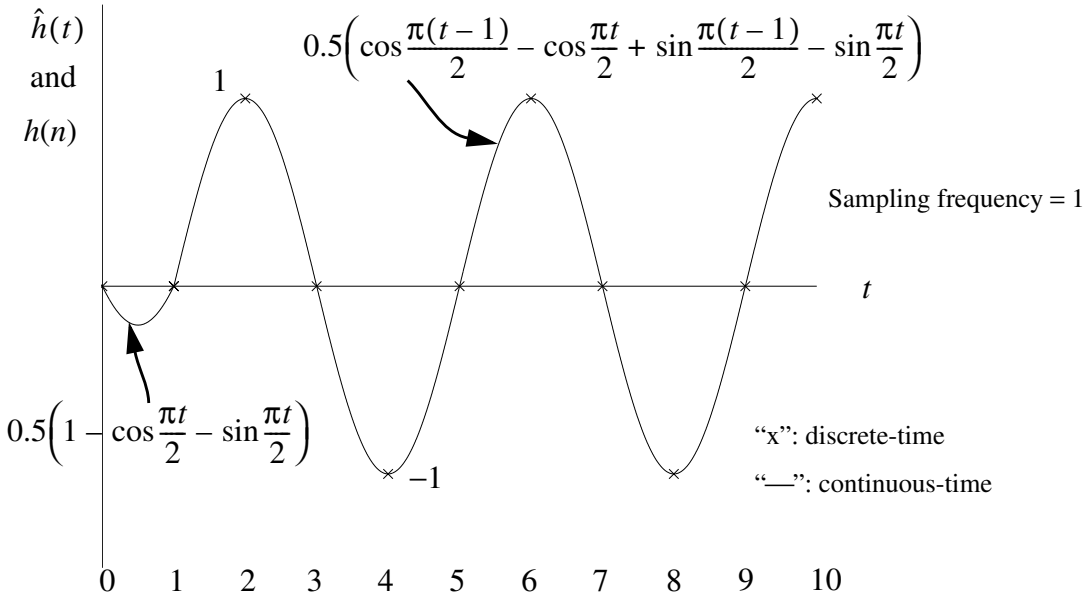

Figure 3.4 : Open-loop impulse response of the second-order bandpass modulator.

the open-loop impulse responses of the discrete-time loop filters match the samples of the impulse response of the continuous-time modulator loops. The continuous-time waveforms shown in Fig. 3.3 and Fig. 3.4 are actually the pulse responses of the continuous-time ΔΣ loop filter as depicted in Fig. 3.2. Detailed analysis of these examples is given in Sec. 3.1.1 and Sec. 3.1.4.

The loop behavior is completely determined by what the sampler inside the loop sees at its sample times, and that can be written as a difference equation. So, if a designer wants to analyze the performance of a continuous-time ΔΣ modulator (*SNR* and stability), he/she should first derive the equivalent z-domain transfer function for the ΔΣ loop. Then further analysis can be done in the z-domain as for traditional discrete-time modulators. Therefore the noise-shaping behavior of "continuous-time" ΔΣ loops can be designed entirely in the "discrete-time" domain and the exact same noise-shaping behavior obtained for either continuous-time or discrete-time systems.

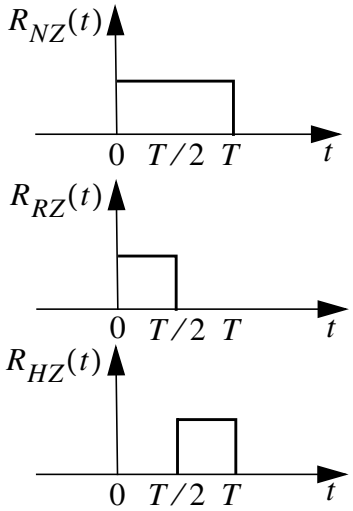

Figure 3.5 : NRZ, RZ, and HZ DAC feedback impulse responses.

Different DAC pulse shaping result in different transformations between continuous-time and discrete-time modulators. By choosing different filters, any of them can be made to match the desired z-domain behavior. We will see there are practical advantages to some over others. Three important possible DAC feedback pulses are non-return to-zero (NRZ), return to-zero (RZ), and half-delay return to-zero (HZ). Their impulse responses represented by $R_{NZ}(t)$, $R_{RZ}(t)$ and $R_{HZ}(t)$ are shown in Fig. 3.5.

3.1.1 NRZ Transformation

The ΔΣ modulator of Fig. 3.1 is shown again in Fig. 3.6 in more detail. The loop filter is represented by $\hat{H}(s)$ and the DAC transfer function by a zero-order-hold (*ZOH*) in which *p* is the opening aperture. For a return-to-zero (RZ) DAC normally *p*=*T*/2, and for a non-return-to-zero (NRZ) DAC *p*=*T*, where *T* is a sampling period. A RZ DAC reduces the nonlinearity that is caused by the fact that the area under a practical pulse depends on the levels of the preceding and following pulses [Sig90]. Fig. 3.2 shows the ΔΣ signal

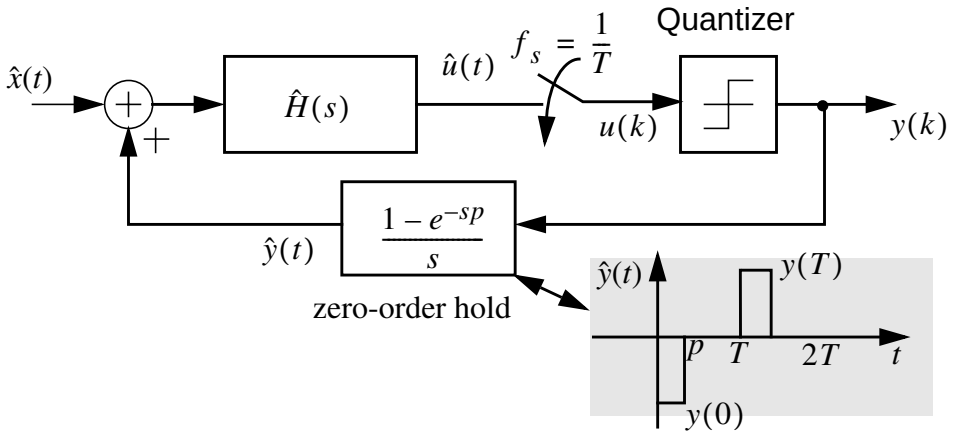

Figure 3.6 : A continuous-time ΔΣ modulator.

path from the output of quantizer back to its input for a NRZ DAC. As can be seen from Fig. 3.2 the overall ΔΣ loop gain is a discrete-time function, so one can derive the exact discrete-time transfer function, *H*(*z*), of the loop given the transfer functions of the continuous-time loop filter, $\hat{H}(s)$, and the *ZOH* as follows:

$$\mathcal{Z}^{-1}[H(z)] = \mathcal{L}^{-1}\left[\frac{1 - e^{-sp}}{s}\hat{H}(s)\right]\Bigg|_{t = nT} \qquad (3.1)$$

Equation (3.1) can be expressed in the time domain by

$$h(nT) = [R_p(t) * \hat{h}(t)]\Big|_{t = nT} = \left(\int_{-\infty}^{\infty} R_p(\tau)\hat{h}(t - \tau)d\tau\right)\Bigg|_{t = nT} \qquad (3.2)$$

where $R_p(t)$, the impulse response of *ZOH*, is a pulse with width of p as shown in Fig. 3.6, $\hat{h}(t)$ is the impulse response of the continuous-time loop filter, $h(n)$ is the overall discrete-time impulse response of the loop, and $*$ denotes time convolution. Since $R_p(t)$ has a pulse waveform, (3.1) and (3.2) are known as the pulse invariant transformation. Consider the case where $p=T$ corresponding to NRZ feedback pulse, $R_{NZ}(t)$ in Fig. 3.5. Then the loop filter NRZ pulse response from (3.2) can be described as following:

$$h(t) = R_{NZ}(t) * \hat{h}(t) = \int_{-\infty}^{\infty} R_{NZ}(\tau)\hat{h}(t-\tau)d\tau = \begin{cases} \int_0^t \hat{h}(t-\tau)d\tau & 0 \le t < T \\ \int_0^T \hat{h}(t-\tau)d\tau & t \ge T \\ 0 & t < 0 \end{cases} \quad (3.3)$$

For a continuous-time loop filter with single-poles described in residue form by

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{s - s_k} \quad (3.4)$$

the impulse response would be

$$\hat{h}(t) = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} u(t) \ . \quad (3.5)$$

Substituting $\hat{h}(t)$ into (3.3), we have

$$h(t) = \begin{cases} \int_0^t \left(\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)} \right) d\tau = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^t e^{-s_k \tau} d\tau \right] = \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k t}(e^{-s_k t} - 1) & 0 \le t < T \\ \int_0^T \left(\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)} \right) d\tau = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^T e^{-s_k \tau} d\tau \right] = \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k t}(e^{-s_k T} - 1) & t \ge T \end{cases} \quad (3.6)$$

Looking at samples of loop impulse response, $h(t)$, at sampling times *i.e.* $t=nT$ gives the discrete-time loop impulse response equivalent

$$h(nT) = \begin{cases} 0 & 0 \le t < T \\ \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k nT}(e^{-s_k T} - 1) & t \ge T \end{cases} \quad (3.7)$$

The z-domain loop transfer function of the loop then can be derived from (3.7)

$$H(z) = \sum_{n=-\infty}^{+\infty} h(n)z^{-n} = \sum_{n=1}^{\infty}\left(\sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}e^{s_k nT}(e^{-s_k T}-1)\right)z^{-n}$$
$$= \sum_{k=1}^{N}\left[\frac{\hat{a}_k}{-s_k}(e^{-s_k T}-1)\sum_{n=1}^{\infty}e^{s_k nT}z^{-n}\right] \qquad (3.8)$$
$$= \sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}\cdot\frac{(1-e^{s_k T})z^{-1}}{1-e^{s_k T}z^{-1}}$$

There are some interesting properties in the pulse invariant transformation given in (3.6)-(3.8) which have to be addressed:

1) The first sample of the loop filter pulse response is zero (3.7). This is described by a z^{-1} delay factor which always exists in the numerator of the pulse invariant transformation function (3.8). This delay is related to the causality property associated with convolution of two ordinary signals which don't contain any impulse function $\delta(t)$ component. That's why, as will be seen in the transformation of any discrete-time $\Delta\Sigma$ loop filter to a continuous-time equivalent, one delay is always absorbed in pulse transformation.

2) The overall continuous-time loop response (3.6) is described by different functions in the regions of $0 \le t < T$ and $t \ge T$, where T is the sampling period. This has already been shown in Fig. 3.3 and Fig. 3.4 for second-order lowpass and bandpass modulators respectively. It should be noted that, however, the overall loop response has continuity at T.

The equivalent discrete-time loop filter (3.8) can be written as

$$H(z) = \sum_{k=1}^{N}\frac{a_k z^{-1}}{1-z_k z^{-1}} \qquad (3.9)$$

where the new residue is

$$a_k = \frac{\hat{a}_k}{-s_k}(1-e^{s_k T}) \qquad (3.10)$$

and the new pole is at $z_k = e^{s_k T}$

Note that (3.9) is the NRZ pulse transformation of (3.4) rewritten here

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{s - s_k} \tag{3.11}$$

This has the properties one would expect: a pole at $s = 0$ transforms to one at $z = 1$, and a pole at $s = j2\pi(f_s/4)$ transforms to one at $z = j$.

As a simple example, look at the first-order lowpass modulator shown in Fig. 3.7, where continuous-time signals are distinguished with "hats" and the "zero-order hold" function converts a sample stream to a non-return to-zero (NRZ pulse) waveform. Its equations can be written by inspection:

$$y(k) = \operatorname{sgn} u(k) = \operatorname{sgn} \hat{u}(kT) \tag{3.12}$$

and

$$u(k+1) = \hat{u}([k+1]T) = \hat{u}(kT) + \frac{1}{\tau} \int_{kT}^{(k+1)T} (\hat{x}(t) - y(k))dt$$

which is a difference equation as far as $u(k)$ is concerned:

$$u(k+1) = u(k) - \frac{T}{\tau} y(k) + \frac{1}{\tau} \int_{kT}^{(k+1)T} \hat{x}(t)dt \tag{3.13}$$

Equations (3.12) and (3.13) describe (exactly!) a first-order ΔΣ loop with a feedback

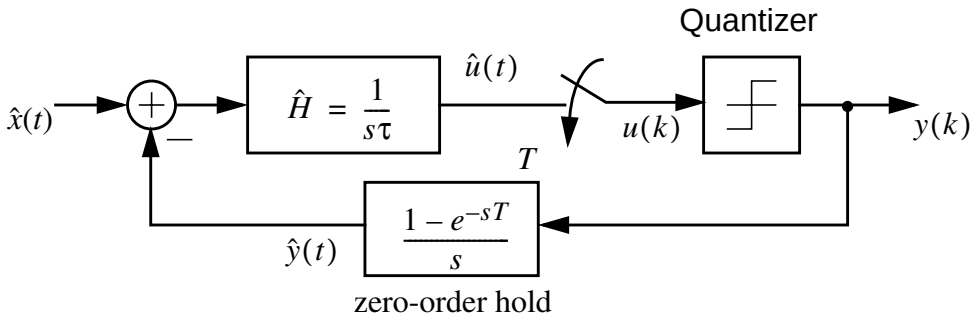

Figure 3.7 : A first-order continuous-time ΔΣ modulator.

gain T/τ and an input signal that is prefiltered by a boxcar integration (hence the comment later in Sec. 3.2 that there is an "implicit anti-alias filtering" in a continuous-

time ΔΣ modulator). It should be noted that a first-order discrete-time ΔΣ modulator with a loop filter $z^{-1}/(1-z^{-1})$ gives the difference equation:

$$u(k+1) = u(k) - y(k) + x(k) \quad .$$

This first-order continuous-time system is generalized [Thu91] using an impulse-invariant transformation, which converts term-by-term between the partial-fraction expansion of a discrete-time response $H(z)$ and a continuous-time $\hat{H}(s)(1-e^{-sT})/s$. Working with the partial-fraction expansion (the first step of inverting the Laplace transform) is the way to guarantee that the impulse responses are equal at sample times kT, and the $(1-e^{-sT})/s$ term accounts for the zero-order hold at the DAC feedback to the continuous-time filter.

Applying (3.10) to the first-order case with $\hat{H}(s) = 1/s$ gives an unfortunate cancellation: $a_k = (1/0)(1-e^{0T}) = 0/0$, but the ambiguity is easily resolved either by using L'Hôpital's rule or by taking a limit of (3.10) as $s_k \to 0$. Looking at an expansion of $e^{s_k T}$:

$$a_k = \frac{\hat{b}_k}{-s_k}(1-e^{s_k T}) = \frac{\hat{a}_k}{-s_k}(1-(1+s_k T+\ldots))$$

shows that for poles at DC

$$s_k = 0 \Rightarrow a_k = \hat{a}_k T \tag{3.14}$$

which gives the form that we found in the special case that derived (3.13). Recall from Fig. 3.7 that $\hat{a}_k = \frac{1}{\tau}$.

Equations (3.9)-(3.11) give a simple translation that allows a designer to take an arbitrary $H(z)$, rewrite it in the form of (3.9), and get an $\hat{H}(s)$ that gives an exact equivalent continuous-time loop. That's enough to design continuous-time bandpass (or lowpass, for that matter) ΔΣ converters, except for a couple of "fine points" that need to be addressed: (3.9) and (3.11) can't handle multiple poles such as those found in a conventional second-order ΔΣ modulator or its bandpass version; and high-linearity feedback DACs use RZ waveforms rather than NRZ. We'll give the corresponding equations for double-pole transfer functions in this section and the RZ and HZ transformations are given in Sec. 3.1.2.

Repeated poles in a rational function produce additional terms (besides those in (3.9)) in

the partial fraction expansion, which have the form

$$\frac{a'_k}{(z-z_k)^2} \tag{3.15}$$

The transformation for this double-pole transfer functions is given in Appendix A. The poles are moved to points s_k with $e^{s_k T} = z_k$, just as before, and the corresponding term in the continuous-time equivalent becomes

$$a'_k \frac{\dfrac{(1-e^{-s_k T}-s_k T)}{(1-e^{s_k T})^2}\dfrac{s}{T} + \dfrac{s_k^2}{(1-e^{s_k T})^2}}{(s-s_k)^2} \tag{3.16}$$

which has repeated poles, just as in the z-domain, but has a numerator with both bandpass (s) and lowpass (constant) terms.

From single-pole equations given in (3.9)-(3.11) and double-pole given in (3.15)-(3.16) it can easily be shown that a conventional second-order ΔΣ modulator with $H(z) = z^{-1}(2-z^{-1})/(1-z^{-1})^2$ has a continuous-time equivalent $\hat{H}(s) = (1+1.5sT)/s^2T^2$ which has already been derived by a different method in [Can85]. This is the example which was given in Sec. 3.1. Its filter transfer function $\hat{H}(s) = (1+1.5sT)/s^2T^2$ has the associated impulse response of $\hat{h}(t) = (t+1.5)u(t)$ where $u(t)$ is the step function. By substituting this $\hat{h}(t)$ into (3.3) the waveforms shown in Fig. 3.3 can be easily verified.

For a complex pole the numerator in (3.16) has complex coefficients, but a conjugate term $\overline{a'_k}/(z-\overline{z_k})^2$ produces a conjugate numerator term. The transfer function of a second-order bandpass ΔΣ modulator with sampling frequency four-times of the in-band signal frequency is

$$\frac{z^{-2}}{1+z^{-2}}. \tag{3.17}$$

This resonator has a pair of complex conjugate poles at $z = \pm j$ giving rise to resonance at $f_s/4$, where f_s is sampling rate. The loop impulse response of this system is a *cosine* waveform which has an unusual feature that its two first samples are zero:

$$h(n) = \begin{cases} 0 & n = 0, 1 \\ \cos\left(\dfrac{(n-2)\pi}{2}\right) & n = 2, 3, \ldots \end{cases} \tag{3.18}$$

This feature agrees with a z^{-2} factor in the transfer function given in (3.17). As was mentioned before, the pulse invariant transformation absorbs one delay in the discrete-time transfer function. The remaining delays (for example one delay in the second-order bandpass example) can be implemented digitally. So, for (3.17) first one needs again to make the partial fraction for $z^{-1}/(1+z^{-2})$.

$$H(z) = \frac{0.5z^{-1}}{1-jz^{-1}} + \frac{0.5z^{-1}}{1+jz^{-1}} \tag{3.19}$$

Applying (3.10) to (3.19) gives the second-order continuous-time equivalent

$$\hat{H}(s) = \frac{\dfrac{\pi}{4T}s + \dfrac{1}{2}\left(\dfrac{\pi}{2T}\right)^2}{s^2 + \left(\dfrac{\pi}{2T}\right)^2} \tag{3.20}$$

This represents the continuous-time loop filter of the one-delay scheme implementing the second-order modulator given in (3.17). It should be noted that in Sec. 3.1.4 it is shown that there is a zero-delay continuous-time loop transfer function solution for this example in which the loop filter's first two samples are zero. Actually Fig. 3.4 represents the continuous-time impulse response of the zero-delay second-order solution. In a zero-delay modulator there is no requirement for any digital delay inside the loop.

The overall continuous-time loop impulse response for the modulator employing the loop filter shown in (3.20) (one-delay scheme) can be obtained by substituting the impulse response of (3.20) *i.e.* $\hat{h}(t) = \dfrac{\pi}{4}\left(\cos\dfrac{\pi}{2}t + \sin\dfrac{\pi}{2}t\right)$ where $T = 1$ into (3.3)

$$h(t) = \begin{cases} h_0(t) = \dfrac{1}{2}\left(1 - \cos\dfrac{\pi}{2}t + \sin\dfrac{\pi}{2}t\right) & 0 < t \le T \\ \\ h_1(t) = \dfrac{1}{2}\left(\cos\dfrac{\pi}{2}(t-1) - \cos\dfrac{\pi}{2}t - \sin\dfrac{\pi}{2}(t-1) + \sin\dfrac{\pi}{2}t\right) & t \ge T \end{cases} \tag{3.21}$$

It should be noted that because of a z^{-1} discrete delay factor inside the loop the overall continuous-time loop impulse response is shifted by T *i.e.* $h(t-T)$ which is shown in Fig. 3.8. The discrete-time loop impulse response (3.18) represented by 'ovals' matches the continuous-time loop response (3.21) at the sampling times as shown in Fig. 3.8.

Another particularly important case [Thu91], [Lon93], [Sch94] is a fourth-order multiple-pole bandpass converter

$$H(z) = \frac{z^{-2}(2+z^{-2})}{(1+z^{-2})^2} \qquad (3.22)$$

Taking out a z^{-1} delay factor from (3.22), using (3.9)-(3.11) and (3.15), (3.16) one can

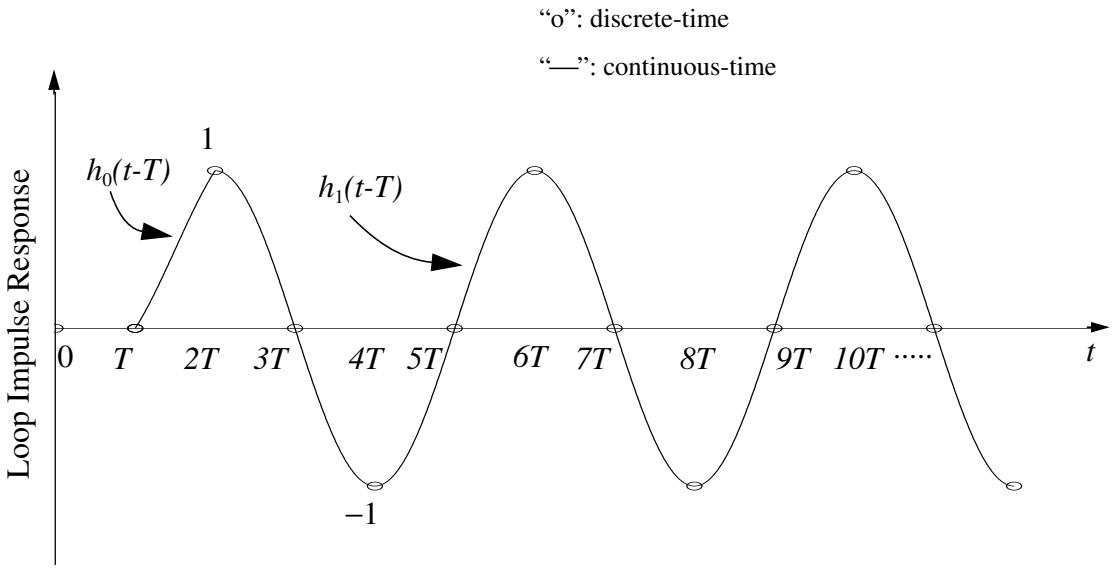

Figure 3.8 : Open-loop impulse response of the one-delay scheme second-order bandpass modulator.

derive the s-domain loop filter of the one-delay modulator scheme. This produces a fourth-order continuous-time filter with a third-order numerator and a double pole at $1/(4T) = f_s/4$

$$\hat{H}(s) = \frac{\left(\frac{\pi}{2}-\frac{1}{4}\right)\frac{s}{T}^3 + \left(\frac{3\pi^2}{16}+\frac{\pi}{4}\right)\frac{s}{T^2}^2 + \left(\frac{\pi^3}{8}+\frac{\pi^2}{16}\right)\frac{s}{T^3} + \frac{3}{4}\left(\frac{\pi}{2T}\right)^4}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \qquad (3.23)$$

The discrete-time loop impulse response of this system (3.22) is

$$h(n) = \begin{cases} 0 & n = 0, 1 \\ -(0.5n + 1)\cos\left(\frac{n\pi}{2}\right) & n \geq 2 \end{cases} \quad (3.24)$$

It can be shown that the NRZ pulse response of the continuous-time multiple-pole fourth-order loop filter given in (3.23) results in the overall continuous-time loop impulse response, $\hat{h}(t)$. For normalized $T = 1$:

$$h(t) = \begin{cases} h_0(t) = 0.75 - 0.25(3 + t)\cos\left(\frac{t\pi}{2}\right) + 0.25(4 + t)\sin\left(\frac{t\pi}{2}\right) & 0 < t \leq T \\ h_1(t) = (1.5 + 0.5t)\sin\left(\frac{t\pi}{2}\right) & t \geq T \end{cases} \quad (3.25)$$

It should be noted that because of a z^{-1} discrete-delay factor inside the loop the overall continuous-time loop impulse response is shifted by T. The continuous-time loop impulse response (3.25) matches the discrete-time loop response (3.24) at sampling times as shown in Fig. 3.9.

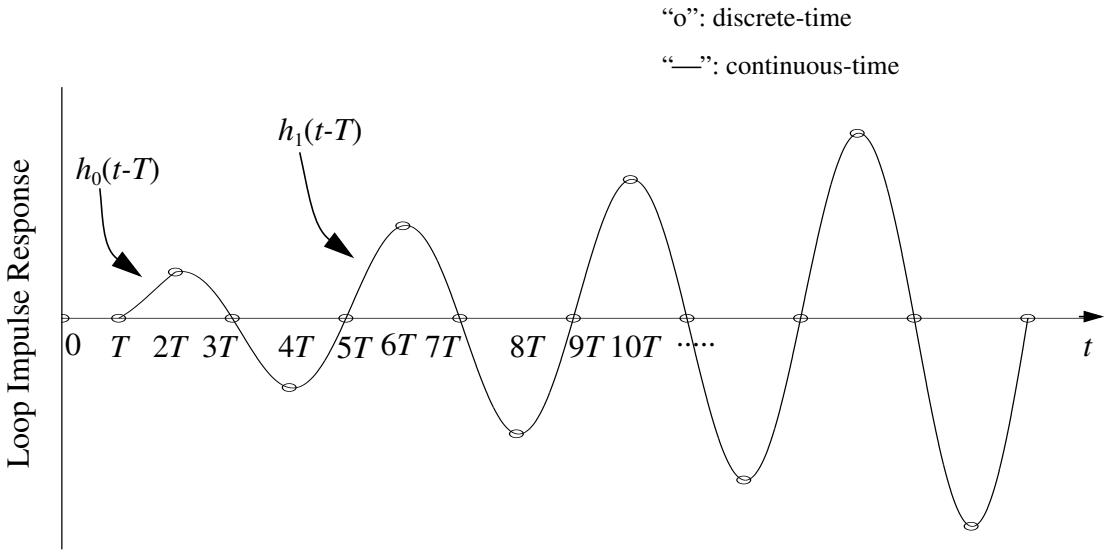

Figure 3.9 : Open-loop impulse response of the one-delay scheme fourth-order bandpass modulator.

The simple way to build a double pole, in continuous time, is with a pair of bandpass resonators [Thu91], [Gail89], [Tro93] but that approach gives a numerator with only an

s^2 term, which doesn't give the right $\hat{H}(s)$. We will show an appropriate structure in Ch. 4 and Ch. 5 to realize the preceding transfer function.

3.1.2 RZ and HZ Transformation

A second generalization of (3.9)-(3.11) is needed to allow the use of return-to-zero (RZ) and half-delay return to-zero DAC waveforms like the ones shown in Fig. 3.5. The effect this has is to change the integration (convolution) boundary in (3.3) from $[0, T]$ (for NRZ DAC) to $\left[0, \frac{T}{2}\right]$ and $\left[\frac{T}{2}, T\right]$ for RZ and HZ DACs respectively.
In an RZ DAC the zero-order hold, $(1 - e^{-sT})/s$, is replaced with a half-sample hold, $(1 - exp(-sT/2))/s$, which would just make a straightforward change in (3.10) for the single pole case

$$a_k = \frac{\hat{a}_k}{-s_k}(1 - e^{s_k T/2})e^{s_k T/2} \tag{3.26}$$

Correspondingly in an HZ DAC the zero-order hold, $(1 - e^{-sT})/s$, is replaced with a half delayed half-sample hold, $exp(-sT/2)(1 - exp(-sT/2))/s$, which would just need another straightforward change in (3.10) for the single pole case

$$a_k = \frac{\hat{a}_k}{-s_k}(1 - e^{s_k T/2}) \tag{3.27}$$

It can be shown that the RZ pulse transformation of the double-pole function given in (3.15) is

$$a'_k e^{-s_k T} \frac{\frac{(1 - e^{-s_k T/2} - s_k T(1 - 0.5e^{-s_k T/2}))}{(1 - e^{s_k T/2})^2}\frac{s}{T} + \frac{s_k^2(1 - 0.5e^{-s_k T/2})}{(1 - e^{s_k T/2})^2}}{(s - s_k)^2} \tag{3.28}$$

and its HZ pulse transformation is

$$a'_k e^{-s_k T/2} \frac{\frac{(1 - 0.5 s_k T - e^{-s_k T/2})}{(1 - e^{s_k T/2})^2}\frac{s}{T} + \frac{0.5 s_k^2}{(1 - e^{s_k T/2})^2}}{(s - s_k)^2} \tag{3.29}$$

The multiple-pole transformation is actually an extension of the single-pole transformation. A multiple-pole function can be considered as a function with distinct

poles in which the poles are hypothetically deviated slightly from each other. Then the single pole transformation (3.9)-(3.11) for NRZ and (3.26), (3.27) for RZ and HZ respectively can easily be applied on the partial fraction expansion form of the new hypothetically single-pole functions. In the second step in order to obtain the original multiple-pole function in the other domain (say *s*-domain) one may use L'Hôpital's rule as many times as necessary ($n-1$ times for a multiple-pole function of order n). In the last step the deviated poles should approach to their original places in order to obtain the limit function value. The example of RZ and HZ double-pole transformations for *z*-domain to *s*-domain (*z2s*) is given in Appendix A.

These programs have been written in "Mathematica" [WM88]. From (3.26) and (3.28) it can be shown that the multiple-pole fourth-order system given in (3.22) has the RZ continuous-time filter (one-delay scheme) as following:

$$\hat{H}(s) = \frac{\frac{9.41421\pi - 9.65685}{16}\frac{s}{T}^3 + \frac{7.24264\pi^2 + 4\pi}{16}\frac{s}{T^2}^2 + \frac{2.35355\pi^3 + 2.41421\pi^2}{16}\frac{s}{T^3} + 1.81066\left(\frac{\pi}{2T}\right)^4}{\left(s^2 + \left(\frac{\pi}{2T}\right)^2\right)^2} \quad (3.30)$$

In Table 3.1, the corresponding NRZ and RZ continuous-time loop transfer functions for some conventional ΔΣ modulators have been shown.

Table 3.1: Examples of *s*- and *z*-domain ΔΣ Modulator Loop Transfer Functions*.

Sigma-Delta Modulators	First Order Lowpass	Second Order Lowpass	Second Order Bandpass (one resonator at $\pi/2T$)	Second Order Bandpass (one resonator at $\pi/2T$), with one digital delay in the s-domain loop	General Second Order Bandpass (one resonator at θ/T)
$H(z)$	$-\frac{z^{-1}}{1-z^{-1}}$	$-\frac{z^{-1}(2-z^{-1})}{(1-z^{-1})^2}$	$\frac{z^{-2}}{1+z^{-2}}$	$z^{-1}\cdot\frac{z^{-1}}{1+z^{-2}}$	$-\frac{z^{-1}(2\cos\theta-z^{-1})}{1-2\cos\theta z^{-1}+z^{-2}}$
NRZ $\hat{H}(s)$	$-\frac{1}{Ts}$	$-\frac{1+1.5Ts}{T^2s^2}$	$\frac{-\frac{\pi}{4T}s+\frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$	$\frac{\frac{\pi}{4T}s+\frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$	$\frac{\frac{\theta}{T}\cdot\frac{\cos2\theta-\cos\theta}{2\sin\theta(1-\cos\theta)}s-\frac{\theta^2}{T^2}\cdot\frac{\sin2\theta-\sin\theta}{2\sin\theta(1-\cos\theta)}}{s^2+\frac{\theta^2}{T^2}}$
RZ $\hat{H}(s)$	$-\frac{2}{Ts}$	$-\frac{2+2.5Ts}{T^2s^2}$	$\frac{-\frac{2.414\pi}{4T}s+\frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$	$\frac{-\frac{\pi}{4T}s+\frac{2.414}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$	$\frac{\frac{\theta}{T}\cdot\frac{\cos\frac{3\theta}{2}-\cos\theta}{2\sin\theta\left(1-\cos\frac{\theta}{2}\right)}s-\frac{\theta^2}{T^2}\cdot\frac{\sin\frac{3\theta}{2}-\sin\theta}{2\sin\theta\left(1-\cos\frac{\theta}{2}\right)}}{s^2+\frac{\theta^2}{T^2}}$

*. The given loop functions are for a modulator with a "summer" as opposed to subtracter in front like Fig. 3.1.

3.1.3 NRZ and RZ Transformations in State Space Form

Any linear system can be expressed by a set of state space equations. In this subsection the discrete-time and continuous-time state space equivalent equations corresponding to the NRZ and RZ transformations given in Sec. 3.1.1 and Sec. 3.1.2 are presented.

A continuous-time and a discrete-time equivalent modulator loop filters represented by their state-space parameters are shown in Fig. 3.10. The continuous-time system is described respectively as the following:

$$\begin{aligned} \boldsymbol{u}'_c(t) &= \boldsymbol{A}_c\boldsymbol{u}_c(t) + \boldsymbol{b}_c\hat{y}(t) \\ \hat{u}(t) &= \boldsymbol{c}_c^T\boldsymbol{u}_c(t) + d_c\hat{y}(t) \end{aligned} \tag{3.31}$$

where $\boldsymbol{u_c}(t)$ is a vector of N states, $\boldsymbol{u}'_c(t)$ the time derivative of $\boldsymbol{u_c}(t)$, $\hat{y}(t)$ the input, $\hat{u}(t)$ the output as shown in Fig. 3.10a, and $\boldsymbol{A_c}$, $\boldsymbol{b_c}$, $\boldsymbol{c_c}$ and d_c the coefficients relating

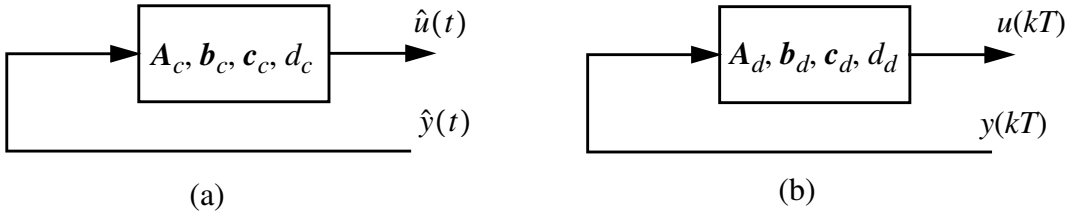

Figure 3.10 : (a) A continuous-time loop filter and (b) a discrete-time loop filter equivalent shown by their state-space parameters.

these variables. $\boldsymbol{A_c}$ is a $N \times N$ matrix, $\boldsymbol{b_c}$ and $\boldsymbol{c_c}$ are $N \times 1$ vectors and d_c is a scalar. Correspondingly the discrete-time equivalent filter shown in Fig. 3.10b can be expressed as

$$\begin{aligned} \boldsymbol{u}_d(n+1) &= \boldsymbol{A}_d\boldsymbol{u}_d(n) + \boldsymbol{b}_d y(t) \\ u(n) &= \boldsymbol{c}_d^T\boldsymbol{u}_d(n) + d_d y(n) \end{aligned} \quad . \tag{3.32}$$

It can be shown [Sch94] that for a continuous-time filter with a zero-order held input signal *i.e.* $\hat{y}(t) = \hat{y}(nT)$ for $nT \le t < (n+1)T$ where T is the sampling period, the discrete-time equivalent parameters can be obtained as the following

$$\begin{aligned} \boldsymbol{A}_d &= \exp(\boldsymbol{A}_c T) \\ \boldsymbol{b}_d &= \boldsymbol{A}_c^{-1}(\boldsymbol{A}_d - \boldsymbol{I})\boldsymbol{b}_c \end{aligned} \tag{3.33}$$

or conversely the continuous-time system can be explained from its discrete-time equivalent

$$\begin{aligned} \boldsymbol{A}_c &= \frac{1}{T}\log_e(\boldsymbol{A}_d) \\ \boldsymbol{b}_c &= (\boldsymbol{A}_d - \boldsymbol{I})^{-1}\boldsymbol{A}_c\boldsymbol{b}_d \end{aligned} . \tag{3.34}$$

This state space transformation which actually demonstrates the NRZ transformation given in Sec. 3.1.1 has already been shown in [Fra90] for state space equations and can be accomplished readily, using the MATLAB function “d2c” [MWI92].

The same transformation can be obtained for a RZ hold input too. An analysis for RZ is given in Appendix D whose final result is as the following:

$$\begin{aligned} \boldsymbol{A}_d &= \exp(\boldsymbol{A}_c T) & \boldsymbol{A}_c &= \frac{1}{T}\log_e(\boldsymbol{A}_d) \\ \boldsymbol{b}_d &= \boldsymbol{A}_c^{-1}(\boldsymbol{A}_d - \boldsymbol{A}_d^{1/2})\boldsymbol{b}_c & \boldsymbol{b}_c &= (\boldsymbol{A}_d - \boldsymbol{A}_d^{1/2})^{-1}\boldsymbol{A}_c\boldsymbol{b}_d \end{aligned} , \tag{3.35}$$

For example, the parameters of the second-order continuous-time and discrete-time lowpass modulators can be shown as the following:

$$\begin{aligned} \boldsymbol{A}_d &= \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} & \boldsymbol{A}_c &= \frac{1}{T}\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \\ \boldsymbol{B}_d &= \begin{bmatrix} 1 & -1 \\ 1 & -2 \end{bmatrix} & \boldsymbol{B}_c &= \frac{1}{T}\begin{bmatrix} 1 & -1 \\ 0.5 & -1.5 \end{bmatrix} \end{aligned} , \tag{3.36}$$

It should be noted $\boldsymbol{B}_d$ and $\boldsymbol{B}_c$ are both 2×2 matrices here, each representing a two-input system. One input is the comparator’s output signal and the other is the modulator’s input signal. The Fig. 3.11 shows the state space diagrams of these modulators.

3.1.4 Zero-Delay Scheme

As mentioned, the overall loop transfer function for a continuous-time modulator is

inherently discrete-time. This is due to the presence of a sampler inside the loop as shown in Fig. 3.1. Therefore, one can implement different equivalent continuous-time modulators depending on the number of delays chosen in the digital side of the loop preceding the DAC and following the comparator. For instance, as shown in Table 3.1, the open loop transfer function of a second-order bandpass modulator is $H(z) = z^{-2}/(1+z^{-2})$. One way to implement the continuous-time loop is to apply

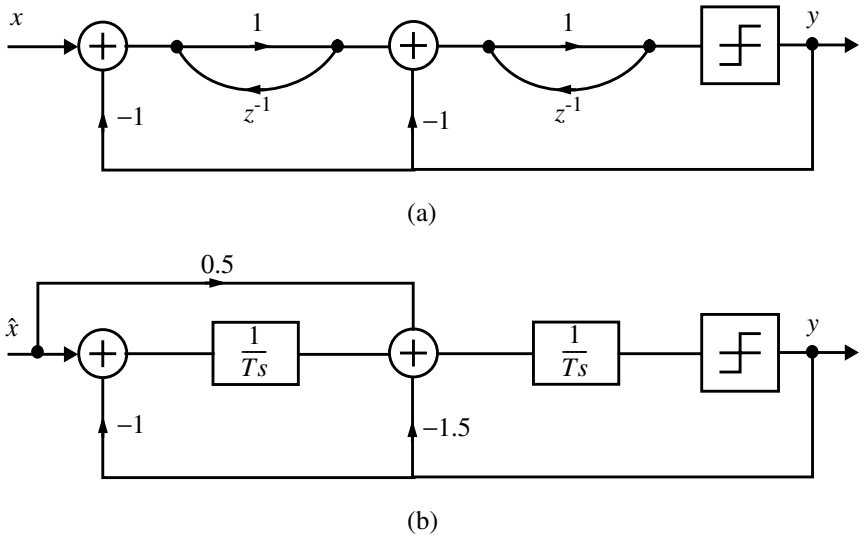

Figure 3.11 : State-space diagram of (a) a discrete-time and (b) a continuous-time second-order lowpass modulators.

the pulse invariant transformation on $H(z)$ (having no digital delay inside the loop) which gives a continuous-time loop filter with a RHP zero (a maximum phase filter) as shown in column 4 of Table 3.1 and graphically in Fig. 3.12a:

$$\hat{H}(s) = \frac{-\frac{\pi}{4T}s + \frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2 + \left(\frac{\pi}{2T}\right)^2} \qquad (3.37)$$

The overall loop continuous-time impulse response with zero discrete-time delay is already shown in Fig. 3.4. As shown in Fig. 3.4 the first two samples of the pulse response of the maximum phase continuous-time filter (3.37) is zero which removes the necessity of a discrete-time delay in the ΔΣ loop. The other way is to have one delay in

the digital side of the loop and to apply the pulse invariant transformation on the remaining part of $H(z)$, *i.e.* $z^{-1}/(1+z^{-2})$, which gives a continuous-time loop filter with a LHP zero (a minimum phase filter) as shown in column 5 of Table 3.1, and graphically in Fig. 3.12a:

$$\hat{H}(s) = \frac{\frac{\pi}{4T}s + \frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2 + \left(\frac{\pi}{2T}\right)^2} \tag{3.38}$$

The overall loop continuous-time impulse response with one discrete-time delay is already shown in Fig. 3.8. It should be noted that in the pulse invariant transformation a z^{-1} is present in the numerator of each partial fraction as shown in (3.9). Thus in order to derive a continuous-time loop filter it is required to keep at least one delay (z^{-1}) in the numerator to ensure causality. This determines the number of possible ways to implement the equivalent continuous-time modulators from a discrete-time modulator.

Obviously, for the second and multiple-pole fourth-order bandpass modulators in (3.17) and (3.22) there are two different ways to implement the continuous-time loop: the zero-delay and one-delay schemes. Both transformation schemes for this fourth-order modulator are graphically illustrated in Fig. 3.12b. The fourth-order continuous-time filter defined by (3.23) is based on the one-delay scheme. As shown in Fig. 3.12b the loop filter for one-delay scheme of multiple-pole fourth-order modulator has a real LHP zero and two complex conjugate LHP zeros. One can derive the continuous-time fourth-order loop filter for the zero-delay scheme modulator by applying the pulse transformation on the whole discrete-time loop filter (3.22) *i.e.* $z^{-2}(2+z^{-2})/(1+z^{-2})^2$. This produces a multiple-pole fourth-order filter with one real RHP zero and two complex conjugate LHP zeros as shown in Fig. 3.12:

$$\hat{H}(s) = \frac{-\left(\frac{\pi}{4}+\frac{1}{4}\right)\frac{s}{T}^3 + \left(\frac{3\pi^2}{16}-\frac{\pi}{4}\right)\frac{s}{T^2}^2 - \left(\frac{\pi^3}{16}-\frac{\pi^2}{16}\right)\frac{s}{T^3} + \frac{3}{4}\left(\frac{\pi}{2T}\right)^4}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \tag{3.39}$$

The zero-delay scheme results in the same discrete-time loop impulse response as the one (or higher)-delay scheme with a lower cost. The loop filter complexity in the zero-delay scheme is the same as that in the one-delay scheme but the one (or higher)-delay

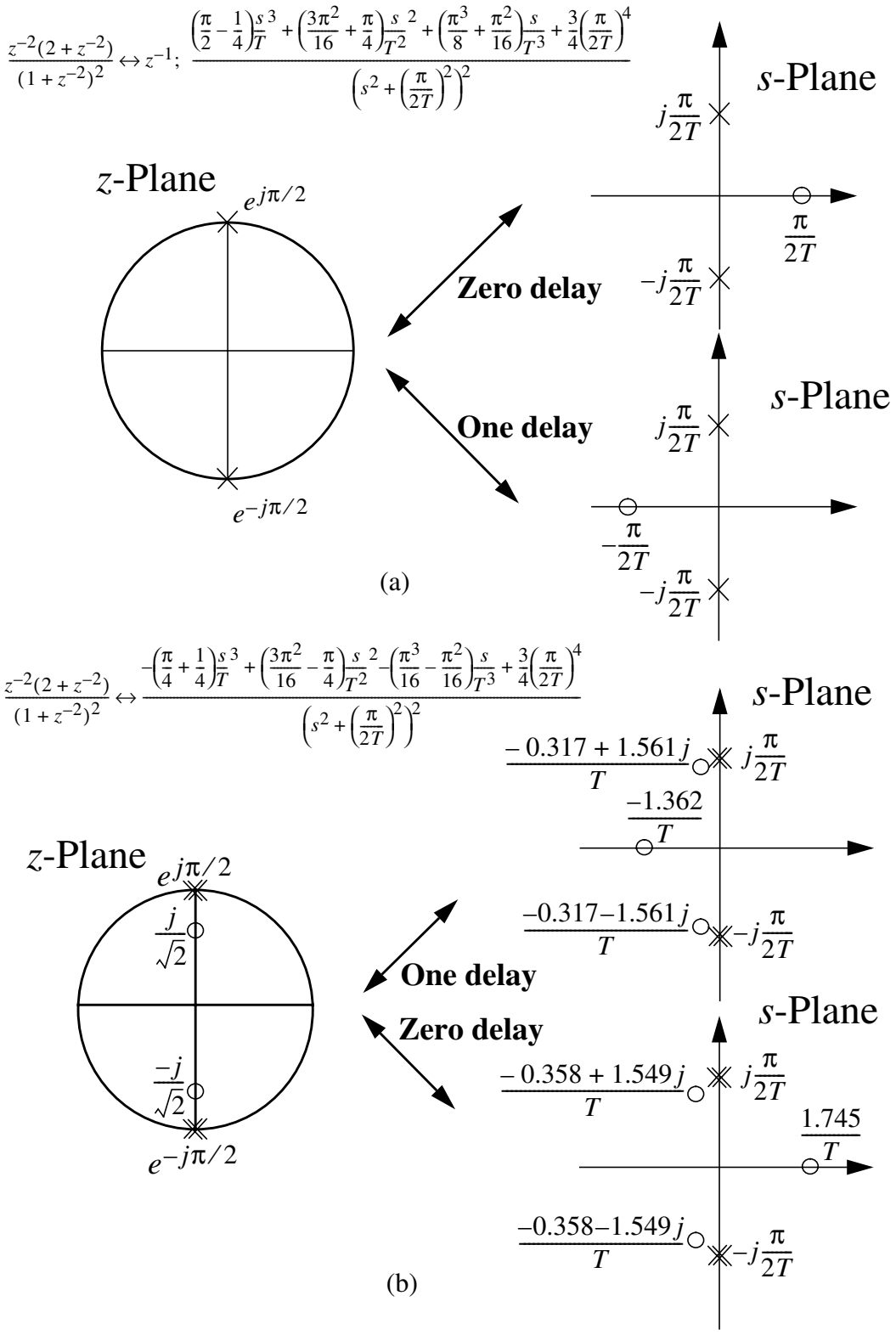

Figure 3.12 : Pole-zero mapping between continuous-time and discrete-time loop filters, (a) second-order loop, (b) multiple-pole fourth-order loop.

scheme requires extra flip-flop(s).

In the following section an analysis on the effect of any extra loop delay on a continuous-time ΔΣ modulator is given. Here a simple explanation for the zero-delay and one-delay second-order bandpass examples defined in (3.37) and (3.38) respectively will be given. As shown in Fig. 3.13 an extra loop delay (*d*) causes the samples to move

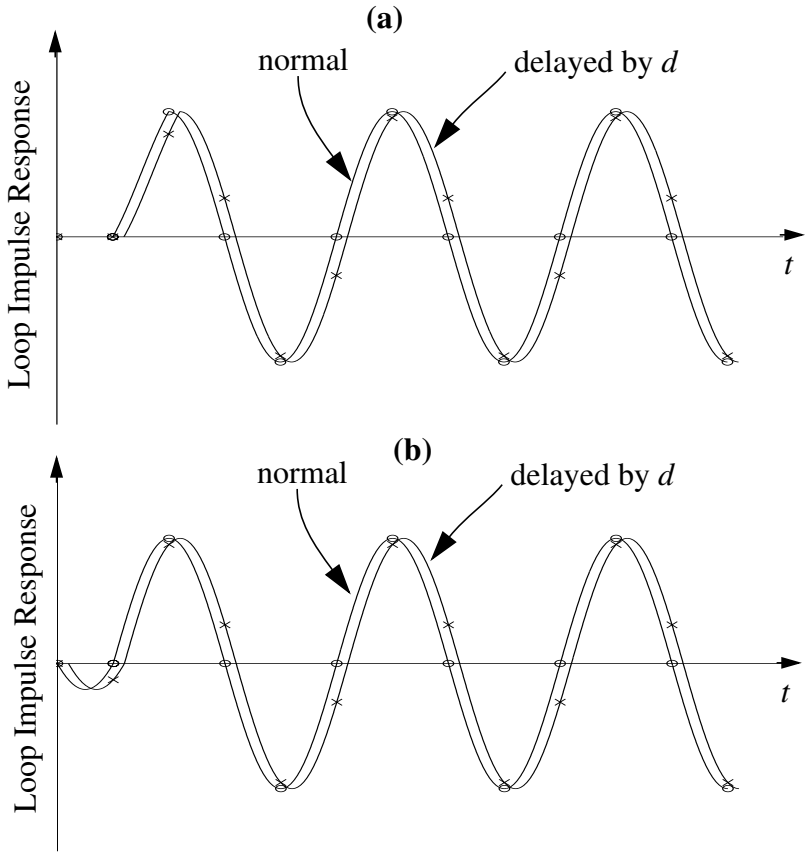

Figure 3.13 : The effect of an extra loop delay on the loop samples in the a) one-delay b) zero-delay schemes of the second-order bandpass modulators.

from their original values represented by ‘ovals’ to some incorrect values represented by ‘x’. The sampling times are assumed fixed (no clock jitter) but the loop impulse response is shifted by *d*. In the one-delay scheme Fig. 3.13a the first and second samples are correct (zeros as they should be) but the remaining samples become incorrect. In the zero-delay scheme as shown in Fig. 3.13b on the other hand, the incorrect[1] values start

from the second sample. However, it should be noted that in the zero-delay scheme $h(t)$ coincides with the ideal loop response for $t \geq T$ whereas in the one-delay scheme this happens for $t \geq 2T$. Therefore, although with an extra loop delay the second sample in the one-delay scheme is still correct (zero), the third sample is a bit more off from the ideal value than that of the zero-delay scheme as can be noticed from Fig. 3.13. The remaining samples (from the fourth sample) are affected similarly in both zero-delay and one-delay schemes. So, from this simple observation it is not very clear that which scheme (zero-delay or one-delay) is more sensitive to extra loop delays. Although ignoring those slight differences in the second and third samples one can expect that both modulators have almost identical sensitivity to extra loop delays. However, since the zero-delay scheme has one less D-flip flop (no D-flip flop for the mentioned second- and/or fourth-order modulators), the zero-delay scheme might be preferred not only because of its lower cost but because it has less propagation delay time in digital side of the modulator. In the next section the extra loop delay difficulty for some continuous-time ΔΣ examples will be analyzed. It will give some insight how the modulator's poles and zeros are affected by extra loop delays. But as will be seen it doesn't provide a general closed form formula for every modulator. Therefore, simulation remains the most trustworthy tool to illustrate the maximum tolerable extra loop delay in a continuous-time modulator.

In terms of stability, since the second-order modulator is a robust system, it can afford more non-ideal loop delay. However, in higher order modulators like the fourth-order system any extra loop delay will cost some *SNR* loss or even could result in instability in the modulator.

3.1.5 The Sensitivity of a Continuous-time ΔΣ Modulator to Unwanted Extra Loop Delays

The ideal open-loop block diagram of a continuous-time modulator was shown back in Fig. 3.2. In Sec. 3.1.4 it was explained that any extra delay in the modulator loop such as

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1. It can be noticed that the sample values form the fourth sample in the zero-delay and the one-delay schemes are the same. This is because it can be shown that $h_1(t\text{-}1)$ in the one-delay scheme given in (3.21) (shown in Fig. 3.8 too) is identical to $h(t)$ for $T \geq 1$ shown in Fig. 3.4 in the zero-delay scheme.

propagation delay time in comparator, latch, flip-flop, DAC, etc. changes the modulator open-loop response at sampling moments 0, T, $2T$, …. This was graphically shown in Fig. 3.13. In this section a more detailed analysis is given.

Any extra loop delay in a ΔΣ modulator loop can be modeled by a $e^{-s\Delta T}$ term as shown in Fig. 3.14 where $0 \le \Delta T \le T$. Notice that the hat signs for the signals in Fig. 3.2 are removed in Fig. 3.14 for simplicity. As shown in Fig. 3.14 the z-transform of the output signal $u(kT - \Delta T)$ is represented by $U(z, \Delta)$. Since the continuous-time signal $u(t)$ is delayed by ΔT which can be anywhere in the $[0, T]$ interval, the new z-transform $U(z, \Delta)$ has to convey the information of the continuous-time signal between sampling instants. This powerful tool is the well-known *modified z-transform* [Kuo63], [Hou85]. The block diagram shown in Fig. 3.14 including any loop delay can be analyzed by the modified z-transform method. The method is essentially a modification of the ordinary z-transform technique obtained by inserting non-integer time delays in the sampled-data system (including continuous-time modulator and/or a switched-C system). It should be noted that in a switched-C modulator the opamp output voltage is sampled after a safe margin of settling which includes the delays caused by comparator and so on. Therefore, in a switched-C modulator only the voltage levels at the sampling moments are important. In comparison in a continuous-time modulator the information contained in the continuous-time signal at comparator between sampling instants is crucial because of the presence of loop delay.

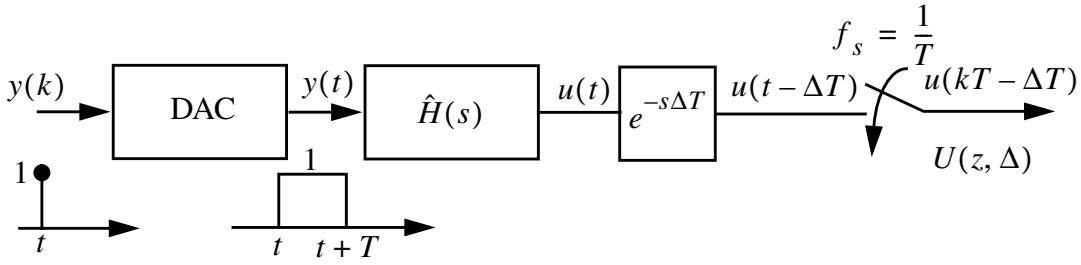


Figure 3.14 : A continuous-time ΔΣ open loop block diagram with an extra loop delay.

From Fig. 3.14 the modified z-transform of $u(t)$ which is sometimes referred to as the delayed z-transform and denoted by $U(z, \Delta)$ is expressed as

$$U(z,\Delta) = \mathcal{Z}[u(t-\Delta)] = \sum_{n=0}^{\infty} u(nT-\Delta T)z^{-n} \tag{3.40}$$

and for $\Delta = 1-m$ it can be written as [Kuo63]

$$U(z,m) = U(z,\Delta)\big|_{\Delta=1-m} = z^{-1}\sum_{n=0}^{\infty} u[(n+m)T]z^{-n} \tag{3.41}$$

It can be noticed that if the response $u(t)$ does not have any jump discontinuity at $t = 0$ when $m = 1$ $(\Delta = 0)$:

$$U(z,1) = U(z) \tag{3.42}$$

and when $m = 0$ $(\Delta = 1)$

$$U(z,0) = z^{-1}U(z)\ . \tag{3.43}$$

Here the manner of obtaining the modified z-transform is presented without proof [Kuo63]. The modified z-transform of $u(t-\Delta T)$ is given by

$$\begin{aligned}\mathcal{Z}_m[u(t-\Delta T)] &= U(z,m)\\ &= z^{-1}\sum\left[\text{residues of } \frac{e^{mT\alpha}}{1-e^{-T(s-\alpha)}}U(\alpha)\right]\\ &\qquad\qquad \text{evaluated only at poles of } U(\alpha)\big|_{z=e^{st}}\end{aligned} \tag{3.44}$$

where $U(s)$ is the Laplace transform of the original continuous-time signal $u(t)$.
For our purpose since most of the transfer functions that we are interested in are rational functions, one may use tables [Hou85]. Some frequently used functions for bandpass ΔΣ modulators are given in Table 3.2.
Now we return to our problem *i.e.* obtaining the z-transfer function of a delayed continuous-time ΔΣ open-loop system. From Fig. 3.14 first one needs to obtain the pulse response of the loop filter *i.e.* the impulse response of $\hat{H}(s)$ followed by DAC. This has been explained in Sec. 3.1.1. For example, recall that the loop response denoted by $h(t)$ for second-order and fourth-order systems were given in (3.21) and (3.25) respectively. The open-loop responses of these systems were shown back in Fig. 3.8 and Fig. 3.9. The open-loop response of the second-order system is represented again in Fig. 3.15. As shown in Fig. 3.15 and already given in (3.3) for an NRZ DAC, due to convolution of a

pulse with the loop filter response $\hat{h}(t)$ the beginning of the overall open-loop response $h(t)$ in $0 \le t \le p$ interval is always different from that in $t \ge p$, where p is the DAC aperture. This slight difference in the first sample can be neglected *i.e.* assuming

$$h(t) = h_1(t) \tag{3.45}$$

to simplify the calculation of the modified z-transform of a delayed continuous-time $\Delta\Sigma$ open-loop system.

Table 3.2: Some transform examples

time function	z-transform	modified z-transform
e^{-at}	$\frac{z}{z-e^{-aT}}$	$\frac{e^{-amT}}{z-e^{-aT}}$
$\sin(at)$	$\frac{z\sin(aT)}{z^2-2z\cos(aT)+1}$	$\frac{z\sin(amT)+\sin[(1-m)aT]}{z^2-2z\cos(aT)+1}$
$t\sin(at)$	$\frac{Tz(z^2-1)}{(z^2+1)^2}$	$T\frac{z^3 m\sin(amT)+z^2(m+1)\cos(amT)-z(2-m)\sin(amT)-(1-m)\cos(amT)}{(z^2+1)^2}$

With this approximation, for example, for the preceding given second-order system with the ordinary z-transform and discrete-time impulse response given in (3.17) and (3.18) respectively we can write:

$$\begin{aligned} \mathcal{Z}_m[h(t) = h_1(t)] &= H(z,m) \\ &= \mathcal{Z}_m\left(\mathcal{Z}^{-1}\left[\frac{z^{-2}}{1+z^{-2}}\right]\right) \\ &= z^{-1}\cdot\mathcal{Z}_m\left(\mathcal{Z}^{-1}\left[\frac{z^{-1}}{1+z^{-2}}\right]\right) \end{aligned} \tag{3.46}$$

where $\mathcal{Z}_m$ denotes to modified z-transform. From the second row in Table 3.2 when $a = \pi/(2T)$ it can be concluded that

$$H(z, m) = z^{-1} \cdot \mathcal{Z}_m\left[\sin\left(\frac{\pi}{2T}t\right)\right] = z^{-1} \cdot \frac{z\sin(m\pi/2) + \sin[(1-m)\pi/2]}{z^2 + 1} \quad .(3.47)$$

From (3.47) it can be noticed that when $m = 1$ (no extra delay) $H(z, m) = H(z)$.

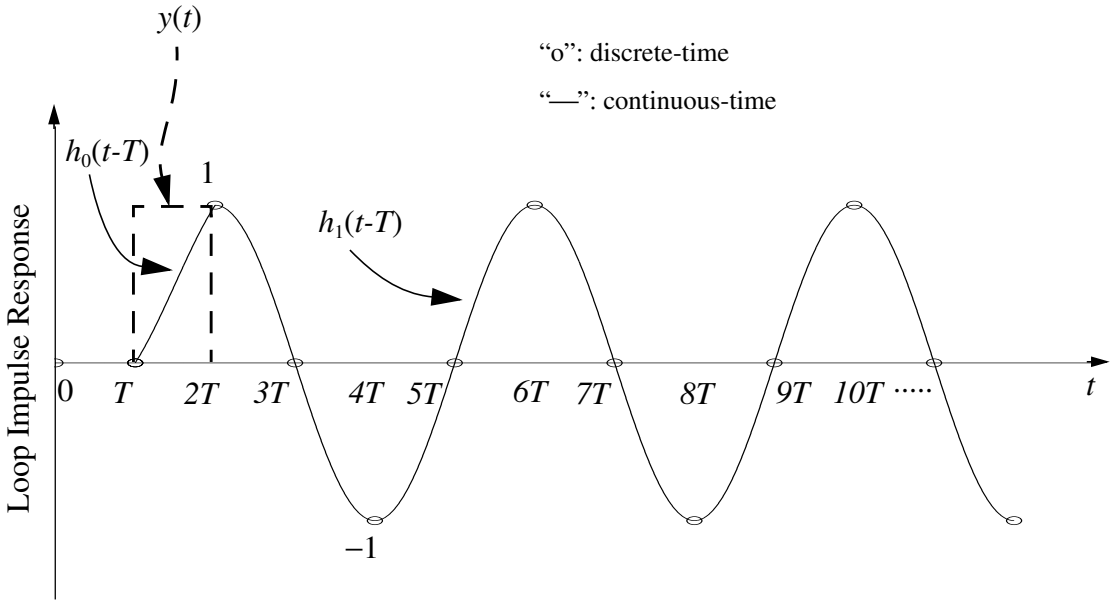


Figure 3.15 : Open-loop impulse response of the one-delay scheme second-order bandpass modulator.

The noise transfer function (*NTF*) for the new loop transfer function then is

$$\begin{aligned} NTF_m(z) &= \frac{1}{1 - H(z, m)} \\ &= \frac{1}{1 - \dfrac{z^{-2}[\sin(m\pi/2) + z^{-1}\sin[(1-m)\pi/2]]}{1 + z^{-2}}} \\ &= \frac{1 + z^{-2}}{1 - z^{-1}\sin[(1-m)\pi/2] + z^{-2}(1 - \sin(m\pi/2))} \end{aligned} \quad .(3.48)$$

From (3.48) it can be noticed that the two poles previously (with no extra delay) both at $z = 0$ now have moved from origin because of the extra loop delay represented by $(1-m)T$. The root locus of this second-order system respect to variations of m , where

$0 \le m \le 1$, is shown in Fig. 3.16. Fig. 3.16 shows the poles' movement from origin

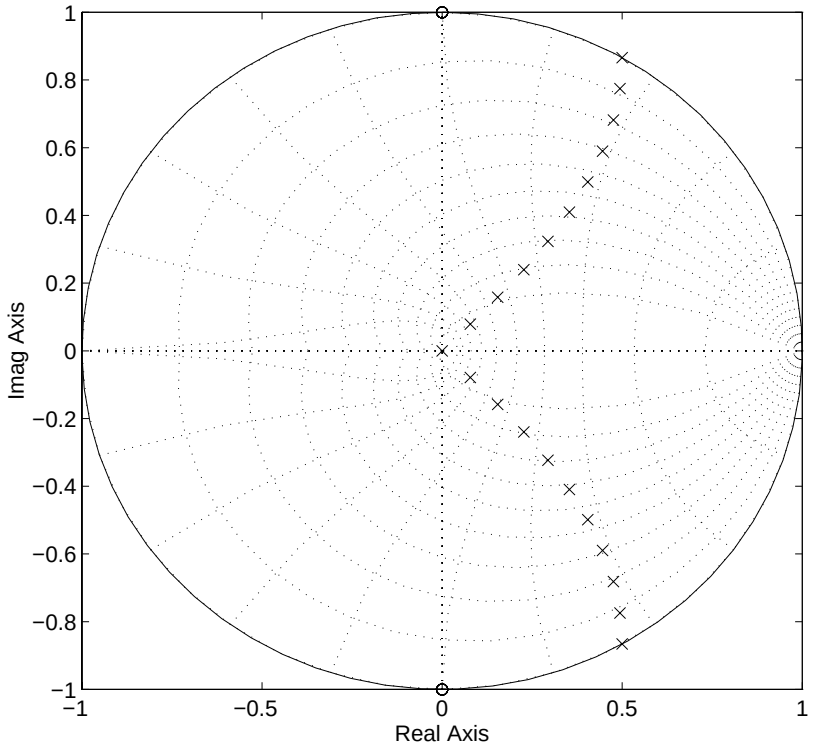


Figure 3.16 : The root-locus of the continuous-time second-order bandpass modulator with loop delay respect to m.

towards the unit circle with increment of loop delay by $0.1T$ steps ($\Delta m = -0.1$).
The same calculation is done for the fourth-order multiple-pole bandpass ΔΣ modulator given in (3.22). The open-loop modified z-transform for this fourth-order system is:

$$\begin{aligned} H(z,m) &= \mathcal{Z}_m\left(\mathcal{Z}^{-1}\left[\frac{z^{-2}(2+z^{-2})}{(1+z^{-2})^2}\right]\right) \\ &= z^{-1}\cdot\mathcal{Z}_m\left(\mathcal{Z}^{-1}\left[\frac{z^{-1}(2+z^{-2})}{(1+z^{-2})^2}\right]\right) \end{aligned} \qquad (3.49)$$

Taking out a z^{-1} delay element from the open-loop system as shown in (3.49) is equivalent to $n \leftarrow n+1$ substitution in the time domain response in (3.24) which results in

$$H(z, m) = z^{-1} \cdot \mathcal{Z}_m[(0.5n + 1.5)\sin(m\pi/2)] \quad . \tag{3.50}$$

The final result, using the transforms given in Table 3.2, is

$$H(z, m) = \frac{b_0 + b_1 z + b_2 z^2 + b_3 z^3}{z(1 + z^2)^2} \tag{3.51}$$

where the numerator coefficients are:

$$\begin{aligned} b_0 &= -0.5(1 - m)\cos(m\pi/2) + 1.5\sin[(1 - m)\pi/2] \\ b_1 &= 0.5(m + 1)\sin(m\pi/2) \\ b_2 &= 0.5(m + 1)\cos(m\pi/2) + 1.5\sin[(1 - m)\pi/2] \\ b_3 &= 0.5(m + 3)\sin(m\pi/2) \end{aligned} \quad .$$

Again from (3.51) it can easily be verified that when $m = 1$ (no extra delay) $H(z, m) = H(z)$. One interesting observation from the open-loop system represented by (3.51) is that it is no longer a fourth-order system as it was for $m = 1$. The order of the modulator has increased to five. For $m = 1$ there is a pole-zero cancellation in (3.51) at $z = 0$, so producing a fourth-order system as expected. However, in reality the continuous-time open-loop modulator is never delay free, so the noise transfer function NTF_m would always have a higher order *i.e.* five poles as opposed to four poles. Now the question is that how this affects the modulator performance. To answer this question the pole-zero root-locus of NTF_m in this fourth-order modulator has been obtained from (3.51) and plotted in Fig. 3.17. Fig. 3.17 shows the poles moving from the origin, with an increment of loop delay by $0.05T$ steps ($\Delta m = -0.05$). The poles move in three different paths. First one single positive real pole has been created which moves outside the unit circle with approximately $0.25T$ extra delay. The two complex conjugate LHP poles move more quickly outside the unit circle at approximately $0.20T$ extra loop delay. The RHP complex conjugate poles stay inside the unit circle for $0 \le m \le 1$.

It should be noted that from (3.46) and (3.49) a z^{-1} was taken out and the modified z-transform in (3.47) and (3.50) was applied to the remaining parts. This may be interpreted to show that the obtained results in (3.47) and (3.51) only represent the modified z-transform of the one-delay scheme. This is not exactly true. Recall from

(3.45) that the preceding analysis was made assuming that $h(t) = h_1(t)$ for $t \geq T$ (NRZ DAC). It should be mentioned too that in the one delay scheme, for example as shown in Fig. 3.13 for the second-order modulator, $h(t) = h_1(t)$ for $t \geq 2T$ whereas in the zero-delay $h(t) = h_1(t)$ for $t \geq T$. Therefore with the preceding approximation as can be noticed from Fig. 3.13, a smaller error is assumed for the third sample in the one-delay scheme and the second sample error in the zero-delay scheme is completely ignored. Therefore, accepting these slight errors in fact the modified z-transforms obtained for both second and fourth-order systems are applicable for both zero-delay and one-delay schemes.

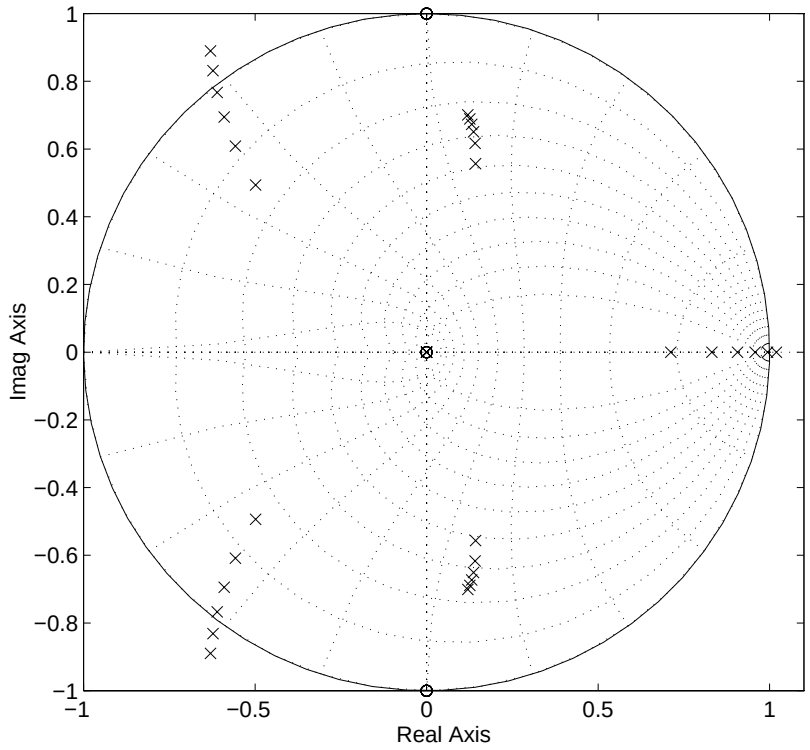


Figure 3.17 : The root-locus of the continuous-time fourth-order multiple-pole bandpass modulator with loop delay respect to *m*.

From the analysis made in this section for the second and fourth-order examples some conclusions can be drawn as follows:

1) The *NTF* zeros are still on the unit circle at the desired locations. Therefore, one can expect to get normal noise-shaping inside the band with extra loop delay (to some

extent). Therefore, *SNR* should not degenerate significantly up to some extra loop delay extent too (in the next section it is shown that in a fourth-order modulator a 10 % extra loop delay produces about 6dB *SNR* loss).

2) The major problem that arises from an extra loop delay is seemed to be associated with the modulator stability as the loop poles move towards the unit circle. So, it is believed that for a real implementation some special considerations should be taken to keep the modulator's extra loop delay by a safe margin. More details for a real implementation and extra loop delays are given in Sec. 8.3.2.

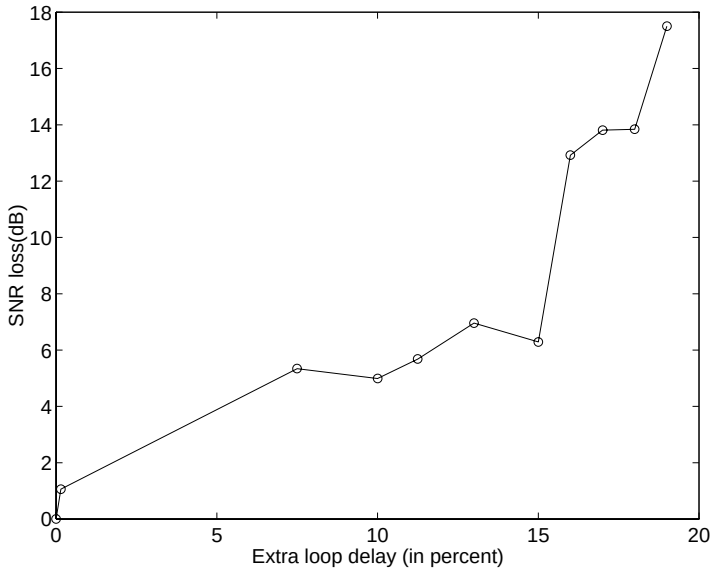


Figure 3.18 : *SNR* loss in a 2MHz bandwidth respect with extra loop delay percentage (d/T), where T is a clock period.

3.1.6 Simulation of $\Delta\Sigma$ Extra Loop Delay

A fourth-order multiple-pole one-delay modulator with macromodel transconductors, comparator and flip-flops has been simulated. The loop filter center frequency was at 50MHz and clock rate at 200MHz. Fig. 3.18 shows the *SNR* loss versus the percentage

of extra loop delay (compared to a clock period) at 2MHz BW for the mentioned modulator in above. The input signal levels for the extra loop delay simulations shown in Fig. 3.18 were at the maximum input amplitude (MSA) obtained from the zero excess delay simulation. As can be noticed from the data shown in Fig. 3.18, at 10% extra loop delay *SNR* drops by almost 6dB (for this OSR). Degradation of *SNR* is much sharper for extra loop delays higher than 15%. A 20% extra loop delay makes the ΔΣ modulator completely unstable. It should be noted that since the linear model with the root locus shown in Fig. 3.17 matches the simulation results, for the lower input levels (than MSA) similar responses with extra loop delay are expected.

As it was shown in Fig. 3.17 that the *NTF* poles move toward the unit circle it is reasonable to expect that some spikes to be generated in the bit-stream spectrum. Especially, the high frequency spike due to the high frequency poles shown in Fig. 3.17 should be noticeable. This was verified by the preceding simulations. For example, the spectrum of the fourth-order one-delay modulator with a 19% extra loop delay is shown in Fig. 3.19 presenting a high frequency spike.

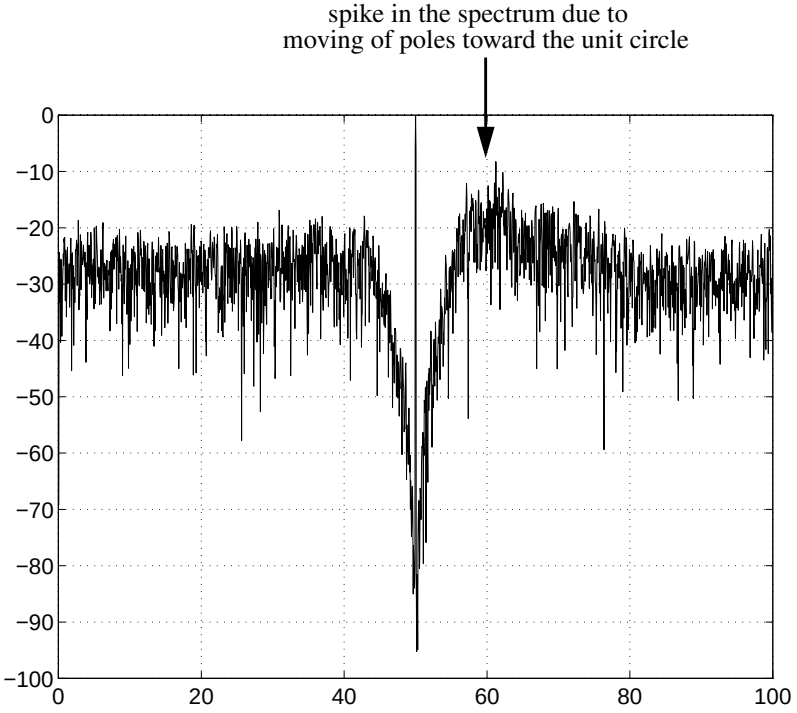


Figure 3.19 : The noise-shaping spectrum for a 19% extra loop delay.

It should be noted that similar simulations were done for the zero-delay scheme fourth-

order modulator too. The *SNR*s for both zero-delay and one delay schemes versus extra loop delay are plotted in Fig. 3.20. For the zero-delay scheme the modulator became completely unstable at 25% extra loop delay however, as shown in Fig. 3.20 its *SNR* drops rapidly with loop delays higher than 20%.

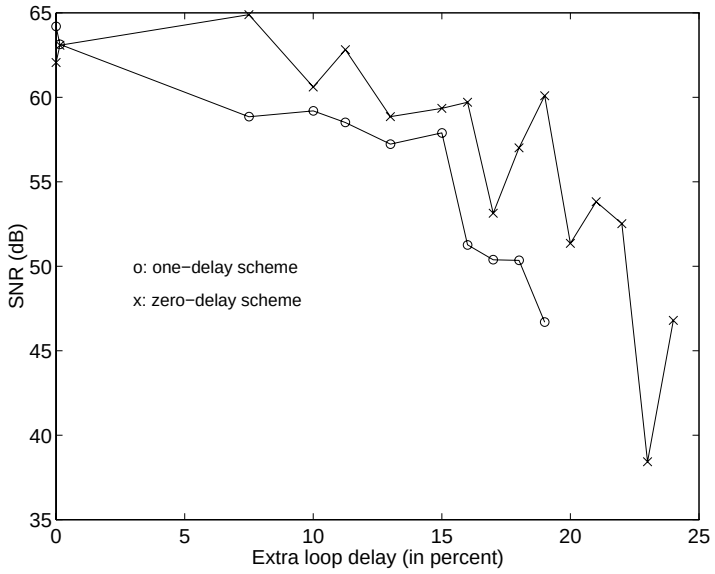


Figure 3.20 : *SNR* in both one-delay and zero-delay schemes for a 2MHz bandwidth respect with extra loop delay percentage (d/T), where T is a clock period.

3.1.7 The Signal Transfer Function

A discrete-time modulator could be expressed with a configuration shown in Fig. 3.21 [Jant93] in which $G(z)$ and $H(z)$ represent feedforward and loop transfer function respectively. The noise transfer function (*NTF*) and the input signal transfer function (*STF*) can be found from $G(z)$ and $H(z)$:

$$\begin{aligned} NTF(z) &= \frac{1}{1-H(z)} \\ STF(z) &= \frac{G(z)}{1-H(z)} \end{aligned} \qquad (3.52)$$

Equation (3.52) shows that *STF* and *NTF* are shaped differently. In a bandpass

modulator $H(z)$ is normally a bandpass filter. Consequently, *NTF* becomes a bandstop filter (having a deep notch at the center frequency). In a lowpass ΔΣ modulator, in contrast, $H(z)$ is a lowpass filter making *NTF* a high pass filter. $H(z)$ is usually selected among the conventional ΔΣ transfer functions or is optimized by any optimization tool to achieve the required noise transfer function (*NTF*). However, generally *STF* can be chosen independently of *NTF.* Normally, $G(z)$ is obtained based on $H(z)$ to meet the signal transfer function (*STF*) specifications, usually 0dB gain and linear phase in-band and high attenuation out-of-band [Jant91]. It should be noted that, however, in most conventional ΔΣ modulators $G(z) = H(z)$ in which the loop filters are in the feedforward path (Fig. 3.1) and no special consideration is required for extra filtering on the input signal.

So, questions regarding signal transfer function in a continuous-time modulator compared to a discrete-time equivalent are "whether an equivalent *STF* can be found when their *NTF* are made equivalent" and even "whether this is necessary". To answer these questions a continuous-time modulator corresponding to the discrete-time modulator given in Fig. 3.21 is shown in Fig. 3.22. As explained in Sec. 3.1 the

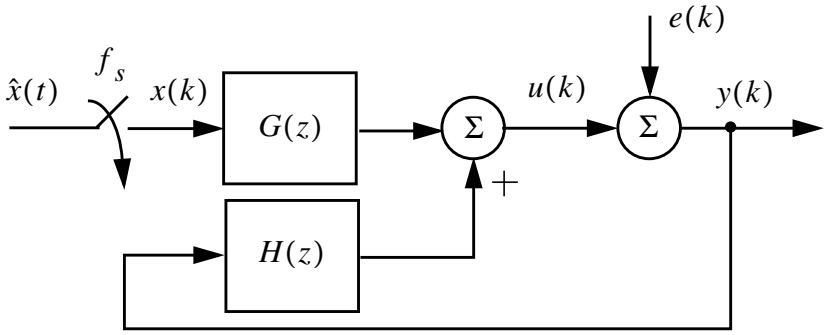


Figure 3.21 : Discrete-time delta-sigma modulator with linearized quantizer model (*G* and *H* transfer functions share poles).

continuous-time loop transfer function $\hat{H}(s)$ is obtained by a pulse invariant transformation of $H(z)$. This is dictated by the DAC pulse shaping utilized in the continuous-time modulator. As shown in Fig. 3.22 there is no pulse shaping device (like

a DAC or *ZOH*) preceding $\hat{G}(s)$. Therefore in order to obtain $\hat{G}(s)$, there is no necessity to apply a pulse invariant transformation on $G(z)$. As shown in Fig. 3.22 the *STF* in a continuous-time modulator is a system whose input signal is continuous-time $\hat{x}(t)$ and its output is discrete-time *y*(*k*). In contrast, in a discrete-time modulator the *STF* is defined completely in *z*-domain in which input and output are discrete-time signals represented by *x*(*k*) and *y*(*k*) in Fig. 3.21. Therefore, it is not possible to define a

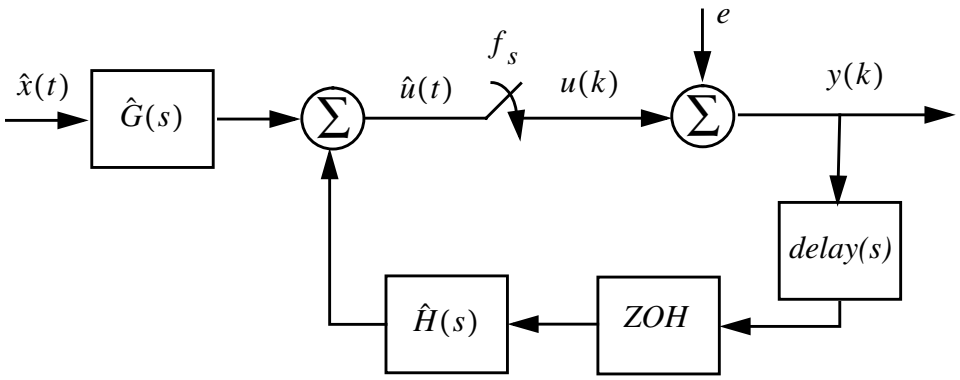


Figure 3.22 : Continuous-time ΔΣ modulator, equivalent to the discrete-time modulator shown in Fig. 3.21.

straight *z*- or *s*-domain transfer function for *STF* in a continuous-time modulator. However, in a continuous-time modulator assuming that the prefilter $\hat{G}(j\omega)$ attenuates the high frequency components significantly and so neglecting the aliasing effect the *STF* frequency response can be approximated by

$$STF_c(\omega) = \frac{Y(e^{j\omega T})}{\hat{X}(j\omega)} = e^{-j\omega T/2} \cdot \frac{\sin(\omega T/2)}{\omega T/2} \cdot \frac{\hat{G}(j\omega)}{1-H(e^{j\omega T})} \ . \qquad (3.53)$$

The proof for this is given in Appendix B. As mentioned in Appendix B, the $e^{-j\omega T/2} \cdot \frac{\sin(\omega T/2)}{\omega T/2}$ term associated with the pulse-shape sampled signals is present in both discrete-time and continuous-time modulators and applies on both systems after aliasing has effected. Therefore, for the purpose of comparison of the *STF* in a continuous-time modulator with its discrete-time counterpart, this term will be neglected:

$$STF_c(\omega) = \frac{Y(e^{j\omega T})}{\hat{X}(j\omega)} = \frac{\hat{G}(j\omega)}{1-H(e^{j\omega T})} \qquad (3.54)$$

So, using a continuous-time prefilter $\hat{G}(s)$ it is not possible to mimic exactly the *STF* in an equivalent discrete-time modulator. However, this is not a shortcoming for a continuous-time modulator because the optimization constraints such as unity-gain and linear phase in-band and high attenuation out-of-band which are frequency response requirements can be applied on prefilter $\hat{G}(s)$ directly in *s*-domain.

It was shown in (3.9)-(3.11) that the relationship between continuous-time filter poles and discrete-time filter poles is given by

$$z_k = e^{s_k T}. \tag{3.55}$$

This implies that to simplify the implementation of the feedforward filter, $\hat{G}(s)$, by sharing its resonators with those of $\hat{H}(s)$, one needs to make the poles of $\hat{G}(s)$ identical to the poles of $\hat{H}(s)$. The *STF* constraints then show how the zeros (numerator) of $\hat{G}(s)$ should be selected. The zeros of the continuous-time prefilter, $\hat{G}(s)$, for low order systems can be selected by simple inspection. For instance, for the second-order bandpass system given in (3.37) or (3.38) a bandpass prefilter could be proposed as follows

$$\hat{G}(s) = \frac{k(s+\alpha)}{s^2 + \left(\frac{\pi}{2T}\right)^2} \tag{3.56}$$

where k defines the $\Delta\Sigma$ modulator gain (to be explained more in Sec. 3.2) and α is the prefilter's zero. In the bandpass modulator one good choice for the prefilter's zero location is at DC *i.e.* $\alpha = 0$.

For higher order modulators, however, the selection of the prefilter's zeros may not be that straightforward. In higher order systems a designer may use any optimization package to meet the requirements of the continuous-time prefilter, $\hat{G}(s)$. For example, for the double-pole fourth-order systems given in (3.23) or (3.39). There are four unknown parameters (gain[2] and three zeros):

$$\hat{G}(s) = \frac{k(s-s0)(s-s1)(s-s2)}{\left(s^2 + \left(\frac{\pi}{2T}\right)^2\right)^2} \tag{3.57}$$

2. In Ch. 2 it was shown that a $\Delta\Sigma$ modulator response is loop gain-invariant. However, the effect of prefilter or *STF* gain is to change the MSA. So k can simply be normalized to 1.

As we mentioned for a bandpass modulator it is always desirable to have a zero at DC or some other real zero on the real (σ) axis close to DC. This guarantees a sharper roll off for frequency selectivity of the bandpass prefilter. Although in the pulse invariant transformation, generally a closed-form mapping cannot be found between zeros in *s*-domain and *z*-domain transfer functions [Gar86], a zero at DC in the *s*-domain is mapped to a zero at DC in the *z*-domain and vice versa. This feature of the pulse invariant transformation will be shown in the double-pole fourth-order example. The discrete-time loop filter for the double-pole fourth-order is $z^{-2}(2+z^{-2})/(1+z^{-2})^2$. It can easily be shown that in order to provide a flat response inside the band and to put zeros at DC and $f_s/2$ for the discrete-time *STF* shown in Fig. 3.21 it is required that:

$$G(z) = 0.5\frac{z^{-1}(1-z^{-2})}{(1+z^{-2})^2} \quad . \tag{3.58}$$

The corresponding continuous-time feedforward transfer function $\hat{G}(s)$ obtained from (3.58) by a NRZ pulse transformation would be

$$\hat{G}(s) = 0.25\frac{\left(\frac{\pi}{2}-1\right)\frac{s}{T}^3 - \pi\frac{s}{T^2}^2 + \left(\frac{\pi}{2}+1\right)\left(\frac{\pi}{2}\right)^2\frac{s}{T^3}}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \tag{3.59}$$

which provides a zero at $s = 0$ corresponding to the zero at $z = 1$ in (3.58). The *STF*s for these two systems are shown in Sec. 3.2.

As another example the *NTF* and *STF* for a fourth-order bandpass spread-pole modulator (with center frequency at 20MHz and bandwidth of 1MHz) have been optimized by "filtorX" [Ous90]. The *NTF* zeros turn out to be at

$$\begin{aligned} z &= exp(\pm\pi/2 \pm 0.02527)\,j \\ &= \pm 0.025268 \pm 0.999681\,j \end{aligned}$$

and poles at

$$z = \pm 0.33447 \pm 0.69822\,j.$$

The *STF* poles are identical to the *NTF* poles and the *STF* zeros which determine the zeros of *G(z)* too are at

$$z = 0, \pm 1$$

The corresponding *s*-domain loop transfer function, $\hat{H}(s)$, and feedforward transfer

function, $\hat{G}(s)$, obtained by the pulse invariant transformation given in (3.9)-(3.11) are

$$\hat{H}(s) = \frac{\frac{b_3}{T}s^3 + \frac{b_2}{T^2}s^2 + \frac{b_1}{T^3}s^1 + \frac{b_0}{T^4}}{(s^2 + \omega^2{}_1)(s^2 + \omega_2^2)} \quad (3.60)$$

and

$$\hat{G}(s) = \frac{\frac{a3}{T}s^3 + \frac{a2}{T^2}s^2 + \frac{a1}{T^3}s^1 + \frac{a0}{T^4}}{(s^2 + \omega^2{}_1)(s^2 + \omega_2^2)} \quad (3.61)$$

where $f_s = 1/T = 4f_o = 80\text{MHz}$, ($b_3$, b_2, b_1, b_0) = (0.8276, 1.6396, 2.7885, 2.8722), (a_3, a_2, a_1, a_0) = (0.0867, 0.4770, 0.9630, 0.0) and $(\omega_1, \omega_2) = (\frac{\pi/2 - 0.02527}{T}, \frac{\pi/2 + 0.02527}{T})$. As shown in $G(z)$ the zero at $z = 1$ in the z-domain is mapped to $s = 0$ in the s-domain in $\hat{G}(s)$ too.

3.2 Implicit Anti-alias (Image) Filtering

In [Can85] it was shown that a lowpass continuous-time ΔΣ modulator provides an inherent anti-alias filtering on the input signal path. In the continuous-time lowpass case, the signal transfer function contains a *"sinc"* term. This will later on be shown for a second-order lowpass example in this section. Since the *"sinc"* zeros are located at integer multiples of the sampling frequency (f_s), clock-image signals are attenuated significantly which otherwise would be aliased into the desired frequency band. We will generalize this observation to the higher order modulators as well as bandpass ΔΣ modulators in this section.

Fig. 3.23a shows another representation of a continuous-time modulator shown in Fig. 3.22. As explained in Sec. 3.1, the loop transfer function is $H(z) = \mathcal{Z}\left[\frac{1 - e^{-sp}}{s}\hat{H}(s)\right]$. Therefore, the noise transfer function (NTF) in Fig. 3.23a is

$$NTF(z) = \frac{Y(z)}{U_1(z)} = \frac{1}{1 - H(z)} \quad (3.62)$$

We know from (3.52) that the *STF* in an equivalent discrete-time modulator (Fig. 3.21) is

given by $\frac{G(z)}{1-H(z)}$. The corresponding *STF* frequency response in the continuous-time modulator shown in Fig. 3.22 and redrawn in Fig. 3.23a was given in (3.54). So as shown in Fig. 3.23b and Fig. 3.23c the frequency response of the filter represented by

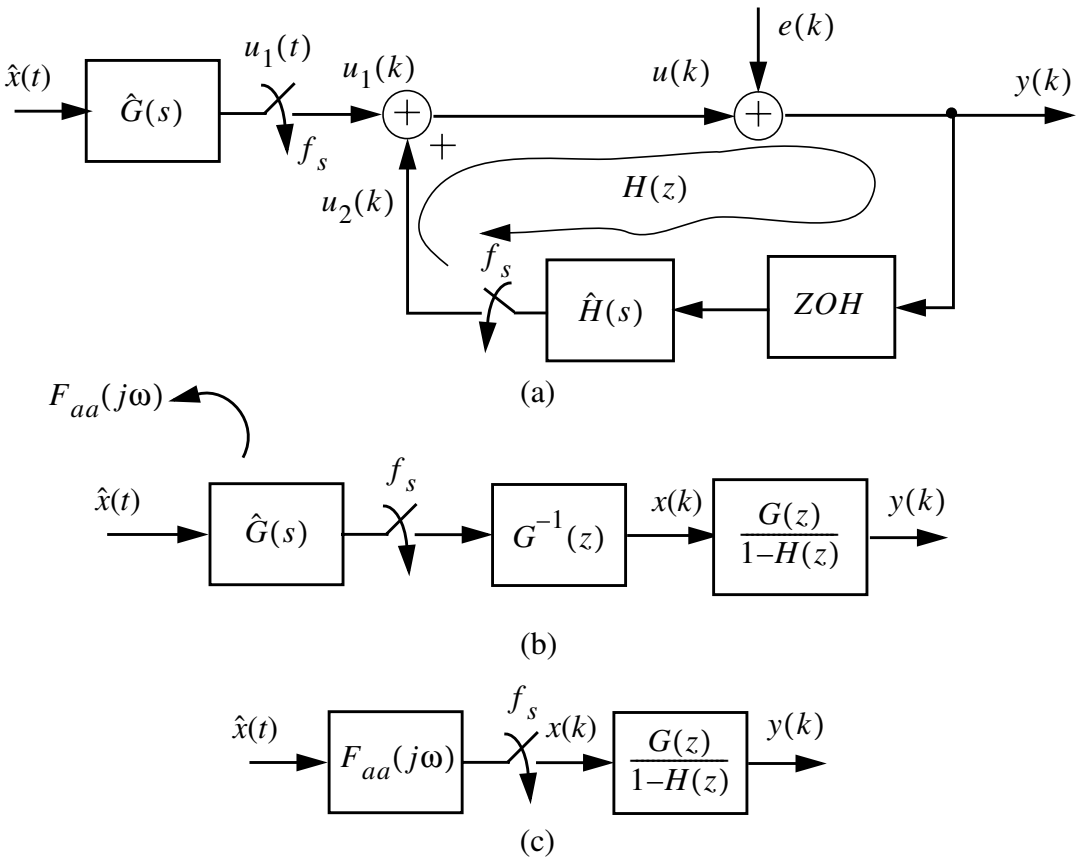


Figure 3.23 : (a) One representation of a continuous-time modulator (b) another arrangement of Fig. 3.23a, and (c) the equivalent discrete-time modulator with an extra input filter shown by $F_{aa}(j\omega)$.

$F_{aa}(\omega)$ in Fig. 3.23c that should be placed in cascade with the input of the discrete-time modulator in order to make its response identical to that of the continuous-time version is

$$\begin{aligned} F_{aa}(\omega) &= \frac{STF_c(\omega)}{STF(e^{j\omega T})} \\ &= \hat{G}(j\omega)G^{-1}(e^{j\omega T}) \cdot \\ &= \frac{\hat{G}(j\omega)}{G(e^{j\omega T})} \end{aligned} \tag{3.63}$$

Recall from Sec. 3.1.7 that $G(z) = H(z)$ for the traditional modulators. The frequency response of the implicit anti-alias filter in those continuous-time modulators would be

$$F_{aa}(\omega) = \frac{\hat{H}(j\omega)}{H(e^{j\omega T})} \tag{3.64}$$

The discrete- and continuous-time *STF*s for three different modulators are shown in Fig. 3.24a and Fig. 3.24b respectively: the second-order bandpass system given in (3.17), (3.38); the fourth-order with $G(z) = H(z)$ [Lon93] and $\hat{G}(s) = \hat{H}(s)$ given in (3.23); and finally the fourth-order with its feedforward filter, $\hat{G}(s)$ arranged to be as (3.59). The latter provides a zero at $s = 0$ [Sch94]. As shown in Fig. 3.24 modulators are operating at one quarter the sampling frequency *i.e.* $f_o = f_s/4$. The discrete-time modulators Fig. 3.24a show the aliasing effect as expected. Any signal at $f = nf_s \pm f_o$ frequencies are aliased directly into the in-band frequency f_o. However, serendipitously, the continuous-time modulators provide nulls exactly at aliasing frequencies $f = nf_s \pm f_o$ as shown in Fig. 3.24b. Before proceeding to further details the implicit anti-aliasing property of a continuous-time modulator can be illustrated by an interpretation of (3.54):

$$\begin{aligned} STF_c(\omega) &= \frac{\hat{G}(j\omega)}{1 - H(e^{j\omega T})} \\ &= \hat{G}(j\omega) \cdot NTF(e^{j\omega T}) \end{aligned} \tag{3.65}$$

It is interesting to note that the continuous-time signal transfer function STF_c zeros like the *NTF* zeros are at $f = nf_s \pm f_o$ except for $n = 0$ *i.e.* the in-band frequency f_o as shown in Fig. 3.24b. This happens because the prefilter[3] $\hat{G}(j\omega)$ is a resonator (integrator in a lowpass modulator) with the resonance frequency of f_o (for integrator $f_o = 0$). Therefore, mathematically there is an ambiguity at f_o in (3.65) *i.e.* a $\infty \times 0$

3. Or $\hat{H}(j\omega)$ for $\hat{G}(j\omega) = \hat{H}(j\omega)$ cases.

product or a $0/0$ division. It will be shown that this is just a mathematical artifact and (3.65) always gives a finite in-band gain for the signal transfer function of the continuous-time modulators as shown in Fig. 3.24b. Besides, equation (3.65) explains a

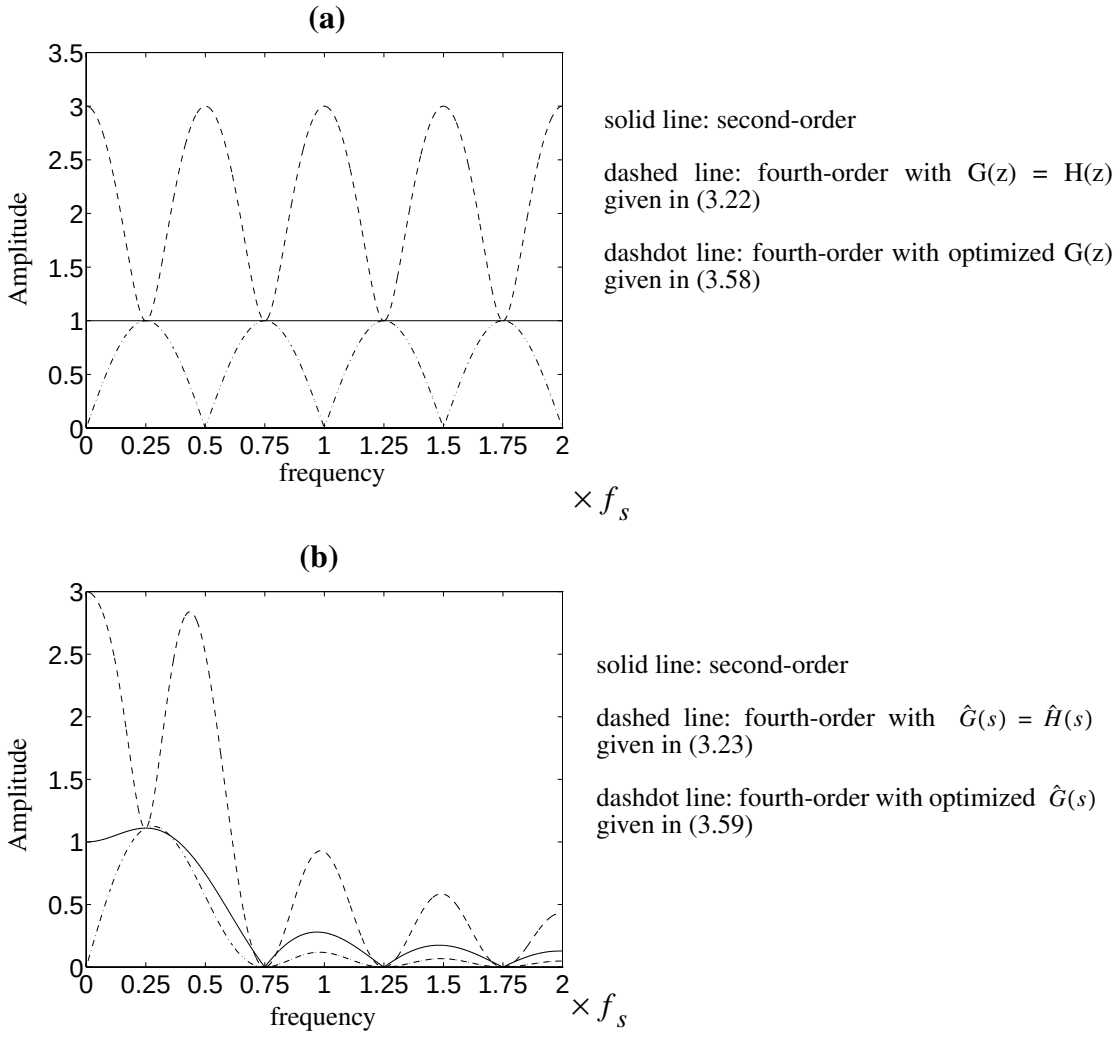


Figure 3.24 : (a) Discrete-time and (b) continuous-time *STF*s for the three examples.

physical property of a continuous-time modulator. It shows what the input signal sees after being filtered by a prefilter $\hat{G}(j\omega)$, which is the modulator noise transfer function frequency response $NTF(e^{j\omega T})$. This is actually a translation of having the sampling action inside the loop Fig. 3.22. In other words because the sampling happens after the

loop filter and preceding the quantizer the aliased signals produced by the sampler are noise shaped (like the quantization noise represented by $e(k)$ in Fig. 3.22). Since the *NTF* nulls are at $= nf_s \pm f_$ frequencies (for both bandpass and lowpass modulators) it turns out that aliasing signals which are in band are attenuated significantly (ideally, rejected).

Previously it was mentioned that the null frequencies of *NTF* are at $= nf_s \pm f_$. Technically, discrete-time filters like *NTF(z)* are not analyzed in this way. The frequency response of a discrete-time filter is normally defined between $(-\pi, \pi)$ or in terms of real frequencies $(-f_s/2, f_s/2)$ where f_s is the sampling frequency. Beyond the spectrum area of $(-f_s/2, f_s/2)$ the discrete-time filter frequency response is replicated. This originates in sampling theory. The signals in the out-of-band spectrum are first aliased into the in-band spectrum $(-f_s/2, f_s/2)$ and then are treated by a discrete-time filter the same way that the originally in-band signals are treated. So keeping in mind that out-of-band signals always produce in-band components we could use the periodic discrete-time frequency response extended to $(-\infty, \infty)$ frequency band as shown in Fig. 3.24a. Table 3.3 which gives the *STF* response of the third example shown in Fig. 3.24 describes this idea as well as the continuous-time anti-alias filtering performance.

As shown in Table 3.3 the aliasing signals at $0.74f_s$, $0.75f_s$, $0.76f_s$, $1.24f_s$ and $1.26f_s$ are attenuated significantly in the continuous-time modulator. In the discrete-time counterpart they appear at the in-band region with almost no loss.

The anti-aliasing feature of a continuous-time modulator is illustrated by deriving the *STF* of the examples shown in Fig. 3.24. For the second-order modulator (3.17), (3.38) (note that $\hat{G}(s) = \hat{H}(s)$) from (3.65) we get:

$$\begin{aligned} \left|STF_c(\omega)\right| &= \frac{\left|\frac{\pi}{4T}j\omega + \frac{1}{2}\left(\frac{\pi}{2T}\right)^{\sim}\right|}{\left|(j\omega)^2 + \left(\frac{\pi}{2T}\right)^2\right|} \cdot \left|1 + e^{-2j\omega T}\right| \\ &= \frac{2\cos(\omega T)\left[\left(\frac{\pi}{2\sqrt{2}\ T}\right)^4 + \left(\frac{\pi}{4T}\omega\right)^2\right]^{1/2}}{\left|\left(\frac{\pi}{2T}\right)^2 - \omega^2\right|} \end{aligned} \qquad (3.66)$$

The zeros of the *STF* given in (3.66) are the same as zeros of $\cos(\omega T)$ at

$\omega = \frac{2n\pi}{T} \pm \frac{\pi}{2T}$ or at $f = nf_s \pm f_o$ where, $n = \pm 1, \pm 2, \pm 3, \ldots$ and $f_o = f_s/4$. These are "image frequencies" at which, in a pure discrete-time system, input signals would alias into the band of interest. In Ch. 6 experimental results for a second-order G_m-C modulator verify that the STF_c nulls are at $f = nf_s \pm f_o$. The numerator of (3.66) also has a zero at $n = 0$ ($\omega = \frac{\pi}{2T}$), which is in the desired band, but this is cancelled by a denominator zero ($\omega^2 - (\pi/(2T))^2$). L'Hôpital's rule can be used to resolve the $0/0$ ambiguity. It shows that $\left|STF_c(\omega = \pi/2T)\right| = \pi/2\sqrt{2} \approx 1.11$. This cancellation of zeros at f_o is a mathematical artifact, and doesn't affect stability.

For the fourth-order system with $\hat{G}(s) = \hat{H}(s)$ given in (3.23):

$$\left|STF_c(\omega)\right| = \frac{4(\cos\omega T)^2 \cdot \left[\left(\frac{3}{4}\left(\frac{\pi}{2T}\right)^4 - \left(\frac{3\pi^2}{16} + \frac{\pi}{4}\right)\frac{\omega^2}{T^2}\right)^2 + \frac{\omega^2}{T^2}\left(\frac{\frac{\pi^3}{8} + \frac{\pi^2}{16}}{T^2} - \left(\frac{\pi}{2} - \frac{1}{4}\right)\omega^2\right)^2\right]^{\frac{1}{2}}}{\left(\left(\frac{\pi}{2T}\right)^2 - \omega^2\right)^2} \qquad (3.67)$$

Again the *STF* zeros are determined by $\cos\omega T$. Resolving the $0/0$ ambiguity at f_o shows that the in-band gain is $\left|STF_c(\omega = \pi/2T)\right| = \pi/2\sqrt{2} \approx 1.11$ *i.e.* the same as the in-band gain (3.66) of the second-order modulator. The last example is the fourth-order modulator having an optimized $\hat{G}(s)$ given in (3.59) which puts a zero at DC. The *STF* for this case would be:

$$\left|STF_c(\omega)\right| = \frac{(\cos\omega T)^2 \cdot \left[\left(\pi\frac{\omega^2}{T^2}\right)^2 + \frac{\omega^2}{T^2}\left(\frac{\left(\frac{\pi}{2} + 1\right)\left(\frac{\pi}{2}\right)^2}{T^2} - \left(\frac{\pi}{2} - 1\right)\omega^2\right)^2\right]^{\frac{1}{2}}}{\left(\left(\frac{\pi}{2T}\right)^2 - \omega^2\right)^2} \qquad (3.68)$$

which provides the same in-band gain as the other two examples *i.e.* $\left|STF_c(\omega = \pi/2T)\right| = \pi/2\sqrt{2} \approx 1.11$. Note that this in-band gain at $f = f_o = 0.25f$ is not the maximum in this case; the maximum gain of this transfer function happens at $f = 0.28f_s$ as shown in Fig. 3.24b.

It was shown that in a continuous-time modulator (Fig. 3.22), like a discrete-time modulator (Fig. 3.21), because of the presence of a sampler on the signal path the input signals beyond the $-\pi/T < \omega < \pi/T$ spectrum region are aliased into the in-band area. However, out-of-band signals, particularly the images of the passband frequency are

attenuated significantly by the implicit anti-alias filter associated with the continuous-time modulator. As shown in Fig. 3.23c a continuous-time ΔΣ modulator can be modeled by a system including an anti-alias filter $F_{aa}(\omega)$ with a frequency response given in (3.63) or (3.64) followed by a sampler and its equivalent discrete-time modulator. The attenuation $F_{aa}(\omega)$ provided at image frequencies is desirable for the overall system (recall that $F_{aa}(\omega)$ zeros are at image frequencies).

For the three given examples the implicit anti-alias filter frequency response are plotted in Fig. 3.25. It should be noted that in the optimized (third example) discrete-time fourth-order *STF* there is a zero at $f_s/2$ as well as DC as shown graphically in Fig. 3.24a and given in Table 3.3. In the corresponding continuous-time modulator, however, there is no zero at $f_s/2$ as shown in Fig. 3.24b. The continuous-time *STF* gain is –21.83 dB as indicated in Table 3.3. Although it is desirable to have a zero at $f_s/2$, it is not crucial

Table 3.3: Gains of the third example modulators given in Fig. 3.24*.

Input frequency, f_o ($\times f_s$)	Aliased in-band frequency ($\times f_s$)	Gain in continuous-time modulator dB	Gain in discrete-time modulator dB
0.0	————	$-\infty$	$-\infty$
0.01	————	-41.01	-41.41
0.25	————	-0.91	0
0.5	0.5	-21.83	$-\infty$
0.74	0.26	-62.32	-0.0172
0.75	0.25	$-\infty$	0
0.76	0.24	-62.80	-0.0172
1.24	0.24	-69.67	-0.0172
1.26	0.26	-69.85	-0.0172

*. Note that the in-band signal is at $f_o = 0.25 f_s$

because as was mentioned the critical frequencies are at $= nf_s \pm f_$ neighborhood which produce the aliased in-band components. Since (3.63) produces a division by zero

at $f_s/2$ frequency in $F_{aa}(\omega)$ at the third example, the

$$F_{aa}(\omega) = \frac{\hat{G}(j\omega)}{H(e^{j\omega T})} \tag{3.69}$$

frequency response instead is plotted in Fig. 3.25.

As the last example we present the implicit anti-alias filter frequency response of a second-order lowpass modulator with $\hat{G}(s) = \hat{H}(s) = -(1 + 1.5Ts)/(T^2 s^2)$ given in Table 3.1. For this system it can be shown that

$$\left|F_{aa}(\omega)\right| = \left|\frac{1 + (1.5\omega T)^2}{5 - 4\cos\omega T}\right|^{1/2} \sin c^2(f/f_s) \tag{3.70}$$

Recall the comment in the beginning of Sec. 3.2 that a lowpass *STF* contains a "*sinc*" term as shown in (3.70).

For three bandpass modulators and a lowpass modulator, we showed that the zeros of the implicit anti-alias frequency response of the continuous-time ΔΣ modulator are at $f = nf_s \pm f_c$; however, this conclusion could be easily generalized to any continuous-time ΔΣ modulator (bandpass or lowpass) derived by the pulse invariant transformation explained in Sec. 3.1. As (3.64) and (3.69) show, the anti-alias frequency response is the product of the feedforward frequency response represented by $\hat{G}(j\omega)$ (in Fig. 3.22) and the inverse of the discrete-time loop frequency response *i.e.* $1/H(e^{j\omega T})$. The resonance (pole) frequency of $\hat{G}(j\omega)$ is at $f = f_c$ and the first notch of the noise transfer function at $f = f_c$ too, so the value of signal frequency response at f_o is $0/0$ which after resolving the ambiguity yields a finite value (like $\pi/2\sqrt{2} \approx 1.11$ for the three bandpass examples).

The feedforward frequency response, $\hat{G}(j\omega)$ doesn't have zero on the $j\omega$ axis (except in a bandpass modulator which could have a zero at DC as shown in Fig. 3.25c and [Sch94]). Thus, the zeros of the signal frequency response are determined by the remaining zeros of the noise transfer function, which obviously are at $f = nf_s \pm f_c$, $n = \pm 1, \pm 2, \pm 3, \ldots$ as obtained for the bandpass examples. It should be noted that for a lowpass continuous time modulator the resonance frequency is at $f_o = 0$ (integrator instead of resonator), so according to the preceding derivation the zeros of signal frequency response are at $f = nf_s$, $n = \pm 1, \pm 2, \pm 3, \ldots$ which is consistent with [Can85].

Therefore a continuous-time ΔΣ modulator compared to a discrete-time (switched-C) modulator has the advantage that it provides free anti-alias filtering to reduce the spurious images of the passband significantly. This is advantageous particularly in bandpass modulators where the ratio of in-band frequency to the clock frequency is normally on the order of $1/4$ (or $1/8$) as opposed to $1/64$ (or $1/128$) in lowpass modulators. So, the complexity of anti-alias filters for switched-C bandpass modulators is much higher than those required for audio base-band ΔΣ modulators. The continuous-time bandpass modulators, however, provide an implicit anti-alias filtering which relaxes (or even removes) the requirement of an extra anti-alias filter. The only price, as will be shown in Ch. 6, is the requirement of a tuning scheme for the continuous-time loop filter used in the ΔΣ modulator.

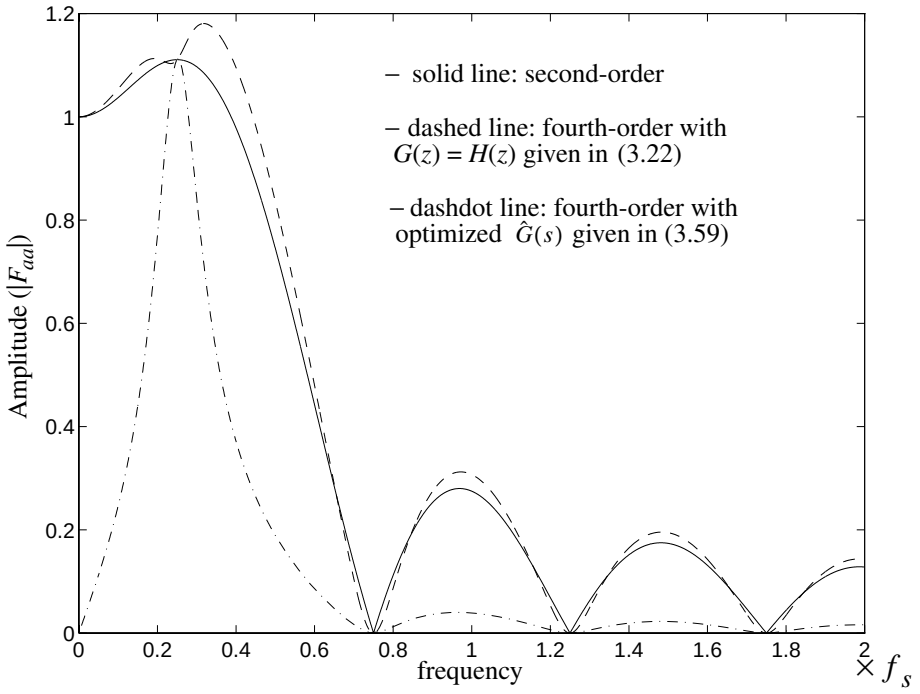


Figure 3.25 : The implicit anti-alias filter frequency response in the three continuous-time examples.

3.3 Simulation Results

3.3.1 Signal-to-Noise Ratio

To verify the equivalence of the ΔΣ loop behavior in the discrete-time and continuous-time modulators related by the transformations given in Sec. 3.1 extensive simulations have been done. Here some examples have been given:

1) For NRZ transformation simulation results for the discrete and continuous-time second-order bandpass modulator given in (3.17), (3.20) respectively and the discrete and continuous-time multiple-pole fourth-order bandpass modulator given in (3.22), (3.23) respectively are shown in Fig. 3.26. In these simulations the input signal is a 20MHz sinusoidal signal and the clock frequency is 80MHz. The *SNR*s shown in Fig. 3.26 have been collected for a 1MHz bandwidth.

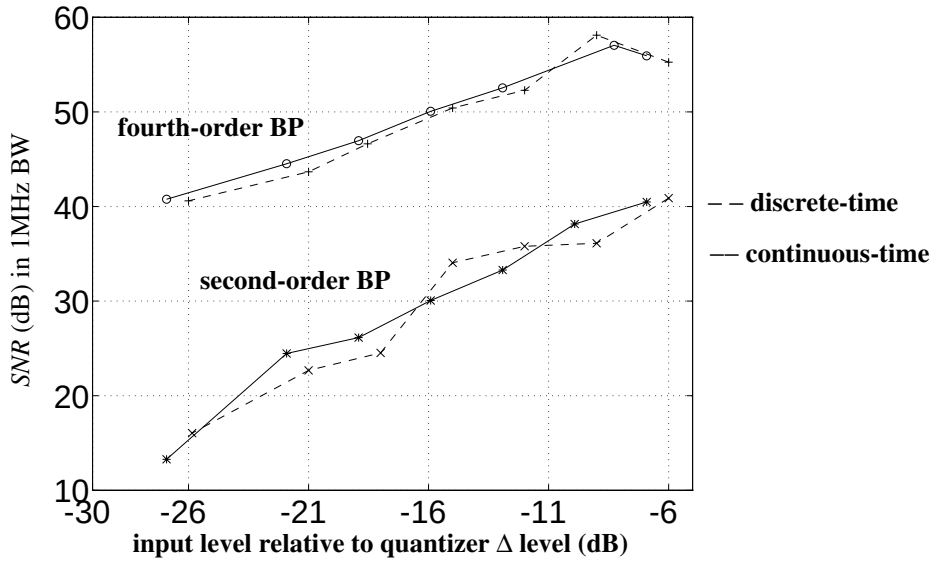


Figure 3.26 : (a) Simulation results of discrete-time and continuous-time modulators derived by the NRZ pulse invariant transformation for a fourth and a second order modulators (f_{in}=20 MHz and BW=1 MHz).

The simulated *SNR*s shown in Fig. 3.26 for discrete and continuous-time modulators are quite close. For example, the *SNR*s of the fourth-order bandpass discrete (3.22) and the continuous-time (3.23) modulators were 55.25 dB and 55.93 dB respectively and

41.68 dB and 40.48 dB for the second-order systems given in (3.17), (3.20) respectively. It should be noted that because the in-band signal gain is 1 (0 dB) for the discrete-time modulators but almost 1.11 (0.9 dB) for the second- and fourth-order continuous-time modulators (explained in Sec. 3.2), the input levels were chosen accordingly (for example −6 dB in discrete-time and −6.9 dB in continuous-time for the maximum input levels), as shown in Fig. 3.26. This gain difference, combined with numerical errors in simulation, is enough to explain the minor differences in *SNR*s observed in simulations.

2) The same simulation has been performed for the RZ multiple-pole fourth-order system given in (3.30). The *SNR* for this continuous-time modulator in a 1MHz bandwidth with 20MHz sinusoidal input and 80MHz clock was 56.7 which happened at −12.3 dB input level[4].

3.3.2 Anti-alias Filtering Simulation

In order to verify the anti-alias filtering performance of the continuous-time modulators discussed in Sec. 3.2 two-tone simulations have been performed. An in-band sinusoidal input in conjunction with an out-of-band sinusoidal signal in the neighborhood of the first aliasing frequency have been applied to the continuous-time ΔΣ modulator. The multiple-pole fourth-order system given in (3.23) with ΔΣ noise shaping notch frequency at 50MHz and the clock frequency at 200MHz was selected. In the first simulation the in-band signal frequency was at 49.95MHz and the out-of-band signal frequency at 149.02MHz both with amplitude –6.9 dB (0.45) relative to the quantizer Δ level. Fig. 3.27 shows the anti-alias filtering characteristic of the multiple-pole fourth-order modulator obtained by taking an FFT on the modulator output bit stream.The 149.02MHz out-of -band tone produces a component close to the in-band aliasing frequency at 50.98MHz. As shown in Fig. 3.27 the aliased component *i.e.* 50.98MHz tone is attenuated by –59.60 dB compared to the in-band signal level. It can be noticed that 149.02MHz input frequency for this modulator appears at $0.745 \times f_s$ in Fig. 3.24b

4. It can be shown that the in-band signal transfer function gain for a RZ continuous-time modulator with the loop filter given in (3.30) is about −12.3 dB relative to the quantization Δ.

and Fig. 3.25. The signal gain at $f_{in} = 0.745 \times f_s$ calculated from (3.67) for this modulator shows –57.61 dB attenuation and the signal gain for the in-band 49.95MHz tone *i.e.* $\sim 0.25 \times f_s$ is 0.91dB (or 1.11 as shown earlier). So, from (3.67) analysis the total loss should be –58.52 dB which is very close to the simulation result. In the discrete-time system, however, from the multiple-pole fourth-order signal transfer function plotted in Fig. 3.24a it can be found that the 149.02 MHz out-of-band tone produces an in-band 50.98MHz tone with 0.034dB (1.004) gain.

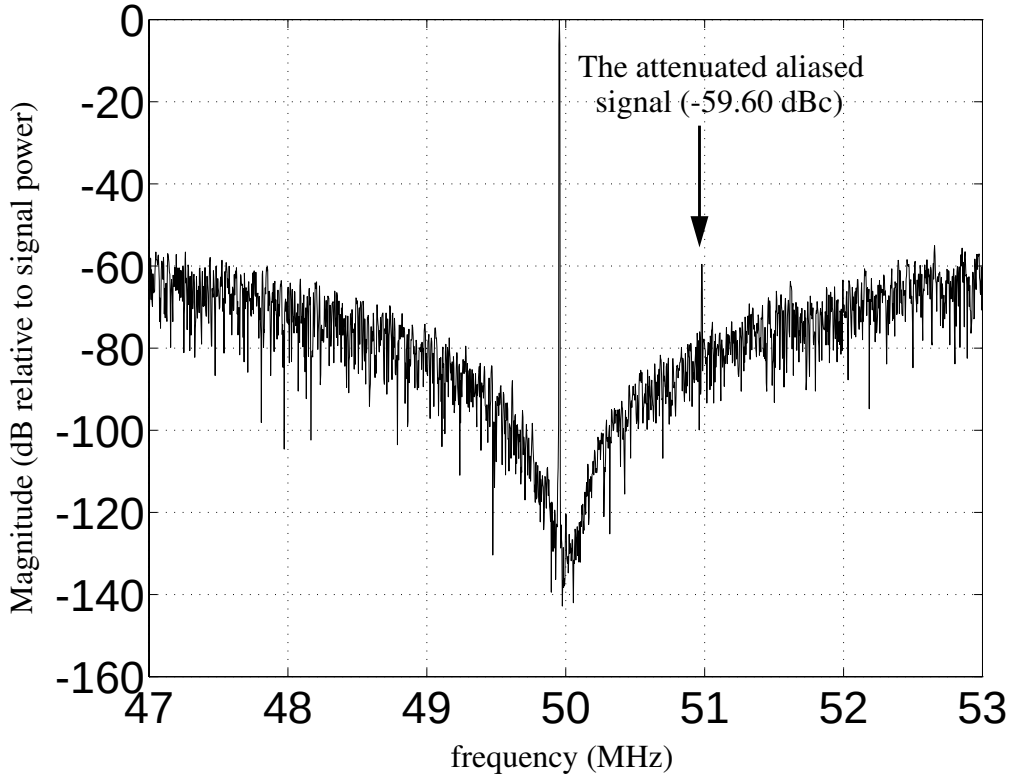


Figure 3.27 : Anti-alias filtering simulation of the multiple-pole fourth-order system (3.23). f_{in} = 49.95MHz and a single tone aliasing signal at f = 149.02MHz.

In a switched-*C* equivalent modulator in order to achieve the same amount of attenuation (–59.6 dB) at 149 MHz (close to $f_s - f_o$) one may use a lowpass anti-alias filter preceding the modulator. Note that the ratio of $f_s - f_o$ to f_o is 3 at the bandpass modulators with the sampling frequency four times as high as the passband. It can be shown [Hue80] with a

0.5 dB passband ripple and a 60 dB stop-band attenuation at the normalized frequency 3 at least a fourth-order lowpass elliptic filter is required. Therefore, for a bandpass switched-*C* filter the expense of the anti-alias filter is the same as the modulator loop filter in the equivalent continuous-time modulator!

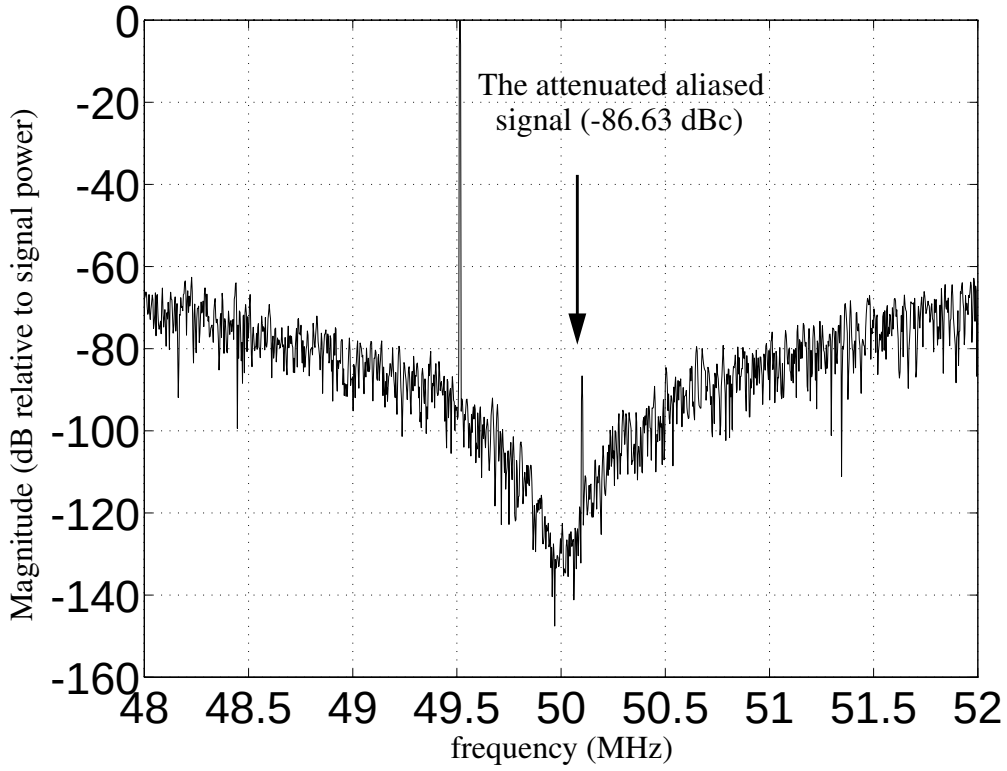


Figure 3.28 : Anti-alias filtering simulation of the multiple-pole fourth-order system (3.23). f_{in} = 49.51MHz and a single tone aliasing signal at f = 149.90MHz.

In the final simulation example the input in-band signal frequency was chosen at 49.51MHz and the out-of-band signal frequency at 149.90MHz both with amplitude −6.9 dB (0.45) relative to the quantizer Δ level. The latter should produce the in-band signal at 50.10MHz. The noise shaping FFT plot of this simulation is shown in Fig. 3.28. As shown in Fig. 3.28 the aliased in-band component is recognizable above the noise floor with a −86.63 dB loss compared to the in-band tone.

It can be shown in order to achieve the same attenuation −86.6 dB at $f_s - f_o$ with an anti-alias filter preceding a switched-C equivalent modulator, at least a fifth-order elliptic filter (with 0.5 dB passband ripple) is required.

3.4 Summary

A comprehensive study of different transformations to design a continuous-time loop filter from a discrete-time equivalent has been presented. A class of zero-digital-delay loop filter scheme for equivalent continuous-time ΔΣ modulators with the same order has been distinguished. The sensitivity of continuous-time ΔΣ modulators to undesired extra loop delays has been discussed. It was shown that one can make a continuous-time ΔΣ loop filter such that the behavior of both discrete-time equivalent and continuous-time ΔΣ loops be exactly identical. However, their signal transfer functions would be different. The continuous-time modulators produce extra filtering resulting in better *STF* specification. It was proven that the continuous-time modulators provide free anti-alias filtering suppressing the passband image signals at $nf_s \pm f_o$ frequencies. Particularly this feature is favorable for a bandpass modulator in which f_s/f_o ratio is usually 4 or so. This means that the stop band frequency ($f_s - f_o$) to the passband frequency (f_o) ratio is usually 3 which requires an expensive anti-aliasing filter in a switched-C modulator otherwise. However, it should be mentioned that for a narrow band bandpass system probably a filter with 3:1 frequency transition is easy enough to get. For example, a narrow band ceramic resonator can be considered.

Chapter 4

Multi-Feedback (Pulse Shaping) Design for LC Bandpass Delta-Sigma Modulator

A new technique for designing an LC bandpass Delta-Sigma modulator is presented in this chapter which is an extension of the work presented in [Sho95]. This method is based on pulse shaping of a DAC output signal such that one can realize a desired (arbitrary) loop transfer function. Especially for higher-order modulators where extra LC sections are added, sufficient parameters provided in the feedback loop. It is shown that by creating more degrees of freedom one can achieve the maximum *SNR* in a given modulator order without constraining the noise transfer function of the modulator.

4.1 An LC Delta-Sigma Modulator

As was mentioned in Ch. 3 it is intuitively obvious that a bandpass ΔΣ modulator requires a bandpass filter (resonator) inside the ΔΣ loop to provide a bandstop noise shaping for quantization noise as shown in Fig. 4.1. Therefore designers [Gail89], [Thu91], [Tro93] generally selected a bandpass loop filter with center frequency at f_o to determine the desired noise shaping notch frequency. This approximate design was based on the assumption that if the ΔΣ loop filter poles are selected properly (close enough to the $j\omega$ axis) then one could expect to have the desired bandstop noise shaping at a frequency band close to the loop filter pole frequencies. However, as shown in Sec. 3.1 the ΔΣ modulator dynamics are determined by the overall ΔΣ loop impulse response

which corresponds to a well defined z-domain transfer function. Given the number of discrete-time delays and the shape of feedback DAC pulse in a continuous-time ΔΣ loop there is only one loop s-domain transfer function which produces the desired loop impulse response (recall from Sec. 3.1). It is not just the loop filter poles (or denominator) that are crucial, but the loop transfer function zeros (or numerator) are an important part of the exact continuous-time modulator loop design too. Otherwise the desired loop impulse response will not be achieved. Consequently the effectiveness of the ΔΣ modulator noise shaping is reduced and in high order loops (greater than fourth-order) modulator instability becomes an inevitable problem. In order to make the (fourth-order) loop stable the designers had to spoil the Q of their resonators. In [Gail89], [Tro93] for example, a damping resistor is placed in parallel with the LC circuit(s) to stabilize the ΔΣ loop, but causes the fourth-order ΔΣ modulator to behave more or less as a second-order system.

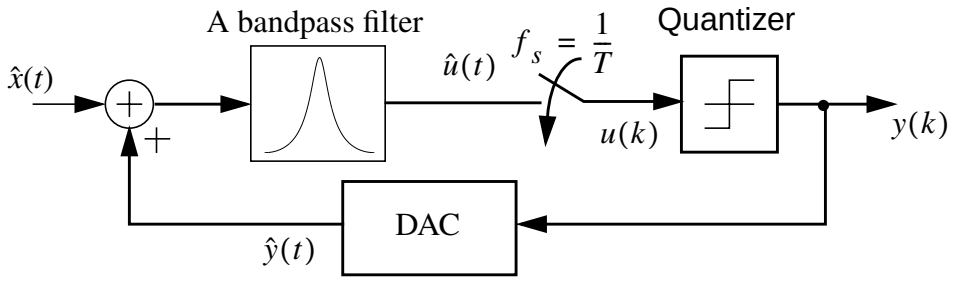


Figure 4.1 : A generic bandpass continuous-time ΔΣ modulator.

The proper s-domain loop transfer functions for implementing a continuous-time equivalent from a given discrete-time (Switched-C) modulator have been recently reported [Sch94] (more detail was presented in Sec. 3.1). A new architecture for a transconductor-C ΔΣ modulator has been given too [Sch94]. The transconductor-C architectures are discussed in Ch. 5 in more detail. For implementing a bandpass continuous-time ΔΣ modulator loop filter, however, a cascade of LC resonators as shown in Fig. 4.2 with

$$H_{LC}(s) = \frac{V_o(s)}{V_i(s)} = \frac{(g_m/C)s}{s^2 + 1/LC} \quad (4.1)$$

(where $g_m = (I_o/2)/V_T$ is the transistor transconductance) is attractive:

1) its architecture is simple,

2) a passive LC resonator has much less nonlinearity than an active resonator such as transconductor-*C*, and

3) LC type filters can present higher frequency capability than active filters.

It is, however, difficult to construct linear high-Q LC resonators on-chip, so these converters have generally relied on off-chip inductors [Gail89], [Thu91], [Tro93]. Since for a bandpass continuous-time ΔΣ modulator, a high-Q[1] resonator is required [Sch94], for on-chip inductance implementation some Q enhancement technique [Dun93], [Pipi94] is necessary. The other problem is that the cascade of LC resonators shown in Fig. 4.2 provides a transfer function with a numerator having only bandpass terms like

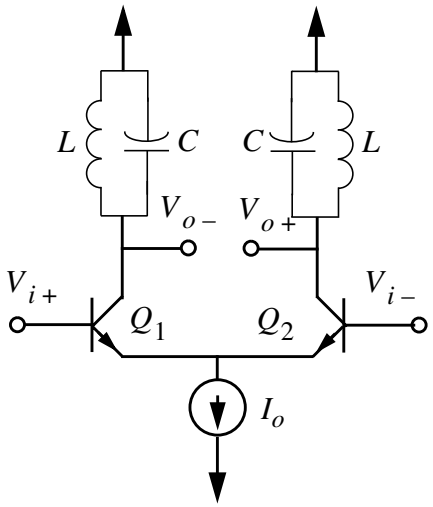


Figure 4.2 : A differential LC resonator.

the transfer functions implemented in [Gail89], [Thu91], [Tro93].

1. In [Sch94] and Ch. 5 it is shown that in a fourth-order multiple-pole bandpass ΔΣ modulator for getting the maximum achievable *SNR*, the typical Q required is at least 50.

$$\hat{H}(s) = \frac{ks^N}{(s^2+\omega^2)^N} \tag{4.2}$$

where N is the number of cascade stages, ω is the resonant frequency, and k is the overall filter gain. As shown in [Sch94] and explained in Sec. 3.1, in a bandpass continuous-time modulator with order $2N$ the proper s-domain loop transfer function numerator is a $2N-1$ th-order polynomial with non-zero coefficients having $2N-1$ distinct zeros, while (4.2) has N zeros at $s = 0$. For example recall from (3.23) that in a multiple-pole fourth-order system the loop filter [Sch94] is

$$\hat{H}(s) = \frac{\left(\frac{\pi}{2}-\frac{1}{4}\right)\frac{s}{T}^3 + \left(\frac{3\pi^2}{16}+\frac{\pi}{4}\right)\frac{s}{T^2}^2 + \left(\frac{\pi^3}{8}+\frac{\pi^2}{16}\right)\frac{s}{T^3} + \frac{3}{4}\left(\frac{\pi}{2T}\right)^4}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \tag{4.3}$$

In this chapter we will address the transfer function implementation problem in LC ΔΣ modulators. We will show how we can reproduce those missing coefficients in the numerator of (4.2) by introducing new DAC pulse shaping coefficients in a ΔΣ loop. This is based on the assumption that the simple LC structure shown in Fig. 4.2 (differential or single-ended) has been utilized. One may add some extra L and C components particularly in a discrete-component implementation to realize arbitrary loop transfer functions or a mixed architecture of LC sections and transconductor-C resonators may be considered. However, because of the poor Q performance of on-chip inductances especially at lower 1GHz frequencies we prefer to fix the ΔΣ loop impulse response while keeping the simple LC resonator sections shown in Fig. 4.2.

4.2 Multi-Feedback Design

The idea is that because one feedback ΔΣ loop supplied to a simple LC section does not give the proper loop impulse response, one might add other parallel loop(s) to fix the overall ΔΣ loop impulse response. A multi-feedback structure for a simple LC modulator shown in Fig. 4.1 is presented in Fig. 4.3. The loop impulse response equations of the multi-feedback system in Fig. 4.3 are:

$$\begin{aligned} R_1(t)^* \; h_{LC}(t) \; &= \; h_1(t) \\ R_2(t)^* h_{LC}(t) &= h_2(t) \\ \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\ R_N(t)^* h_{LC}(t) \; &= \; h_n(t) \end{aligned} \tag{4.4}$$

Since the system is linear we can write

$$[R_1(t) + R_2(t) + \ldots + R_N(t)]^* h_{LC}(t) \; = \; h(t) \tag{4.5}$$

where $h(t)$ is the desired loop impulse response associated with the ideal loop transfer function $\hat{H}(s)$ being excited by a straight NRZ, RZ or HZ pulse. Equation (4.5) can be expressed directly by the discrete-time loop impulse response equivalent $h(n)$:

$$[R_1(t) + R_2(t) + \ldots + R_N(t)]^* h_{LC}(t)\Big|_{t \, = \, nT} \equiv h(n) \quad . \tag{4.6}$$

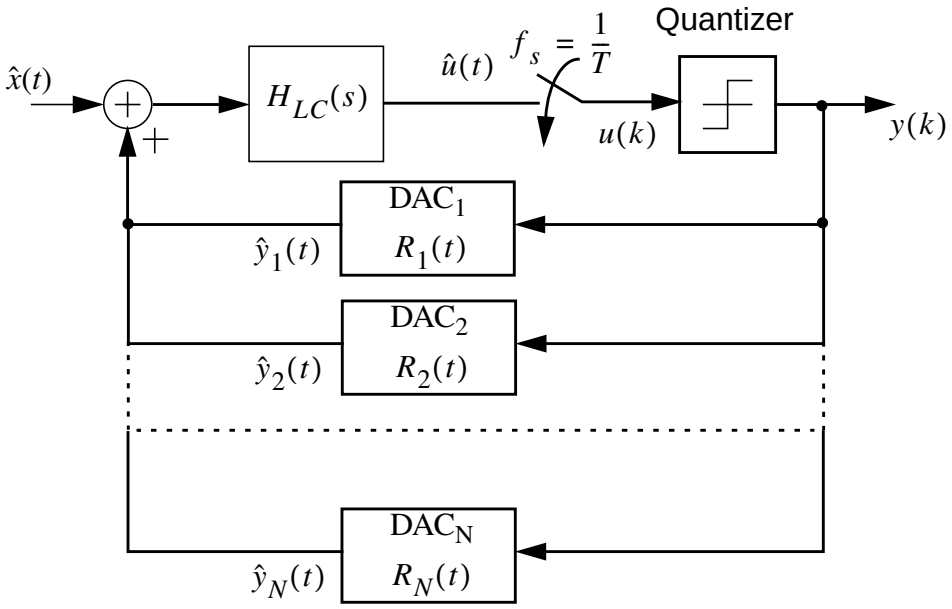


Figure 4.3 : A multi-feedback representation of a LC modulator.

If all pulse waveforms given in (4.5) or (4.6) have the same shape, for example rectangular between $[0, T]$, then their summation just provides a gain for the ΔΣ loop which is not enough for implementing $h(n)$. Therefore, it is required that individual

pulses $R_i(t)$ have different waveforms. One simple arrangement is that $R_i(t)$ pulses don't overlap. For example $R_i(t)$ can be defined as following

$$R_i(t) = \begin{cases} \alpha_i & t_{i-1} < t \le t_i \\ 0 & \text{otherwise} \end{cases} . \tag{4.7}$$

Since each feedback loop encloses a DAC producing a distinct pulse signal shape, the proposed multi-feedback structure is called a system with pulse shaping feedback.

4.2.1 DAC Pulse Shaping

We begin with a second-order bandpass case. The discrete-time loop transfer function [Sch94], [Sing94] is

$$\frac{z^{-2}}{1+z^{-2}}. \tag{4.8}$$

Recall from Sec. 3.1.1 that the loop impulse response of this system is a *cosine* waveform (3.18) with first two samples zero:

$$h(n) = \begin{cases} 0 & n = 0, 1 \\ \cos\left(\dfrac{(n-2)\pi}{2}\right) & n = 2, 3, \ldots \end{cases} \tag{4.9}$$

In a continuous-time modulator the overall loop impulse response is obtained by convolution of the *s*-domain loop filter with the DAC impulse response. Three different possible DAC feedbacks — non-return to-zero (NRZ), return to-zero (RZ), and half-delay return to-zero (HZ) — were introduced in Sec. 3.1. Their impulse responses represented by $R_{NZ}(t)$, $R_{RZ}(t)$ and $R_{HZ}(t)$ were shown in Fig. 3.5 too. The overall discrete-time loop transfer functions in a continuous-time modulator employing a simple LC filter *i.e.*

$$\frac{\omega s}{(s^2+\omega^2)} = \mathcal{L}[h_2(t)] \tag{4.10}$$

where $h_2(t) = \omega\cos(\omega t)$ and $\omega = \pi/(2T)$, for NRZ, RZ, and HZ feedback pulses respectively are

$$\mathcal{Z}[R_{NZ}(t) \ *h_2(t)\big|_{t=nT}] = \frac{z^{-1}(1-z^{-1})}{1+z^{-2}}$$

$$\mathcal{Z}[R_{RZ}(t) \ *h_2(t)\big|_{t=nT}] = \frac{z^{-1}\left(\left(1-\frac{1}{\sqrt{2}}\right)-\frac{1}{\sqrt{2}}z^{-1}\right)}{1+z^{-2}} \qquad (4.11)$$

$$\mathcal{Z}[R_{HZ}(t) \ *h_2(t)\big|_{t=nT}] = \frac{z^{-1}\left(\frac{1}{\sqrt{2}}-\left(1-\frac{1}{\sqrt{2}}\right)z^{-1}\right)}{1+z^{-2}}$$

As (4.11) shows the loop impulse response of a system including any feedback: NRZ, RZ, or HZ by itself can not implement the required *cosine* loop impulse response given in (4.9). In particular, none of them provides a pure z^{-2} term to make the second sample zero. However, with a linear combination of any of two preceding feedback pulses given in (4.11), for example, RZ and HZ as shown in Fig. 4.4, it is possible to produce the desired second-order loop function $z^{-2}/(1+z^{-2})$. As Fig. 4.4 shows the quantized signal is fed back to a RZ DAC and a HZ DAC. The HZ DAC can be modeled by a half delay block $z^{-1/2}$ followed by a RZ DAC as shown in Fig. 4.4. The DAC output pulses are then scaled by k_{rz} and k_{hz} coefficients accordingly in such a way that the overall loop transfer function implements the desired second-order system (4.8). This requires finding two unknown coefficients from two simple linear equations. For example, for k_{rz} and k_{hz} from (4.8) and (4.11) the equality

$$k_{rz}z^{-1}\left(\left(1-\frac{1}{\sqrt{2}}\right)-\frac{1}{\sqrt{2}}z^{-1}\right)+k_{hz}z^{-1}\left(\frac{1}{\sqrt{2}}-\left(1-\frac{1}{\sqrt{2}}\right)z^{-1}\right)\equiv z^{-2} \qquad (4.12)$$

implies that

$$\begin{aligned} k_{rz}\left(1-\frac{1}{\sqrt{2}}\right)+k_{hz}\frac{1}{\sqrt{2}} &= 0 \\ -k_{rz}\frac{1}{\sqrt{2}}-k_{hz}\left(1-\frac{1}{\sqrt{2}}\right) &= 1 \end{aligned} \qquad (4.13)$$

which results in $k_{rz} = -(1+1/\sqrt{2})$ and $k_{hz} = 1/\sqrt{2}$.

As shown in Fig. 4.4 there is no digital delay in the ΔΣ loop preceding the DACs. This represents a zero-delay continuous-time scheme. Recall from Sec. 3.1.1 and (3.20) that it is possible to have a second-order continuous-time system in which one delay is realized digitally [Sho]. In that case the loop coefficients need to satisfy

$$k_{rz}z^{-1}\left(\left(1-\frac{1}{\sqrt{2}}\right)-\frac{1}{\sqrt{2}}z^{-1}\right)+k_{hz}z^{-1}\left(\frac{1}{\sqrt{2}}-\left(1-\frac{1}{\sqrt{2}}\right)z^{-1}\right)\equiv z^{-1} \tag{4.14}$$

which implies

$$\begin{aligned} k_{rz}\left(1-\frac{1}{\sqrt{2}}\right)+k_{hz}\frac{1}{\sqrt{2}} &= 1 \\ k_{rz}\frac{1}{\sqrt{2}}+k_{hz}\left(1-\frac{1}{\sqrt{2}}\right) &= 0 \end{aligned} \tag{4.15}$$

This set of equations results in $k_{rz} = -1/\sqrt{2}$ and $k_{hz} = 1 + 1/\sqrt{2}$.

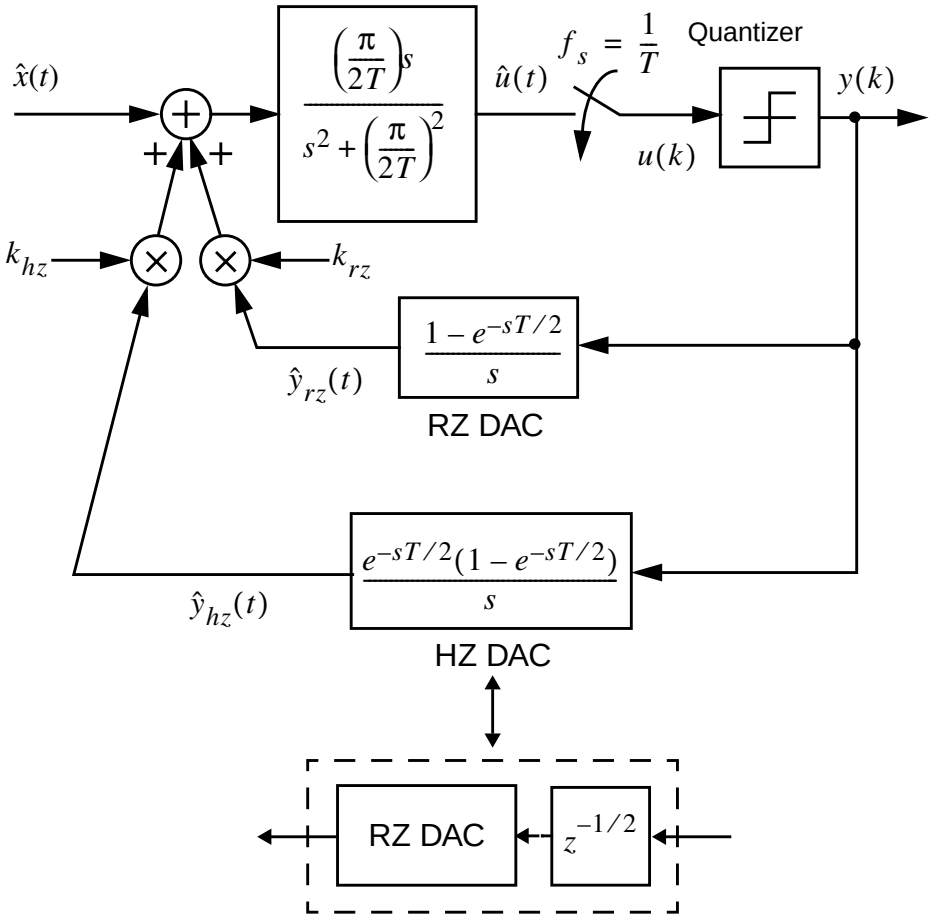


Figure 4.4 : A second-order multi-feedback (RZ and HZ) ΔΣ modulator with a LC resonator loop filter.

The coefficients of the zero-delay second-order system (shown in Fig. 4.4) for three different combinations of NRZ, RZ and HZ pulses are given in Table 4.1. The

Table 4.1: Second-order LC modulator parameters.

Coefficients		Combinations		
		RZ−HZ	NRZ−RZ	NRZ−HZ
Zero-delay coefficients	k_{nz}		$1/\sqrt{2}$	$-(1+1/\sqrt{2})$
	k_{rz}	$-(1+1/\sqrt{2})$	$-1/(\sqrt{2}-1)$	
	k_{hz}	$1/\sqrt{2}$		$1/(\sqrt{2}-1)$
One-delay coefficients	k_{nz}		$1+1/\sqrt{2}$	$-(1/\sqrt{2})$
	k_{rz}	$-(1/\sqrt{2})$	$-1/(\sqrt{2}-1)$	
	k_{hz}	$1+1/\sqrt{2}$		$1/(\sqrt{2}-1)$

corresponding coefficients for one-delay scheme is given in Table 4.1 too.

For implementing the fourth-order bandpass system from a cascade of two simple LC resonators, $\omega s/(s^2+\omega^2)$, as shown in Fig. 4.5 four coefficients are required. In Fig. 4.5 the shorter loops (the paths with k_2 coefficients) each contains a resonator whose convolution with the corresponding feedback pulse results in the transfer functions given in (4.11). The longer loops (the paths with k_4 coefficients) each include a cascade of two resonators

$$\frac{\omega^2 s^2}{(s^2+\omega^2)^2} = \mathcal{L}[h_4(t)] \qquad (4.16)$$

where $h_4(t) = 0.5\,\omega^2[t\cos\omega t + (\sin\omega t)/\omega]$ and $\omega = \pi/(2T)$. The transfer function on these paths for NRZ, RZ, and HZ feedback pulses respectively are

$$\mathcal{Z}\Big[R_{NZ}(t) \ *h_4(t)|_{t=nT}\Big] = 0.25\frac{\pi z^{-1}(1-z^{-1}-z^{-2}+z^{-3})}{(1+z^{-2})^2}$$
$$\mathcal{Z}\Big[R_{RZ}(t) \ *h_4(t)|_{t=nT}\Big] = \frac{\pi z^{-1}(0.161612-0.265165z^{-1}+0.015165z^{-2}+0.088388z^{-3})}{(1+z^{-2})^2} \qquad (4.17)$$
$$\mathcal{Z}\Big[R_{HZ}(t) \ *h_4(t)|_{t=nT}\Big] = \frac{\pi z^{-1}(0.088388+0.015165z^{-1}-0.265165z^{-2}+0.161612z^{-3})}{(1+z^{-2})^2}$$

The required multiple-pole loop transfer function for a fourth-order system as shown in [Lon93], [Sch94] and (3.22) is $z^{-2}(2+z^{-2})/(1+z^{-2})^2$. The discrete-time and continuous-time (one-delay scheme) loop impulse response of this system are given in (3.24) and (3.25) respectively and graphically shown in Fig. 3.9. It should be noted that because of a z^{-1} discrete delay factor inside the loop (Fig. 4.5) the overall continuous-time loop impulse response is shifted by T in Fig. 3.9.

The continuous-time loop filter shown in (4.3) for an NRZ pulse can be implemented by a transconductor-C architecture directly [Sch94]. For the fourth-order LC modulator, it is obvious from (4.17) that none of the simple NRZ, RZ or HZ modulators can implement this transfer function directly. However, from (4.11) and (4.17), it can be shown that with any combination of two pulses like RZ and HZ it is possible to build an ideal fourth-order loop transfer function. Fig. 4.5 depicts a system with RZ DAC and HZ DAC feedback pulses and four loop coefficients k_{4rz}, k_{4hz}, k_{2rz} and k_{2hz} which provide four degrees of freedom for implementing a desired fourth-order loop transfer function. This requires solving four linear equations — two from (4.11) and two from (4.17) — to obtain the four unknown coefficients. As shown in Fig. 4.5 in this algorithm by adding each extra LC section two new coefficients are added too. The new coefficients guarantee a sufficient number of parameters for implementing any arbitrary loop transfer function.

The coefficients of the fourth-order multiple-pole system (with one digital delay inside the loop like the one shown in Fig. 4.5) for three different combinations of NRZ, RZ and HZ pulses are given in Table 4.2. For instance, the four RZ and HZ coefficients shown in Fig. 4.5 are $k_{4rz} = -0.450158$, $k_{4hz} = 1.08678$, $k_{2rz} = -0.633883$ and $k_{2hz} = 2.98744$. Recall from Sec. 3.1.4 that there is a zero-delay solution [Sho] for a

multiple-pole fourth-order continuous-time modulator too for which the proper coefficients can be found.

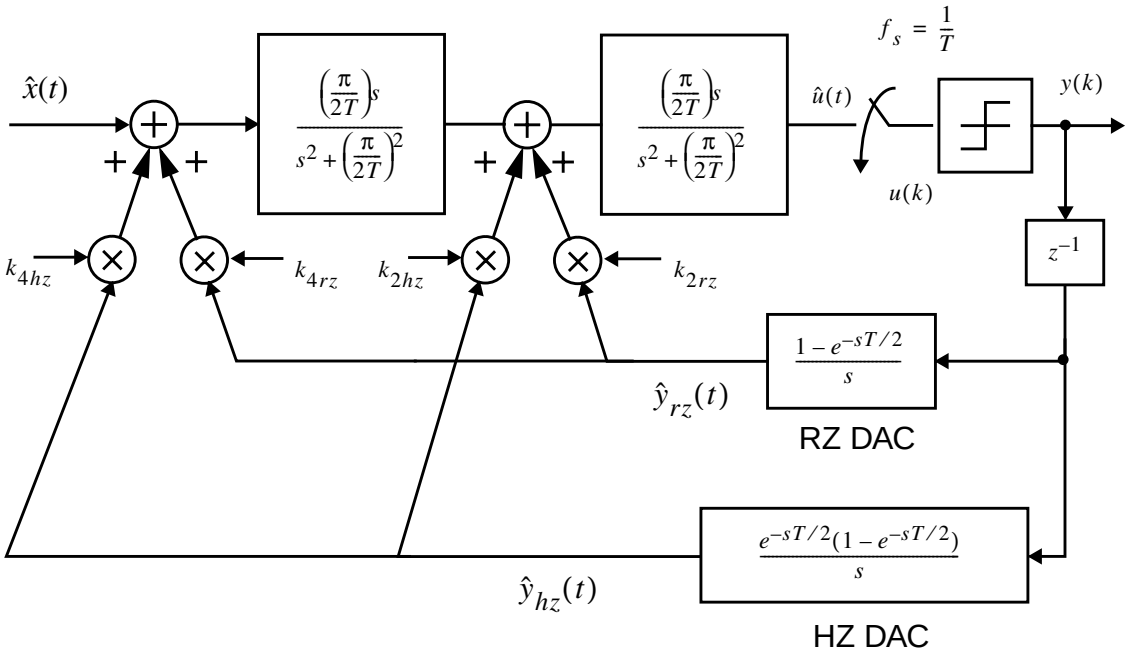


Figure 4.5 : A fourth-order multi-feedback (RZ and HZ) ΔΣ modulator with cascade of two LC resonator loop filters.

4.2.2 Signal Transfer Function

Although the loop transfer function of the given LC systems and their discrete-time counterparts are made equal, their input signal transfer functions are different [Sho] (shown in Sec. 3.1.4 for different continuous-time modulators). Recall from (3.54) that the signal transfer function in a continuous-time modulator is defined as $STF_c(\omega) = \hat{G}(j\omega)/[1-H(e^{j\omega T})]$. For example for the second order and fourth-order LC systems shown in Fig. 4.4 and Fig. 4.5 the *STF*s respectively are:

$$\left|STF_c(\omega)\right| = \frac{2\omega_o \omega \cos\omega T}{(\omega_o^2 - \omega^2)(5+4\cos 2\omega T)^{1/2}} \quad \text{and} \qquad (4.18)$$

$$\left|STF_c(\omega)\right| = \frac{4\omega_o^2\ \omega^2(\cos\omega T)^2}{(\omega_o^2\ -\omega^2)^2(21+24\cos 2\omega T+4\cos 4\omega T)^{1/2}} \qquad (4.19)$$

where $\omega_o = \frac{\pi}{2T}$. It can be shown that the in-band signal gain (at ω_o) in the second-order and the fourth-order LC modulators shown in Fig. 4.4 and Fig. 4.5 are $\pi/2$ and $(\pi/2)^2$ respectively. This signal gain difference causes a given *SNR* in the different LC systems to happen at different input signal levels.

Table 4.2: Multiple-pole fourth-order LC modulator parameters.

Coefficients		Combinations		
		RZ−HZ	NRZ−RZ	NRZ−HZ
Fourth-Order coefficients	k_{4nz}		1.08678	–0.450158
	k_{4rz}	–0.450158	–1.53694	
	k_{4hz}	1.08678		1.53694
Second-Order coefficients	k_{2nz}		2.98744	–0.633883
	k_{2rz}	–0.633883	–3.62132	
	k_{2hz}	2.98744		3.62132

4.3 Simulation Results

The maximum *SNR*s in a 2 MHz bandwidth, with a sinusoidal input at 50 MHz, for the second-order discrete-time system and the second-order LC modulator shown in Fig. 4.4 were 47.9 dB and 46.4 dB which occurred at input amplitude 0.49 and 0.39 respectively. For the fourth-order discrete-time and LC systems, the maximum *SNR*s in the same bandwidth and frequency were 65.4 dB and 64.27 dB which happened at input amplitude 0.49 and 0.31 respectively. The bit stream spectrum of the multiple-pole fourth-order LC modulator for a 0.31 input sine wave at 50 MHz is shown in Fig. 4.6

(the clock rate is 200 MHz).

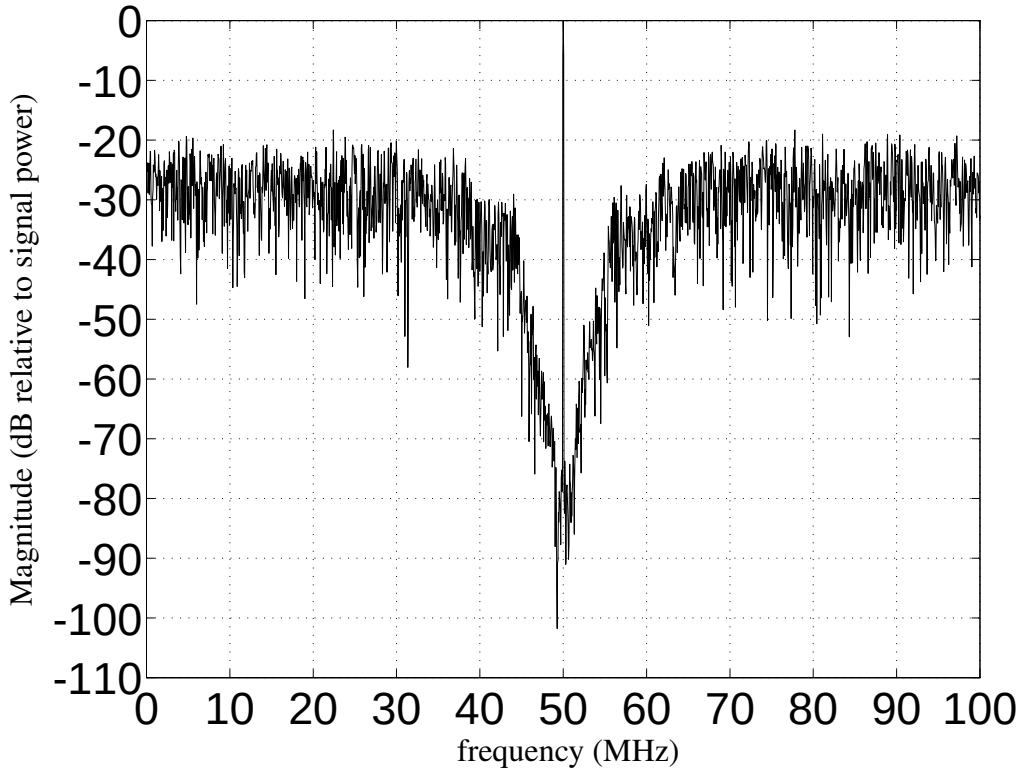


Figure 4.6 : The bit stream spectrum of simulated 4th-order LC modulator (input frequency is at 50MHz).

4.4 Summary

The design of a continuous-time LC bandpass ΔΣ modulator has been discussed. It has been shown that by employing a DAC pulse shaping technique it is possible to force the time domain response of a cascaded LC ΔΣ modulator loop to match that of the discrete-time ΔΣ modulator loop equivalent. The general architecture for a LC ΔΣ modulator with DAC pulse shaping is given. Adding two degrees of freedom at the input of each simple bandpass LC resonator section by means of pulse shaping allows complete control of noise shaping for an arbitrary ΔΣ modulator order. At any LC bandpass ΔΣ modulator with order of *2N*, the new *2N* unknown coefficients can easily be found by

solving a set of *2N* linear equations. A second-order and a multiple-pole fourth-order modulator, the two most common bandpass examples, have been shown. The simulation results for these examples verified the theory.

Chapter 5

Transconductor-*C* Filter Design for Continuous-Time Delta-Sigma Modulator

In Ch. 3 an exact method for designing the *s*-domain transfer functions for continuous-time ΔΣ loop filters was given. An nth-order modulator requires a loop filter whose denominator has an order n and generally its numerator has an order $n-1$. Note that in a bandpass modulator, since the poles of the loop filter are complex conjugate pairs, the denominator order n is always even. The problem of transfer function implementation with *LC* sections was discussed in Ch. 4. The techniques of transconductor-*C* filter design for ΔΣ loop filters along with a practical transconductor-*C* ΔΣ modulator design are studied in this chapter.

5.1 Transconductor-*C* Filters

The transconductor-capacitor (TC) or G_m-*C* technique is a well-known approach for implementing high-speed continuous-time filters. They were commercially used quite early [Mou80] with bipolar technology. They have been developed in different technologies such as CMOS [Gop90], [Kru88], [Kho91], [Snel92], bipolar [Veir92] and BiCMOS [Gro92], [Lab93], [Wil93], [Shov92]. They have been chosen for many industrial applications including the read channel of disk drives [Kho91], [Lab93], [Veir92], high-speed data links [Shov92], digital TV [Gop90], HDTV [Wil93], etc.

In this chapter a new application for TC filters working as ΔΣ modulator loop filters is introduced. Although discrete-component off-chip *LC* bandpass continuous-time filters

for ΔΣ modulator application have been employed [Gail89], [Thu91], [Tro93], the practical BiCMOS TC ΔΣ modulator given in this chapter is the first fully monolithic continuous-time bandpass modulator[1] implemented.

5.1.1 A Generic Transconductor-*C* Biquad (second-order) Filter

The basic building block of a TC filter is a transconductor-*C* integrator which is composed of a transconductor element represented by g_m and a pair of capacitors C as shown in Fig. 5.1. A transconductor is a two port voltage controlled source device (or a

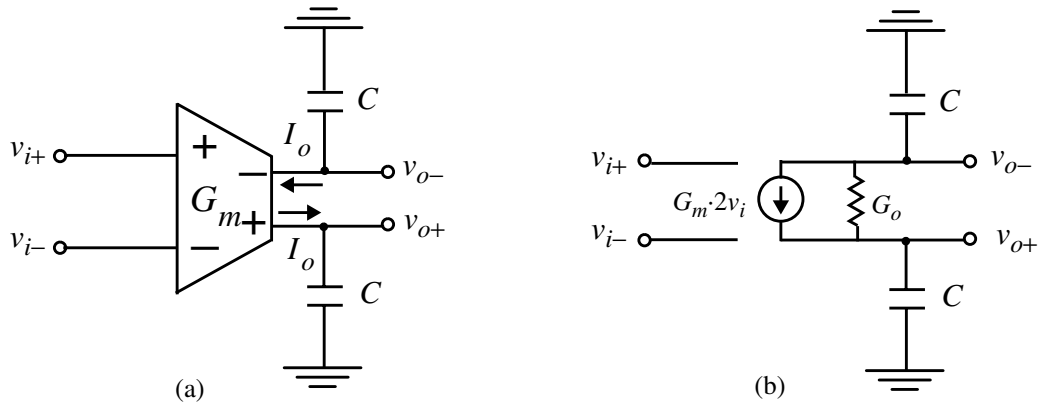


Figure 5.1 : (a) A simple Transconductor-*C* Integrator, (b) a model for the TC integrator in (a).

voltage-to-current converter) with finite output impedance which ideally should be linear handling large swing signals *i.e.* $I_o = G_m \cdot 2V_i$ where $2V_i = V_{i+} - V_{i-}$. So for $2V_o = V_{o+} - V_{o-}$ it easily can be shown that the TC integrator transfer function is

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{G_m}{C/2}}{s + \frac{G_o}{C/2}} \qquad (5.1)$$

where G_o is the output conductance of the transconductor which limits the integrator's gain to a finite value g_m / g_o and moves the unity-gain frequency from $2G_m/C$ to

1. A fourth-order continuous-time lowpass modulator using integrated passive R-C opamp integrators has been implemented [Red91] and a G_m-C lowpass continuous-time modulator has been developed in a Ph.D program [Bre95].

$2G_m\sqrt{1-(G_o/G_m)^2}/C$.

To design a second-order system (resonator), two transconductors, one with positive gain and the other negative, can be connected back to back in a loop as shown in Fig.

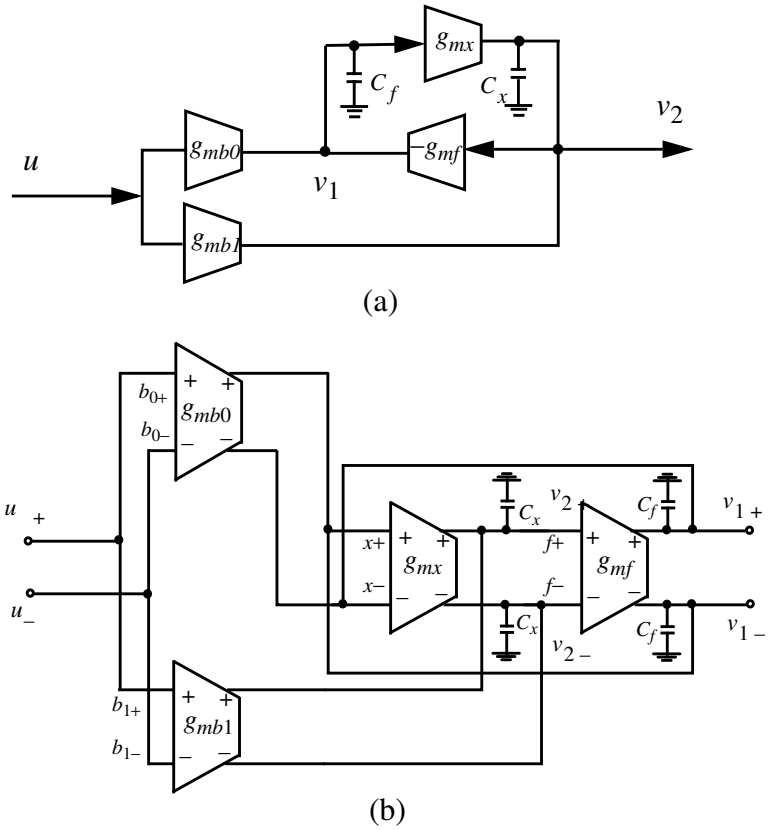


Figure 5.2 : A transconductor-*C* resonator (a) single-ended (b) differential.

5.2a. Implementation of a transconductor with a negative sign is performed by cross-coupling in the balanced differential transconductors as shown in Fig. 5.2b. It can be shown that the two transfer functions for this second-order system are

$$\frac{V_1}{U} = \frac{\frac{g_{mb0}}{C_f}s - \frac{g_{mb1}g_{mf} + g_{mb0}(g_{ox}+g_{ob1})}{C_xC_f}}{s^2 + \left(\frac{g_{of}+g_{ob0}}{C_f} + \frac{g_{ox}+g_{ob1}}{C_x}\right)s + \frac{g_{mx}g_{mf} + (g_{of}+g_{ob0})(g_{ox}+g_{ob1})}{C_xC_f}} \quad (5.2)$$

and

$$\frac{V_2}{U} = \frac{\frac{g_{mb1}}{C_x}s + \frac{g_{mb0}g_{mx} + g_{mb1}(g_{of} + g_{ob0})}{C_xC_f}}{s^2 + \left(\frac{g_{of} + g_{ob0}}{C_f} + \frac{g_{ox} + g_{ob1}}{C_x}\right)s + \frac{g_{mx}g_{mf} + (g_{of} + g_{ob0})(g_{ox} + g_{ob1})}{C_xC_f}} \quad (5.3)$$

As can be noticed from (5.2) and (5.3) the transconductors represented by g_{mb0} and g_{mb1} control the zero of resonator's transfer function and those shown by g_{mx} and g_{mf} implement the transfer function poles.

5.1.2 Resonator with Infinite Q

Recall from Ch. 3 that in a bandpass ΔΣ modulator the loop filter is ideally a perfect resonator (*e.g.* see Table 3.1). This means that the loop filter Q is infinite so the poles are exactly on $j\omega$ axis. On the other hand (5.2) and (5.3) imply that because of the finite output impedance of transconductors the second-order transfer functions provide a finite-Q filter. The second problem is that the resonant frequency is influenced by the transconductors' output resistances too.

In order to compensate for the transconductors' finite resistances and control the filter's Q, particularly for high-Q filters, one may employ an extra transconductor in the resonator loop which is configured as a negative resistor (self-connected transconductor [Shov92], [Nau92][2]), a controlled damping resistor [Snel92], or a negative impedance circuit (NIC) [Veir92], [Tak91]. A second-order system with a negative self-connected transconductor in the loop for Q enhancement is shown in Fig. 5.3. The transfer function (5.2) now becomes

$$\frac{V_1}{U} = \frac{\frac{g_{mb0}}{C_f}s - \frac{g_{mb1}g_{mf} + g_{mb0}(g_{ox} + g_{ob1} + g_{oQ} - g_{mQ})}{C_xC_f}}{s^2 + \left(\frac{g_{of} + g_{ob0}}{C_f} + \frac{g_{ox} + g_{ob1} + g_{oQ} - g_{mQ}}{C_x}\right)s + \frac{g_{mx}g_{mf} + (g_{of} + g_{ob0})(g_{ox} + g_{ob1} + g_{oQ} - g_{mQ})}{C_xC_f}} \quad (5.4)$$

For some g_{mQ} the s coefficient of the denominator in (5.4) would be zero which consequently produces the desired infinite Q.

2. For setting a finite Q it is usual to employ a positive self-connected transconductor as a resistor in the loop [Alin92], [Kwa91].

A second method for remedying the non-ideal effects (such as the transconductor's finite impedance and/or parasitic elements) which deteriorate the Q of a TC filter is the phase compensation or excess phase cancellation [Gop90], [Kho91], [Wys94]. A third method for controlling the Q of a TC filter or integrator phase can be distinguished in TC-amp integrators (Miller integrator). This is explained in more detail in Sec. 5.4.

In an ideal integrator the amplitude rolls off by –20 dB and phase is –90° for all frequencies. However, because of the finite output impedance in a transconductor (5.1) there is a low frequency pole which shifts the phase from zero toward –90° over almost a frequency decade. The –90° (*i.e.* perfect integration) condition only occurs at infinite frequency. Accepting some trivial phase error, however, the one-pole system may meet a filter design requirement at very high frequencies (*e.g.* $\omega \gg \frac{g_o}{(C/2)}$ in (5.1)). Furthermore, in a practical circuit the second parasitic pole and/or RHP zero in a Miller integrator (see Sec. 5.4) contribute more phase lag. This is the so called excess phase in an integrator. The effect the parasitic elements have is then to disturb the ideal unity-gain frequency. This effect can be compensated by reducing the excess phase in a circuit. This is usually performed by creating a phase lead through an extra LHP zero [Gop90].

5.2 Filter Architecture

In Table 3.1 it was shown that a general second order bandpass filter is needed for a second-order continuous-time bandpass ΔΣ modulator. In Sec. 3.1.1 and Sec. 3.1.2 for higher order loops, it was shown that the filter's loop denominator is composed of a product of resonators (multiple or spread for that matter). For example a fourth-order system includes two resonators. That's why the cascade of the resonators shown in Fig. 5.2 and/or Fig. 5.3 intuitively seems to be a good candidate for a bandpass ΔΣ modulator's filter. For example a fourth-order ΔΣ TC modulator using cascade of two resonators is shown in Fig. 5.4. It corresponds to the architecture shown back in Fig. 3.22. Recall from Sec. 3.1.7 that it is preferred to have control on the signal transfer function as well as the loop transfer function. This is possible by choosing appropriate feedforward and loop transfer functions represented by $\hat{G}(s)$ and $\hat{H}(s)$ in Fig. 3.22. As will be shown the structure shown in Fig. 5.4 provides enough degrees of freedom to

implement an arbitrary pole-zero combination for both loop and feedforward transfer functions.

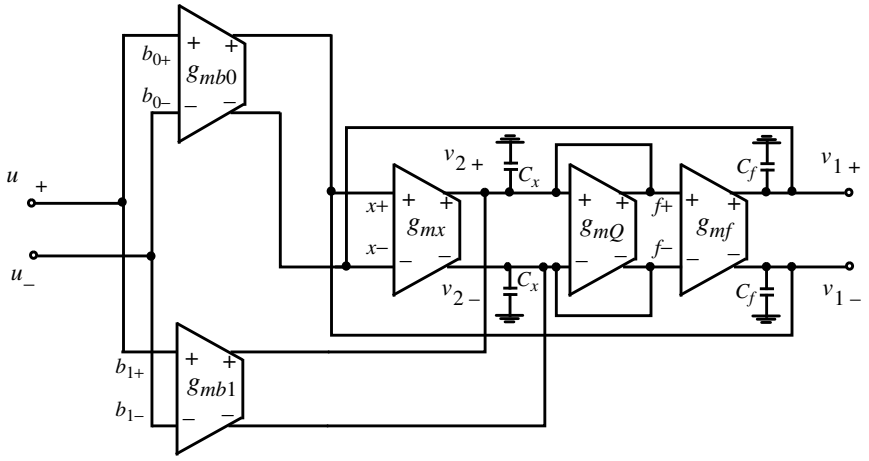


Figure 5.3 : A transconductor-*C* resonator with Q enhancement.

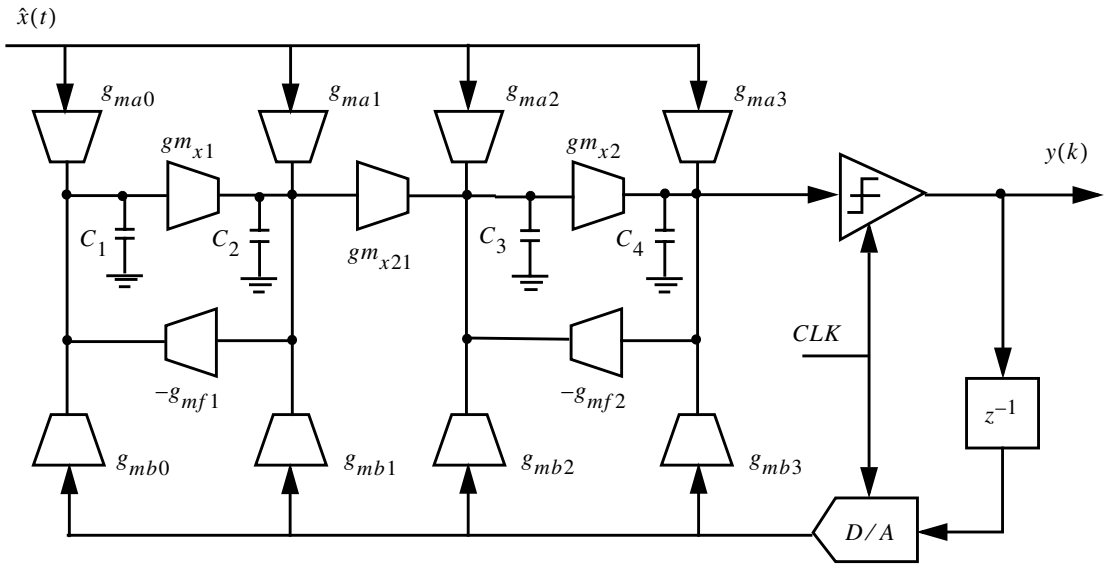


Figure 5.4 : A 4th-order ΔΣ TC modulator single-ended schematic (including cascade of two resonators).

As indicated in (5.2) and (5.3) for a single stage resonator it can easily be verified that in Fig. 5.4 the transconductors represented by (g_{ma0}, g_{ma1}, g_{ma2}, g_{ma3}) and (g_{mb0}, g_{mb1},

g_{mb2}, g_{mb3}) implement the zeros of $\hat{G}(s)$ and $\hat{H}(s)$ respectively, while the transconductors represented by (g_{mx1}, g_{mf1}) and (g_{mx2}, g_{mf2}) implement the common poles. The transconductor represented by g_{mx21} is for coupling of the first resonator to the second which appears to have influence on both loop and feedforward transfer function's zeros.

It can be shown that the loop transfer function from the DAC output to the quantizer input neglecting the transconductor's output impedances is

$$\hat{H}(s)=\frac{\frac{g_{mb3}}{C_4}s^3+\frac{g_{mb2}g_{mx2}}{C_3C_4}s^2+\left(\frac{g_{mb1}g_{mx21}g_{mx2}}{C_2C_3C_4}+\frac{g_{mb3}g_{mx1}g_{mf1}}{C_1C_2C_4}\right)s+\frac{g_{mb2}g_{mx1}g_{mf1}g_{mx2}+g_{mb0}g_{mx1}g_{mx21}g_{mx2}}{C_1C_2C_3C_4}}{\left(s^2+\frac{g_{mx1}g_{mf1}}{C_1C_2}\right)\left(s^2+\frac{g_{mx2}g_{mf2}}{C_3C_4}\right)} \tag{5.5}$$

For the feedforward transfer function, $\hat{G}(s)$, the g_{mb}'s in (5.5) should be replaced with the corresponding node g_{ma}'s. The denominators of the feedforward and the loop transfer functions are identical as they share (g_{mx1}, g_{mf1}, C_1, C_2) and (g_{mx2}, g_{mf2}, C_3, C_4) loop circuitry.

By comparing the TC transfer functions with the ideal $\hat{G}(s)$ and $\hat{H}(s)$ explained in Ch. 3 the ΔΣ TC modulator component values can be obtained. For example, to implement the fourth-order multiple pole loop filter $\hat{H}(s)$ given in (3.23) and the feedforward filter $\hat{G}(s)$ in (3.59), it can be shown that the transconductor values shown in Fig. 5.4 should be as follows:

$$\begin{cases} g_{mb0} = -\frac{1}{\pi}g_m \\ g_{mb1} = \frac{1}{\pi}g_m \\ g_{mb2} = \left(\frac{3}{4}+\frac{1}{\pi}\right)g_m \\ g_{mb3} = \left(1-\frac{1}{2\pi}\right)g_m \end{cases}, \quad \begin{cases} g_{ma0} = \frac{1}{\pi}g_m \\ g_{ma1} = \frac{1}{\pi}g_m \\ g_{ma2} = -\frac{1}{\pi}g_m \\ g_{ma3} = \frac{1}{4}\left(1-\frac{2}{\pi}\right)g_m \end{cases}. \tag{5.6}$$

$$g_{mx1} = g_{mf1} = g_{mx2} = g_{mf2} = g_{mx12} = g_m$$

where $\omega_o = \pi/2T = g_m/C$, $T=1/f_s$ is the sampling period and $C_1 = C_2 = C_3 = C_4 = C$.

5.3 Sensitivity to the Loop Filter Parameters (Q and Resonant Frequency)

Recall from Sec. 3.3.1 that the signal-to-noise ratios of the ideal discrete-time and continuous-time ΔΣ modulators connected by a pulse invariant transformation given in Ch. 3 were very close. For example, the maximum *SNR*s of the multiple-pole fourth-order bandpass discrete-time (3.22) and the continuous-time (3.23) modulators were 55.25 dB and 55.93 dB respectively. The *SNR*s were obtained from simulations at 1 MHz bandwidth with a 20 MHz sinusoidal input having a 80 MHz clock. The input signal amplitude at discrete-time and continuous-time modulators were −6 dB and −6.9 dB (relative to the quantizer level) respectively which accounts for different signal transfer function (or in-band gain) explained in Sec. 3.2.

The ideal TC ΔΣ architecture shown in Fig. 5.4 with the loop filter given in (5.5) was simulated too. The values of the transconductors and the capacitors of the loop filter were selected in such a way that the transfer function given in (5.5) implemented exactly the ideal fourth-order ΔΣ loop transfer function given in (3.23). The resonance frequency was chosen again at 20 MHz *i.e.*

$$(g_{mx1}g_{mf1})/C_1C_2 = (g_{mx2}g_{mf2})/C_3C_4 = (2\pi \cdot 20\ \text{MHz})^2 .$$

Again the *SNR* for the fourth-order TC modulator was simulated with a 20 MHz sinusoidal input and −6.9 dB amplitude level for 1 MHz bandwidth having a 80 MHz clock. The resulting *SNR* was 55.11 dB, very close to the 55.93 dB obtained from the ideal continuous-time and 55.25 dB from the ideal discrete-time modulator simulations.

The same simulations for a spread-pole fourth-order ΔΣ modulator with the loop filter given in (3.60) have been performed. The corresponding *SNR*s for the discrete-time and continuous-time modulators with the ideal transfer functions were 62.58 dB and 60.51 dB respectively and 59.87 dB for the transconductor-*C* architectural simulation.

This implies that the architecture introduced in Fig. 5.4 is a good candidate for implementation of a desired TC ΔΣ loop filter. However, as is well known the transconductor-*C* filters are subject to fabrication tolerances, temperature variations and parasitic effects. Hence, some tuning circuitry is often required to keep the TC filter parameters like its Q and the resonance frequency within the desired specifications.

Sometimes, particularly in low Q filters, designers may choose some careful designs to reduce the sensitivity of a TC filter to parasitic components instead of using automatic tuning. Despite these considerations there is always some error in filter specifications in real life. Therefore, the sensitivity of the fourth-order ΔΣ modulator shown in Fig. 5.4 to its loop filter's parameters, Q and resonance frequency, has been studied as an example.

A plot of *SNR* loss at a BW of 1MHz against the resonators' Qs (the Q of both resonators were changed equally) for the one-delay fourth-order modulator with 12% excess loop delay is shown in Fig. 5.5. For Q of less than 30 idle channel tones started to appear and for Q of less than 20 the noise shaping degraded significantly. From Q=30 to Q=50 the *SNR* improved by 3 dB for each Q increment of 10. From Q=50 to Q=60, the *SNR* improvement was just 0.4dB and the *SNR* loss at Q=60 was 2 dB. Obviously, at Q of infinity the *SNR* loss is 0 dB.

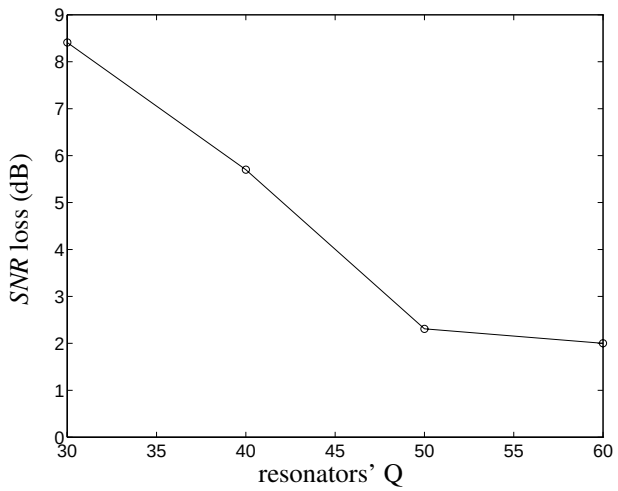


Figure 5.5 : *SNR* loss versus Q of resonators for a modulator with 12% excess loop delay.

The same simulations were performed for the fourth-order modulator with negative Q resonators. It should be noted that in a master-slave tuning scheme for tuning the Q of a slave bandpass ΔΣ modulator the master resonator is actually an open-loop oscillator. Therefore, the non-linear behavior of the master oscillator may cause the poles of the slave or modulator's resonators to move into the RHP. This will result in a ΔΣ modulator

with the *NTF* zeros outside the unit circle. A modulator with the *NTF* zeros outside the unit circle is the so called chaotic ΔΣ modulator [Risb94]. For low order modulators (for example the fourth-order bandpass) this shouldn't affect the modulator's stability and in fact it is known to be beneficial to reduce the tonal behavior significantly. Fig. 5.6 shows

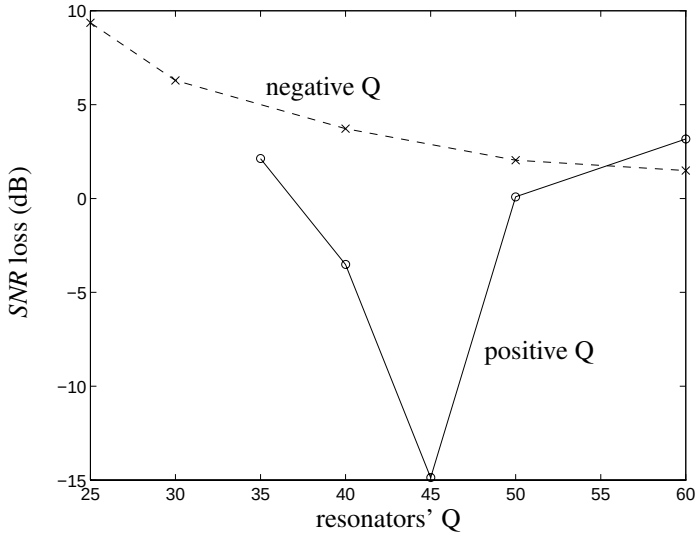


Figure 5.6 : *SNR* loss versus negative and positive Q of resonators for a modulator with zero excess loop delay.

the simulation *SNR* loss (at BW=1MHz) against negative and positive resonators' Qs for the same fourth-order modulator without any extra loop delay. Although as shown in Fig. 5.6 the *SNR* losses were bigger in the modulator with negative Q, the tonal behavior was significantly lower. Moreover, the modulator was still stable with resonators with Q=−25. However, it became unstable for positive Qs lower than 35.

For positive Q as shown in Fig. 5.6, *SNR* is increased for a particular Q (Q=45 here). The reason for this was the tonal behavior observed for this particular Q simulation. Tonal behavior for a specific input level in a ΔΣ modulator can push quantization noise outside the band which as a result deepens the noise-shaping notch and increases the *SNR* (as long as there are not big in-band tones). This tonal behavior is not predictable and can not be looked as a robust way to increase the *SNR* of a modulator.

The *SNR* is much more sensitive to the resonance frequencies. For the spread-pole example, the simulations show that shifting both resonance frequencies ω_1 and ω_2 where

$\omega_1 < 2\pi f_o < \omega_2$ to out-of-band by 1% *i.e.* $(\omega_1 - 0.01\omega_1) \leftarrow \omega_1$ and $\omega_2 \rightarrow (\omega_2 + 0.01\omega_2)$ causes a 10 dB *SNR* loss but when ω_1 and ω_2 are shifted both symmetrically inside the band, the *SNR* loss is much less. For example, when ω_1 and ω_2 are interchanged *i.e.* $\omega_1 \rightarrow \omega_2$ and $\omega_1 \leftarrow \omega_2$ (3.3% frequency change, in this example), the *SNR* loss is around 4.5dB. This may imply that because of inaccuracy of tuning algorithms it may be better to deliberately shift the resonance frequencies slightly inward to the in-band frequency in a spread-pole design. In this example this is around 0.8% *i.e.* $\omega_1 \rightarrow (\omega_1 + 0.008\omega_1)$ and $(\omega_2 - 0.008\omega_2) \leftarrow \omega_2$, which causes 4 dB *SNR* loss, but makes the system less sensitive to resonance frequency changes. However, because most of the conventional $\Delta\Sigma$ modulators usually rely on the multiple-pole loop filters and secondly the f_o error (standard deviation) of the tuning algorithms is on the order of 1-5% [Gop90], [Mar92], [Kho91], [Kwa91] relocating the resonance frequencies of a $\Delta\Sigma$ loop filter from their original places is not very beneficial. The only real solution is to employ an accurate tuning scheme and to include some overhead margin for the loop filter's parameter deviations in the initial design.

5.4 Transconductor–*C*–Amplifier Devices

For many high-speed transconductor-*C* filters a simple single-stage transconductor (sometimes just an inverter structure [Nau92]) is used. However, the DC gain of this kind of transconductor is very low and usually parasitic capacitances are high. Therefore, normally a very wide range of tuning is required to compensate the non-ideal effects such as parasitic capacitances and poor output impedance. Another class of transconductors with the general structure shown in Fig. 5.7 can be recognized as transconductor-Miller-integrator (TMI) or transconductor-*C*-amplifier (transconductor-*C*-opamp). Basically it consists of two stages. The first stage is a conventional transconductor and the second stage is a high gain amplifier or opamp with feedback from a Miller capacitor usually in series with a resistor (triode mode NMOS device as shown in Fig. 5.7). Since "Op amp" (operational amplifier) usually refers to a multiple-stage amplifier with a low-impedance output stage, the more general term "TC-amp" (for transconductor-*C*-amplifier) is used in this dissertation.

Some important features for this class of transconductors are:

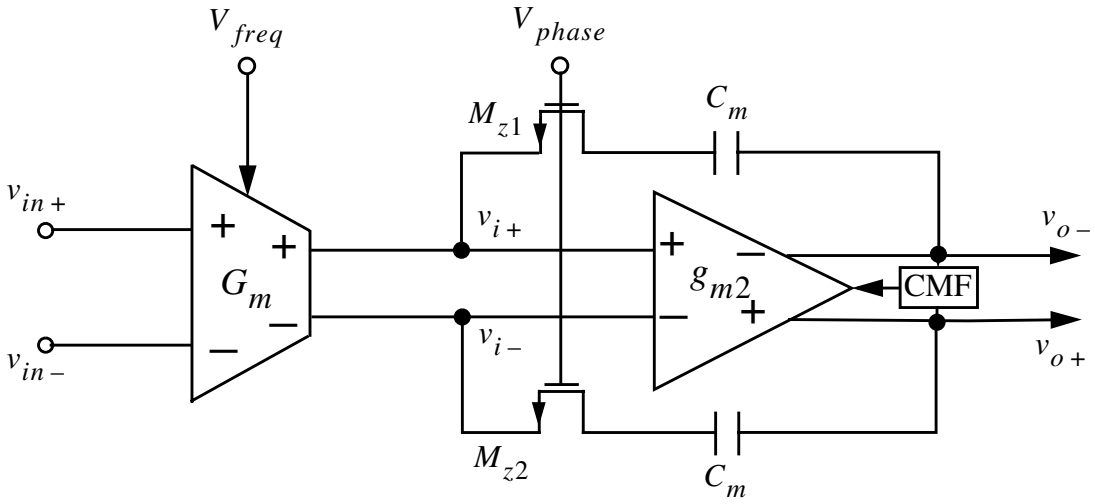


Figure 5.7 : Simplified schematic of a differential TC-amp integrator where M_{z1} and M_{z2} perform excess phase compensation.

1) Since the gain of second-stage amplifier is high the voltage swing at the input of the second-stage amplifier is low (behaving as a virtual ground). Thus a very small portion of the first stage transconductor's output current flows to the parasitic capacitances connected between the amplifier inputs and ground. The low input voltage swing at the second-stage amplifier input lowers its non-linearity contribution in the entire circuit as opposed to ordinary open-loop multi-stage amplifiers in which the very last stage is responsible for producing a major non-linearity. The non-linearity issue is discussed in more detail in Sec. 5.4.6.
2) The unity-gain frequency of a TC-amp integrator shown in Fig. 5.7 is given by $2G_m/C_m$ like a single-stage transconductor shown in Fig. 5.1. Therefore, the unity gain frequency of a TC-amp can be tuned through adjusting the input stage transconductance, G_m, for example with a frequency control voltage V_{freq} as shown in Fig. 5.7.

3) The entire TC-amp DC gain is the product of the DC gain of the input transconductor and the second-stage amplifier. Thus, producing a very high DC gain for a TC-amp is easier. The high DC gain with use of a feedback Miller capacitance moves the dominant pole frequency to ω_o / A_{dc}. A proof for this is given in Appendix C. Creating a very low dominant pole is always desirable for making a good quality integrator. The reason is that if the second pole (and/or other parasitic poles and zeros) are located at a high frequency far from the operating frequency an almost flat −90° phase and a −20 dB/decade gain frequency response in a very wide frequency range could be achieved.

4) The undesired excess phase of a TC-amp produced by higher parasitic poles and zeros can be compensated through adjusting the (Miller) resistors placed in series with the Miller capacitors. For example, with a voltage controlled MOSFET resistor which is tuned by a gate voltage V_{phase} as shown in Fig. 5.7. This is explained in more detail in Sec. 5.4.4 and Sec. 5.4.5.

The trade off between a TC-amp and a simple structure transconductor is speed. Of course a simpler transconductor can afford faster operation compared to a two-stage TC-amp when both are implemented in a same technology. However, as will be shown in a 0.8µm BiCMOS process[3] it is possible to achieve a TC-amp bandpass filter for a ΔΣ modulator working at IF frequencies up to 100MHz which has been the primary objective of this work and to enjoy the advantages mentioned above.

5.4.1 Transconductor-*C*-Amplifier Biquad

To design a second-order system (resonator), two TC-amp integrators, one with positive gain and the other negative, can be connected back to back in a loop as shown in Fig. 5.8. Implementation of an integrator with a negative sign is performed by cross-coupling in a balanced differential transconductor as shown in Fig. 5.8. In order to supply the input signal a multi (two)-input transconductor has been used as shown in Fig. 5.8. The

3. Northern Telecom 0.8µm BiCMOS process.

transconductors are tuned by V_{freq} and the overall phase of each TC-amp integrator by V_{ph}. Assuming that all the current of the transconductor stages shown in Fig. 5.8

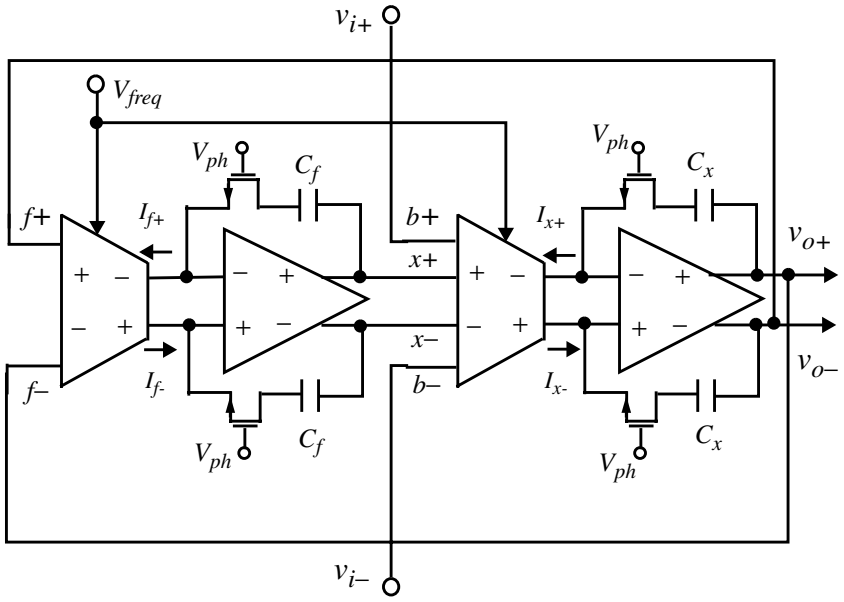


Figure 5.8 : A simplified second-order TC-amp based biquad loop

completely flows into the Miller branches across the amplifier stages (the real virtual ground assumption at the input of amplifiers), it can be shown that the bandpass transfer function for this second-order system is as the following:

$$\frac{V_o}{V_i} = \frac{\dfrac{g_{mb}}{C_x} \cdot \dfrac{1}{1 + g_{mx}g_{mf} \cdot R_{ph}^2} s(1 + R_{ph}C_x s)}{s^2 + \dfrac{g_{mx}g_{mf} \cdot R_{ph}}{1 + g_{mx}g_{mf} \cdot R_{ph}^2}\left(\dfrac{1}{C_f} + \dfrac{1}{C_x}\right)s + \dfrac{g_{mx}g_{mf}}{C_x C_f} \cdot \dfrac{1}{1 + g_{mx}g_{mf} \cdot R_{ph}^2}} \qquad (5.7)$$

where the g_{mb} represents the input transconductance and the g_{mf} and g_{mx} terms represent the loop transconductances. The NMOS transistors in the Miller branches are represented by R_{ph} i.e. a linear resistor which can be varied by V_{ph}. From (5.7) it can be noticed that the variation of R_{ph} changes the s coefficient in the denominator and consequently the Q of the filter. It should be noted that the $1/(1 + g_{mx}g_{mf} \cdot R_{ph}^2)$ term in (5.7) is negligible in our design: for example at 50MHz center frequency it varies between 1 to 0.96. So, the variation of Q by R_{ph} almost doesn't affect the center

frequency f_o. Taking into account the exact effect of the amplifier stages with finite gain and parasitics makes (5.7) very complicated. However, one can simply notice that the V_{ph} voltage only adjusts the phase of each TC-amp integrator inside the loop which in turn tunes the Q of the overall filter.

5.4.2 A BiCMOS Differential Transconductor

A BiCMOS transconductor circuit has been designed to work as the input transconductor G_m of the TC-amp integrator shown in Fig. 5.7. A schematic diagram of a differential BiCMOS transconductor is shown in Fig. 5.9. The input devices are NMOS transistors working in triode mode. In these transistors the following inequality is satisfied $V_{DS} \leq V_{GS}-V_{th}$ such that they are biased deeply in triode. The input NMOS drain-source voltage V_{DS} is in order of 100 mV and V_{GS} is biased at analog ground (2.5 V here). The drain-source voltage V_{DS} is set by the base voltage of Q_1 and Q_2 labelled V_{freq} in Fig. 5.9. The transconductance of an NMOS transistor in triode regime can simply be expressed by $g_m = \mu_n C_{ox} \frac{W}{L} V_{DS}$. So, in order to control the g_m of the input transistors one can change their V_{DS} through changing the BJT Q_1 and Q_2 base voltage V_{freq} and consequently change the resonance frequency.

One major problem in the circuit shown in Fig. 5.9 is that its half-circuit common-mode

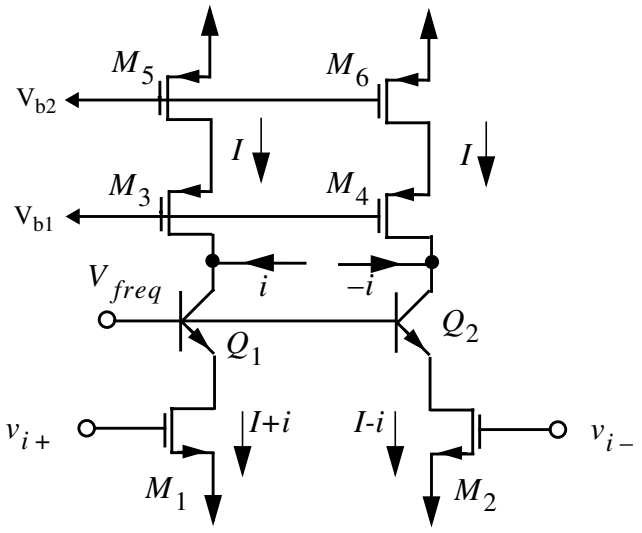


Figure 5.9 : A differential BiCMOS transconductor.

gain is high, equal to its differential gain. For example for the practical circuit which will be discussed shortly the half-circuit DC common-mode gain was 12 dB. As shown in Fig. 5.7 there is a common-mode feedback for the second-stage amplifier. In order to avoid the necessity of another strong individual common-mode feedback for the first stage circuit it is required that the common-mode gain in the input transconductor be very small.

The high common-mode gain problem for the input transconductor can be solved by modifying the circuit shown in Fig. 5.9 to a fully differential cross-coupled transconductor shown in Fig. 5.10. The output cross-coupling connection reduces the

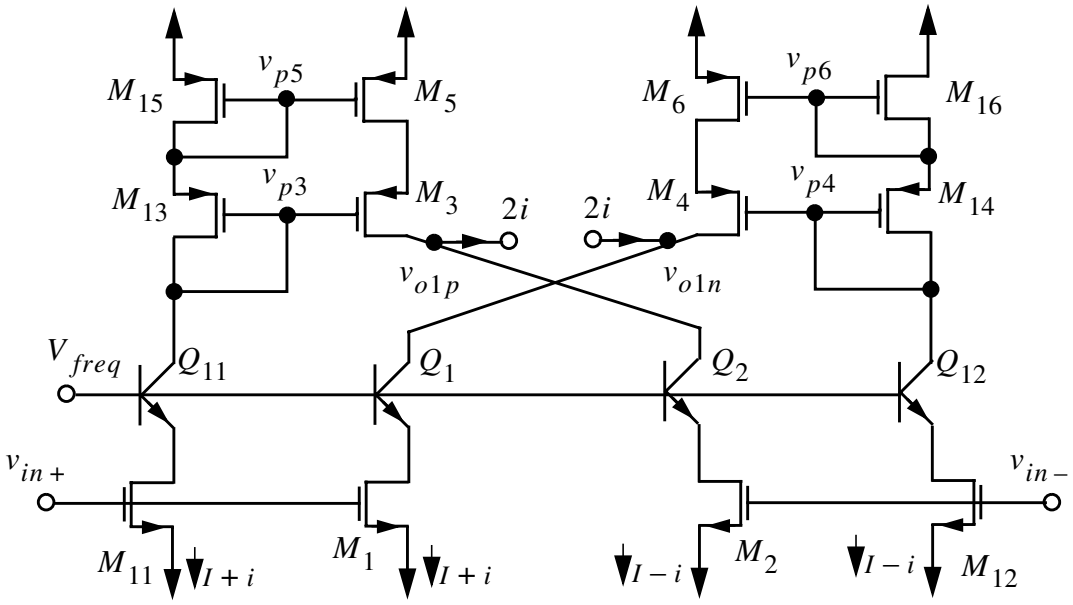


Figure 5.10 : A practical differential cross-coupled BiCMOS transconductor.

common-mode gain of the BiCMOS transconductor significantly. The simulated half-circuit DC common-mode gain of a practical circuit shown in Fig. 5.10 was -26.0[4] dB *i.e.* 38.0 dB (80 times) smaller than the common-gain of the circuit shown in Fig. 5.9. The inter-stage common-mode voltage should properly be set by an additional common-mode feedback circuit, but that was not included. This level is therefore defined by the output impedance of the first stage, and may be biasing the second stage devices at the

4. The half-circuit DC CMRR of this circuit is about 44 dB.

edge of saturation, increasing distortion. This effect on the practical circuit especially the implemented ΔΣ modulator is discussed in Chapter 8.

5.4.3 The Second-Stage Amplifier

Since the two stage TC-amp integrator is insensitive to parasitics the design of the second stage amplifier is not very crucial. However, in order to achieve high gain and to have high speed capability a differential bipolar circuit with cascode PMOS load has been designed. The amplifier circuit with its continuous-time common-mode feedback is shown in Fig. 5.11. The second-stage amplifier by itself provides a DC gain greater than

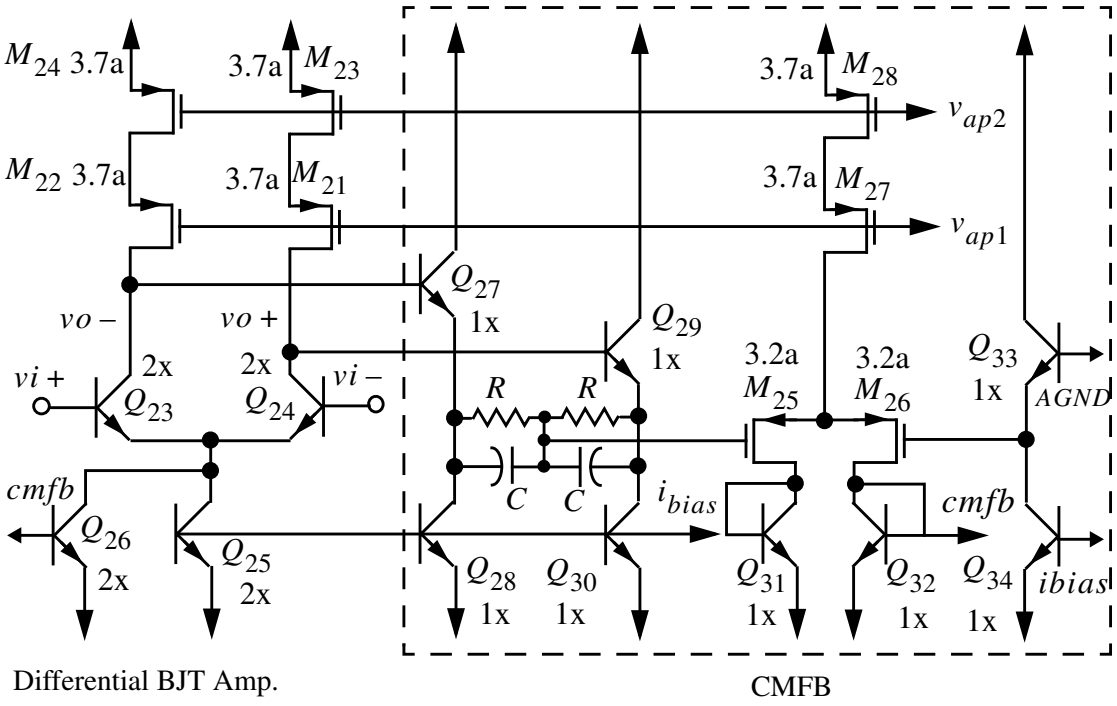


Figure 5.11 : Schematic diagram of the practical differential amplifier with continuous-time CMFB used for the TC-amp integrator.

57 dB and its unity-gain bandwidth with the output C_{load} = 2.5 pF was 820 MHz, with a 77° phase margin. This backs up the comment earlier about achieving a high speed performance using a TC-amp. The gain and phase frequency responses of the second stage amplifier with C_{load} = 2.5 pF are shown in Fig. 5.12. A more detailed analysis for the first stage transconductor and the second stage amplifier is given in Sec. 5.4.5 and

Sec. 5.4.6.

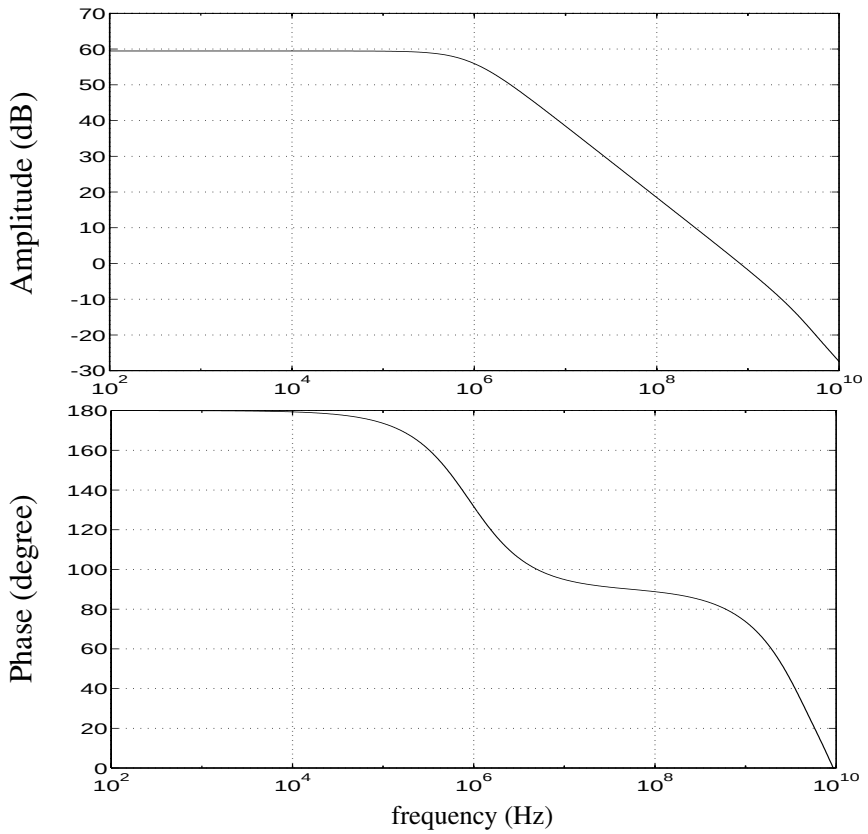


Figure 5.12 : Frequency response of the second-stage amplifier (with 2.5 pF capacitive load).

5.4.4 Excess Phase Cancellation

Before proceeding to a detailed small-signal analysis for explaining the effect of a Miller resistor on a TC-amp integrator performance a simple intuitive expression with a practical simulation is given in this section. A non-ideal integrator can be modelled by an s-domain polynomial transfer function $T(s) = \frac{num(s)}{den(s)}$. Consider two integrators in a closed loop system as shown in Fig. 5.13. One can find the closed loop frequency response

$$F(j\omega) = \frac{G_1(\omega)e^{j\varphi_1(\omega)}}{1 + G_1(\omega)G_2(\omega)e^{j[\varphi_1(\omega)+\varphi_2(\omega)]}} \qquad (5.8)$$

where $G_1(\omega)$, $G_2(\omega)$ are the integrators' gain and $\varphi_1(\omega)$, $\varphi_2(\omega)$ their phase frequency response (gain and phase are real functions). It is evident from (5.8) that for identical integrators with $-\pi/2$ phase we have $F(j\omega) = -j \cdot G(\omega)/(1-G^2(\omega))$. So if the $-\pi/2$ phase condition happens at the unity-gain frequency *i.e.* ω_o the perfect integration at each individual integrators and consequently the resonance requirement (and/or infinite-Q condition) for the closed-loop system is met at that frequency. For nonidentical loop integrators the infinite-Q condition occurs at a loop phase of $-180°$ and loop gain of unity[5] *i.e.* at some frequency ω' where

$$\begin{cases} \varphi(\omega') \equiv \varphi_1(\omega') + \varphi_2(\omega') = -180° \\ G(\omega') \equiv G_1(\omega')G_2(\omega') = 1 \end{cases} \qquad (5.9)$$

It is interesting to note that at the resonance frequency, $\omega' = \omega_o$, neither loop integrator

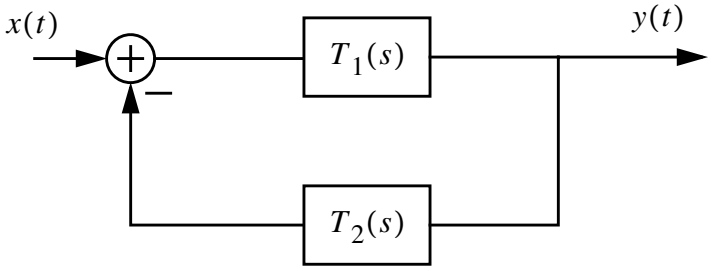


Figure 5.13 : A resonator implemented by two integrators in a closed loop system.

necessarily has unity gain. This is important when the resonator loop integrators are different. Recall from (5.6) that the resonator loop transconductor sizes are nominally

5. The Q of infinity for a resonator system produces an oscillation condition. This analysis is valid only for a linear system. In a non-linear system in order to sustain the oscillation the loop gain is required to be greater than one [Cla71]. However an amplitude-limiting mechanism is performed by the non-linearity of an active device to fix the oscillation level [Cla71].

identical g_m, however, the sizes of the feedback transconductors from DAC and the feedforward transconductors represented by g_{mb}'s and g_{ma}'s respectively in Fig. 5.4 are different. In the real circuit the resonator loop, DAC feedback and feedforward transconductors are implemented by a multi-input circuit which will be discussed in Sec. 5.5. This makes a small difference between the transconductors' gain and phase responses.

This is explained by an example. A second-order system including two different TC-amp integrators (Fig. 5.7) with practical circuits shown in Fig. 5.10 and Fig. 5.11 was simulated. By adjusting the Miller resistors *i.e.* R_z (for this simulation resistors were placed in series with the Miller capacitors instead of NMOS transistors in triode mode shown in Fig. 5.7) the maximum Q was achieved. Fig. 5.14 shows the Q of the second-

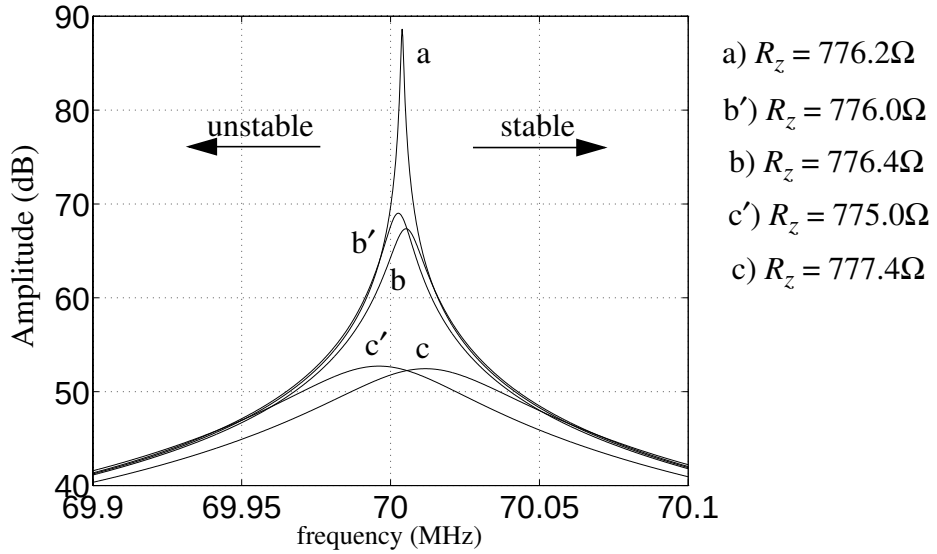


Figure 5.14 : Tuning of the Q of the filter by adjusting the loop integrators' phases. (a) shows –180° loop phase, (b) and (c) leading, and (b') and (c') lagging phase conditions. The expanded frequency axis exaggerates Q sensitivity.

order system for some different Miller resistor values. Note that the cases "b" and "c" are stable meaning that the loop poles in Fig. 5.13 are in LHP, case "a" shows poles on the $j\omega$ axis and cases "b′"and "c′" are unstable. The explanation is that assuming unity-

gain for the loop gain at the resonant frequency *i.e.* $G(\omega_o) = 1$, the sufficient stability condition is,

$$\varphi(\omega) > -180^\circ \ . \qquad (5.10)$$

Higher R_z values correspond to bigger phase lead which according to (5.10) makes the system more stable, or in the other word moves the loop poles further into the LHP. As R_z is decreased the desired poles on the $j\omega$ axis is attained and with lower R_z values the loop phase won't satisfy (5.10) any more which shows that the loop poles have moved into the RHP. Recall from Sec. 5.3 and Fig. 5.5 that the minimum required Q for the fourth-order bandpass modulator was 30 and at Q=50 the modulator operates almost like the ideal condition when its Q is infinity. The simulated R_z values of the resonator for Q of 30 and 50 were 826Ω and 806Ω respectively. This means to achieve a satisfactory noise-shaping a matching in order of 4-6% between the Miller resistors (or NMOS transistors used as controllable resistors) is required.

The frequency responses of the individual integrators including the loading effect of the second integrator in the loop are plotted in Fig. 5.15. As shown the unity-gain frequencies of the loop integrators are different: ≈85.41MHz for T_1 and ≈57.94MHz for T_2. The resonance condition given in (5.9) (at 70MHz) happens at a particular value of Miller resistors, i.e. $R_z = 766.2\Omega$. Changing the Miller resistors has no (or a very small) effect on the gain of integrators; however, it does influence the phase response of the integrators and consequently the Q of the resonator significantly. Therefore, one can obtain the required Q value by adjusting the Miller resistors.

The gain and phase plots of the T_1 integrator for two Miller resistor R_z values at the band of interest are shown in Fig. 5.16. At the resonance frequency 70MHz, by changing R_z form 776.2Ω to 700Ω the phase is changed by ≈–1.384° ($-89.167^\circ \rightarrow -90.551^\circ$) while the gain is changed only by ≈–0.053dB (1.603dB →1.550dB). With the same R_z values the phase and gain changes for the second integrator T_2 were ≈–1.386° and ≈–0.065dB respectively. This provides enough range for tuning the Q of a filter as manifested in Fig. 5.16c.

The integrators used for the preceding simulations were a realization of the BiCMOS TC-amp opamp configuration introduced in Sec. 5.4.2. The effect of the phase compensation on a second-order filter was generally explained and verified by HSPICE

simulations. Now a small signal analysis of the practical circuits used will be given which explains how the excess phase of integrators is adjusted in a TC-amp topology.

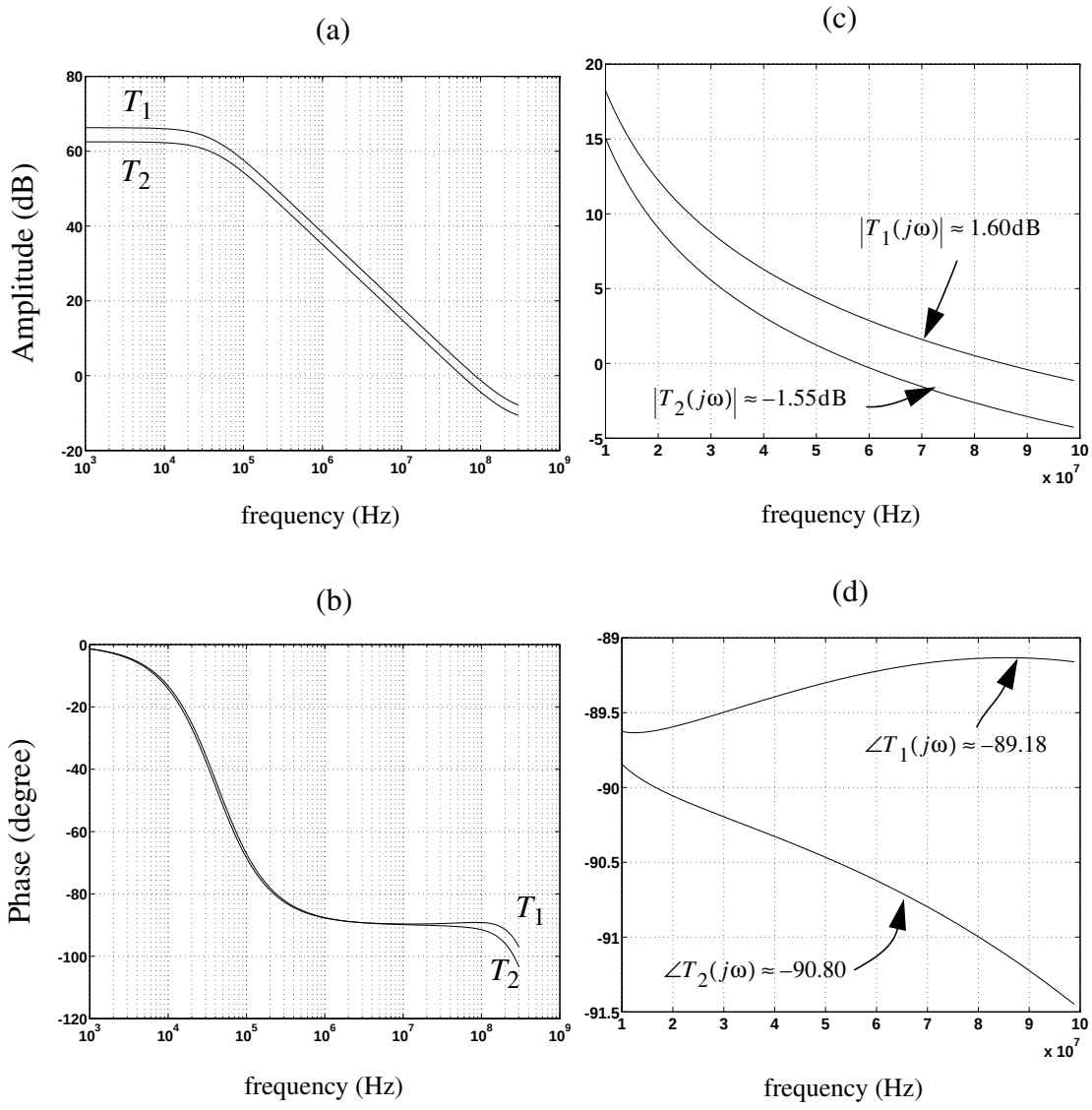
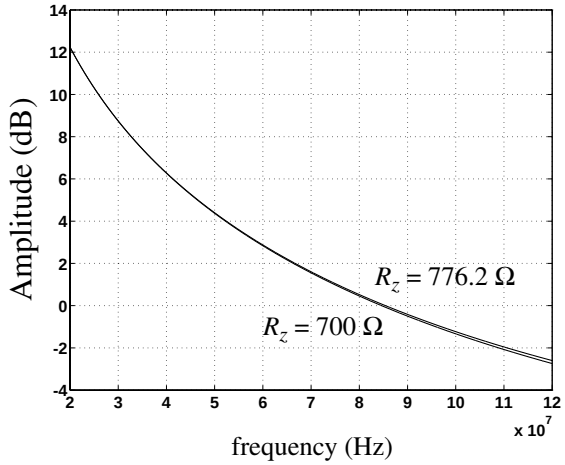
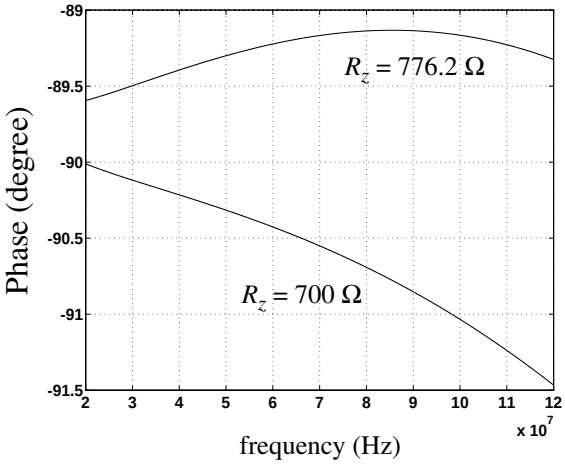


Figure 5.15 : (a) Amplitude and (b) phase frequency response of loop integrators, (c) and (d) same as (a) and (b) plotted in the band of interest.

(a)



(b)



(c)

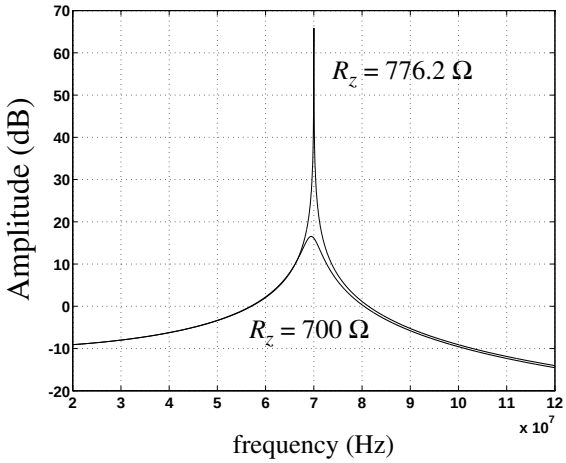


Figure 5.16 : The effect of an R_z change on (a) gain (b) phase of integrator T_1 and (c) on resonator Q.

5.4.5 Small Signal Analysis

The basic topology of the BiCMOS transconductor back in Fig. 5.10 followed by the second-stage bipolar amplifier (Fig. 5.11) is shown in Fig. 5.17 with the Miller capacitor and resistor. The current from the first stage BiCMOS transconductor is supplied to the

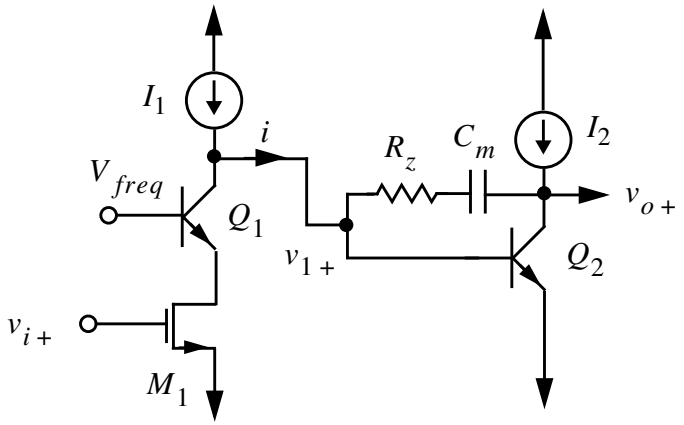


Figure 5.17 : A simplified half circuit schematic of TC-amp.

second stage amplifier which is configured as a Miller integrator. The second stage amplifier is a common emitter (CE) bipolar amplifier with a very high gain (60 dB and 57 dB in T_1 and T_2 *i.e.* the first and second integrators in the resonator loop as was represented in Fig. 5.13). One may consider a CE common-base (CB) cascode configuration at the second stage for increasing the output impedance of the integrator and reducing the effect of the collector-base (CB) capacitance of CE transistors on the total integrating time constant [Lab93]. In our design this was not needed, because firstly the output impedance is dominated by the PMOS current source devices, not the bipolar transistor. The cascode PMOS transistors in Fig. 5.11 provide high enough impedance for the required overall high gain (66 dB in T_1 and 63 dB in T_2). Secondly the bipolar collector-base capacitance is fairly low compared to the Miller capacitance, (10 fF / 1 pF) = 0.01 in this design. Besides, excess phase cancellation is required for the $\Delta\Sigma$

application which compensates the effect of the collector-base parasitic capacitance.

The very high gain of the second stage CE bipolar amplifier produces a fairly good virtual ground for the transconductor output current at the Miller input node v_1 (Fig. 5.17). This has the following advantage mentioned earlier: a very low signal excursion (about 1.4 mV for a 1 V output swing) at the input of the second stage even at resonance and as a result substantially reduced nonlinearity from the second stage amplifier at high frequencies. Simulations showed that having only a common-mode feedback at the second stage is enough and there is no requirement for an extra common-mode feedback for the first stage transconductors individually. Recall from Sec. 5.4.2 that the common-gain of the practical cross-coupled transconductor shown in Fig. 5.10 is −26 dB. However, because a device mismatching can happen in the fabrication and besides the interstage impedance for common-mode signal is high determined by the PMOS active loads in the first stage transconductors, it is required to implement an individual common-mode circuit for the first stage transconductor. This will be discussed in detail in Sec. 7.2.

In Sec. 5.4.4 the effect of the Miller resistor R_z in series with the Miller capacitor on the Q of a second-order system was demonstrated with the simulation results. In order to get more insight into the TC-amp integrator circuit behavior including the effect of R_z throughout small signal analysis has been presented in Appendix C.

The overall zeros and poles of the two-stage TC-amp integrator for the maximum-Q case (R_z = 776.2 Ω) are shown in Fig. 5.18a. The pole and the zero associated with the first stage amplifier are

$$p_{11} = -\,853.5 \text{ MHz and } z_{11} = +\,608.8 \text{ MHz.} \qquad (5.11)$$

and those of the second stage amplifier are

$$\begin{aligned} z_1 &= -280.6 \text{ MHz} \\ p_1 &= -45.88049 \text{ KHz} \\ p_{2,3} &= -0.95\times10^9 - j1.91\times10^9 \text{ Hz} \end{aligned} \qquad . \qquad (5.12)$$

Fig. 5.18b shows the frequency response comparison (gain and phase) of the real circuit

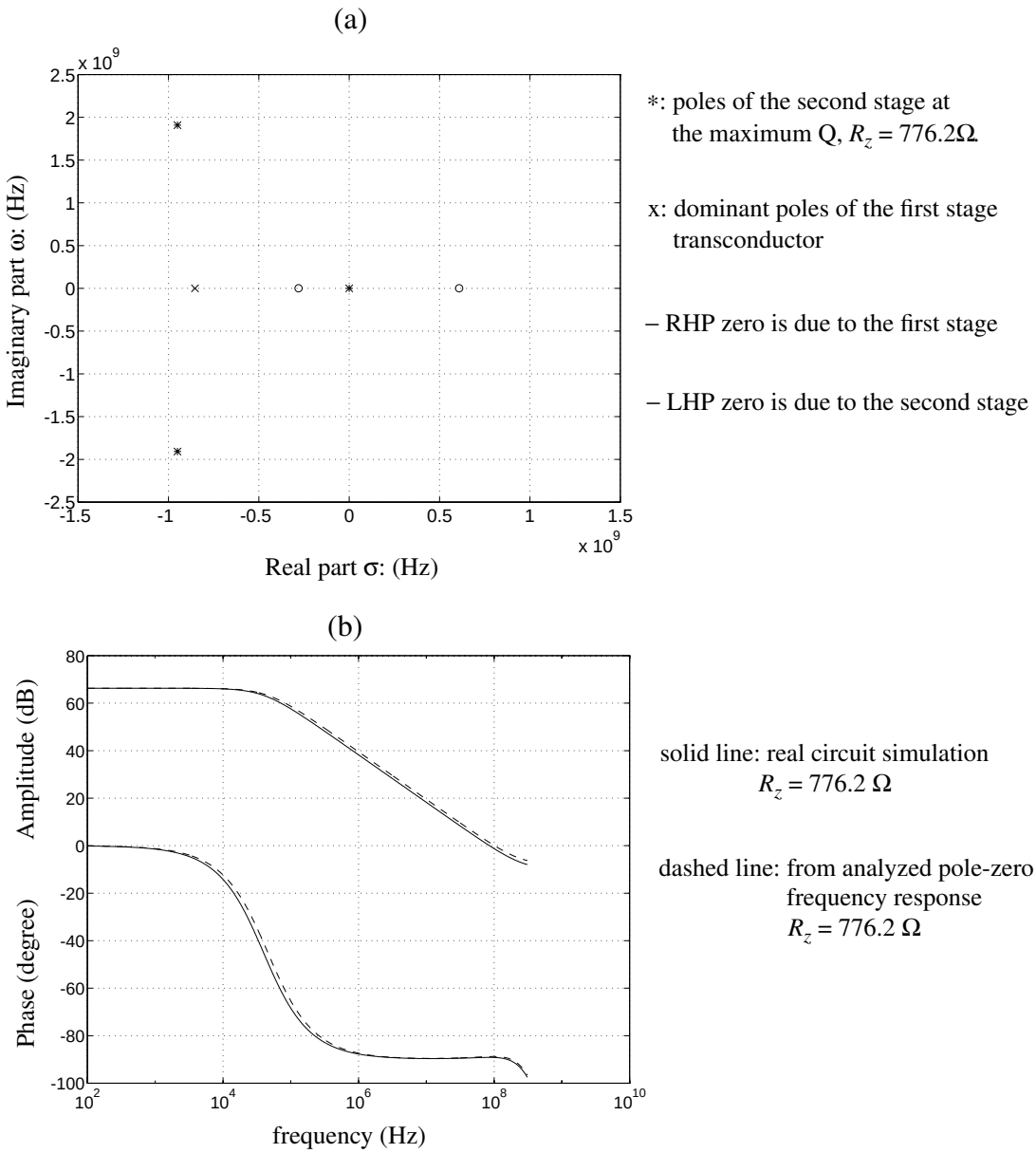


Figure 5.18 : (a) Poles and zeros of the whole TC-amp integrator, (b) frequency response of a system with the given poles and zeros along with that of the practical circuit simulation.

simulation (R_z = 776.2 Ω) with that obtained from the analyzed poles and zeros of the two stage TC-amp integrator shown in Fig. 5.18a. As Fig. 5.18b shows the proposed

pole-zero model from the foregoing analysis matches well with the simulation result for the frequency band of interest (lower than 100 MHz). For example the gain and phase differences at 50 MHz are 1.70 dB and 0.92°. This difference (particularly the phase) is not trivial for an integrator; however, the gross matching of the phase and gain between simulation and analysis implies that the given small signal analysis provides a fairly good insight into the frequency performance of the proposed two-stage TC-amp integrator. As was mentioned using R_z variation in the pole-zero model one should be able to mimic the simulation frequency response more closely. Fig. 5.19 shows the simulation frequency response of the TC-amp integrator circuit for R_z = 776.2 Ω (same as in Fig. 5.18b) and the frequency response of the pole-zero model for R_z = 752.4 Ω.

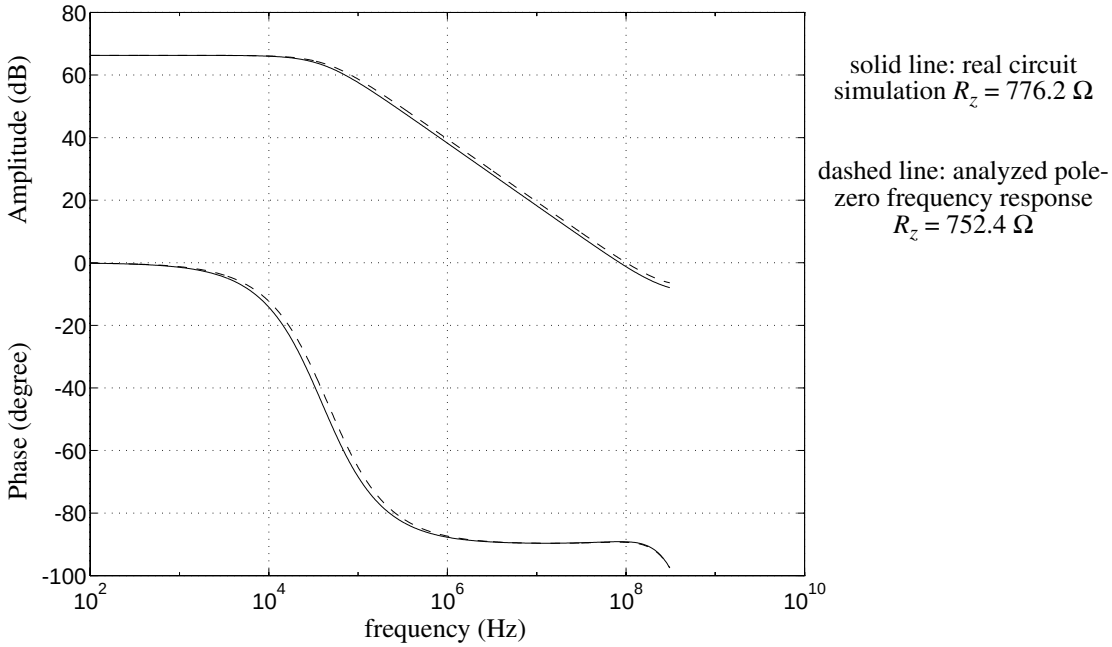


Figure 5.19 : The model matches to simulation at different R_z value (R_z = 752.4 Ω).

This R_z variation causes the poles and the RHP zero of the second stage amplifier to move from the location given in (5.12) to

$$\begin{aligned} z_1 &= -289.8 \text{ MHz} \\ p_1 &= -45.88074 \text{ KHz} \\ p_{2,3} &= -0.97\times10^9 \pm j1.93\times10^9 \text{ Hz} \end{aligned} \quad . \qquad (5.13)$$

At the new poles and zeros configuration given in (5.13) and (5.11) the gain and phase differences at 50 MHz (shown in Fig. 5.19) are 1.53 dB and $-1.96\times10^{-3^\circ}$ respectively. As is apparent from (5.12) and (5.13) the change of the LHP zero is much larger than the poles. More importantly, the simulation showed that the frequency response of the model is not very sensitive to the poles variation (keeping the LHP zero unchanged). For example with the same zero given in (5.12) and the poles

$$\begin{aligned} p_1 &= -45.78599 \text{ KHz} \\ p_{2,3} &= -2.32\times10^8 \pm j5.51\times10^8 \text{ Hz} \end{aligned}$$

which are associated with R_z = 9.85 kΩ the gain and phase differences at 50 MHz are 1.30 dB and $-3.54\times10^{-6^\circ}$ respectively. However, the LHP zero movement has significant effect on the excess phase cancellation as shown in Fig. 5.19.

The proposed pole-zero model didn't match perfectly the simulation results with the same circuit parameter values particularly with the identical R_z resistances. This is due to neglecting of some parasitic effects resulted from many simplifications made in the small signal analysis. However this model presents a root and zero locus for the entire TC-amp circuit (shown in Appendix C) in which one can study the effects of the poles and zeros variation individually in order to understand the ideas behind the excess phase cancellation for the filter's Q tuning.

5.4.6 Non-linearity Analysis

One important feature of a transconductor is its linearity performance. Particularly when used for a ΔΣ loop filter any major circuit non-linearity could result in the in-band intermodulation and/or signal-to-noise degradation. In this section a non-linearity analysis for the BiCMOS transconductor opamp circuit shown back in Fig. 5.10 and Fig. 5.11 is presented.

5.4.6.1 Input-stage BiCMOS Transconductor Non-linearity

Fig. 5.17 shows a simplified differential version of this transconductor. The input NMOS transistors M_1 and M_2 operate in the triode or linear region having gate–source voltage V_{GS} and drain–source voltage V_{DS}. One fairly accurate formula to define the transistors'

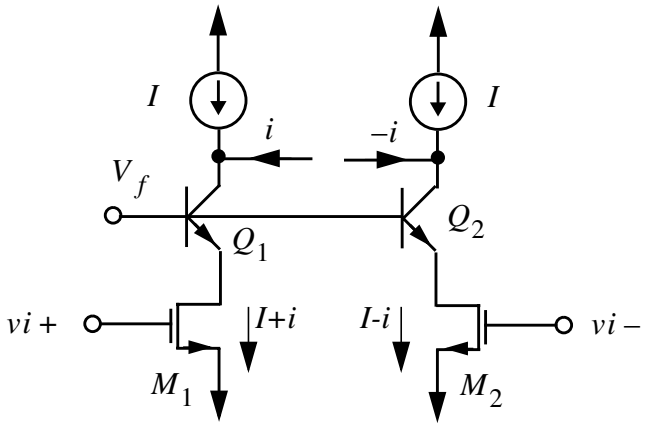


Figure 5.20 : A simplified differential circuit schematic of the BiCMOS transconductor shown in Fig. 5.10.

characteristics in the triode region is

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_t)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \qquad (5.14)$$

V_{GS} in this circuit is defined by input DC common-mode voltage superimposed on an input AC signal. V_{DS} is a base–emitter voltage drop V_{BE} below the frequency control voltage V_f applied to the BJT cascode transistors Q_1 and Q_2. At the same time the BJT emitter current which is identical to the input NMOS drain current is equal to

$$I_D = I_E = I_S \cdot e^{V_{BE}/V_T} \text{ or } V_{BE} = V_T \cdot \ln\frac{I_D}{I_S} \qquad (5.15)$$

where I_S is a constant (dependent on technology) describing the transfer characteristic of BJT transistor in the forward-active region. V_T is the thermal voltage in a bipolar transistor (26 mV at room temperature) which is defined by kT/q where q is the electron charge, k Boltzmann constant and T the absolute temperature. From (5.14) and (5.15) one can conclude that

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_t)\left(V_f - V_T\cdot\ln\frac{I_D}{I_S}\right)-\frac{1}{2}\left(V_f - V_T\cdot\ln\frac{I_D}{I_S}\right)^2\right] \quad (5.16)$$

Obviously as (5.16) and (5.15) indicate the modulation of V_{BE} and subsequently V_{DS} with I_D is a cause of non-linearity in the circuit. From (5.16) one can obtain the small signal transconductance of the input NMOS devices as follows:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2K\cdot I_D\left(V_f - V_T\cdot\ln\frac{I_D}{I_S}\right)}{I_D + 2K\cdot V_T(V_{GS}-V_t) - K\cdot V_T\left(V_f - V_T\cdot\ln\frac{I_D}{I_S}\right)} \quad (5.17)$$

where $K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$. Since the second and third term of the denominator in (5.17) is small compared to the first term I_D

$$g_m = \mu_n C_{ox}\frac{W}{L}\left(V_f - V_T\cdot\ln\frac{I_D}{I_S}\right) \quad (5.18)$$

which is like ignoring the squared term in (5.16).

For a differential input signal shown in Fig. 5.17 after expanding the 'ln' function in (5.16) into a Taylor series with $I_D = I + i$ where I and i are DC and AC currents respectively

$$I+i = \mu_n C_{ox}\frac{W}{L}\left\{(V_{GS+}-V_t)\left[V_f - V_T\left(\ln\left(\frac{I}{I_S}\right)+\frac{i}{I}-\frac{1}{2}\left(\frac{i}{I}\right)^2+\frac{1}{3}\left(\frac{i}{I}\right)^3+\ldots\right)\right]-\right. \quad (5.19)$$

$$\left.\frac{1}{2}\left[V_f - V_T\left(\ln\left(\frac{I}{I_S}\right)+\frac{i}{I}-\frac{1}{2}\left(\frac{i}{I}\right)^2+\frac{1}{3}\left(\frac{i}{I}\right)^3+\ldots\right)\right]^2\right\}$$

$$I-i = \mu_n C_{ox}\frac{W}{L}\left\{(V_{GS-}-V_t)\left[V_f - V_T\left(\ln\left(\frac{I}{I_S}\right)-\frac{i}{I}-\frac{1}{2}\left(\frac{i}{I}\right)^2-\frac{1}{3}\left(\frac{i}{I}\right)^3+\ldots\right)\right]-\right.$$

$$\left.\frac{1}{2}\left[V_f - V_T\left(\ln\left(\frac{I}{I_S}\right)-\frac{i}{I}-\frac{1}{2}\left(\frac{i}{I}\right)^2-\frac{1}{3}\left(\frac{i}{I}\right)^3+\ldots\right)\right]^2\right\}$$

Subtracting equations in (5.19) and neglecting the terms with the orders higher than four, one can derive

$$V_i \frac{V_{DS}}{V_T} = -V_i \left\{ \frac{1}{2}\left(\frac{i}{I}\right)^2 + \frac{1}{4}\left(\frac{i}{I}\right)^4 + \ldots \right\} + \left\{ \left[\frac{I}{K \cdot V_T} + 2(V_{on} - V_{DS})\right]\left(\frac{i}{I}\right) + \left(\frac{2}{3}(V_{on} - V_{DS}) - V_T\right)\left(\frac{i}{I}\right)^3 + \ldots \right\} \quad (5.20)$$

where $K = 0.5\mu_n C_{ox} W/L$, $V_i = V_{GS+} - V_{GS-}$ is the input differential voltage, $V_{DS} = V_f - V_T \cdot \ln(I/I_S)$ the quiescent drain-source voltage and $V_{on} = (V_{GS+} + V_{GS-})/2 - V_t$ the input common-mode (bias) voltage minus NMOS threshold voltage. Moreover, I_m is the peak amplitude of the drain current swing in the input NMOS devices and I is the drain quiescent current. At first glance it seems that since the first bracket in the right side of (5.20) comprises the even-order terms this analysis will predict even-order harmonics. However, with using the power series

$$\frac{1}{1+x} = 1 - x + x^2 - x^3 + \ldots \approx 1 - x$$

(5.20) can be simplified to

$$V_i \frac{V_{DS}}{V_T} = \left\{ 1 - \frac{V_T}{V_{DS}}\left[\frac{1}{2}\left(\frac{i}{I}\right)^2 + \frac{1}{4}\left(\frac{i}{I}\right)^4 + \ldots\right] \right\} \cdot \left\{ \left[\frac{I}{K \cdot V_T} + 2(V_{on} - V_{DS})\right]\left(\frac{i}{I}\right) + \left(\frac{2}{3}(V_{on} - V_{DS}) - V_T\right)\left(\frac{i}{I}\right)^3 + \ldots \right\} \quad (5.21)$$

It is apparent from (5.21) that only odd-order harmonic distortions can be predicted from this analysis. Finally ignoring the terms with power of four and higher in the first bracket in the right side of (5.21) we obtain

$$V_i \frac{V_{DS}}{V_T} = a'_1\left(\frac{i}{I}\right) + \left(a'_3 - \frac{V_T}{2V_{DS}}a'_1\right)\left(\frac{i}{I}\right)^3 + \left(a'_5 - \frac{V_T}{2V_{DS}}a'_3 - \frac{V_T}{4V_{DS}}a'_5\right)\left(\frac{i}{I}\right)^5 + \ldots = a_1\left(\frac{i}{I}\right) + a_3\left(\frac{i}{I}\right)^3 + a_5\left(\frac{i}{I}\right)^5 + \ldots \quad (5.22)$$

where a' are the coefficients of the second bracket in the right side of (5.21).

Equation (5.22) represents the input voltage V_i as a function of the output current while in reality the input voltage is considered as an independent variable. One can reverse the

dependency of variables in (5.20) by a power series [Car94]:

$$\frac{i}{I} = b_1\left(V_i\frac{V_{DS}}{V_T}\right) + b_2\left(V_i\frac{V_{DS}}{V_T}\right)^2 + b_3\left(V_i\frac{V_{DS}}{V_T}\right)^3 + b_4\left(V_i\frac{V_{DS}}{V_T}\right)^4 + \ldots \qquad (5.23)$$

where the "*b*" coefficients in (5.23) can be obtained from the "*a*" coefficients in (5.22)

$$b_1 = \frac{1}{a_1};\ b_2 = -\frac{a_2}{(a_1)^3} = 0;\ b_3 = \frac{2a_2 - a_1a_3}{(a_1)^5};\ b_4 = \frac{5a_1a_2a_3 - a_1^2a_4 - 5a_2^3}{(a_1)^7} = 0 \qquad (5.24)$$

From (5.23) it is apparent that the lower V_{DS}/V_T the more linear a transconductor can be achieved. In the BiCMOS transconductor shown in Fig. 5.17 and Fig. 5.10 $V_{DS} = 77$ mV. Ignoring higher terms from (5.23) an approximate linearized effective transconductor can be defined:

$$g_{meff} = \frac{g_{m1}}{1 + \dfrac{V_T}{V_{DS}}} \qquad (5.25)$$

where $g_{m1} = \mu_n C_{ox}\dfrac{W}{L}V_{DS}$. In Appendix C it is shown that g_{m1} = 271.6 µS and the effective transconductance is 211 µS at V_{DS} = 77 mV.

The second and third harmonic distortions can be obtained from (5.23) and (5.24):

$$\left|HD_2\right| = 0;$$

$$\left|HD_3\right| = \left|\frac{b_3}{4b_1}\right|\left(V_i\frac{V_{DS}}{V_T}\right)^2 = \frac{1}{4}\left|\frac{a_3}{(a_1)^3}\right|\left(V_i\frac{V_{DS}}{V_T}\right)^2 = \qquad (5.26)$$

$$\frac{1}{4}\cdot\left|\frac{\left[\frac{2}{3}(V_{on} - V_{DS}) - V_T\right] - \frac{V_T}{2V_{DS}}[I/(K\cdot V_T) + 2(V_{on} - V_{DS})]}{[I/(K\cdot V_T) + 2(V_{on} - V_{DS})]^3}\right|\left(V_i\frac{V_{DS}}{V_T}\right)^2$$

As (5.26) show the harmonic distortions are function of the input signal amplitude V_i.

5.4.6.2 Open-Loop Transconductor Simulations

For the input stage transconductor shown back in Fig. 5.10 disconnected from the second stage amplifier (loaded with two grounded 0.8pF capacitances) with the numerical parameters given in Sec. 5.4.5 computer simulations were performed. The

harmonic distortions were obtained by taking the FFT of the signals from the circuit time domain simulations. The harmonic distortion terms of the transconductor's differential output current for a 0.13 V sinusoidal input at 78.125 MHz[6] were

$$HD_2 = -55.8 \text{ dB}, HD_3 = -82.7 \text{ dB}, HD_4 = -117.1 \text{ dB and } HD_5 = -121.3 \text{ dB}. \quad (5.27)$$

While from (5.26) the second and third harmonic distortion terms are

$$HD_2 = 0 \text{ (in linear scale) and } HD_3 = -97.4 \text{ dB}. \quad (5.28)$$

The single stage transconductor's output voltage harmonic distortions from simulation were

$$HD_2 = -121.9 \text{ dB}, HD_3 = -92.0 \text{ dB}, HD_4 = -121.1 \text{ dB and } HD_5 = -122.0 \text{ dB}. \quad (5.29)$$

which shows the effect of filtering on the output current.

It should be noted that I_m and I for an AC input voltage of 0.13 V (V_i) and a DC input bias of 2.5 V (V_{cmi}) were 20 μA and 869.1 μA respectively.

The simulation (5.29) and analysis (5.28) results show that the third-order harmonic distortion predicted by (5.26) are a bit optimistic. Moreover, a large second-order harmonic distortion component was observed at the output current (5.27) which is zero from analysis. There are some reasons for this difference. One reason is that (5.14) presents a simple approximation for a MOS transistor characteristic at triode regime. A more advanced approximation may be presented [Kla94] by

$$I_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_t)V_{DS} - \frac{1}{2}(1+\delta)V_{DS}^2}{[1 + \theta_A(V_{GS} - V_t) + \theta_B V_S](1 + \theta_C V_{DS})} \quad (5.30)$$

where $\theta_C = (LE_c)^{-1}$, θ_A, θ_B and E_c have to be considered as parameters; δ relates to the effective L (length) and W (width) compared to the drawn $L$and W in the layout and V_S is the substrate voltage. Obviously the presence of V_{DS} in denominator in (5.30) would dramatically affect the derivations made from (5.16) to (5.26) and consequently the harmonic distortions.

---

6. In the transient analysis an input frequency (close to the unity gain frequency) is chosen such that after taking FFT it would appear exactly at one FFT bin. The unity gain frequency of the single stage input transconductor (just loaded with two grounded 0.8pF capacitance) is 61 MHz. Recall from Sec. 5.4.4 that the unity gain frequency of the entire TC-amp is 85.41 MHz.

5.4.6.3 The Second-stage Amplifier Non-linearity

Before proceeding to a non-linearity analysis for the second-stage amplifier the entire two-stage integrator simulation results are presented here. The simulated harmonic distortions for the differential output voltage of the entire TC-amp circuit with the same input frequency 78.125 MHz (as the single-stage transconductor) but 0.1 V peak amplitude which produces the same I_m swing in the first stage transconductor as in the single stage transconductor were

$$\mathrm{HD}_2 = -100.8 \text{ dB}, \mathrm{HD}_3 = -92.9 \text{ dB}, \mathrm{HD}_4 = -111.8 \text{ dB and } \mathrm{HD}_5 = -106.6 \text{ dB} \quad (5.31)$$

By comparing (5.29) with (5.31) one can notice that in the two-stage integrator the harmonic distortions have not deteriorated noticeably. Particularly the third-order harmonic distortions are almost identical.

The second stage differential amplifier is shown in Fig. 5.21 to which the currents i_p and

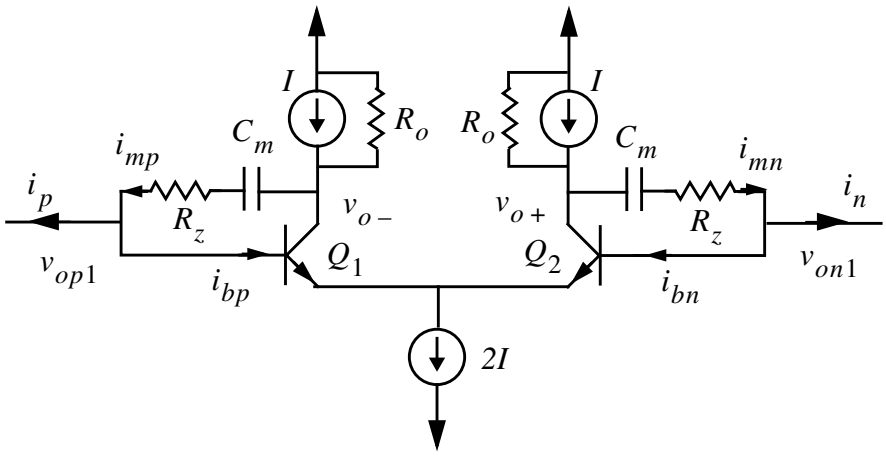


Figure 5.21 : A simplified model for the second stage amplifier.

i_n are supplied from the first stage transconductor. Equation (5.19) gave an estimate for the non-linearity incurred on the first stage transconductor output current. The non-linear currents 'i_p' and 'i_n' are then supplied to the second stage amplifier shown in Fig. 5.21. The differential output voltage of the second-stage amplifier can be written as

follows

$$V_o(t)=$$

$$= \frac{1}{C_m}\int_0^t [i_{mp}(t') - i_{mn}(t')]dt' + R_z[i_{mp}(t) - i_{mn}(t)] + (v_{op1}(t) - v_{on1}(t)) \quad (5.32)$$

$$\approx \frac{1}{C_m}\int_0^t [i_p(t') - i_n(t')]dt' + R_z[i_p(t) - i_n(t)] + v_{o1}(t)$$

For a sinusoidal input current where $i_m(t) = I_m \cos\omega t$ and $i_b(t) = I_b \cos(\omega t + \theta)$ simulations have shown that $I_b \ll I_m$. This is the rationale for the approximation made in (5.32) *i.e.* $i_{mp}(t) - i_{mn}(t) \approx i_p(t) - i_n(t)$. As mentioned this current has been distorted by the first stage transconductor, so it contains higher order harmonics as well as the fundamental frequency:

$$i(t) = i_p(t) - i_n(t) = \sum_1^\infty b_n \cos n\omega t \quad (5.33)$$

Substituting (5.33) into (5.32) the contribution of the second stage amplifier in the overall non-linearity can be understood

$$V_o(t) = \frac{1}{C_m}\int_0^t \sum_1^\infty b_n \cos n\omega t' dt' + R_z \sum_1^\infty b_n \cos n\omega t + v_{o1}(t)$$

$$= \sum_1^\infty \left(\frac{b_n}{nC_m\omega} \sin n\omega t + R_z b_n \cos n\omega t \right) + v_{o1}(t) \quad (5.34)$$

$$= \sum_1^\infty b_n \left[\frac{1}{(nC_m\omega)^2} + R^2{}_z \right]^{1/2} \cos\left(n\omega t - \operatorname{atan}\left(\frac{1}{nR_z C_m \omega} \right) \right) + v_{o1}(t)$$

As shown in the sigma term in (5.34) the higher order harmonics are multiplied by $[1/(nC_m\omega)^2 + R^2{}_z]^{1/2}$ term. Ignoring $v_{o1}(t)$ term, one can calculate the output voltage harmonic distortions:

$$HD_n = \frac{[1/(nC_m\omega)^2 + R^2{}_z]^{1/2}}{[1/(C_m\omega)^2 + R^2{}_z]^{1/2}} \cdot \frac{b_n}{b_1} = \frac{[1/(nC_m\omega)^2 + R^2{}_z]^{1/2}}{[1/(C_m\omega)^2 + R^2{}_z]^{1/2}} \cdot HD_{n-i} \quad (5.35)$$

where HD_{n-i} is the n-th order harmonic distortion of the input current to the second stage amplifier. So, the effect of the Miller capacitance in series with a resistor is reducing the input current harmonic distortion as shown in (5.35) *i.e.* filtering action.

It should be noted that in our real circuit the NMOS devices working in triode regime have been used as voltage-controlled resistors in series with Miller capacitors. These devices are not quite linear [Tsiv94] as passive resistors used in the preceding analysis. There are some recommended schemes to alleviate their non-linearity in the context of MOSFET-C filters [Tsiv86], [Cza86] which are not discussed here because as will be shown shortly they are not a major source of non-linearity in this circuit.

The second term in (5.34) $v_{o1}(t)$ although very small could contribute significantly in nonlinearity of the second stage amplifier output voltage. The input differential voltage can be defined by BJT equation

$$v_{o1} = V_T \cdot \ln\frac{i_{cp}}{i_{cn}} \qquad (5.36)$$

where i_{cp} and i_{cn} are the collector currents in the BJT transistors Q_1 and Q_2. Assuming very high impedance active load for the second stage amplifier *i.e.* very high R_o shown in Fig. 5.21 one can simply assume $i_{cp} = i_p$ and $i_{cn} = i_n$. Then (5.19) can be substituted to (5.36) to analyze the effect of the second stage amplifier on the overall TC-amp non-linearity.

However, since the input signal of the second stage amplifier is usually operating at very low voltage levels, for example 2.3 mV and 9.5 mV for the input voltage levels of 0.1 V and 0.3 V respectively, the second stage amplifier can be analyzed individually. A simplified half circuit schematic of the second stage differential BJT amplifier shown in

Fig. 5.21 is shown in Fig. 5.22. Considering a single tone[7] input for the BJT amplifier

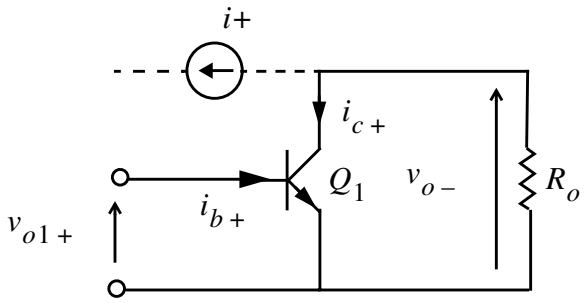


Figure 5.22 : A simplified half circuit schematic of second stage amplifier.

and removing the + and – signs for the symbols shown in Fig. 5.22:

$$i_c(t) = I_o \cdot e^{\frac{V_{BEQ} + V_1 \cos(\omega t)}{V_T}} = I_o \cdot e^{\frac{V_{BEQ}}{V_T}} \cdot e^{x\cos(\omega t)} \qquad (5.37)$$

where $x = V_1/V_T$ is the normalized peak amplitude voltage of the half circuit input signal. It is well known from Fourier series expansion [Cla71] and Bessel function theory [Trat68], [Gra52] that

$$e^{x\cos(\omega t)} = I_0(x) + 2\sum_{1}^{\infty} I_n(x)\cos n\omega t \qquad (5.38)$$

where $I_n(x)$ is a modified Bessel function of the first kind, of order n and argument x. The modified Bessel functions are all monotonic and positive for $x \geq 0$ and $n \geq 0$; $I_0(0)$ is unity, whereas all higher order functions start at zero. As $x \to 0$,

$$I_n(x) \to \frac{(x/2)^n}{n!} \qquad (5.39)$$

when n is a positive integer.

So owing to the closed form exponential equation for a bipolar transistor characteristic, substituting (5.38) into (5.37) we obtain

7. The intermodulation effects of the higher order components supplied to the second-stage amplifier are neglected here. However, the intermodulation for the entire TC-amp integrator is shown in Sec. 5.4.6.5.

$$\begin{aligned} i_c(t) &= I_o \cdot e^{\frac{V_{BEQ}}{V_T}} \left[I_0(x) + 2\sum_{1}^{\infty} I_n(x) \cos n\omega t \right] \\ &= I_o \cdot e^{\frac{V_{BEQ}}{V_T}} I_0(x) \left[1 + 2\sum_{1}^{\infty} \frac{I_n(x)}{I_0(x)} \cos n\omega t \right] \end{aligned} \tag{5.40}$$

It is apparent from (5.40) that the average (or DC) value of $i_c(t)$ is affected by the input voltage x

$$\overline{i_c(t)} = I_o \cdot e^{\frac{V_{BEQ}}{V_T}} I_0(x) \tag{5.41}$$

In the differential circuit Fig. 5.21 the input signals have −180° phase difference. So from (5.38) one can obtain

$$e^{x\cos(\omega t + \pi)} = I_0(x) + 2\sum_{1}^{\infty} I_n(x) \cos(n\omega t + \pi) = I_0(x) + 2\sum_{1}^{\infty} (-1)^n I_n(x) \cos n\omega t \tag{5.42}$$

Consequently, the differential voltage is deduced from (5.40) and (5.42)

$$\begin{aligned} V_o(t) &= 2R_o \cdot I_o \sum_{1}^{\infty} [1 - (-1)^n] I_n(x) \cos n\omega t \\ &= 4R_o \cdot I_o \sum_{n=0}^{\infty} I_{2n+1}(x) \cos(2n+1)\omega t \end{aligned} \tag{5.43}$$

where R_o is the amplifier's output impedance. As is apparent from (5.43) the even order harmonics are zero in the assumed pure differential circuit. The harmonic distortion contribution of the second stage amplifier can simply be discovered from (5.43)

$$HD^b_{2n+1}(x) = \frac{I_{2n+1}(x)}{I_1(x)} \tag{5.44}$$

where '*b*' superscript stands for the distortion in BJT transistors.

For example at 0.1 V and 0.3 V input voltage levels which respectively produce 2.3 mV and 9.5 mV peak (in each half circuit) at the input of the second stage amplifier from

(5.44) we get

$$\begin{aligned} HD_3{}^{b}\Big|_{x=\frac{2.3\times10^{-3}}{VT}} &= -69.74dB \rightarrow 3.259\times10^{-4} \\ HD_3{}^{b}\Big|_{x=\frac{9.5\times10^{-3}}{VT}} &= -45.17dB \rightarrow 5.517\times10^{-3} \end{aligned} \qquad (5.45)$$

Fig. 5.23 shows the third and fifth harmonic distortions of a differential BJT amplifier

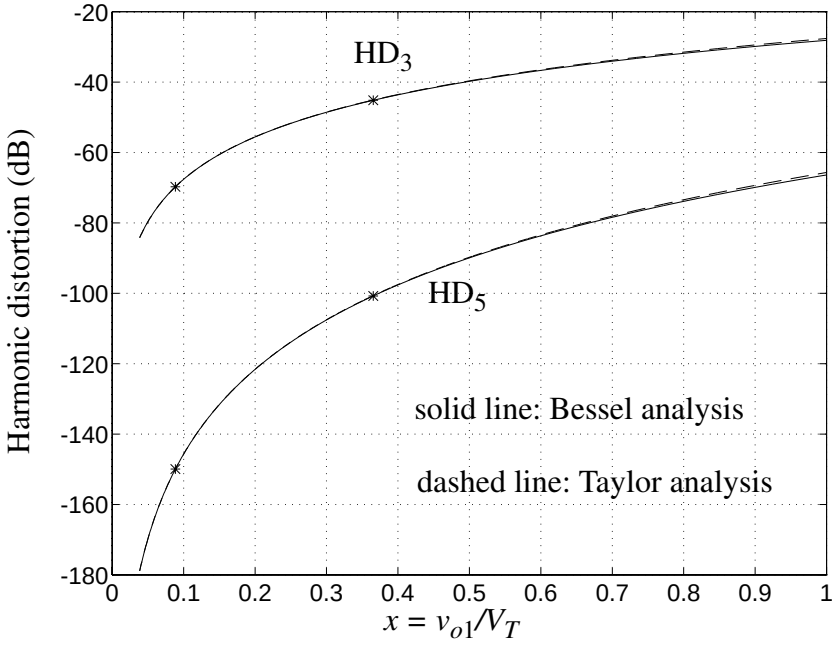


Figure 5.23 : The third and fifth harmonic distortion of a differential BJT amplifier vs. the normalized input amplitude.

obtained from (5.45) superimposed on the analysis results obtained from Taylor series which are not given here to save space. As shown in Fig. 5.23 the results obtained by Bessel functions are so close to those from Taylor series expansion as to be almost indistinguishable. The '*' points in Fig. 5.23 indicate the second stage amplifier harmonic distortions at BJT input levels of 2.3 mV and 9.5 mV. For example the third and fifth order harmonic distortions with an input signal amplitude 2.3 mV are $HD_3 = -69.7$ dB and $HD_5 = -149.9$ dB. This implies that for low amplitude levels like 2.3 mV the second-stage amplifier almost doesn't contribute in the non-linearity of the circuit.

However, as shown in Fig. 5.23 at high amplitude levels the non-linearity contribution of the second stage BJT amplifier could be significant.

5.4.6.4 Closed-loop Transconductor Simulations

In an open-loop simulation of a transconductor especially in a two-stage circuit since there is no output-input feedback for the entire TC-amp system, there is usually a transient response in the beginning of a simulation (and/or in a practical situation). This produces unbalanced signals at differential nodes which consequently could result in some error in simulation results. For example due to unsymmetric signals at a differential stage even-order harmonic distortions could appear. Therefore for simulation a TC-amp integrator was placed in a closed loop to make a simple single-pole lowpass filter. Fig. 5.24 shows a schematic diagram of this closed-loop TC-amp integrator

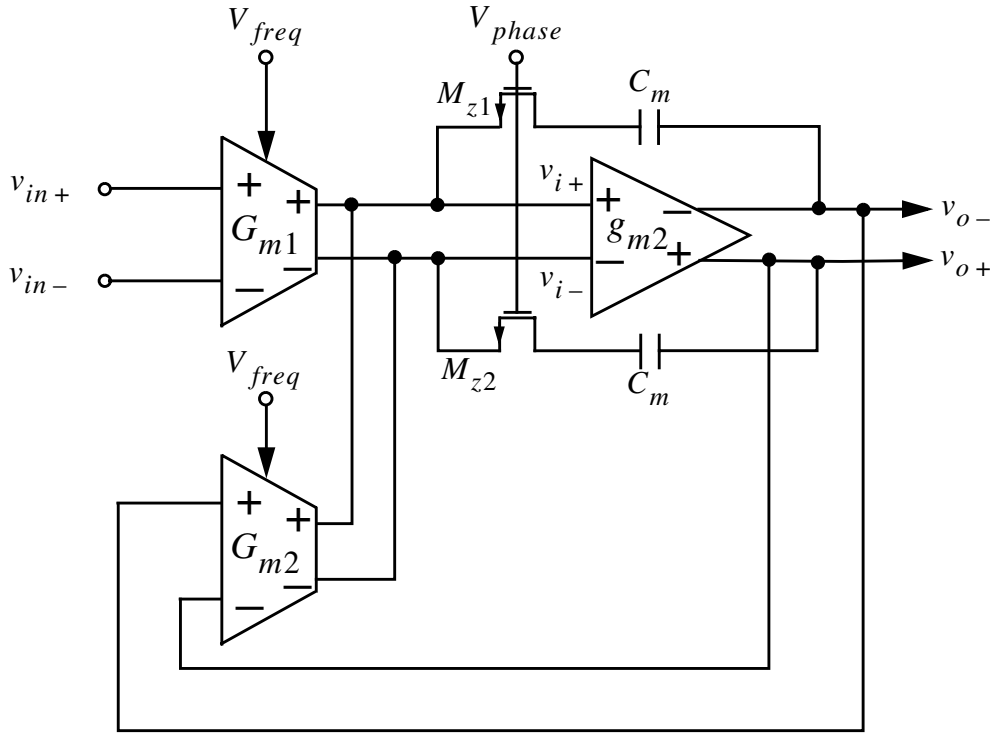


Figure 5.24 : The TC-amp integrator configured as a simple single-pole lowpass filter.

configured as a lowpass filter.

The harmonic distortions of the lowpass filter shown in Fig. 5.24 with the NMOS phase

controlling transistors M_{z1} and M_{z2} in triode regime for a sinusoidal input at 50 MHz and 0.1 V amplitude were

$$\mathrm{HD}_2 = -100.7 \text{ dB}, \mathrm{HD}_3 = -84.6 \text{ dB}, \mathrm{HD}_4 = -105.9 \text{ dB and } \mathrm{HD}_5 = -99.8 \text{ dB}. \quad (5.46)$$

The same simulation but with NMOS transistors M_{z1} and M_{z2} replaced by passive resistors giving the same phase-frequency response as with NMOS devices resulted in

$$\mathrm{HD}_2 = -101.5 \text{ dB}, \mathrm{HD}_3 = -89.8 \text{ dB}, \mathrm{HD}_4 = -106.4 \text{ dB and } \mathrm{HD}_5 = -102.2 \text{ dB}. \quad (5.47)$$

Hence the comment earlier that the NMOS triode-mode devices in series with the Miller capacitors don't contribute too much in the non-linearity of the TC-amp integrator.

A closed-loop simulation comprising a single stage BiCMOS transconductor shown back in Fig. 5.10 has been performed. With sinusoidal input at 37 MHz and 0.1 V amplitude the results were as following

$$\mathrm{HD}_2 = -102.9 \text{ dB}, \mathrm{HD}_3 = -95.1 \text{ dB}, \mathrm{HD}_4 = -107.0 \text{ dB and } \mathrm{HD}_5 = -102.4 \text{ dB}. \quad (5.48)$$

Again as the closed-loop simulation show the two-stage TC-amp integrator (5.47) and the single-stage transconductor (5.48) produce very close harmonic distortion components.

5.4.6.5 Two-tone Intermodulation Simulation

Two input sinusoidal signals both with 0.1 V amplitude levels and frequencies at 51.27 MHz and 56.15 MHz were supplied to the closed-loop integrator configured as a simple lowpass filter shown in Fig. 5.24. The in-band signal spectrum is shown in Fig. 5.25. The third-order intermodulation distortions as shown in Fig. 5.25 appear at 46.39 MHz and 61.03 MHz with respectively −85.5 dB and −83.8 dB attenuations.

5.5 A Practical Fourth-order ΔΣ Modulator

A single-ended schematic diagram of a 4th-order ΔΣ TC modulator was shown back in Fig. 5.4. A practical fully differential modulator using the TC-amp integrators described in Sec. 5.4 is implemented which is shown in Fig. 5.26.

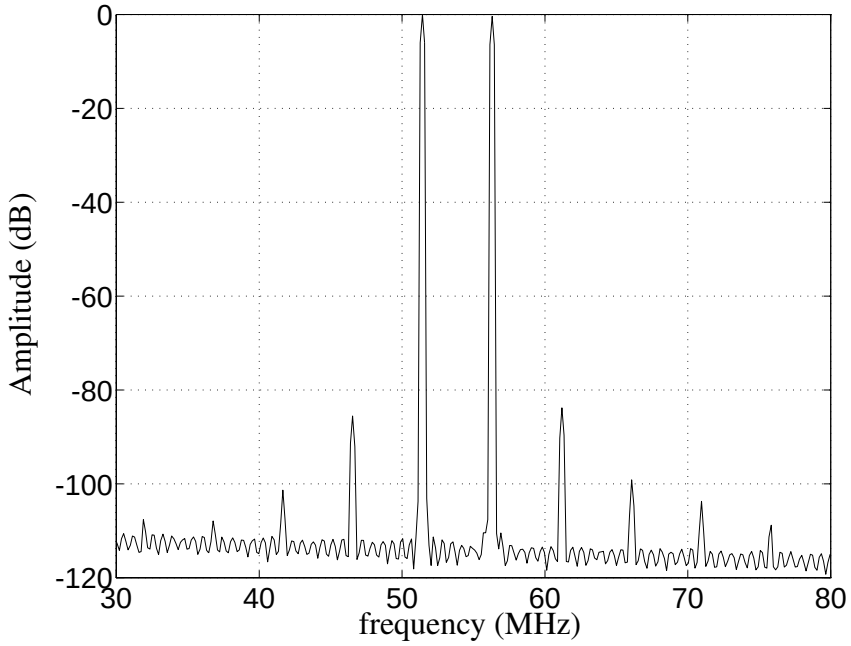


Figure 5.25 : The simulated spectrum of the output signal of Fig. 5.24 when supplied by two tones with 0.1 V amplitude levels and frequencies at 51.27 MHz and 56.15 MHz.

5.5.1 Loop Filter Center Frequency Control

The transconductor values, therefore the size of the input NMOS transistors of the fourth-order ΔΣ modulator loop filter are ratioed as the requirement given in (5.6). In Sec. 5.4.4 and Sec. 5.4.5 it was explained how the Q of each second-order resonator shown in Fig. 5.26 can be controlled through changing the Miller resistor R_z. In the practical circuit this was done by the control voltage labeled V_{phase} in Fig. 5.7 which changes the resistance of the NMOS devices working in the triode mode (not shown in Fig. 5.26). As explained in Sec. 5.4.2 and shown back in Fig. 5.10 the control voltage V_{freq} supplied to the base of the BJT transistors in the input cross-coupled transconductor determines the bias V_{DS} voltages and the transconductor values. From (5.18) it is evident that V_{freq} (V_f) determines the transconductance g_m value for the input devices and so that for the entire TC-amp integrator as given in (5.25). Fig. 5.27 shows the change of the fourth-order loop filter's center frequency with respect to V_{freq} variation. Note that V_{phase} is identical in all simulations. As shown in Fig. 5.27 for this

V_{phase} the maximum Q occurs at 50 MHz.

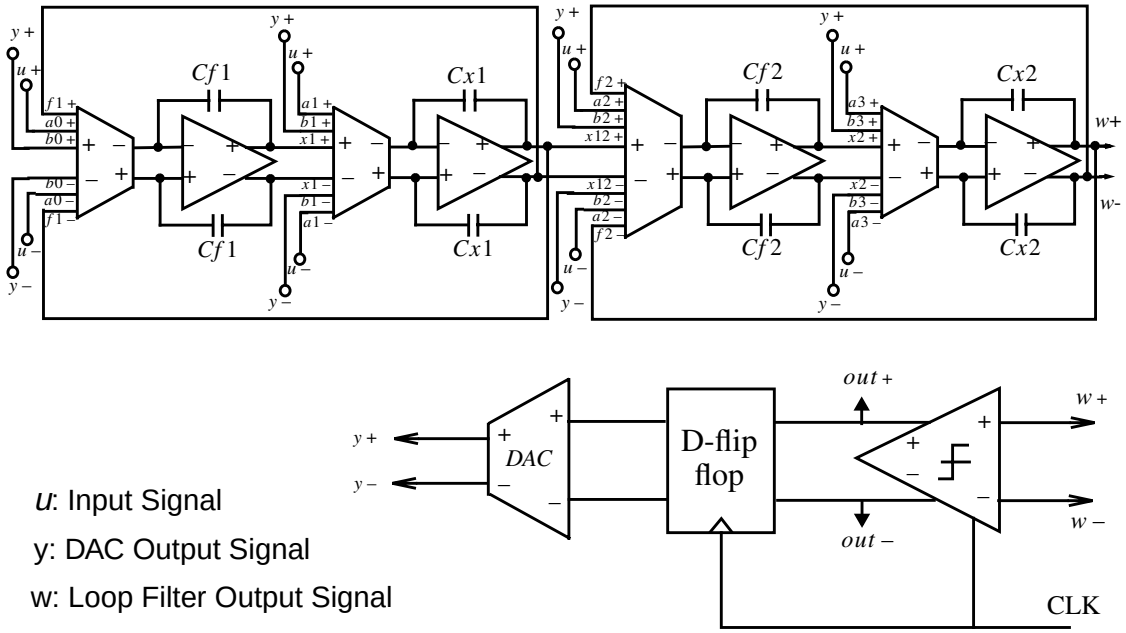


Figure 5.26 : A 4th-order TC-amp ΔΣ modulator.

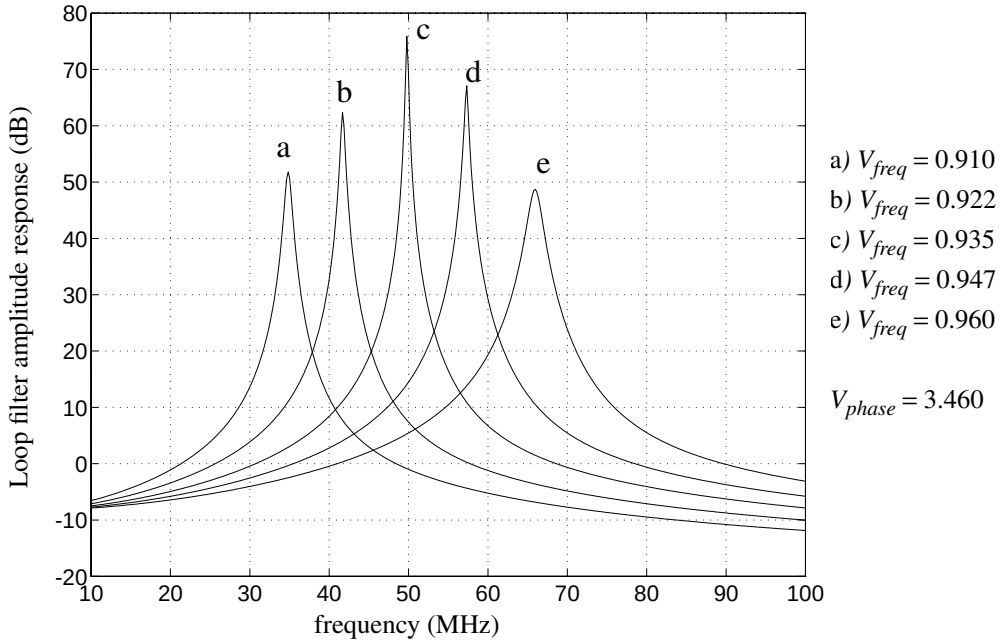


Figure 5.27 : The fourth-order ΔΣ modulator center frequency control by changing V_{freq}, in every simulation V_{phase} = 3.460.

5.5.2 ΔΣ Modulator Loop Components

A description of the modulator loop components shown in Fig. 5.26 is as follows:

5.5.2.1 Multi-input Transconductors

The multi-input transconductors shown in Fig. 5.26 have been implemented by adding extra input NMOS devices in parallel. A simplified three-input transconductor is shown in Fig. 5.28. This way one can add the input signal "*u*" with the ΔΣ DAC output signal

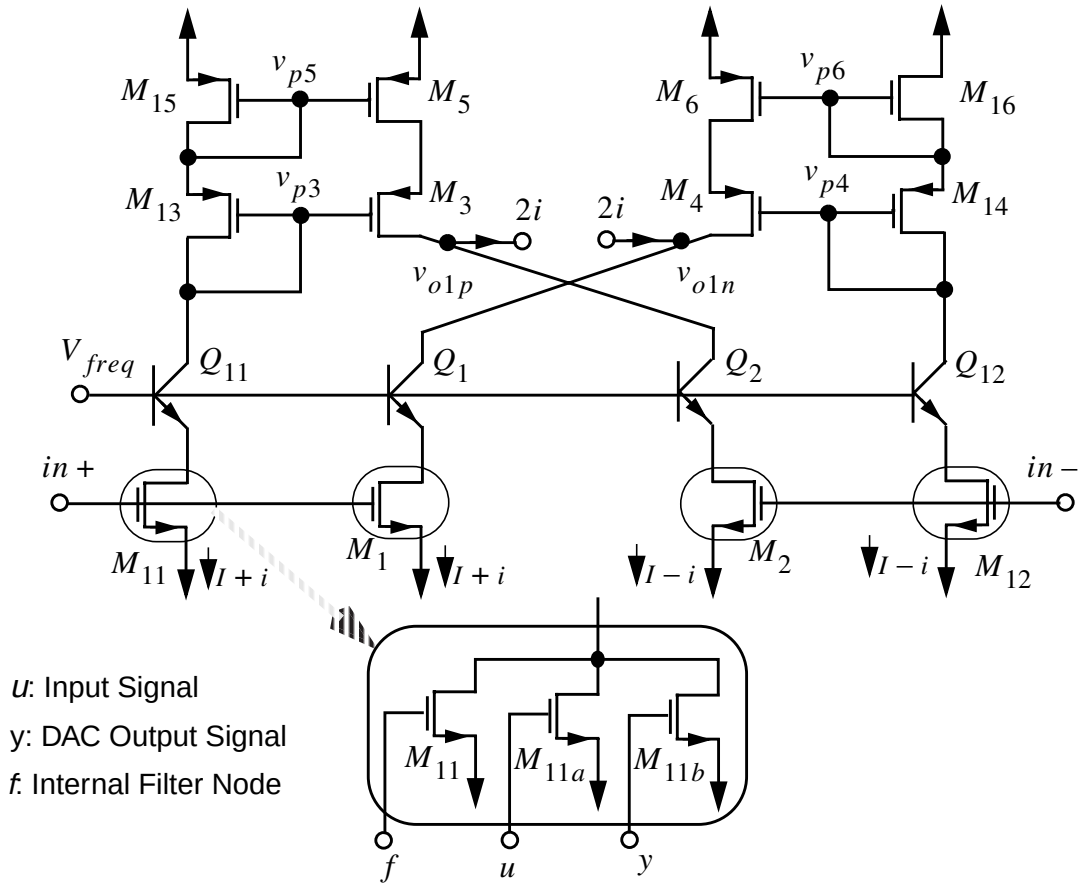


Figure 5.28 : A three-input transconductor.

and an internal loop filter node signal represented by "*y*" and "*f*" respectively in Fig. 5.28 and Fig. 5.26. Having selected the input NMOS device dimensions an arbitrary feedforward and loop ΔΣ loop filter can be designed.

5.5.2.2 Two-level DAC

A two-level high speed current steering DAC shown in Fig. 5.29 is designed to reduce an extra loop delay produced by the DAC's propagation delay time. From simulation the DAC's propagation delay time loaded with 0.75 pF at each its differential output nodes (the total capacitance load of the loop filter) was about 100 ps. With off-chip V_{dac} voltage and I_{dac} current shown in Fig. 5.29 the DAC output common-mode voltage and swing amplitude can be controlled independently.

5.5.2.3 Latched Comparator and D-flip flop

For ΔΣ quantizer a latched clocked comparator [Long92], [Bre95] has been used. The comparator comprises a preamplifier followed by a latch as shown in Fig. 5.30. For D-flip flop shown in Fig. 5.26, two latches like the one shown in Fig. 5.30 have been cascaded. The overall simulated propagation delay time of the comparator and the D-flip flop followed by the DAC loaded with a 0.75 pF at each DAC's differential output node was about 0.8 ns.

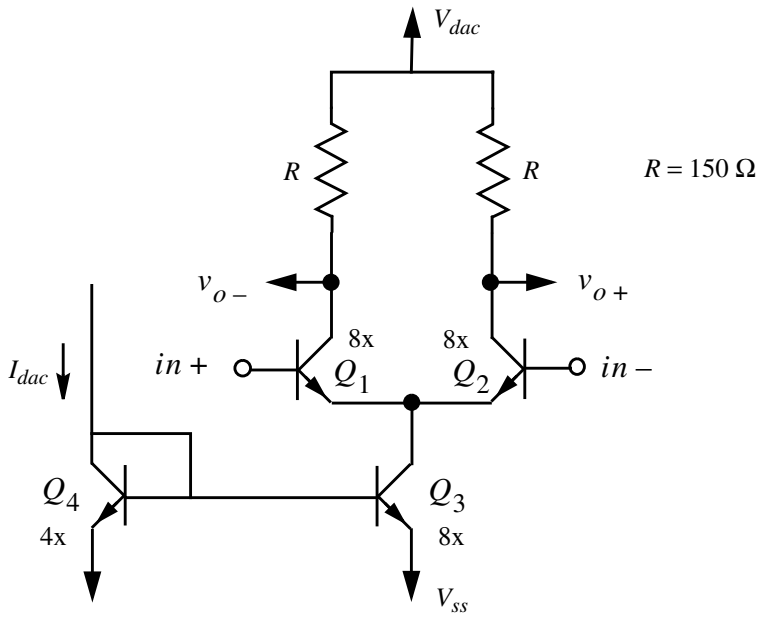


Figure 5.29 : A schematic of two-level current steering DAC.

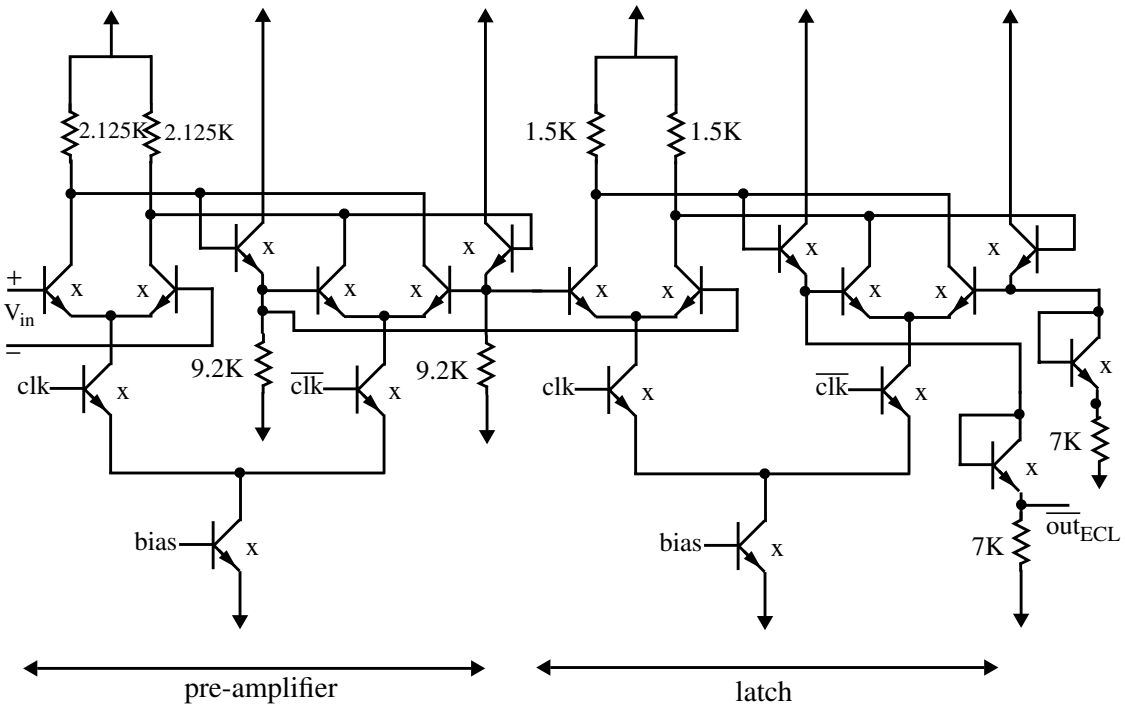


Figure 5.30 : A pseudo-ECL latched comparator.

5.5.3 The TC-amp ΔΣ Modulator Simulated *SNR*

The one-delay multiple-pole fourth-order modulator with the loop filter given in (3.23) has been simulated. The input signal was a sinusoidal signal at 50 MHz with −6 dB amplitude (relative to the quantization Δ level). First the modulator with all ideal components including the ideal fourth-order loop filter given in (3.23) was simulated. In the second simulation, the ideal loop filter was substituted by a fourth-order TC-amp filter with the architecture shown in Fig. 5.26. The open loop TC-amp filter's Q was set at infinity and its center frequency at 50 MHz. However, in the second simulation the other modulator's components such as the comparator, the loop delay (D-flip flop) and DAC were ideal while 100 ps extra loop delay was deliberately introduced. In the third (last) simulation everything used real circuits with the schematic diagram shown from Fig. 5.26 to Fig. 5.30. As was mentioned in Sec. 5.5.2 the extra loop delay produced by the comparator, D-flip flop and DAC loaded with the loop filter was around 0.8 ns. A bandpass noise-shaping spectrum obtained from a simulation of the real circuits is

shown in Fig. 5.31.

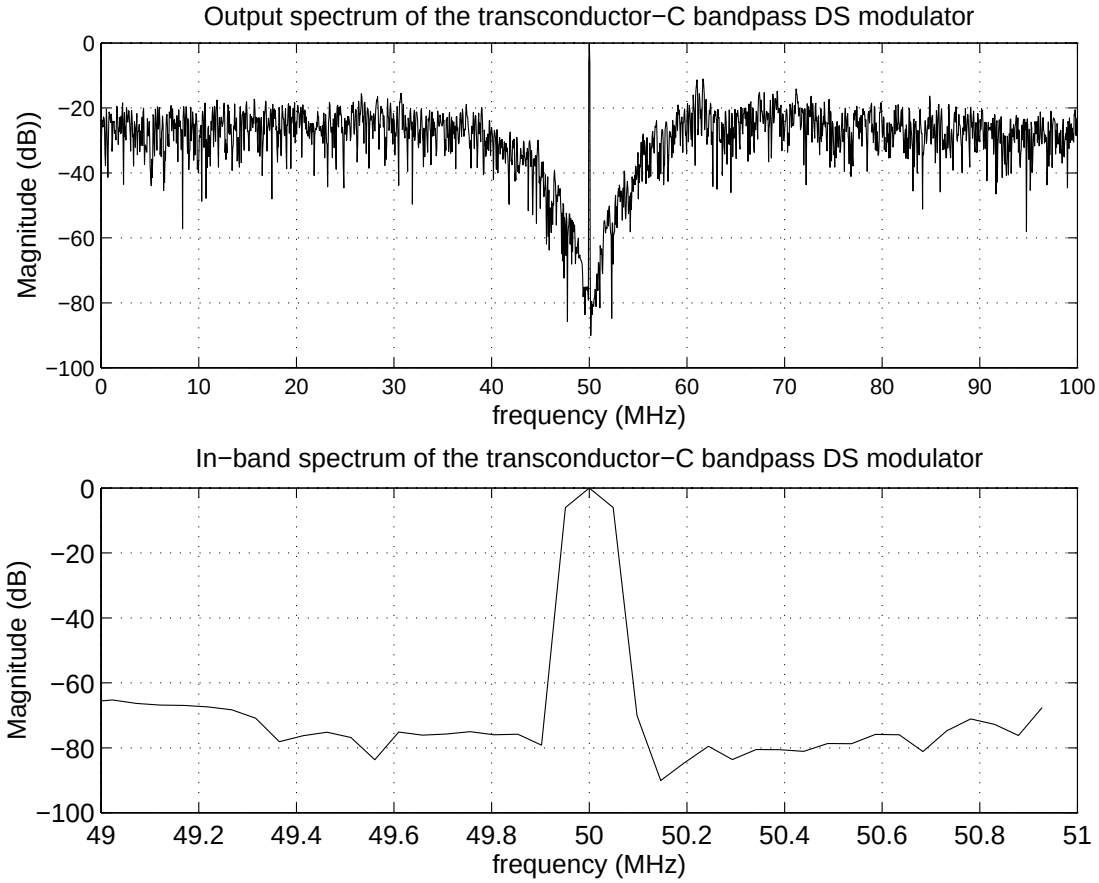


Figure 5.31 : A bandpass noise-shaping spectrum of the fourth-order modulator obtained from simulation of real circuits.

Table 5.1: The *SNR* simulation results for fourth-order modulators

Simulations	input peak amplitude* (mV)	*SNR* (dB) at given bandwidth		
		2 MHz	4 MHz	6 MHz
ideal loop components	490	63.4	47.8	41.0
real circuit loop filter; ideal digital loop components; 100 ps extra loop delay	75	59.4	44.8	38.6
real circuit modulator (0.8 ns extra loop delay)	50	56.3	41.4	35.1

*. Always −6 dB relative to the DAC output signal.

The maximum simulation *SNR* results for the three preceding cases and some different bandwidths are given in Table 5.1. From the simulation results given in the second and first rows of Table 5.1 it can be inferred that the effect of non-idealities in the real circuit filter is almost 3 dB *SNR* loss at every oversampling ratio (bandwidth). Another 3 dB *SNR* loss is produced by the extra loop delay which is apparent from comparison of the third and second rows in Table 5.1.

5.6 Summary

A transconductor-*C* filter architecture to implement the continuous-time bandpass or lowpass modulator loop filters has been introduced. A practical transconductor-amp (TC) integrator has been designed and developed for use as a very high-Q (infinite-Q) $\Delta\Sigma$ loop filter. The simulated third order intermodulation products of the practical $\Delta\Sigma$ loop filter with 0.1 V two-tone in-band (50 MHz) signals were lower than −80 dB. The simulated maximum signal amplitude (MSA) of the practical $\Delta\Sigma$ modulator at 50 MHz was $50\,\mathrm{mV_p}$ (with a 0.1 V DAC signal swing) which resulted in 56.3 dB ($9\frac{1}{2}$ bits) maximum *SNR* at 2 MHz bandwidth and 35.1 dB (6 bits) at 6MHz bandwidth.

A two level current steering DAC circuit was designed. Its propagation delay time including the effect of the loop filter capacitive load (almost 0.4 pF single-ended) was about 100 ps. The overall $\Delta\Sigma$ extra loop delay including the propagation delay times of the comparator, D-flip flop and the DAC at 200 MHz clock rate was about 0.8 ns. It was shown that the effect of this extra loop delay was to reduce the MSA and so the maximum *SNR* by about 3 – 4 dB at a 50 MHz input signal.

Chapter 6

Testing of a Prototype Second-Order Bandpass Delta-Sigma Modulator

A transconductor-C biquad filter chip [Shov92] tuned at f_o = 50 MHz with a built-in latched comparator has been used to make an experimental ΔΣ loop nominally clocked at f_s = 200 MHz. A second filter chip was utilized as the voltage-controlled oscillator (VCO) in a PLL to implement a master-slave tuning scheme. The biquad filters were implemented in a 0.8 µm BiCMOS process.

6.1 Modulator Implementation

A block diagram of the modulator including the tuning circuitry is shown in Fig. 6.1a. The tuning scheme is discussed later in Sec. 6.2. The dashed lines in Fig. 6.1a enclose the chips used, while the additional blocks in the figure are off-chip components. The biquad filter chip was fully differential and consisted of five transconductor blocks. For simplicity the single-ended block level schematic of the filter is shown in Fig. 6.1b where the g_m terms represent the biquad transconductors. Further details on the biquad can be found in [Shov92]. The comparator output is fed to a variable attenuator (represented by k in Fig. 6.1a) whose output is added to the input signal by a passive combiner network. The attenuator is used to adjust the sensitivity of the ΔΣ A/D and to increase its linearity while keeping the dynamic range unchanged (within limits).
It can be shown that the transfer function of the filter in Fig. 6.1b is

$$\frac{W}{U} = \frac{\frac{g_{mb1}}{C}s + \frac{g_{mb0}g_{mx} + g_{mb1}(g_{of} + g_{ob0})}{C^2}}{s^2 + \left(\frac{g_{of} + g_{ob0} + g_{ox} + g_{ob1} + g_{oQ} - g_{mQ}}{C}\right)s + \frac{g_{mx}g_{mf} + (g_{of} + g_{ob0})(g_{ox} + g_{ob1} + g_{oQ} - g_{mQ})}{C^2}} \quad (6.1)$$

where the g_o terms represent the transconductor output conductances. The

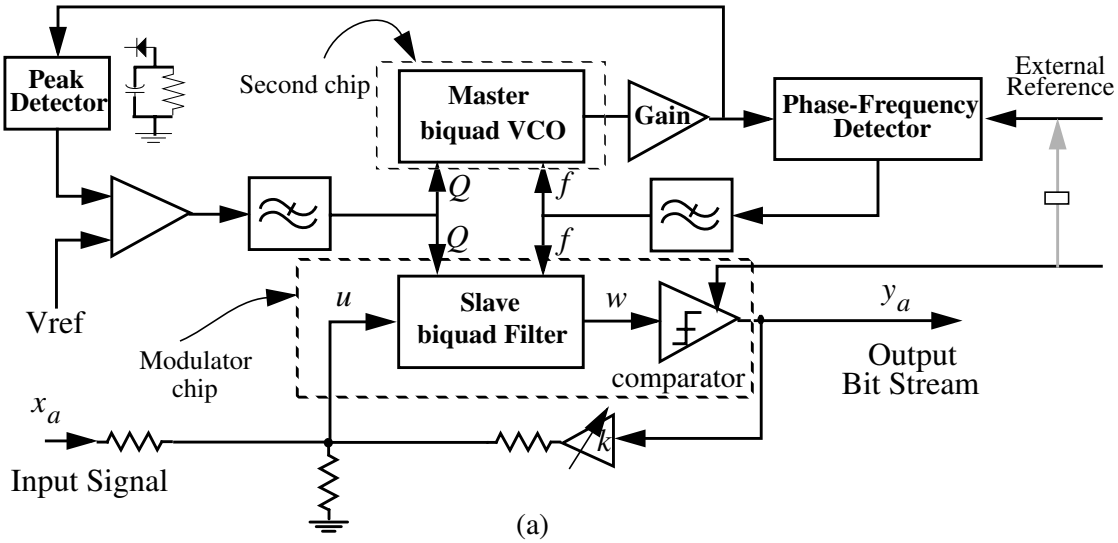


Figure 6.1 : Single ended diagram of (a) the second-order Sigma-Delta modulator with tuning circuitry, (b) G_m-C biquad filter.

transconductor terms represented by g_{mx} and $-g_{mf}$ in Fig. 6.1b are used to tune the poles of the filters as can be inferred from the constant term in the denominator of (6.1) which in our example was $\omega_o=2\pi(50)$ Mrad/s. The transconductor represented by $-g_{mQ}$ is set negative, cancelling out the effect of the transconductors' output conductances in the s coefficient in the denominator of (6.1). This way one can achieve an infinite Q filter as

required for the second-order transfer function in (3.37). The transconductor terms in the branches represented by g_{mb0} and g_{mb1} in Fig. 6.1b should be tuned to set the required zero for the loop transfer function. It can be shown that if $g_{mx} = g_{mf} = g_m$ then it is required to have $g_{mb0} = -g_{mb1} = 0.5g_m$ in order to make the filter's zero given in (6.1) the same as the ideal transfer function's zero given in (3.37). However, as (6.1) shows, there would be some errors in zero location due to the finite transconductors' output resistance ($1/g_o$ values). This error doesn't lead to a modulator instability as the second-order bandpass ΔΣ modulator is a robust system; however, it reduces the maximum achievable *SNR*.

6.2 Automatic Tuning

As mentioned in Sec. 5.3 continuous-time filters are subject to fabrication tolerances, temperature variations and parasitic effects, hence a tuning scheme is required especially with high speed circuits. To correct the transfer function of the second-order ΔΣ loop filter, a master-slave tuning circuit was implemented. The master-slave tuning scheme is commonly used for the frequency and Q-tuning of a main filter (slave). The resonance frequency of the master voltage-controlled filter (VCF) [Gop90], or the master voltage-controlled oscillator (VCO) [Nau92], [Kho91] is locked to an external accurate frequency by a PLL system. The Q of the master VCF or VCO can be controlled by comparing the amplitude of the master output signal to a reference voltage. The main filter (slave) is tuned by the same frequency and Q control voltages of the master.

For tuning the ΔΣ modulator loop filter, a practical master-slave scheme was implemented which is shown in Fig. 6.1a. The ideal second order bandpass ΔΣ loop transfer function in (3.37) represents an infinite Q filter with two poles on the $j\omega$ axis as shown in Fig. 3.12a. Notice that this transfer function can be regarded as a typical oscillator. Therefore, the VCO master-slave tuning scheme is naturally suited for this purpose. It should be noted that unlike traditional master-slave schemes which tune an open-loop slave filter, the slave filter in our continuous-time ΔΣ modulator is working in a closed-loop system. As will be shown in Section Sec. 6.3, tuning of the open loop master resonance frequency (VCO) will result in the tuning of the ΔΣ loop resonance frequency and therefore the tuning of the bandpass ΔΣ noise transfer function (NTF)

notch frequency. The Q of the filters (master and slave) were tuned by comparing the amplitude of the VCO output signal with a reference voltage. The amplitude of the VCO output signal was detected by a Schottky diode peak-detector as shown in Fig. 6.1a.

The tunablity of a continuous-time bandpass ΔΣ converter center frequency with its inherent anti-alias filtering can be advantageous over a bandpass switched-C ΔΣ converter and could provide a new approach for channel selection in digital radio receivers. The idea is shown in Fig. 6.2. Having a tunable bandpass ΔΣ converter at the

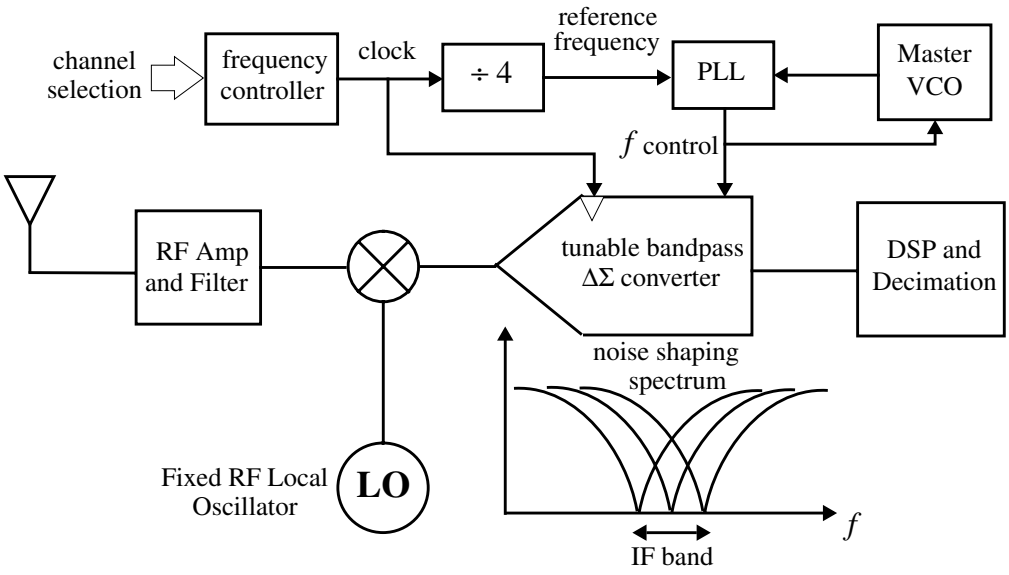


Figure 6.2 : Block diagram showing the possible channel selection at the IF stage by a tunable bandpass ΔΣ modulator.

IF stage removes the necessity of channel selection at the RF. So, as illustrated in Fig. 6.2, one may use a fixed local oscillator (presumably a SAW or crystal oscillator) and move the synthesizer to the IF stage which would consume less power as it would operate at lower frequency. Moreover, since the ΔΣ master-slave tuning scheme shown in Fig. 6.1a uses a PLL (it is already in IF), the only requirement for channel selection at the IF is a frequency controller as shown in Fig. 6.2.

It should be noted that because the ΔΣ modulator center frequency in this example is one quarter of the clock frequency (ΔΣ NTF zeros are at $\pm j$ as shown in Fig. 3.12a), by

changing the reference frequency the clock frequency should be changed accordingly. This relationship is shown in Fig. 6.1a by the dotted line connection between the clock and the external reference signal and by the frequency divider (by 4) as shown in Fig. 6.2.

6.3 Experimental Results

With the second-order bandpass TC filter [Shov92], although not optimized for a ΔΣ modulator application, it became possible to make a prototype modulator in order to perform some experimental tests. The noise-shaping response, intermodulation and particularly the anti-alias filtering measurements along with the master-slave tuning were the important parts of these experiments.

6.3.1 Signal-to-Noise Ratio (*SNR*)

The measured *SNR* is plotted against the input signal power in Fig. 6.3 for two different

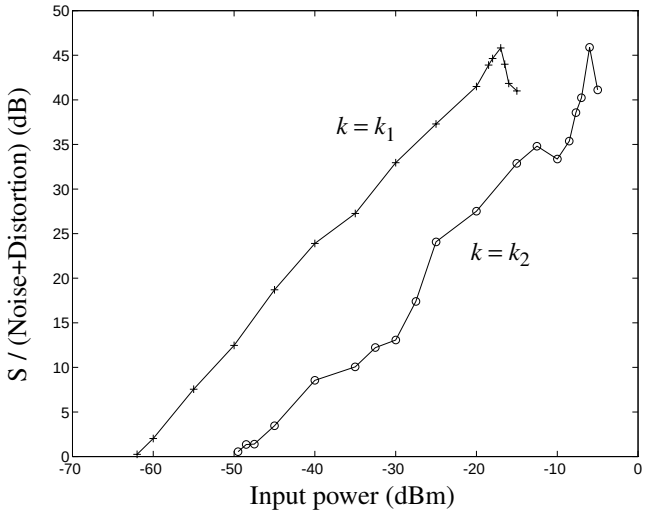


Figure 6.3 : Measured *SNR* versus input signal level for different gain values ($k_1 = k_2$-10 dB), for BW = 200 KHz.

loop gain (k) values. The input signal was a 50 MHz sinusoid and the clock frequency was 200 MHz. The output digital data was supplied to a logic analyzer. The plots shown in Fig. 6.3 were obtained by taking a 2^{18}–point Hanning windowed FFT of the ΔΣ bit

stream for each input signal level. As can be seen from Fig. 6.3 the maximum *SNR* in a 200 KHz bandwidth is 46 dB, and occurs for input level of $P_{in} = -17$ dBm with $k = k_1$. By increasing the gain the same *SNR* was achieved at $P_{in} = -6$ dBm (for $k = k_2$), where $k_2 - k_1 = 10$ dB.

The noise shaping spectrum obtained by taking an FFT (using a Hanning window) of the 200 MHz ΔΣ modulator output bit stream for a sinusoidal input signal of $P_{in} = -17$ dBm with $k = k_1$ is plotted in Fig. 6.4. It should be noted that the signal transfer function from input to output provides 13 dB and 0 dB gain for $k = k_1$ and $k = k_2$ respectively, which is not shown in Fig. 6.3 and Fig. 6.4.

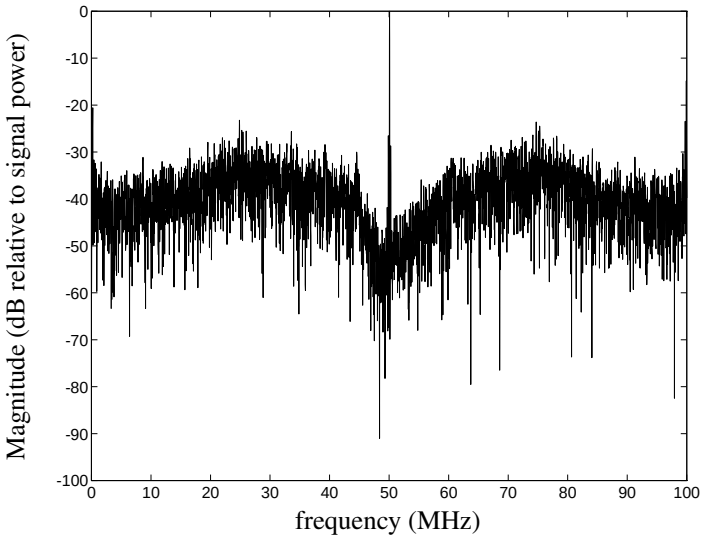


Figure 6.4 : Experimental output spectrum of the second-order modulator.

6.3.2 Linearity

Analog-to-digital conversion at the IF (or RF) stage for digital radio receivers puts linearity constraints on the bandpass A/D converter. The linearity of the ΔΣ modulator is limited by the linearity of the filter inside the loop which in our case is a transconductor-*C* filter. Fig. 6.3 shows that for higher loop gain (higher loop gain, $k = k_2$), the second-order ΔΣ modulator presents higher integral and differential nonlinearity. Although ΔΣ A/D converters are considered to be highly linear A/Ds, in low order ΔΣ modulators

(first-order lowpass and second-order bandpass), the noise and distortion depend on the signal level [Can92] and also on signal frequency in the second-order bandpass ΔΣ modulator, so causing more nonlinearity. As the *SNR* plot for lower loop gain ($k = k_1$) in Fig. 6.3 shows this non-linearity (noise dependency on signal level) was overcome significantly by reducing the loop gain.

Another important linearity measure in A/D converters is the third-order intermodulation product (IM3). Fig. 6.5 shows a plot of IM3 level against the input signal level (for $k = k_1$). Two in-band tones at equal power levels with a 50 KHz

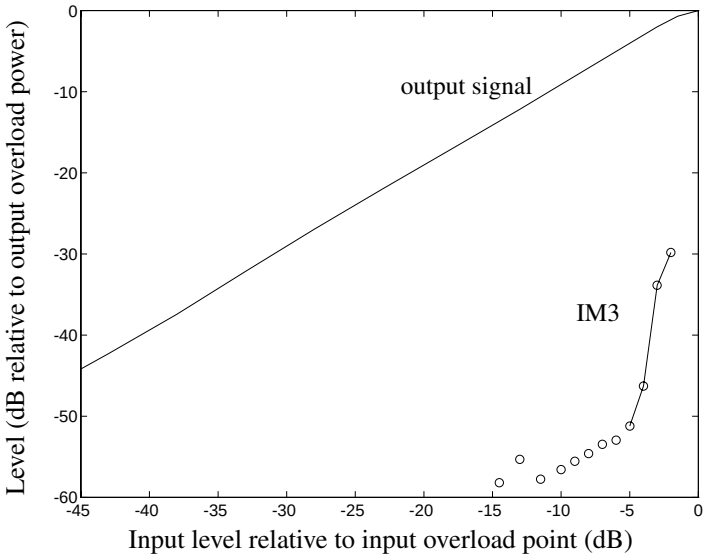


Figure 6.5 : Measured output signal and IM3 level v.s. the input signal level.

separation were applied to the modulator and the IM3 products were obtained again by taking a 2^{18}–point FFT of the ΔΣ bit stream. Although IM3 products for each tone at −3 dB input signal level (relative to the input overload point) are fairly high *i.e.* 21 dB below the output tone levels, for tones at −5 dB relative input level the IM3 products drop to 40 dB below the output tone level, giving 1% distortion. Fig. 6.6 shows the performance of the ΔΣ modulator intermodulation when two input tones at a −5 dB level (relative to overload) are supplied. For signal levels lower than −15 dB, IM3 levels are buried in the noise floor, so no in-band intermodulation was observed. Third-order

intermodulation here is bigger than what was reported in [Thu91]. The reason is attributed to the fact that the on-chip transconductor-*C* resonators used here are more non-linear than the discrete off-chip LC components used in [Thu91].

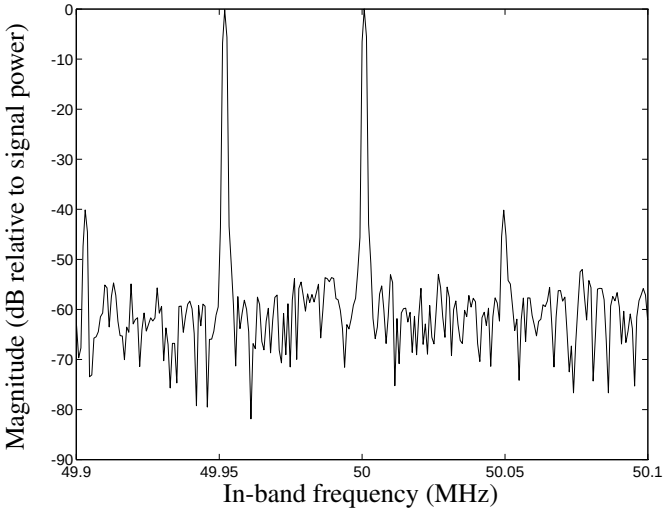


Figure 6.6 : Intermodulation (linearity) performance of ΔΣ modulator with two in-band input tones having −5 dB power relative to overload point.

6.3.3 Anti-alias (Image) Performance

Table 6.1 lists the attenuation of the signals aliased into the in-band region (50 MHz) for various frequencies in the first (150 MHz) and second image frequency (250 MHz) bands. The level of aliased in-band signals at the higher and lower frequencies of images increase which verifies that the zeros of signal frequency response are at the image frequencies ($f = nf_s \pm f_c, n = 1, 2, 3,\ldots$) as was shown theoretically in Sec. 3.2.

Table 6.1: The measured implicit anti-alias filter frequency response.

f_{in} (MHz)	aliased frequency (MHz)	attenuation (dB)
149.6	50.4	34
149.8	50.2	39
150	50	42
150.2	49.8	39
150.4	49.6	34
249.6	49.6	39
250	50	49
250.4	50.4	45

6.3.4 ΔΣ NTF Notch Frequency Control

As explained in Sec. 6.2 and illustrated in Fig. 6.1a, by changing the external reference frequency it was possible to change the bandpass ΔΣ NTF notch frequency using the master-slave tuning scheme.

Fig. 6.7 shows the experimental results of the ΔΣ NTF zeros (notches) tuned to three different frequencies (45 MHz, 55 MHz and 65 MHz) while the clock frequency in each case was changed accordingly *i.e.* $f_s = 4f_o$. The ΔΣ NTF notch frequency has been tuned between 40 MHz and 67.5 MHz providing a practical 50% tuning range. The transconductor-*C* bandpass filter is tunable over the range of 10 MHz to 100 MHz [Shov92], however, at low frequencies its high-Q performance degrades. As shown in Fig. 5.5 for getting the maximum achievable *SNR*, the typical Q required for a bandpass ΔΣ modulator is at least 50. Therefore, the low frequency limit of the ΔΣ tuning range is due to the low Q performance of the transconductor-*C* filter (at frequencies lower than 40 MHz).The high frequency limit of the ΔΣ tuning range is due to the frequency

limitation of the off-chip phase-frequency detector used (Fig. 6.1a).

Figure 6.7 : Experimental result for tuning of the ΔΣ modulator noise-shaping center frequency. The three different tuned ΔΣ NTF notch frequencies are at 45 MHz, 55 MHz and 65 MHz, respectively.

As expected a frequency mismatch was observed between the master VCO (external reference) and the slave ΔΣ. The frequency offset between the external reference (master VCO frequency) and the ΔΣ NTF notch frequency (slave resonance frequency) over the entire tuning band was almost fixed at 6.5 MHz. For example, for ΔΣ center frequencies at 45 MHz, 55 MHz and 65 MHz shown in Fig. 6.7 the corresponding external reference frequencies were 38.5 MHz, 48.5 MHz and 58.5 MHz respectively. Although the master-slave tuning scheme is prone to mismatch between the master and the slave filters, this offset can be reduced significantly using careful design and layout techniques and by placing both the master and slave filters on a single chip.

6.4 Summary

A second-order transconductor-*C* ΔΣ modulator prototype along with a master-slave tuning scheme has been constructed with two separate transconductor-*C* filters. The notch center frequency of the ΔΣ modulator was tuned from 40 MHz to 67.5 MHz. It

was observed that since the master and slave filters were on two separate chips from different batches the matching between the master and slave was not very good (on the order of 10 %). This suggested that to achieve a better matching in a master-slave tuning scheme for a $\Delta\Sigma$ modulator implementation it is imperative to place both master biquad and slave $\Delta\Sigma$ loop filter on the same die which as will be explained in Chapter 8 is done for the fully monolithic fourth-order modulator. The anti-alias filtering property of a continuous-time $\Delta\Sigma$ modulator proven analytically in Sec. 3.2 was verified here with experiments.

Chapter 7

Circuit Noise and Power Considerations

In design of the continuous-time filters the dynamic range—which is defined as the ratio of the maximum input signal to the minimum input signal that the circuit can handle linearly—is a very important parameter. It can be defined more exactly by spurious-free dynamic range (SFDR). The maximum input signal in the SFDR is the input level which just starts to create some distortion products above the noise floor. The minimum signal level is obtained from the input-referred noise in the band of interest. Both measures are obtained by integrating the noise power spectral density at a certain bandwidth.
This chapter studies how the dynamic range of the transconductor-*C* filter used can be improved. It shows the trade-offs which have to be considered for this purpose.

7.1 Noise Analysis for the Transconductor-amp-*C* Integrator

The input stage cross-coupled differential transconductor was shown in Fig. 5.28. From simulations it was found that the devices in this stage are the major noise contributor in the overall circuit. Actually this is true when the first stage has enough high gain. Since it is known that:

$$F = F_1 + (F_2 - 1)/G_1 + (F_2 - 1)(F_3 - 1)/G_1G_2 + \ldots \qquad (7.1)$$

where F the noise factor of the overall circuit, is the amount of the noise that the whole circuit adds to the input signal *i.e.* $F = (S_i/N_i)/(S_o/N_o)$ and F_1, F_2, …, G_1, G_2, … are the noise factors and gains of the first stage, second stage and so on, respectively.
Fig. 7.1a and Fig. 7.1b show a half circuit of a simple input differential transconductor

and its equivalent noise sources, from which the noise performance of input stage devices can be analyzed.

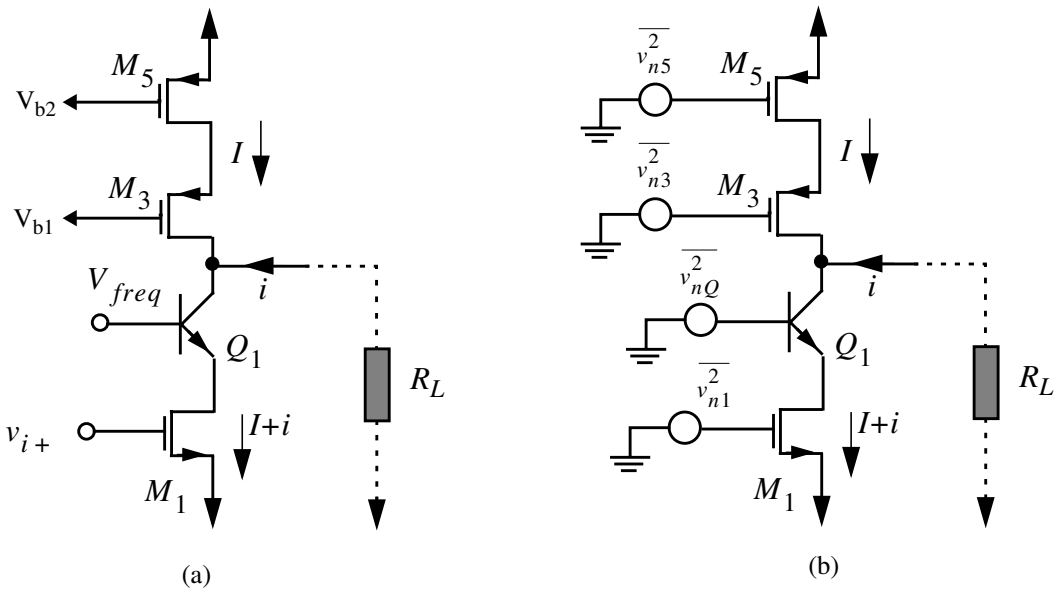


Figure 7.1 : (a) A half circuit schematic of the differential BiCMOS transconductor shown in Fig. 5.28, (b) device equivalent noise sources are added.

7.1.1 Cascode Active Load

The noise produced by PMOS active load devices *i.e.* M_3 and M_5 is shown in Fig. 7.1. A simple model for MOS mean square noise voltage and current is given in [Gray84] and [Greg86]:

$$\overline{v_n^2} = \frac{8kT}{3g_m}\Delta f, \qquad \overline{i_n^2} = \frac{8kT}{3}\cdot g_m\Delta f \tag{7.2}$$

where k is Boltzmann's constant, T absolute temperature, g_m the MOS transconductance and Δf the bandwidth in which noise is measured. The $\overline{v_n^2}/\Delta f$ noise power spectral density unit is (V^2/Hz).

A more general model has been introduced [Nic87], [Alin92], [ANA93] which can express more closely the noise performance of the MOS devices in the saturation region as well as triode region:

$$\overline{i_n^2} = \frac{8kT}{3}\cdot(g_m + g_{mb} + g_{ds})\Delta f = \text{NEF}\cdot\frac{8kT}{3}\cdot g_m\Delta f \tag{7.3}$$

where g_m is the input transconductance, g_{mb} the body-effect transconductance and g_{ds} the drain or output conductance. It should be noted that (7.3) may not be very accurate for a deep triode region, however it is close enough to give a good understanding of the excess noise in the triode-mode transconductor shown in Fig. 7.1. The NEF in (7.3) is a factor, the so called noise excess factor, which depends on the actual realization and transistor operating mode. For instance from (7.3) for a MOS operating in triode mode and neglecting g_{mb} it can easily be shown [Alin92] that:

$$\text{NEF} = \frac{V_{GS} - V_t}{V_{DS}} \tag{7.4}$$

For instance, for the NMOS transistor operating in triode mode (M_1 shown in Fig. 7.1), the NEF for V_{GS}=2.5 V, V_{DS}=0.2 V and V_t=0.7 V is 9 *i.e.* 19 dB. This number is big mainly because the g_{ds} term is a dominant factor in a MOS transistor in triode mode which could be even bigger than the g_m.

Since the PMOS active load devices shown in Fig. 7.1 are biased in the saturation region, the g_{mb} and g_{ds} terms are negligible compared to the g_m term (both total about 20% of g_m in this circuit). So, the simple formula given in (7.2) is used here. The equivalent output noise current produced by M_5 is simply given by:

$$\overline{i_{n5}^2} = g_{m5}^2 \cdot v_{n5}^2 = \frac{8kT}{3} \cdot g_{m5}\Delta f \tag{7.5}$$

which passes through the M_3 cascode transistor with almost unity current gain. However, the output noise produced by M_3 is attenuated significantly due to the high drain impedance of M_5. A small signal model for the PMOS cascode active load is shown in Fig. 7.2 from which it can be shown that:

$$\overline{i_{n3}^2} = \frac{\overline{v_{n3}^2}}{(1/g_{m3} + r_{ds5})^2} \tag{7.6}$$

For the same size M_3 and M_5 transistors it can be shown from (7.5) and (7.6) that

$$\frac{\overline{i_{n5}^2}}{\overline{i_{n3}^2}} = g_{m5}^2(1/g_{m3} + r_{ds5})^2 = (1 + g_{m5}r_{ds5})^2 \tag{7.7}$$

which with the numerical values in this example *i.e.* $g_{m5} = g_{m3} = 4.8\,\text{mS}$ and

g_{ds5} = 0.334 mA/V would be 24 dB. Therefore, the noise effect of M_3 can be neglected.

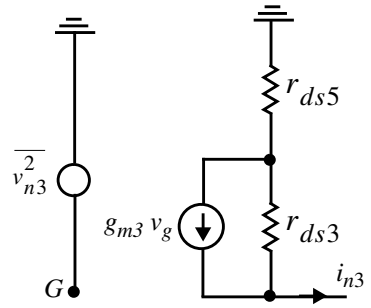


Figure 7.2 : A small signal model of the PMOS devices of Fig. 7.1.

The noise of M_5 may also be forced arbitrarily low by biasing it at a low g_m (using a small W/L device), at the cost of signal swing.

7.1.2 Bipolar Cascode Transistor

Another major noise source in the transconductor circuit shown in Fig. 5.28 and Fig. 7.1 is the bipolar cascode transistor. Actually simulations show that they are the dominant noise sources in this circuit. The equivalent base referred noise of Q_1 shown in Fig. 7.1b is [Gray84]:

$$\overline{v_{nQ}^2} = 4kT\left(r_b + \frac{1}{2g_{mQ}}\right)\Delta f \qquad (7.8)$$

which produces an output current noise as the following

$$\overline{i_{nQ}^2} = \frac{4kT\left(r_b + \frac{1}{2g_{mQ}}\right)}{\left(1/g_{mQ} + r_{ds1}\right)^2}\Delta f \qquad (7.9)$$

From (7.5) and (7.9) given r_b=92Ω, r_{ds1}=62Ω and $g_{m\mathrm{Q}}$=53mS one can show that $\overline{i_{nQ}^2}/\overline{i_{n5}^2} \sim 3\mathrm{dB}$ which is in agreement with the simulation results.

7.1.3 Input NMOS Triode-Mode Devices

The noise expression for the input NMOS devices operating in triode mode was given in

(7.3) and (7.4) which show that

$$\frac{\overline{i_{nQ}^2}}{\overline{i_{n1}^2}} = \frac{\left(r_b + \frac{1}{2g_{mQ}}\right)}{\left(\frac{2}{3}g_{m1}\right)(1/g_{mQ} + r_{ds1})^2} \qquad (7.10)$$

It can be shown that for g_{m1}=230 μS and NEF=9: $\overline{i_{nQ}^2}/\overline{i_{n1}^2} \sim 20\text{dB}$. Unfortunately, this is contrary to good design principles of low noise amplifier circuits in which the very first input device should be the dominant noise source. From (7.9) and (7.10) it can be shown that $\overline{i_{nQ}^2}$ can be lowered by increasing r_{ds1} which for a MOS device in triode mode is given by:

$$r_{ds1} = 1/[\mu_n C_{ox}(W/L)_1(V_{GS} - V_t - V_{DS})] \ . \qquad (7.11)$$

This can be accomplished by reducing the $(W/L)_1$ coefficient or/and reducing $(V_{GS} - V_t - V_{DS})$. Reducing $(W/L)_1$ decreases the g_{m1} value which in turn increases the input referred noise voltage of the input NMOS devices; however, since the $\overline{i_{nQ}^2}/\overline{i_{n1}^2}$ coefficient is almost inversely proportional to $g_{m1}r_{ds1}^2$ and so directly proportional to $(W/L)_1$, overall it would reduce the $\overline{i_{nQ}^2}/\overline{i_{n1}^2}$ coefficient. However, too much reduction of the g_{m1} value may increase the net input referred noise voltage. This is because of two effects: Firstly reduction of the input device transconductor directly increases the input referred noise voltage due to the input device (7.2). Secondly it lowers the input stage voltage gain which as a result highlights the second stage amplifier noise as given in (7.1). This effect is shown later in Table 7.1. It should be noted that in a high-Q bandpass filter since the out-of-band gain of the first stage transconductor is usually very low, the input referred noise at a very wide bandwidth (e.g. 100MHz as shown in Table 7.1) can be determined by the second stage amplifier. But for the passband (e.g. 10MHz as shown in Table 7.1), as mentioned, the first stage transconductor is the major source for the input referred noise.

Another factor to control the noise in this circuit is to increase the integrating capacitor values. This happens because in order to achieve the same center passband frequency the V_{DS} voltage then has to be increased which results in a higher g_{m1} and higher r_{ds1}. This is beneficial for lowering the $\overline{i_{nQ}^2}/\overline{i_{n1}^2}$ coefficient (7.10), the $\overline{i_{nQ}^2}$ absolute value (7.9) and the noise contribution of the input device M_1 (7.2) as well.

So far the noise produced in the half circuit was analyzed. The noise in the differential circuit is higher by a factor of 2 compared to the half circuit. Another factor of 2 is applicable because of the cross-coupled configuration shown back in Fig. 5.28.

There is another aspect of compromise in this transconductor design which is between excess noise and linearity. Recall from (5.23)-(5.26) that the lower V_{DS}/V_T the more linear a transconductor can be achieved where V_T is the thermal voltage in a bipolar transistor (about 26 mV at room temperature). However, as shown in (5.25) lower V_{DS}/V_T or basically lower V_{DS} means lower input transconductance g_m which as can be noticed from (7.2) and (7.3) increases the input-referred noise of the transconductor. Therefore, the excess noise of the transconductor from the input NMOS devices can be reduced at the cost of linearity.

7.2 Power Minimization and CM feedback

One way to reduce the power consumption of the circuit is to lower the supply voltage. However, in order to maintain a wide output voltage swing the number of transistors should then be reduced between the rail supplies. The cascode PMOS active load shown in Fig. 7.1 can hardly be afforded for a 3V or lower supply design. A simple active PMOS load doesn't improve the noise performance of the circuit too much since its noise contribution, for the same size devices, is equal to that of the top PMOS device in the cascode configuration shown in Fig. 7.1 *i.e.* M_5. Recall from Sec. 7.1.1 that the noise contribution of M_3 in the cascode load was negligible.

A low-voltage input stage transconductor has been designed which is shown in Fig. 7.3. The new transconductor compared to the old one shown back in Fig. 5.28 has three main differences:

1) As mentioned it only includes a simple PMOS active load compared to a cascode PMOS load, thus increasing swing.

2) Unlike the cross-coupled configuration in the old one it has only a simple differential

structure, improving noise by 3dB at the cost of CMRR.

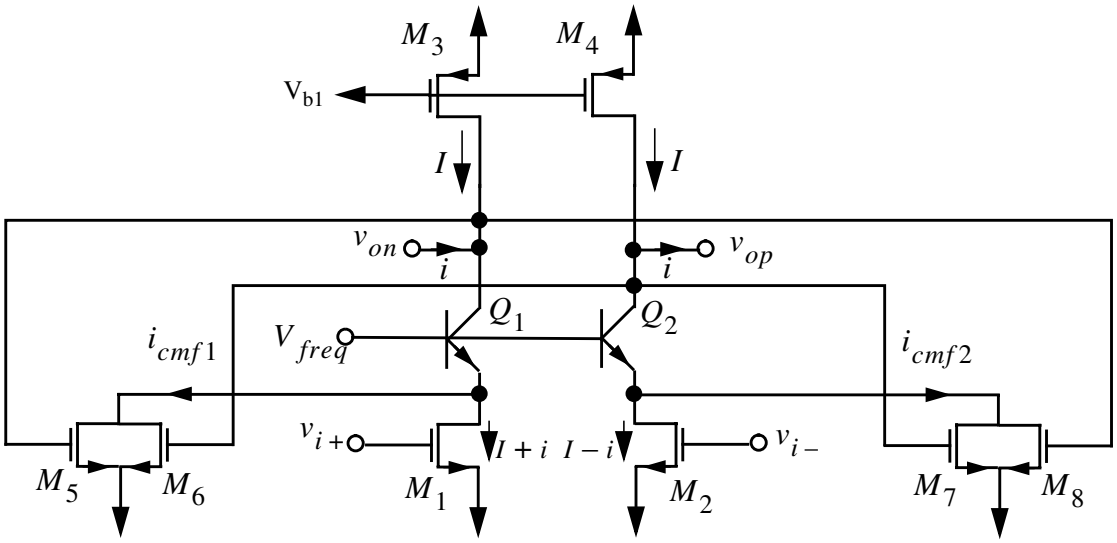


Figure 7.3 : A low-voltage design for the first stage transconductor.

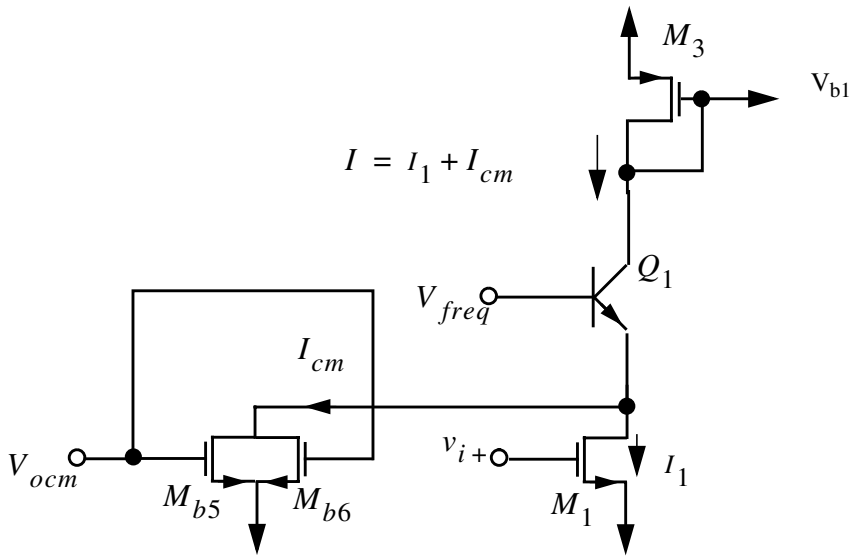


Figure 7.4 : Bias circuitry for the transconductor shown in Fig. 7.3.

3) To provide an extra common-mode feedback at the first stage transconductor four NMOS transistors *i.e.* M_5, M_6, M_7 and M_8 operating in triode mode have been added. This topology was chosen because these devices are biased similarly to the

input devices. The gates of these devices are biased at the output common-mode voltage (analog ground) and their V_{DS} are identical to that of the input devices. Therefore, with the same size transistors as the input NMOS devices the common-mode transistors sink the same amount of current as the input devices. This increases the input transconductor's power consumption. So, in this structure the power consumption and noise, as will be shown later, are traded off for CMRR performance.

It should be mentioned that the CM currents in transistors M_5, M_6, M_7 and M_8 shown in Fig. 7.3 are referenced to the bias CM current I_{cm} produced by M_{b5} and M_{b6} in the bias circuit shown in Fig. 7.4. Recently a very similar common-mode feedback circuit for this kind of BiCMOS triode-mode transconductors has been presented [Yang95], [Yan95]. A version of the circuit in [Yang95], [Yan95] is shown in Fig. 7.5. The principle of the CM feedback circuits in Fig. 7.3-Fig. 7.4 and Fig. 7.5 are the same. As can be noticed from Fig. 7.5 the CM feedback current I_{cmfb} (the total current of M_5 and M_6) is referenced to the bias current I_1 produced by M_7.

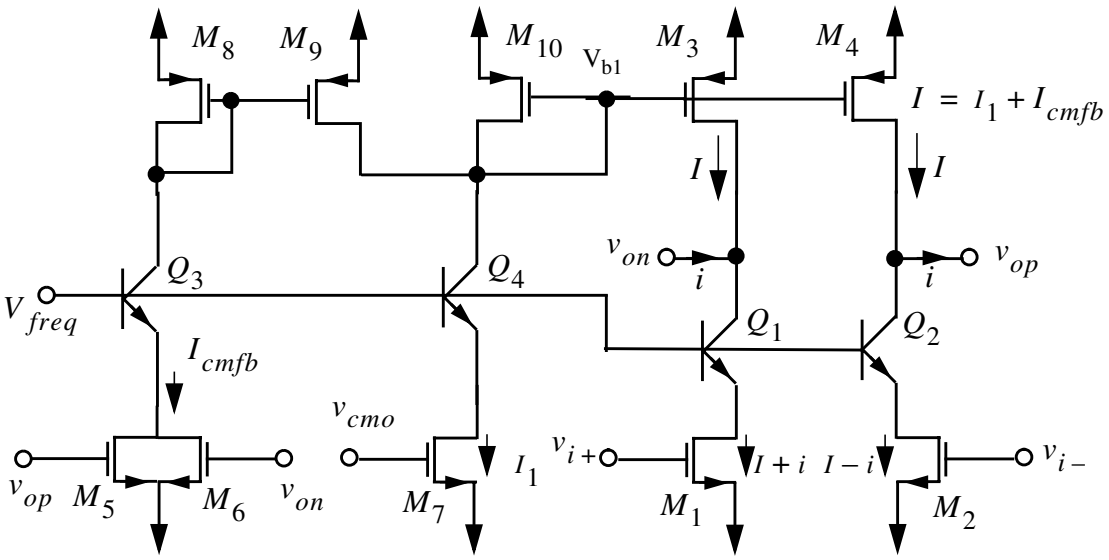


Figure 7.5 : Another approach for CM feedback.

In order to operate the whole ΔΣ loop filter at a 3V voltage supply or lower, it is required to replace the PMOS cascode load of the second stage amplifier shown back in Fig. 5.11 with a simple PMOS load too.

7.3 Comparison of Different Designs

Table 7.1 demonstrates a comparison of the power and noise specifications of the fourth-

Table 7.1: Noise and Power Comparison among Different Designs

No.	ΔΣ Loop Filter	Input Device Width (μm)	Caps. (pF)	Extra CMFB M_5–M_8 (W/L)	V_{DS}* (mV)	Tuning Range (MHz) **	Power (mw)	Integrated Input and Output Referred Noise Voltage (mV) at Certain BW					
								100MHZ		10MHZ		1MHz	
								I/P	O/P	I/P	O/P	I/P	O/P
1	5V Design (cross-coupled)	25	0.8	Non	37	10–150	114	4.8	75	2.38	74.5	0.805	60.3
2	5V Design	1.59	0.4	4/0.8	271	1–110	177	4.5	45.1	1.81	45.06	0.607	37.1
3	New 3V Design	5	2.0	4/0.8	269	5–55	87	1.23	10.8	0.383	10.77	0.129	8.59
4	New 3V Design	2.5	2.0	20/0.8	588	5-27	73	1.30	10.0	0.421	10.00	0.140	8.04
5	New 3V Design	10	2.0	4/0.8	150	3-35	75	1.27	10.5	0.370	10.53	0.124	8.60
6	New 3V Design	15	2.0	50/0.8	110	2.5-38	78	1.41	13.0	0.443	12.98	0.148	10.5
7	New 3V Design	5	3.2	4/0.8	407	3–36	98	0.93	7.06	0.278	7.047	0.093	5.32
8	New 3V Design	5	3.2	20/0.8	407	2–28	77	0.95	5.55	0.227	5.533	0.075	4.08
9	New 3V Design	10	3.2	4/0.8	220	3-27	88	0.94	7.14	0.241	7.129	0.080	5.78

*. V_{GS} in every case is set to analog ground: 2.5V and 1.5V for 5V and 3V single supplies respectively.
**. Over the given tuning range the minimum Q of 30 was guaranteed which happens at lower limit. At lower frequencies the high Q performance of the filter is degraded.

order ΔΣ bandpass loop filters among several designs whose center frequencies are tuned at 25MHz and their Q at 25.

A summary of the filter specifications is as follows:

① The first row describes a 5V cross-coupled active cascode-load design shown back in Fig. 5.28. As shown by the figures in Table 7.1 unfortunately this design is neither optimized for noise nor for power. However, since the input NMOS devices are strongly biased in the linear mode (with a low V_{DS}=37 mV) a very wideband tuning range of the center frequency can be achieved by a small change of the frequency control voltage (and so V_{DS}) represented by V_{freq} in Fig. 7.1a. As shown in Table 7.1 a tuning range greater than a decade can be achieved (10MHz−150MHz). Besides, since the NMOS input devices are fairly large it provides a better transconductor matching compared to the other designs given in Table 7.1. This would result in a more accurate realization of the filter's poles and zeros and so a better ΔΣ loop transfer function implementation. This design also lacks a proper common-mode feedback.

② In the second design the minimum size input transistors have been chosen. The input stage transconductor is similar to that shown in Fig. 7.3 except that the cascode PMOS active load is used here. Recall from Sec. 7.1.2 and Sec. 7.1.3 that the smaller input transconductance g_{m1} tends to reduce the equivalent noise of the cascode bipolar transistor Q_1 which was the dominant part in the first example. Simulations showed that the equivalent output noise of the cascode bipolar transistor Q_1 was reduced by a factor of 3 in a 100MHz bandwidth. The overall noise of this design is a bit better than that of the first one as shown in Table 7.1, however, the power consumption is bigger despite

the smaller input transistors. This is because of the large extra common-mode feedback transistors (41⁄0.8) added here.

③ The design no. 3 and the rest given in Table 7.1 are based on the schematic shown in Fig. 7.3. Another basic difference between previous designs (no. 1 and no. 2) and the new designs is that in the previous designs dummy transistors biased at analog ground were placed in parallel with the input devices to make a very close matching between the two resonators in the fourth-order ΔΣ loop filter shown back in Fig. 5.26. Again this costs more power consumption which can be noticed from the higher power dissipation of the no. 2 example compared to the no. 3.

The input transistor size, integrating capacitor value and the extra common-mode transistors' sizes have been examined in these examples in order to find an optimum case for the filter's noise and power consumption. As can be found from Table 7.1, the input referred noise and so the dynamic range (DR) of the filter[1] in a 10MHz bandwidth (from 20MHz to 30MHz) is improved in example no. 3 by 16dB compared to that in the example no. 1. In the meantime the power consumption is improved by a factor of 0.76.

④ Lower size input devices *i.e.* W=2.5μm here, as mentioned in Sec. 7.1.3, don't reduce the circuit noise even with smaller extra common-mode transistors.

⑤ Larger input devices compared to the no. 3 example *i.e.* W=10μm as shown in Table 7.1 don't influence the filter's noise performance very much. On one

1. Recall that every filter in Table 7.1 is tuned at 25MHz center frequency with a Q=25.

hand larger input devices tend to keep the input referred noise lower. On the other hand, as shown by (7.9) and explained in Sec. 7.1.2, larger input NMOS devices results in some smaller output impedance in the input devices, r_{ds1}, and so larger output current noise from the cascode bipolar transistors. As a result the overall noise performance of this example is similar to that of the no. 3 one while consuming less power and giving better matching due to the larger input devices.

⑥ From larger input devices (compared to example 5) *i.e.* W=15μm as shown in Table 7.1 deteriorates the filter's noise performance. This is because the noise terms produced by the cascode bipolar devices dominate when the output impedance of the large input devices, r_{ds1}, is reduced significantly.

⑦,⑧ The no. 7 and no. 8 examples show how the integrating capacitor would affect the circuit noise. As can be noticed from Table 7.1 higher integrating capacitors (compared to the no. 3 example) require higher V_{DS} voltage to produce the same center frequency (25MHz here). This as mentioned in Sec. 7.1.2 reduces the bipolar noise a lot. The trade off here is as the following:

at some high V_{DS} voltage the input NMOS devices move to the saturation region which then limits the upper frequency tuning range of the filter. So, considering the fabrication tolerance, operating center frequency and the noise budget the V_{DS} voltage and consequently the integrating capacitors can be chosen. By comparison of the no. 8 and no. 3 examples it can be observed that a larger capacitor (by a factor of $3.2/2.0$) in conjunction with a smaller CM transistor sizes reduces the input referred noise in a 10MHz bandwidth

by 4.5dB.

In conclusion from the comparison of the no. 8 and no. 1 examples one can see that the input referred noise and so the DR in the new design is improved by 20dB (in a 10MHz bandwidth) at a cost of a factor of 5 in maximum operating frequency.

One other important feature of a continuous-time ΔΣ loop filter design is its common-mode feedback performance which unfortunately requires a compromise with the filter's noise performance and its tuning range. The noise degradation due to a stronger common-mode feedback circuit can be readily noticed from Table 7.1. Higher common-mode feedback results in higher thermal noise. In the meantime, the relationship between the first stage CMFB, maximum allowable frequency control voltage V_{freq} to maintain devices in linear operation and/or the frequency tuning range of the loop filters given in Table 7.1 can be explained as follows:

The upper frequency limit of the designs given in Table 7.1 are obtained very conservatively. The highest possible V_{freq} voltage associated with a maximum tunable frequency given in Table 7.1 is that which still results in an almost constant output CM voltage (analog ground) over the entire power supply DC swing of the input CM voltage (from negative to positive supply voltage) and more importantly the bipolar transistors Q_1 and Q_2 in Fig. 7.3 are still in active region. This can be described with numerical values for the transconductor shown in Fig. 7.3 and parameters given in the seventh row of Table 7.1. With V_{GS} of the input NMOS devices M_1 and M_2 sitting at analog ground 1.5 V and $V_{on} = 0.75$, $V_{DS} \geq 0.75$ satisfies that the input devices are still in the triode-mode region. This sets the maximum voltage for $V_f = V_{DS(max)} + V_{BE} \approx 1.65$ and so the maximum frequency, 36.2 MHz to which the center frequency of the filter can be tuned linearly. Increasing V_f shouldn't ideally change the center frequency any more since in saturation transconductances g_m of the input NMOS devices are not a function of V_{DS}. However, a very slight frequency increment to 38 MHz was obtained by increasing V_f to 2V. It should be noted that since we don't want that the bipolar transistors to operate in saturation mode, considering a minimum 0.5 V for V_{CE}, then

the maximum allowable V_f is 1.85 V at which the filter's center frequency is at 37.6 MHz. It should be noted that the maximum frequencies reported in Table 7.1 are those due to the maximum V_{DS} voltages at which devices still are operating in triode mode region.

It should also be noted that it is desirable to keep the filter's output CM voltage constant over the entire linear mode operation of the input NMOS devices too (simulations verified that this can simply be achieved if the output CM voltage stays at its nominal value *i.e.* analog ground for the high end of the devices' linear mode operation *i.e.* at the maximum V_{DS} in which the input devices are still in linear mode operation). This guarantees that the full linear range of the transconductance tuning (therefore the center frequency) versus V_{DS} has been used:

$$g_{m1} = \mu_n C_{ox} \frac{W}{L} V_{DS} \qquad (7.1)$$

without disruption of the CMFB operation. From Table 7.1 only the no. ②, ③, ④ and ⑦ examples satisfy the preceding characteristic meaning that CMFB is strong enough over the entire linear mode operation of the input devices. It should be noted that the preceding characteristic is desirable for a very wide frequency tuning range. In a practical application it is only required to compensate nonidealities from a real implementation such as fabrication tolerance, temperature drift and so on which differ among different technologies but are normally not larger than 50%. So, in order to preserve the noise and power performance of a continuous-time filter one may limit the filter's frequency tuning range as much as possible. For instance, the no. ⑧ and no. ③ examples in Table 7.1 can be compared for this purpose.

The MSA (maximum signal amplitude), the input dynamic range, *i.e.* $20\log[\mathrm{MSA}/(\mathrm{N_t}+\mathrm{N_q})]$ where $\mathrm{N_t}$ is the input referred thermal noise voltage integrated over a 1MHz bandwidth centered at 25MHz for this example and $\mathrm{N_q}$ the in-band quantization noise obtained from the transient simulation neglecting the device thermal noise sources. The simulated *SNR* of the modulators employing some of the loop filters given back in Table 7.1, neglecting the device thermal noise sources, for a 1MHz bandwidth are shown in Table 7.2. It should be noted that the loop center frequency is again at 25MHz. The input and output referred noise figures given in Table 7.2 are obtained from the filters set to their maximum Q as expected for a normal

bandpass ΔΣ modulator loop filter.

As shown in Table 7.2 the quantization noise and the MSA (so the signal-to-quantization noise) in different designs are very close. However, the input referred thermal noise voltage has improved substantially from the first design. This in turn has improved the dynamic range of the modulator by 13.9dB from the first design to the last one (for a 1MHz bandwidth) as can be observed from Table 7.2. It should be noted that in a design

Table 7.2: MSA, DR and *SNR* of the ΔΣ modulators with some of the loop filters given in Table 7.1.

No. from Table 7.1	ΔΣ Loop Filter	Input Device Width (μm)	Caps. (pF)	Extra CMFB M_5–M_8 (W/L)	V_{DS} (mV)	Power (mW)	Integrated Input and Output Referred Noise	N_q* (mV)	MSA (mV)	S/N** (dB)	DR*** (dB)
1	5V Design (cross-coupled)	25	0.8	Non	37	114	0.935	0.110	75	63	38.1
3	New 3V Design	5	2.0	41/0.8	269	87	0.149	0.075	87	61	50.5
7	New 3V Design	5	3.2	41/0.8	407	98	0.109	0.070	62	59	50.8
8	New 3V Design	5	3.2	20/0.8	407	77	0.089	0.070	62	59	52.0

*. Quantization noise integrated at 1MHz bandwidth.

**. This is the simulated S/N_q of the ΔΣ modulator (at 1MHz BW) employing the corresponding loop filter.

***. Dynamic range is defined by $20\log_{10}$(MSA/Noise) where noise is the integrated input-referred noise at a certain bandwidth (1MHz here) when Q is set the maximum.

with a good noise figure for a low bandwidth (high OSR) (assuming that the noise shaping notch Q is high enough) the thermal noise and quantization noise are in the same order; however, for a high bandwidth (low OSR) the quantization noise becomes the dominant factor. By contrast in a design with a bad noise figure for a low bandwidth the thermal noise is much bigger than the quantization noise and for a high bandwidth usually the thermal and quantization noise are comparable. This can be readily verified for a low bandwidth (BW=1MHz) from the first and last rows in Table 7.2. For a larger

bandwidth (BW=5MHz) the quantization noise in the last row example in Table 7.2 is 2.5mV but its input referred thermal noise is only 0.195mV which result in a 27dB DR. However, these numbers in 5MHz bandwidth for the first example of Table 7.2 are 3.9mV, 2.0mV and 15dB respectively which shows a comparable thermal noise compared to the quantization noise.

7.4 Regular Transconductor-*C* Design

By removing every amplifier (opamp) stage followed by the transconductor-amp-*C* sections shown back in Fig. 5.26 a regular transconductor-*C* (TC) design can be implemented which would be a multi-input version of the loop filter shown back in Fig. 5.4. The obtained TC filter shown in Fig. 7.6 should ideally behave the same way as the original TC-amp loop filter. The only difference between the architectures shown in Fig. 7.6 and the TC-amp one back in Fig. 5.26 is in the sign of their integrators. It can easily

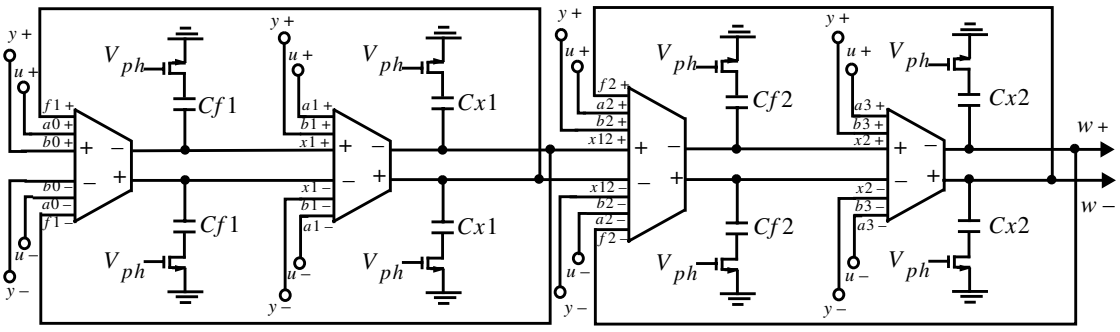


Figure 7.6 : The regular TC version of the loop filter shown in Fig. 5.26.

be verified that the new TC integrators have a negative sign whereas the original TC-amp integrators have a positive sign. This influences the numerator polynomial given in (5.5). However, this can easily be resolved by changing the sign of g_{mb2} and g_{mb0} transconductors. The NMOS transistors which are placed in series with the integrating capacitors work in triode mode acting as variable resistors. By controlling the V_{ph} one can simply tune the phase of the integrators and hence the Q of the loop filter. Of course, this structure implemented by regular transconductors is more sensitive to parasitic

components than the TC-amp structure. Besides, it is more sensitive to the loading effects such as the comparator's input impedance than the TC-amp loop filter. So, using a buffer stage preceding the comparator or an adaptive tuning scheme may be necessary.

7.5 Summary

A thermal noise analysis for the implemented triode-mode BiCMOS transconductor was presented. It was found that the cross-coupled transconductor-*C* filter explained in Chapter 5 with the first stage transconductor building block shown in Fig. 5.28 is not optimized in terms of the input-referred noise. Nevertheless, its tunablity and speed was twice as high as those of the other low noise circuits introduced in the chapter. In the new low-noise low-voltage (3V) designs an individual common-mode feedback was placed for the first stage transconductors. Therefore, the new low-noise 3V-supply transconductor-*C* circuits didn't enjoy a significant power consumption reduction compared to the previous cross-coupled transconductor. But the power consumption of the new designs were still slightly lower than that in the previous one. In conclusion it was shown that in the studied triode-mode transconductor-*C* $\Delta\Sigma$ modulator speed, tunablity and linearity should be compromised for a higher dynamic range and lower input-referred noise.

Chapter 8

Testing Results of the Monolithic Modulators and Filters with Future Suggestions

Two chips have been implemented in an NT BiCMOS technology in two different fabrication runs. The first parts, called ZA09, included a fourth-order continuous-time transconductor-*C* modulator with a second-order (biquad) filter on the same chip. The one-delay fourth-order chip with a schematic shown back in Fig. 5.26 composed of a fourth-order transconductor-*C* filter (as explained in Chapter 5) to implement the transfer function given in (3.23). The biquad filter with the structure shown back in Fig. 5.8 and shown again here in Fig. 8.1 was actually a replica of the fourth-order modulator loop filter's biquads shown back in Fig. 5.26. It was implemented for the master-slave tuning scheme explained in Sec. 6.2. The second parts, called ZA14, basically realized the same fourth-order continuous-time modulator implemented in ZA09 except with some slight layout differences to improve the matching in some devices.
Extensive measurements have been done on the preceding chips. In this chapter the measurement results will be given. Finally the chapter will be concluded with some explanations and suggestions to improve the performance of continuous-time transconductor-*C* $\Delta\Sigma$ modulators for future implementations.

8.1 ZA09 Results

In this section first the measurement results from the biquad filters and then those of the $\Delta\Sigma$ modulators from ZA09 will be given. The following is the performance achieved in a ZA09 chip.

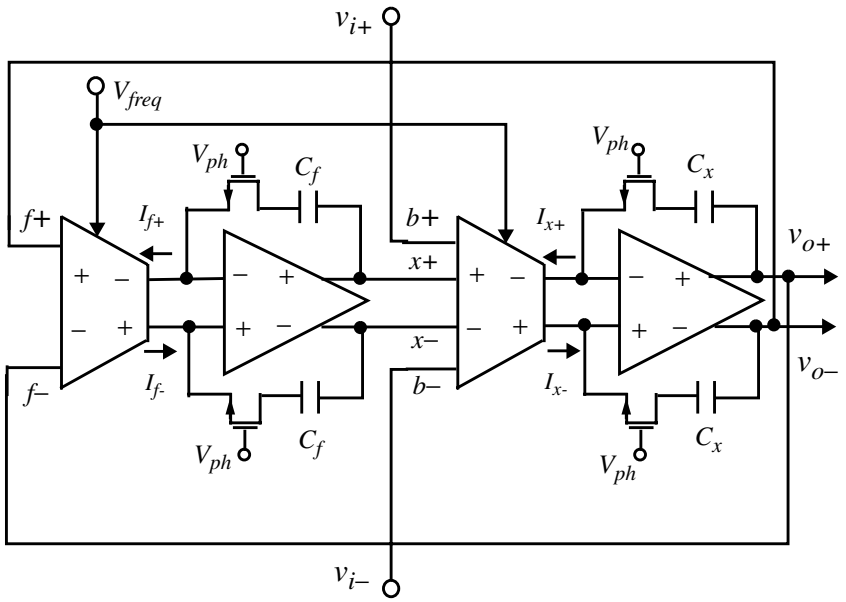


Figure 8.1 : A simplified second-order TC-amp based biquad loop

8.1.1 Layout Plot

Fig. 8.2 shows a layout plot of the fourth-order modulator and the biquad bandpass filter. The active area of the fourth-order ΔΣ modulator and biquad filter is approximately $2300\mu m \times 1700\mu m$ ($1650\mu m \times 1060\mu m$ active area). The master bias cell may be recognized at the upper left corner of the plot. The four op-amps of the fourth-order modulator and the two op-amps of the biquad filter are the six distinct squares surrounding the main analog section of the chip including the transconductors and the poly-poly capacitors. Integrating poly-poly capacitors appear in the middle of the analog section. The CMOS ΔΣ loop transconductors and those of the biquad filter are inter-digitated transistors placed at upper and lower sides of the capacitors. The stand-alone bipolar pseudo ECL parts including comparator, D-flip flop, DAC and the 50Ω chain bipolar buffer can be recognized on the right most side of the plot. The 50Ω chain bipolar buffer is a three-stage emitter-follower configuration in series with sizes of 1x, 4x and 15 x respectively which can handle enough current for a 50Ω output load like a spectrum analyzer. There is another 50Ω chain bipolar buffer for the biquad filter which appears at the upper right of the plot.

Figure 8.2 : Layout plot of the fourth-order modulator and the biquad bandpass filter.

The ΔΣ modulator and biquad filter dissipate power approximately proportional to the center frequencies. For example, the modulator's power consumptions at 50 MHz and 25 MHz are 218 mW and 114 mW respectively.

8.1.2 Biquad Filter Results

The center frequency of the bandpass filter has been varied by the control voltage represented with V_{freq} in Fig. 8.1. A wide range of frequency tuning from 25MHz to 110MHz has been achieved. Fig. 8.3 shows a plot of the filter's frequency response operating at three different center frequencies *i.e.* 30 MHz, 70 MHz and 110 MHz. The Q of the filter was adjusted by the control voltage V_{ph} (Fig. 8.1) almost without changing its center frequency as expected. Fig. 8.4 shows a plot of the filter Q adjustment with f_o=50 MHz. The other experimental results including the intermodulation linearity performance and the filter's dynamic range are summarized in Table 8.1. All of the

Table 8.1: Experimental Results Obtained From The Filter at Q=3 and 50MHz

Parameters	Measured Values
Frequency Tuning Range	25MHz-110MHz
IM_3, 71mV_{rms} (-10dBm) at 50MHz center frequency	–52dBc
IM_3, 71mV_{rms} (-10dBm) at 70MHz center frequency	–47dBc
Input Referred IIP_3 (Intermodulation Intercept Point)	11dBm
SFDR (Spurious Free Dynamic Range) in 200KHz bandwidth (at 50MHz)	41dB
SNR @ 1% TIMD (Total Intermodulation Distortion) in 200KHz (at 50MHz)	48dB
Peak Output Passband Noise Density (at 50MHz)	−112dBm/Hz
1dB Compression Input Level	180mV_{rms} (−1.9dBm)
Power Dissipation (at 50MHz)	90mW
Active Area	0.35mm^2

figures in Table 8.1 (unless mentioned) have been obtained from the measurements of

the filter with Q of 3 and f_o = 50MHz.

Figure 8.3 : The center frequency of the bandpass filter is tuned at three different frequencies: 30MHz, 70MHz and 100MHz.

Figure 8.4 : Three different Q adjustments for the bandpass filter centered at 50.5MHz: Q=8, Q=18, Q=170.

A short explanation of the measurements and parameters given in Table 8.1 are as follows:

– The IM3 figures given in Table 8.1 show the third order intermodulation product levels respect to the total input power in the two-tone measurement at the given frequencies (the tones are 200 KHz apart closely spaced from the filter's center frequency):

IM3 = either tone power + 3dB − third order intermodulation product power.

Of course, as expected the level of both input tones should be identical. The figures given in the second and third rows of Table 8.1 are for −10 dBm (71 mV_{rms}) total input signal level; the level of each input tone was at −13 dBm. The Fig. 8.5 shows the third-order intermodulation spurious-free spectrum for input tones each at −15 dBm or −12 dBm (56 mV_{rms}) total input level. It should be noted that the gain at −15 dBm input signal level was about −6 dB so, giving a −21 dBm output signal for each tone as shown in Fig. 8.5.

– The Input referred third-order intermodulation intercept point IIP_3 given in the fourth row in Table 8.1 was obtained from a two-tone measurement with each input tone at −13 dBm giving the fundamental output level at −19 dBm (−6 dB gain) and the third-order intermodulation level at −67 dBm:

$IIP_3 = \Delta/2$ + input signal level, where Δ is the difference between the output fundamental level and the third-order intermodulation level.

– SFDR or spurious free dynamic range in Table 8.1 was obtained from the two-tone experiment shown in Fig. 8.5 in which the third-order intermodulation products are at noise floor (for the spectrum analyzer resolution bandwidth at 1KHz):

SFDR = each output tone power + 3dB − integrated output noise over the band of interest

It should be noted that the noise power density as shown in Table 8.1 was −112 dBm/Hz.

– Another interesting parameter shown in Table 8.1 is the *SNR* at 1% total intermodulation distortion (1% TIMD). The measurement is similar to the two-tone SFDR measurement except that the inputs are increased to a level that the third-order intermodulation products become –40 dB lower than the fundamental signal power.

Figure 8.5 : Two-tone intermodulation spurious-free output level.

8.1.3 ΔΣ Modulator Results

A noise-shaping response of the ZA09 fourth-order ΔΣ modulator was achieved at a 25 MHz center frequency with 100 MHz clock rate. A spectrum of the bandpass noise shaping at 25 MHz is shown in Fig. 8.6. Fig. 8.7 shows the in-band spectrum of the same noise-shaping shown in Fig. 8.6. From Fig. 8.7 it can be noticed that the notch is not as deep as expected from the full circuit simulations like the one shown in Fig. 5.31. A discussion is given in Sec. 8.3 to explain the problems associated with ZA09 and ZA14 chips. However, one of the most important reasons why the notch shown in Fig. 8.7 is not very deep is the low Q performance of the loop filter at 25MHz. The maximum achievable Q at 25MHz in ZA09 part was about 4 which is not a desirable figure at all.

Recall from Sec. 5.3 that the minimum recommended Q was 30.

The measured *SNR* in a 2MHz, 1MHz and 200 KHz bandwidths were 25 dB, 28.5 dB and 34.5 dB respectively. This is a 3dB/octave improvement with oversampling, characteristic of a flat noise floor. From Fig. 8.6 two out-of-band peaks at 19 MHz and 31 MHz can be noticed. This could be a sign showing that the modulator's noise transfer function poles are near unit circle which for example could have been caused by extra loop delay. However, in Sec. 8.3.2 it will be shown that at 100MHz the actual extra loop delay should not be a big problem. Therefore, those peaks may have been caused by other sources. For example, the low-Q performance of the loop filter at 25MHz can result in a tonal behavior. Recall that this was verified from the simulations of finite-Q ideal transconductor-*C* filters in Sec. 5.3. Another source of problem could be lack of individual common-mode feedback in the first-stage transconductors which could cause a big non-linearity. Sec. 8.3 explains in more detail some possible reasons for this problem and why the modulators didn't work at higher frequencies.

Figure 8.6 : A bandpass noise-shaping spectrum of the fourth-order ZA09 chip at 25MHz.

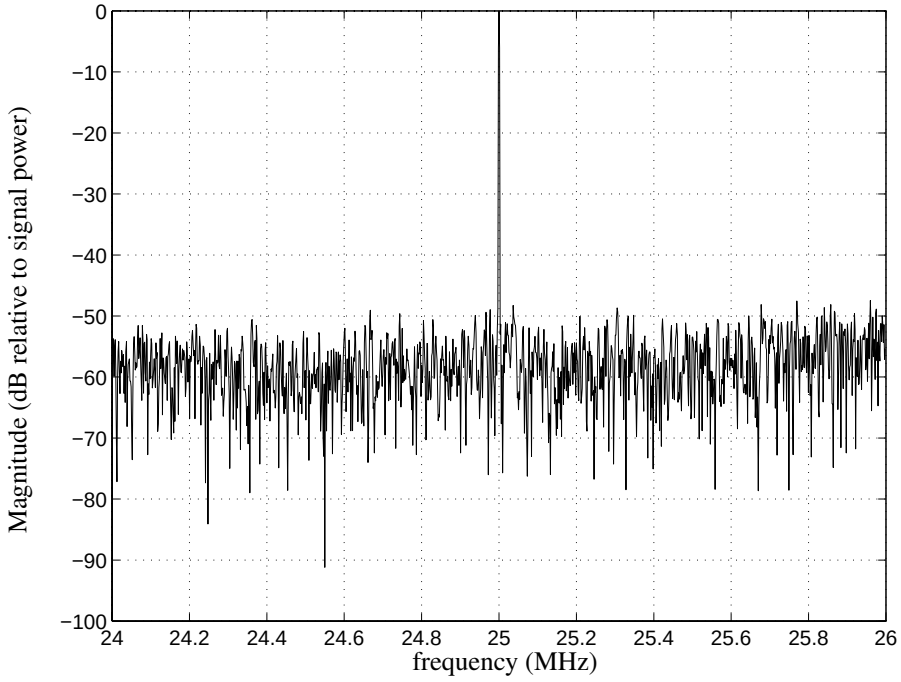


Figure 8.7 : In-band spectrum of the fourth-order ZA09 chip at 25MHz.

8.2 ZA14 Results

The same kind of measurements explained in Sec. 8.1 have been performed on the ZA14 parts which are as follows.

8.2.1 Biquad Filter Results

The same filter measurements explained in Sec. 8.1.2 were performed for the biquad filters in ZA14 parts. Table 8.1 summarizes a typical measurement results obtained from

Table 8.2: Experimental Results Obtained From The Filter at Q=3 and 50MHz

Parameters	Measured Values
Frequency Tuning Range	8MHz-80MHz
IM3, 71mV$_{rms}$ at 50MHz center frequency	–47dBc
IM3, 71mV$_{rms}$ at 70MHz center frequency	–43dBc
Input Referred IIP$_3$ (Intermodulation Intercept Point)	10.5dBm
SFDR (Spurious Free Dynamic Range) in 200KHz bandwidth (at 50MHz)	40dB
SNR @ 1% TIMD (Total Intermodulation Distortion) in 200KHz (at 50MHz)	47dB
Peak Output Passband Noise Density (at 50MHz)	−112dBm/Hz
1dB Compression Input Level	180mV$_{rms}$ (−1.9dBm)
Power Dissipation (at 50MHz)	90mW
Active Area	0.35mm^2

the ZA14 biquad filters.

8.2.2 ΔΣ Modulator Results

Unfortunately the noise-shaping obtained from ZA14 modulators didn't give the high frequency and high *SNR* performances achieved in simulations.

Bandpass noise-shaping was obtained from the fourth-order chip for frequencies lower than 10MHz *i.e.* 8MHz-10MHz (note that the lower frequency limit of the filters was 8MHz as given in Table 8.1). Fig. 8.8 shows a noise-shaping spectrum of a fourth-order ZA14 chip at 10 MHz center frequency with 40 MHz clock rate. The *SNR* for 4MHz, 1MHz and 200 KHz bandwidths were 21 dB, 23 dB and 24 dB respectively. As can be noticed the *SNR* is only increased by 3dB from 4MHz bandwidth to 200KHz bandwidth. This is because of the unwanted sideband noises produced around the output signal tone which can be more clearly observed from Fig. 8.9. Again it should be mentioned that the Q of the filter at 10MHz was 2.5 even lower than the ZA14 part at 25MHz. Therefore, it can not be expected that a very good notch depth will be achieved.

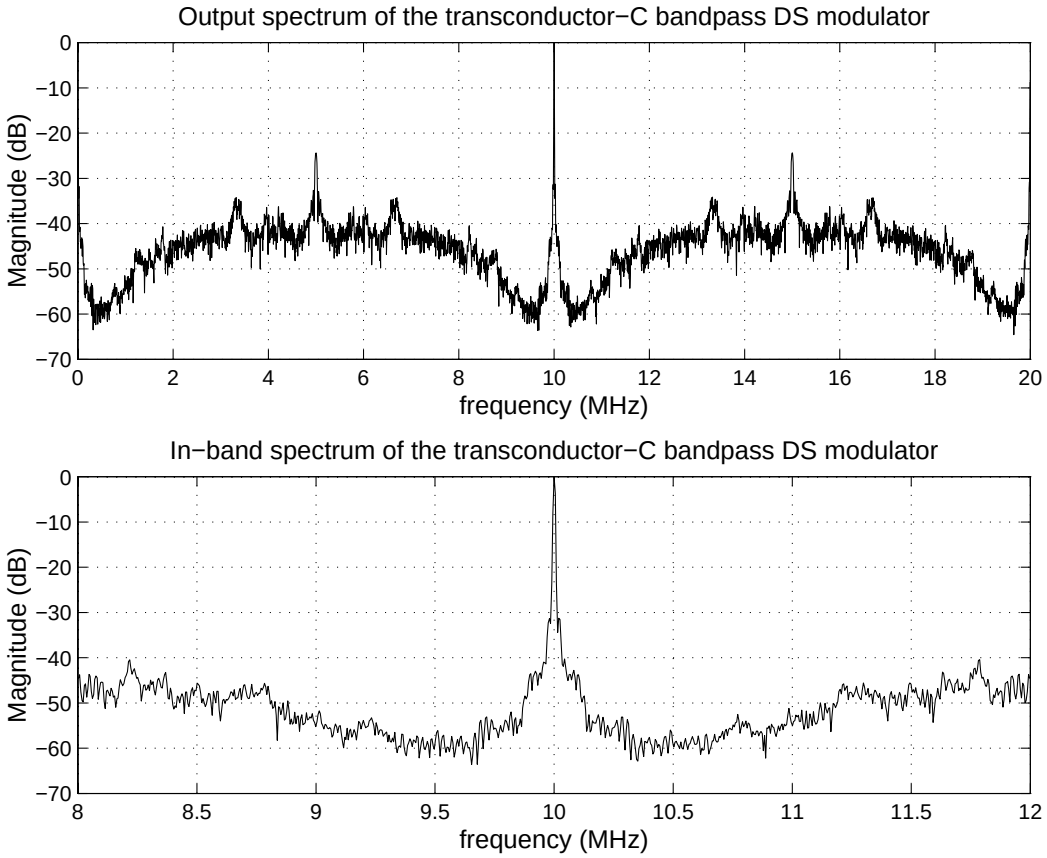


Figure 8.8 : A bandpass noise-shaping spectrum of the fourth-order ZA14 chip at 10MHz.

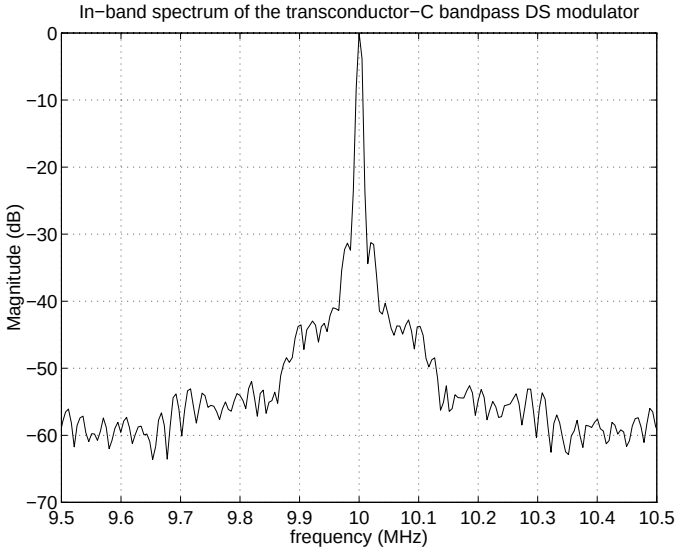


Figure 8.9 : In-band region of the spectrum shown in Fig. 8.8.

8.3 Problems in ZA09 and ZA14 Parts

This section summarizes an extensive investigation done on the problems observed in the implemented chips. At the same time suggestions and conclusions have been inferred for the transconductor-C $\Delta\Sigma$ implementations in the future.

8.3.1 Low-Q at Working Speed

In Sec. 8.1.3 and Sec. 8.2.2 it was mentioned that the Q of the loop filters at 25MHz (ZA09) and 10MHz (ZA09) were 4 and 2.5 respectively. This low Q, of course, can not provide a deep noise-shaping spectrum. Besides from the simulations given in Sec. 5.3 the *SNR* loss would be significant. Furthermore, the tonal behavior in the $\Delta\Sigma$ spectrum becomes inevitable as can be observed from Fig. 8.6 and Fig. 8.8. This was verified by simulations in Sec. 5.3 too. Much higher Q was achieved at higher frequencies, for example, Fig. 8.4 shows a biquad filter in ZA09 with Q of 170 at 50MHz. Basically in both parts it was noticed that higher Q could be obtained at higher frequencies. However, as will be explained in the following sections because of some other difficulties such as the loop propagation delay times, common-mode feedback problem, etc. the $\Delta\Sigma$ parts couldn't operate at frequencies higher than 25MHz.

8.3.2 High Loop Propagation Delay Time

In Sec. 5.5.2.3 it was explained that the overall loop delay including that of comparator, D-flip flop and DAC was about 800ps. There are some other delays due to the parasitic elements of the metal interconnections too. In the layouts of ZA09 and ZA14 there are two main sources of delays in interconnects. An extra delay comes from the interconnects between the output of DAC and the loop filter connections, the metal length between DAC and the loop filter is 1200µ (1000 square) with about a 100Ω distributed resistor which produces a 50 ps delay for charging the filter's input capacitive load. It should be mentioned that the total single-ended input capacitance of the loop filter was about 0.4 pF. Another source of extra loop delay is the metal interconnections within the loop filter *i.e.* connections between op-amps and transconductors. The

interconnections inside the loop filter can be modeled with three simple RC circuit in series as shown in Fig. 8.10 where *R,* the metal resistance, is about 100Ω and *C*, the input capacitances of the transconductors inside the resonator loops, is about 0.3 pF. The propagation delay time due to this interconnection parasitic elements is about 150 ps. Therefore in total the extra loop delay of this chip can increase to 1ns from the 800ps observed in full circuit simulations.

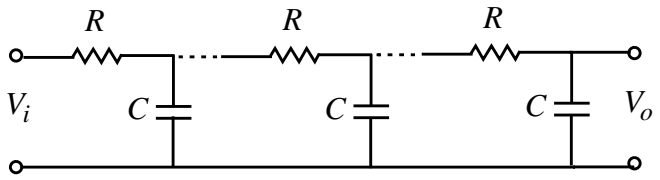


Figure 8.10 : A simple lumped RC model for interconnect parasitic elements inside the loop filter.

In Sec. 3.1.6 it was shown that a fourth-order multiple-pole modulator became unstable for approximately a 20 % extra loop delay. However, a modulator on the verge of instability or even with the loop poles close to the unit circle as shown in Fig. 3.17 can not be considered as a reliable modulator. A robust proof is not presented to set a safe upper extra loop delay limit for a $\Delta\Sigma$ modulator here. However, for each modulator extensive simulations should be performed which along with the modulator's pole-zero map on the z-plane provide a good understanding of the modulator's behavior with extra loop delays. Besides, it should be noted that, as explained in Sec. 2.3.3, due to the comparator's step nonlinearity the loop gain is not a simple linear constant. So, even with no extra loop delay the $\Delta\Sigma$ loop poles as shown back in Fig. 2.9 and Fig. 2.10 are not quite fixed and move on a certain trajectory in normal $\Delta\Sigma$ operation. This means that in practice extra caution should be taken for setting an upper limit for the extra loop delay. Moreover, even neglecting the essence of nonlinear operation of a $\Delta\Sigma$ modulator, one should notice that the *SNR* deteriorates with extra loop delay as presented in Fig. 3.18. For example, from Fig. 3.18 it can be noticed that at 10 % extra loop delay the *SNR* loss (for OSR = 50) is about 6dB. This reduces the usefulness of the modulator for a given order in presence of extra loop delay.

With the preceding observations and the results given in Sec. 3.1.5 and Sec. 3.1.6 the author believes that, for example, in a multiple-pole fourth-order modulator with the

pole-zero map and *SNR* loss plot shown back in Fig. 3.17 and Fig. 3.18 respectively, the maximum tolerable extra loop delay is perhaps not higher than 10 %. For instance, at a 50 MHz center frequency with a 200 MHz clock rate the maximum allowable extra loop delay is 500 ps. In other words, with the mentioned total 1ns propagation delay time in the practical circuit including comparator, D-flip flop, DAC and interconnection parasitic elements the maximum clock speed is 100 MHz. This is the maximum clock rate achieved in ZA09. Considering a 10 % extra loop delay as a maximum limit might be argued to be a bit conservative since firstly in Sec. 3.1.6 it was shown that the fourth-order bandpass modulator was stable up to a 20 % extra loop delay, secondly in Sec. 5.5.3 it was shown that the full circuit simulation showed good results at 200MHz clock rate even with 800 ps propagation delay time *i.e.* 16% extra loop delay. The answer is that the 10 % extra loop delay for the multiple-pole fourth-order modulator was suggested for a good reliability, besides a 10% extra loop delay doesn't degenerate the modulator's *SNR* too much (5dB loss as shown in Fig. 3.18). Regarding the reliability in a $\Delta\Sigma$ modulator it is discussed [Risb94] that in some high-order modulators or a modulator with a chaotic behavior the unstable characteristic of the modulator may be discovered only with very long simulations. It is known that an ideal fourth-order bandpass modulator is behaving like its second-order lowpass counterpart which is proved to be reliable. However, with extra loop delays which cause the modulator's poles to move near the unit circle and even may increase the order of noise transfer function as was shown in Fig. 3.17 and (3.51), the reliability of the modulator can be questioned.

Apart from the 10% extra loop delay suggestion, the question for ZA09 and ZA14 parts still remains why the modulators didn't work at higher clock rates than 100MHz. This might be related to the common-mode problem in the first stage transconductors too which is explained in the next section.

8.3.3 Common-Mode Problem in the First Stage Transconductors

In Sec. 5.4.2 it was mentioned that no individual common-mode feedback was implemented for the first stage transconductors. A strong common-mode feedback shown back in Fig. 5.11 keeps the output voltage of the op-amps and therefore the input

voltage of the transconductors fixed at analog ground. However, the inter-stage (the transconductors' outputs or the op-amps' inputs) common-mode voltages are defined by the output impedance of the transconductor which can vary for example by fabrication tolerances and mismatching between load and bias (or current mirror) devices. Besides, the transconductors' output common-mode voltages are disturbed by any glitch in the feedback high-speed DAC pulses supplied to the transconductors' inputs which in turn may change the transconductors' output common-mode voltages when no common-mode feedback exists for the transconductors. This could force the input bipolar devices of the second stage amplifiers shown back in Fig. 5.11 into saturation if the inter-stage voltages raise from a certain level, for example 2.4 V with a $1V_{p\text{-}p}$ output voltage swing assumption for the second stage amplifier. It should be noted that the output common-mode voltage of the first stage circuit in ZA09 and ZA14 parts (without introducing any mismatching condition) was biased at 2.0 V.

In order to investigate the effect of the common-mode inter-stage voltage drifts the width (W) of the main output PMOS active load devices have been increased compared to those of the current mirror devices. This is just a way to simplify the simulation of the common-mode voltage drift which in practice can originate from many other sources associated with fabrication tolerances and any device parameter mismatching such as threshold voltage V_T and drain-source saturation current I_{ds}. For the 5V cross-coupled design with the parameters given in the first row in Table 7.2 and the schematic shown in Fig. 8.11, for example, the widths of M_3-M_6 have been increased compared to those of M_{13}-M_{15}. The ΔΣ simulations showed that the maximum tolerable mismatch between the active load and the current mirror PMOS device sizes to keep the modulator stable at the maximum input level (MSA) and still produce a good noise-shaping is only 0.1 %. It should be mentioned that with the 0.1% mismatching the *SNR* loss for the 5V cross-coupled design, for instance at a 1MHz bandwidth with a 200MHz clock was 6dB. With 0.2 % width mismatching the noise-shaping performance deteriorates significantly and many undesired tones appear inside the band. Simulation showed that with the mentioned 0.2 % mismatch the transconductor's output CM voltages rise almost by 0.28 from 1.97 V and 2.13 V to 2.25 V and 2.41 V in the first and the second biquads respectively. As mentioned this biases the second stage amplifiers into saturation region

and so produces a large amount of distortion. Recall from Sec. 5.4.5 that since a second stage amplifier has a very high gain $\sim 60\,\text{dB}$ the inter-stage differential signal swing is in order of $1 \sim 2\,\text{mV}$. So, a distortion in the first stage transconductor could only come form a common-mode voltage drift and not a large differential swing. Fig. 8.12 shows the poor noise-shaping spectrum of the simulated modulator with a $0.2\,\%$ width mismatching in the PMOS devices.

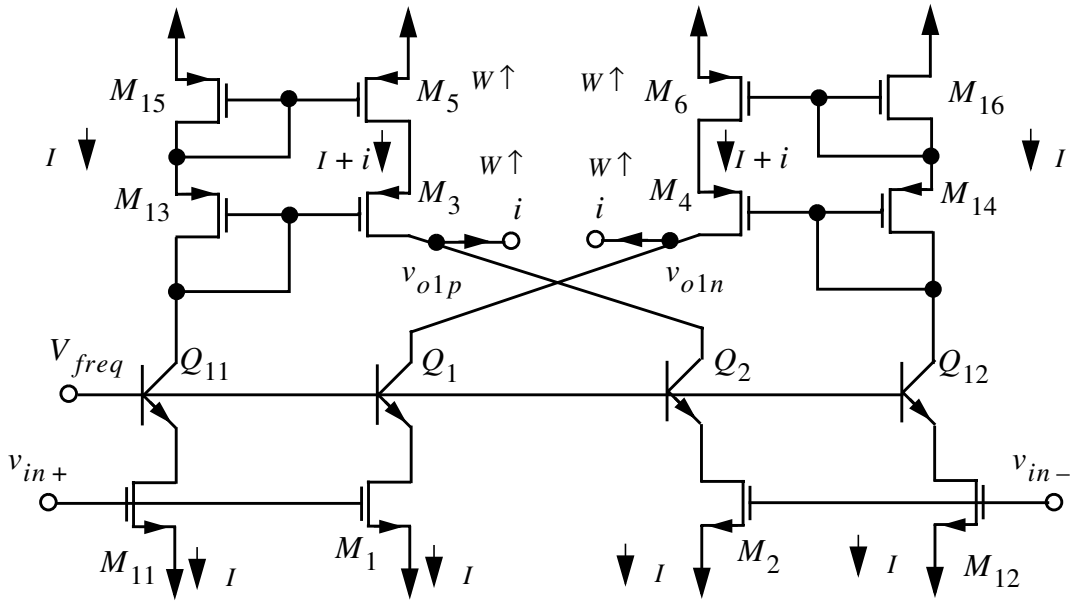


Figure 8.11 : Simulating a CM voltage drift by changing of load device widths.

The same simulations have been performed to test the inter-stage CM voltage drifts in the 3V design presented in Sec. 7.2 with the transconductor schematic shown in Fig. 7.3 and the parameters given in the third row of Table 7.2. Recall that the NMOS transistors M_5-M_8 shown in Fig. 7.3 are the common-mode feedback devices for the first stage transconductor. It was observed that even with $20\,\%$ mismatching between PMOS bias and active load devices the modulator was still stable. Of course, since with a mismatch the Q of the loop filter may be slightly reduced the noise-shaping spectra can be slightly degraded too. For example, with $20\,\%$ mismatching the *SNR* at 1MHz bandwidth was about $10\,\text{dB}$ lower (from $59\,\text{dB}$ as given in the third row of Table 7.2 to $49.3\,\text{dB}$). However, this can be resolved with tuning of the Q. Fig. 8.13 shows the simulated spectrum of the new modulator with $10\,\%$ mismatching between PMOS bias and active load devices. As can be noticed from Fig. 8.13 the noise-shaping spectra for $10\,\%$

mismatching is still very satisfactory. The *SNR* for 1MHz bandwidth has just dropped by 1.5 dB (from 59 dB to 57.5 dB).

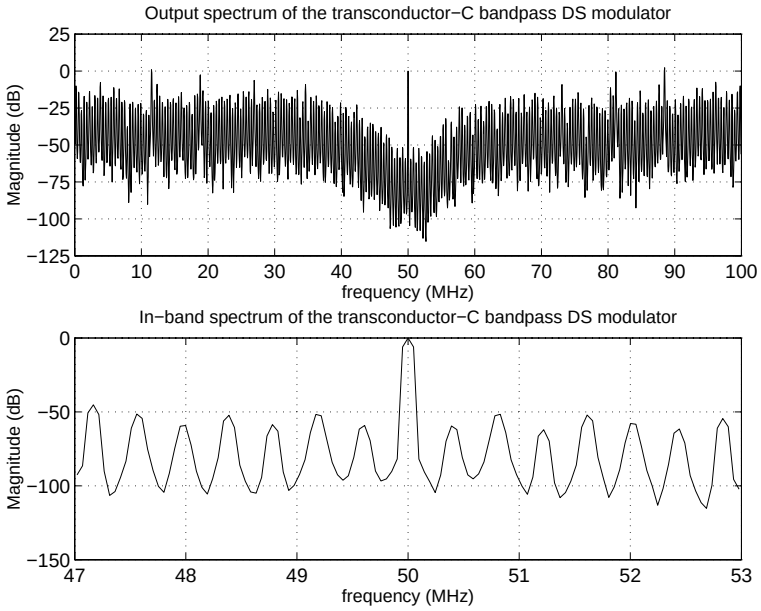


Figure 8.12 : The simulated spectrum of the ZA09 / ZA14 fourth-order modulators with 0.2% mismatching between PMOS current mirror and active load devices.

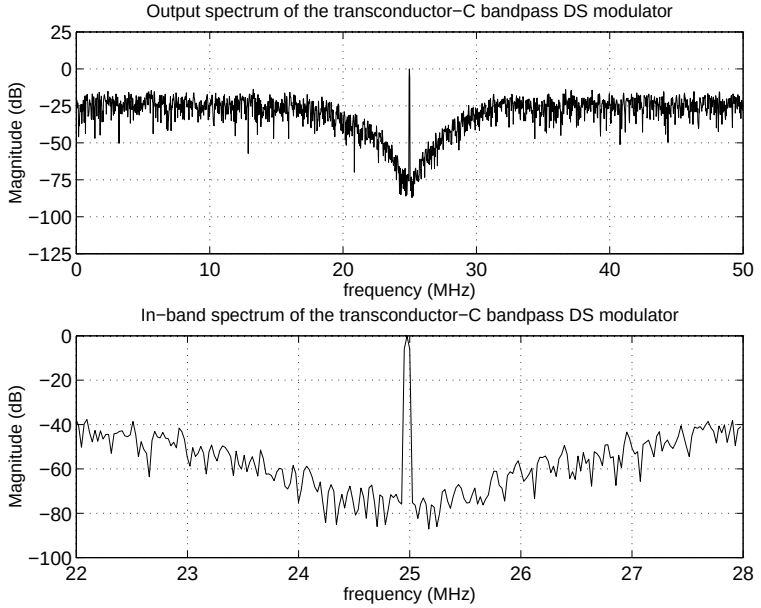


Figure 8.13 : The simulated spectrum of the new 3V fourth-order modulator with 5% mismatching between PMOS bias and active load devices.

8.4 Clock Jitter Effects

For conventional analog-to-digital converters usually the peak timing error Δt is limited by $(2^{-N}/\pi)T$ or

$$\frac{\Delta t}{T} = \frac{2^{-N}}{\pi} \tag{7.1}$$

where N is the ADC resolution and T is the clock rate. It should be noted that (7.1) is derived for a Nyquist-rate converter. It can be easily shown that for an oversampling $\Delta\Sigma$ modulator the permitted peak timing error can be increased by the ratio of the sampling rate to twice the maximum input signal frequency R. For example, for a bandpass $\Delta\Sigma$ modulator with $R = 2$ (clocking four times faster than the input frequency) one can find that roughly a maximum 3ps clock jitter can be allowed for a 200 MHz clock rate in order to achieve a 10 bit converter. This is believed to be very conservative and restrictive for oversampling switched-*C* converters [Snel]. In this section the effect of the clock jitter on a continuous-time modulator is studied.

In Sec. 3.1.5 the effects of the extra loop delay on a continuous-time modulator were analytically studied and demonstrated by simulation as well. From that discussion it can be generally deduced that any change in a feedback DAC pulse waveform including straight delay, a trapezoidal waveform as opposed to the rectangular (which comes from finite rise and fall transition times), glitches due to high speed effects, and finally a clock timing error (jitter) would change the overall loop impulse response and therefore the modulator's noise-shaping spectrum. Unlike a continuous-time modulator, in a switched-*C* modulator the clock jitter only produces errors in the sampling moments of the input signal. This is because the feedback signal only depends on the final settled voltage of the op-amps and not on the feedback pulse waveforms during the entire clock cycle. So, a small clock jitter doesn't change the final settled voltage of the op-amps associated with the feedback values.

For the implemented ZA09 / ZA14 fourth-order transconductor-*C* modulators many simulations have been performed to study clock jitter effects. Clock sources with random Gaussian distribution jitters and assigned standard deviations σ have been generated in MATLAB and then have been used for ELDO [ANA93] simulations. Of

course, for a clock with a random Gaussian jitter the peak timing error can not exactly be defined but from the jitter standard deviation one can figure out the probability of occurrence of a certain peak timing error (jitter). For example, for a random Gaussian clock with a 1ps standard deviation jitter the probability that the peak jitter be less than 3ps and 1.65 ps are 99.73 and 90.11 % respectively. In the meantime, in order to relate the clock jitter in the time domain with the phase noise in the frequency domain a single tone signal is supplied to an ideal sample-and-hold and a FFT of the output signal has been taken. Fig. 8.14 shows the spectrum of a sample-and-held sinusoidal signal when the input sinusoid is sampled with a random Gaussian clock having 1ps standard deviation. The result was obtained by taking a 2^{14} point FFT of the output waveform. The input sinusoidal frequency was 50 MHz and the clock rate 200 MHz. The phase noise of the output spectrum shown in Fig. 8.14 at 200 KHz offset frequency from the

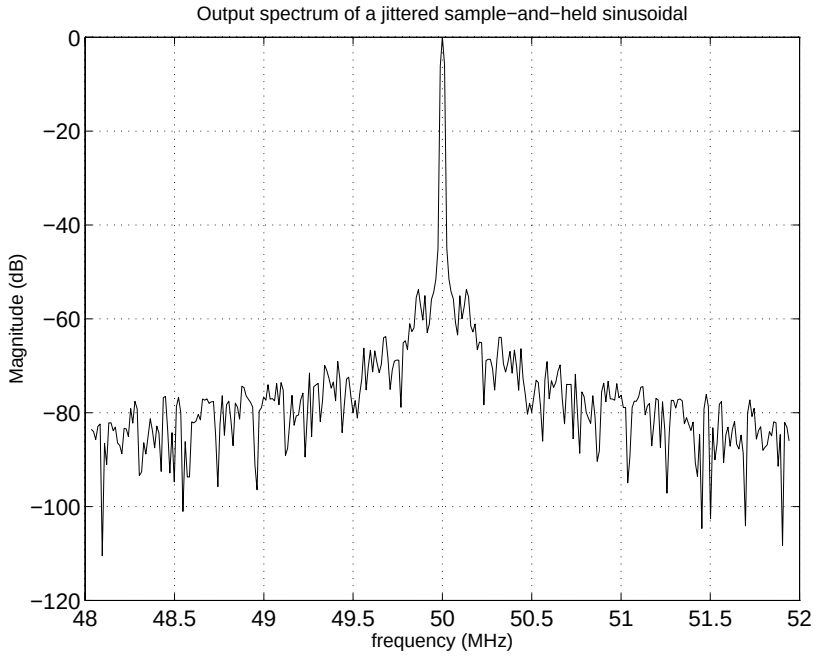


Figure 8.14 : Spectrum of a sinusoidal signal after passing through a sample-and-hold which is clocked with a random Gaussian clock; jitter standard deviation = 1ps.

50MHz carrier is about −102 dBc/Hz which has been calculated as following:

Phase noise = Noise power level @ 200KHz offset relative to the signal level − 10log(FFT resolution bin bandwidth) (7.2)

The same 2^{14} point FFT was taken from the output bit stream of the simulated ZA09 /

ZA14 fourth-order bandpass ΔΣ modulator with the characteristics given in the first row of Table 7.2 when it was clocked with the same random Gaussian pulse (with 1ps standard deviation). The simulated spectrum results with a 1ps standard deviation 200 MHz clock is shown in Fig. 8.15. The phase noise at 200 KHz offset frequency from the carrier was −101 dBc/Hz *i.e.* almost identical to that of the clock. It shows that the effect of the clock jitter appears almost directly at the spectrum of the continuous-time modulator output bit stream. It should be mentioned that the simulated power spectral density of the output bit stream at 200 KHz offset frequency from the carrier in a simulation with no clock jitter was −137 dBc/Hz. The modulator's *SNR* with the clock

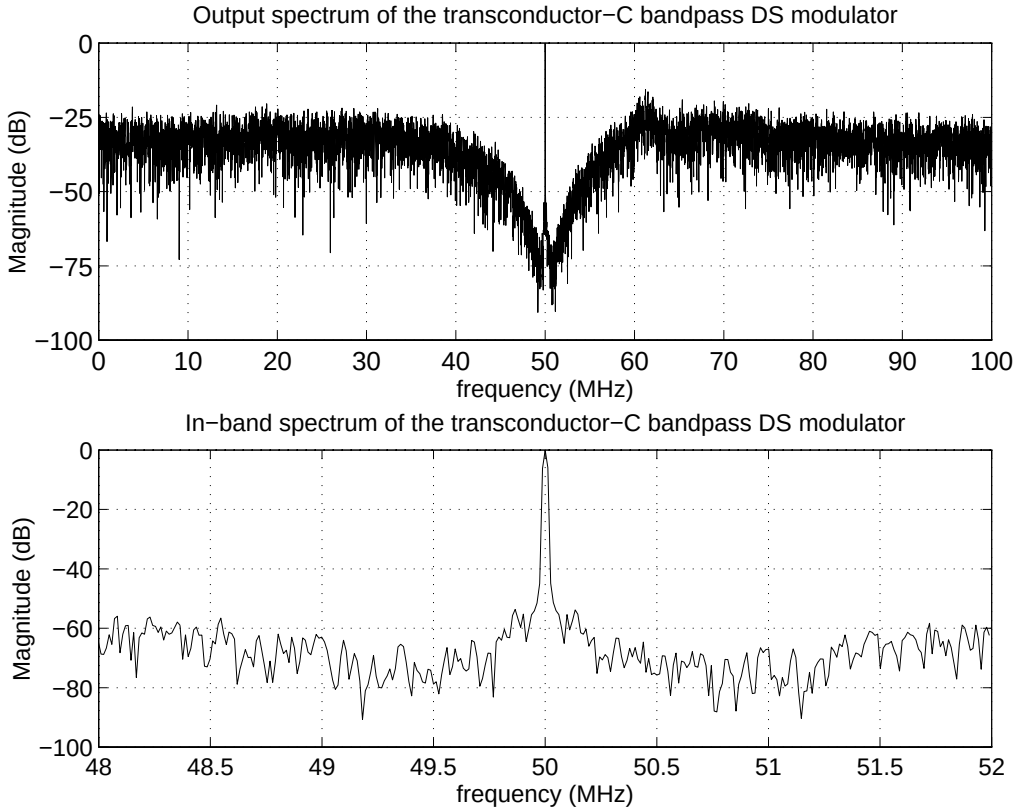


Figure 8.15 : The simulated spectrum of the ZA09 / ZA14 fourth-order modulators clocked with a 200MHz clock having a 1ps standard deviation jitter.

with 1ps jitter standard deviation was reduced from 56 dB to 42 dB *i.e.* a 14 dB loss for a bandwidth of 2MHz. The preceding results along with the results of some other

simulations are summarized in Table 8.3 and Table 8.4. It should be noted that the phase noise figures given in the second columns of Table 8.3 and Table 8.4 have been

Table 8.3: Clock Jitter simulation result summary.

Clock jitter standard deviation	Phase noise of S/H sinusoidal signal (200KHz from carrier)	Noise power spectral density of the bit stream (200KHz from carrier)	*SNR* at 400KHz BW	*SNR* loss due to jitter (2MHz BW)
0ps	−172dBc/Hz*	−137dBc/Hz	75dB	0dB
1ps	−102dBc/Hz	−101dBc/Hz	43dB	32dB
3ps	−92dBc/Hz	−92dBc/Hz	34dB	41dB
5ps	−88dBc/Hz	−88dBc/Hz	29dB	46dB

*. Ideally this values should be $-\infty$ dBc/Hz. The given value shows our FFT accuracy.

Table 8.4: Clock Jitter simulation result summary.

Clock jitter standard deviation	Phase noise of S/H sinusoidal signal (1MHz from carrier)	Noise power spectral density of the bit stream (1MHz from carrier)	*SNR* at 2MHz BW	*SNR* loss due to jitter (2MHz BW)
0ps	−202dBc/Hz*	−113dBc/Hz	56dB	0dB
1ps	−118dBc/Hz	−108dBc/Hz	42dB	14dB
3ps	−107dBc/Hz	−102dBc/Hz	33dB	23dB
5ps	−103dBc/Hz	−105dBc/Hz	28dB	28dB

*. Ideally this values should be $-\infty$ dBc/Hz. The given value shows our FFT accuracy.

calculated from (7.2). The third column figures were obtained similarly too. But the latter doesn't represent the phase noise information directly because at the output $\Delta\Sigma$ bit stream spectrum the phase noise is superimposed on top of shaped quantization noise. However, as can be noticed from Table 8.3 for low bandwidths the output spectral

density of the ΔΣ modulator is almost identical to that of clock jitter. In other words as mentioned, the phase noise property of the sampling clock is almost directly transferred to the spectrum of the continuous-time modulator output bit stream. As shown in Table 8.3 the signal-to-noise ratio of a continuous-time ΔΣ modulator could rapidly be degraded with the sampling clock jitter increment. For example, with a 3ps standard deviation in which the peak timing error is less than 5ps for almost $90\,\%$ of occasions, the fourth-order modulator resolution is dropped by 7 bits to $5\frac{1}{2}$ bits which is a significant loss. By comparison of Table 8.3 and Table 8.4, one can notice that the effect of clock jitter is much more highlighted at high oversampling ratios (lower bandwidths). For example, as shown in the fourth columns of Table 8.3 and Table 8.4 the *SNR*s at $200\,\text{KHz}$ and $2\,\text{MHz}$ bandwidths are almost the same in the presence of clock jitter.
Again as can be noticed from comparison of the second and third columns in Table 8.3, at low bandwidths (200KHz here) the phase noise at the output of a simple sample-and-hold is almost identical to the noise density at the output bit stream spectrum of the continuous-time ΔΣ modulator. Therefore, it can be concluded that clock jitter is no bigger a problem for a transconductor-*C* ΔΣ modulator than for a switched-*C* one. The effect of clock jitter on a ΔΣ modulator *SNR* should be estimated for a given clock jitter in a system in order to test whether the required specifications can be met before any realization.

8.5 Future Work

Many possibilities for future work have been presented in Ch. 7 and in this chapter. These included the methods to design a better transconductor-*C* loop filter for a ΔΣ modulator to improve its noise factor, dynamic-range, linearity, power consumption, reliability and higher frequency operation. It was shown that unfortunately none of the mentioned features in above can be improved without compromising some other one(s). This makes the design of a continuous-time ΔΣ modulator in general and transconductor-*C* modulator in particular very challenging and exciting. More work still needs to be done before a continuous-time modulator can be applied reliably to a system.
The following aspects of research and work in this area can be done to develop the use of

continuous-time techniques such as transconductor-*C* for implementing the analog-to-digital converters for high intermediate frequencies:

1) Simpler structures of transconductor-*C* filters can be considered for a ΔΣ modulator loop filter implementation to improve its frequency capability without trading-off the other features of the modulator.

2) An adaptive tuning for a transconductor-*C* modulator other than the master-slave scheme approach used in Ch. 6 can be studied. This adaptive tuning should be able not only to tune the loop filter's parameters (such as its Q and center frequency) which are altered by fabrication tolerances, etc. but also to compensate for some new difficulties that arise from the new structures such as sensitivity to extra loop delay, etc.

3) A new continuous-time filter transfer function for the practical non-zero extra loop delay modulator can be obtained from the *modified z-transform*. It should be mentioned that the fourth-order modulator was implemented based on the zero excess loop delay assumption. From simulation the actual excess loop delay can be easily estimated from the propagation delay times in the loop components. Recall from Sec. 5.5.2.3 and Sec. 8.3.2 that the extra loop delay for the fabricated chips was about 1ns *i.e.* 20% for 200MHz clock rate. Having known the actual extra loop delay a new continuous-time loop filter can be obtained from the *modified z-transform* such that the resulting entire loop transfer function matches the ideal discrete-time transfer function.

4) The zero-delay scheme can be fabricated. This may reduce the difficulty of extra loop delay since there is no requirement to have any D-flip flop (a full digital delay) in

the loop. With the same comparator and DAC used in ZA09 / ZA14 this means that the loop delay can be reduced by 7% for a 200MHz clock.

5) A more systematic and perhaps automated technique for diagnosis of problems in a fabricated continuous-time modulator can be studied.

6) A 3-level DAC can be used as opposed to single-bit DAC in the continuous-time modulator which can avoid a possible instability in the system caused by non-idealities such as extra loop delay. It should be noted that a 3-level DAC (unlike the multi-level DACs) can be designed to have a desirable linearity.

7) A mixed continuous-time discrete-time (such as transconductor-*C* switched-*C*) modulator may be looked at as a way to benefit from the good features of each type. This may result in better linearity and higher resolution at the cost of speed in a straight transconductor-*C* technique.

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Appendix A: Multiple-pole transformation

I. NZ pulse transformation of a double-pole function.

If we consider

$$H(z) = \frac{a_k}{(z - e^{s_k T})^2} = \frac{a_k}{(z - e^{s_{k1} T})(z - e^{s_{k2} T})} \tag{A-1}$$

where $(s_{k1} \neq s_{k2}) \to s_k$ then:

$$H(z) = \frac{\dfrac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{z - e^{s_{k1} T}} + \frac{\dfrac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{z - e^{s_{k2} T}} \tag{A-2}$$

So from single-pole transformation (3.9)-(3.11):

$$\hat{H}(s) = \left(\frac{-s_{k1}}{1 - e^{s_{k1} T}}\right) \frac{\dfrac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{s - s_{k1}} + \left(\frac{-s_{k2}}{1 - e^{s_{k2} T}}\right) \frac{\dfrac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{s - s_{k2}}$$

$$= \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{(s_{k1} - s_{k2}) + \left(s_{k2} e^{s_{k1} T} - s_{k1} e^{s_{k2} T}\right)}{(e^{s_{k2} T} - e^{s_{k1} T})(1 - e^{s_{k1} T})(1 - e^{s_{k2} T})} s + \frac{s_{k1} s_{k2}}{(1 - e^{s_{k1} T})(1 - e^{s_{k2} T})} \right] \tag{A-3}$$

$$= \frac{a_k}{(s - s_{k1})(s - s_{k2})} [c_1 s + c_0]$$

Obviously if we let $s_{k1}, s_{k2} \to s_k$ there would be a $\frac{0}{0}$ ambiguity at the coefficient of s *i.e.* c_1. However, applying the L'Hôpital's rule on that coefficient

$$\lim_{s_{k1},\, s_{k2} \to s_k} c_1 = \lim_{s_{k1},\, s_{k2} \to s_k} \frac{-1 + e^{s_{k1} T} - s_{k1} T e^{s_{k2} T}}{T e^{s_{k2} T}} = \frac{-e^{s_k T} + (1 - T s_k)}{T} \tag{A-4}$$

Therefore

$$\hat{H}(s) = \frac{\dfrac{(1-e^{-s_k T}-s_k T)}{(1-e^{s_k T})^2}\dfrac{s}{T} + \dfrac{s_k^2}{(1-e^{s_k T})^2}}{(s-s_k)^2} \qquad \text{(A-5)}$$

II. RZ and HZ pulse transformation of a double-pole function.

II-1. RZ:

(*This program provides the RZ transformation for a double-pole discrete-time transfer function in the form of ck/(z-z0)^2 s-domain*)

```
Adouble = ck/((z - Exp[sk1 T])(z - Exp[sk2 T]));
k1 = -ck/(Exp[sk2 T] - Exp[sk1 T]);
k2 = -k1;
z1 = Exp[sk1 T];
z2 = Exp[sk2 T];
(* having known the RTZ transformation for single-pole transfer functions*)
Ah1 = -k1 sk1/((z1^0.5 - z1)(s - sk1));
Ah2 = -k2 sk2/((z2^0.5 - z2)(s - sk2));
Ah = Together[Ah1 + Ah2];
(* Finding Num and Den of Ah *)
Aah = Simplify[Ah (s-sk1)(s-sk2)];
numAh = Numerator[Aah];
denAh = Denominator[Aah];
(* using L'Hôpital's rule*)
numAh1 = D[numAh, {sk1,1}];
denAh1 = D[denAh, {sk1,1}];
LimitnumAh1 = numAh1 /. sk1 -> sk2;
LimitdenAh1 = denAh1 /. sk1 -> sk2;
LimitAh1 = Simplify[LimitnumAh1/(LimitdenAh1 (s - sk2)(s - sk2))];
LimitAh = LimitAh1 /. sk2 -> sk
num = Numerator[LimitAh];
```

```
num = Collect[num, s];
den = Denominator[LimitAh];
b0=Coefficient[num,s,0];
b1=Coefficient[num,s,1];
```

II-2. HZ:

```
(* This program provides the HZ transformation for a double-pole discrete-time transfer
function in the form of ck/(z-z0)^2 s-domain*)

Adouble = ck/((z - Exp[sk1 T])(z - Exp[sk2 T]));
k1 = -ck/(Exp[sk2 T] - Exp[sk1 T]);
k2 = -k1;
z1 = Exp[sk1 T];
z2 = Exp[sk2 T];
(* having known the HZ transformation for single-pole transfer functions *)
Ah1 = -k1 sk1/((1 - z1^0.5)(s - sk1));
Ah2 = -k2 sk2/((1 - z2^0.5)(s - sk2));
Ah = Together[Ah1 + Ah2];
(* Finding Num and Den of Ah *)
Aah = Simplify[Ah (s-sk1)(s-sk2)];
numAh = Numerator[Aah];
denAh = Denominator[Aah];
(* using L'Hôpital's rule*)
numAh1 = D[numAh, {sk1,1}];
denAh1 = D[denAh, {sk1,1}];
LimitnumAh1 = numAh1 /. sk1 -> sk2;
LimitdenAh1 = denAh1 /. sk1 -> sk2;
LimitAh1 = SLimitAh = LimitAh1 /. sk2 -> sk
num = Numerator[LimitAh];
num = Collect[num, s];
den = Denominator[LimitAh];
```

```
b0=Coefficient[num,s,0];
b1=Coefficient[num,s,1];
Simplify[LimitnumAh1/(LimitdenAh1 (s - sk2)(s - sk2))];
```

Appendix B: Signal transfer function

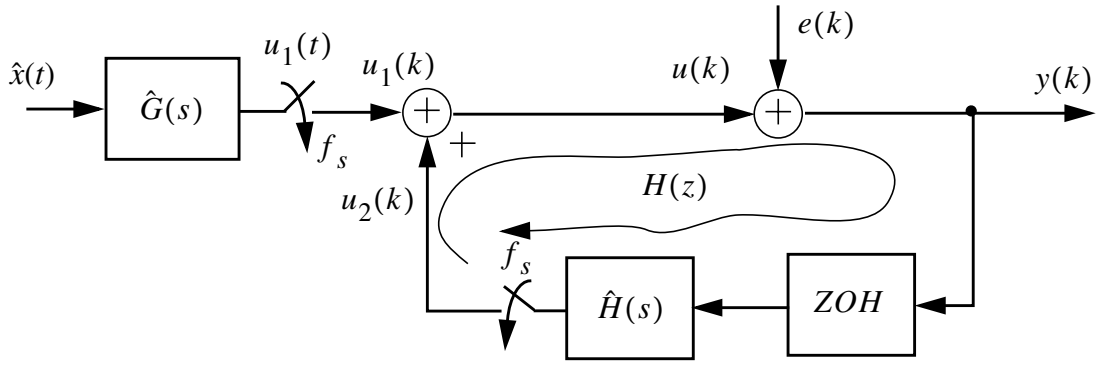

Figure B.1 : Another representation of a continuous-time modulator shown back in Fig. 3.22.

From Fig. B.1 for an ideal sampler $u_1(k) = u_1(t)\big|_{t = kT}$, then from Fourier transform theory the spectrum of the discrete-time signal $U_1(e^{j\omega T}) = F[u_1(k)]$ can be related to the spectrum of the continuous-time signal $U_1(j\omega) = F[u_1(t)]$ []:

$$\begin{aligned} U_1(e^{j\omega T}) &= \sum_{k=0}^{\infty} u_1(kT)e^{-jn\omega T} \\ &= \frac{1}{T}\sum_{k=-\infty}^{\infty} U_1\left(j\omega + j\frac{2\pi k}{T}\right) \end{aligned} \tag{B-1}$$

However, since in practice there is no zero-width sample (usually pulse shape), then in Fig. B.1 $u_1(k)$ should be substituted by $u_1^*(\mathrm{t})$ where,

$$u_1^*(t) = \sum_{k=0}^{\infty} u_1(t)[u(t-kT) - u(t-kT-T)] \tag{B-2}$$

Therefore, from Laplace Transform theory

$$U_1^*(s) = \frac{1-e^{-sT}}{s}\sum_{k=0}^{\infty} u_1(t)e^{-snT} \tag{B-3}$$

and so the sampled signal spectrum would be

$$
\begin{aligned}
U_1^*(j\omega) &= \frac{1-e^{-j\omega T}}{j\omega}\sum_{k=0}^{\infty} u_1(kT)e^{-j\omega nT} \\
&= \frac{1-e^{-j\omega T}}{j\omega T}\sum_{k=-\infty}^{\infty} U_1\left(j\omega + j\frac{2\pi k}{T}\right) \qquad . \qquad \text{(B-4)} \\
&= e^{-j\omega T/2}\cdot\frac{\sin(\omega T/2)}{\omega T/2}\cdot\sum_{k=-\infty}^{\infty} U_1\left(j\omega + j\frac{2\pi k}{T}\right)
\end{aligned}
$$

Note the linear phase factor followed by a "*sinc*" function which comes from the characteristic of the sampled-and-hold signal spectrum.

So the spectrum of the output signal $y(k)$ can be obtained from (B-4) as follows:

$$
Y(e^{j\omega T}) = e^{-j\omega T/2}\cdot\frac{\sin(\omega T/2)}{\omega T/2}\cdot\frac{\sum_{k=-\infty}^{\infty}\hat{X}\left(j\omega + j\frac{2\pi k}{T}\right)\cdot\hat{G}\left(j\omega + j\frac{2\pi k}{T}\right)}{1-H(e^{j\omega T})} \qquad \text{(B-5)}
$$

As shown in (B-5) the input signal $\hat{x}(t)$ is first filtered by the continuous-time prefilter $\hat{G}(j\omega)$ then the output is sampled which, of course, aliases the spectrum. The aliasing signals which would be folded exactly into the in-band are located at $\imath f_s \pm f_o$ frequencies where f_s is the sampling frequency and f_o the center frequency of $\Delta\Sigma$ modulator. However, since the frequency response of prefilter $\hat{G}(j\omega)$ usually attenuates the signals at these frequency bands, one may neglect the higher replicated spectrum terms in (B-5) and come up to an approximate signal frequency response for a continuous-time modulator:

$$
STF_{c(S/H)}(\omega) = \frac{Y(e^{j\omega T})}{\hat{X}(j\omega)} = e^{-j\omega T/2}\cdot\frac{\sin(\omega T/2)}{\omega T/2}\cdot\frac{\hat{G}(j\omega)}{1-H(e^{j\omega T})} \qquad \text{(B-6)}
$$

where S/H stands for sampled-and-hold. It should be noted that in an equivalent switched-*C* modulator as shown in Fig. 3.21 the sampler is in front of modulator, therefore

$$
X(e^{j\omega T}) = e^{-j\omega T/2}\cdot\frac{\sin(\omega T/2)}{\omega T/2}\cdot\sum_{k=-\infty}^{\infty}\hat{X}\left(j\omega + j\frac{2\pi k}{T}\right). \qquad \text{(B-7)}
$$

Here, again the signal spectrum is aliased after sample-and-hold and then is shaped by

the "*sinc*" function. However, there is no inherent continuous-time prefiltering as in a continuous-time modulator. So, the aliasing signals at $\imath f_s \pm f_o$ frequencies are folded into the in-band without any attenuation and since $\sin(\omega T/2)/(\omega T/2)$ amplitude is almost unity at in-band frequency f_o, the undesired aliasing signals appear in the output spectrum with no loss.

In fact by comparing (B-5) and (B-7) in a continuous-time and discrete-time modulators, it is evident that the "*sinc*" term associated with the pulse-shape sampled signals applies on both systems after aliasing has effected. So, it should not be misinterpreted as an anti-alias filtering in either modulator. For the purpose of comparison of the *STF* in a continuous-time modulator with its discrete-time counterpart, this term is neglected in this work:

$$STF_c(\omega) = \frac{Y(e^{j\omega T})}{\hat{X}(j\omega)} = \frac{\hat{G}(j\omega)}{1-H(e^{j\omega T})} . \qquad \text{(B-8)}$$

Appendix C: The TC-amp circuit small signal analysis

C.1 Second-Order Amplifier

A simplified small signal model for the second stage amplifier of the TC-amp integrator is shown in Fig. C.1. First ignoring collector-base capacitance C_μ and assuming $R_z = 0$ one can write the nodal equations:

$$\boldsymbol{A} \cdot \boldsymbol{v} = \boldsymbol{i}$$

$$\boldsymbol{A} = \begin{bmatrix} s(C_\pi + C_m) + g_\pi & -sC_m \\ -sC_m + g_m & s(C_m + C_o) + g_o \end{bmatrix} \qquad \text{(C-1)}$$

$$\boldsymbol{v} = \begin{bmatrix} V_1 & V_o \end{bmatrix}, \qquad \boldsymbol{i} = \begin{bmatrix} I & 0 \end{bmatrix}$$

where the poles can be found from the determinant of $\boldsymbol{A}$ *i.e.*

$$\Delta(s) = s^2 C_m C_\pi \left(1 + \frac{C_o}{C_\pi} + \frac{C_o}{C_m}\right) + sC_m \left[g_m + g_\pi \left(1 + \frac{C_o}{C_m}\right) + g_o \left(1 + \frac{C_\pi}{C_m}\right)\right] + g_o g_\pi$$

With $g_\pi \gg g_o$ approximation

$$\frac{V_o}{I} = \frac{sC_m - g_m}{C_m C_\pi \left(1 + \frac{C_o}{C_\pi} + \frac{C_o}{C_m}\right)(s - p_1)(s - p_2)} \qquad \text{(C-2)}$$

and the zero and the poles are at

$$z_1 = \frac{g_m}{C_m}$$

$$p_1 = -\frac{g_o \cdot g_\pi}{C_m\left(g_m + g_\pi\left(1 + \frac{C_o}{C_m}\right)\right)} = -\frac{(go \cdot g\pi)/\left(C_m C_\pi\left(1 + \frac{C_o}{C_\pi} + \frac{C_o}{C_m}\right)\right)}{|p_2|} \qquad \text{(C-3)}$$

$$p_2 = -\frac{g_m + g_\pi\left(1 + \frac{C_o}{C_m}\right)}{C_\pi\left(1 + \frac{C_o}{C_\pi} + \frac{C_o}{C_m}\right)}$$

The numerical values of the parameters in the foregoing equations obtained from HSPICE simulations of a realized BiCMOS TC-amp integrator are as following:

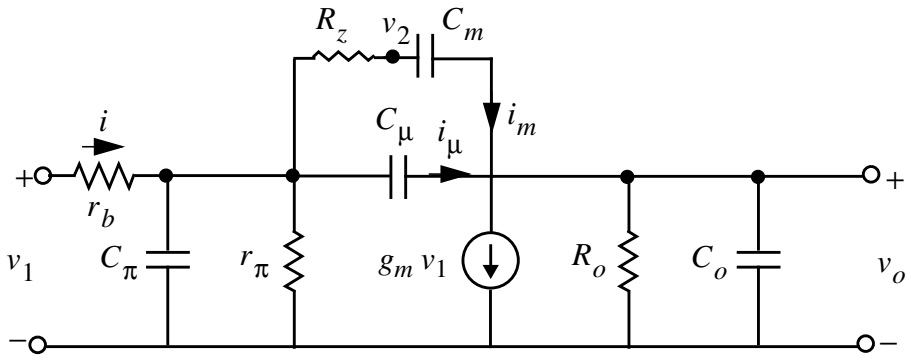

Figure C.1 : Simplified small signal model of the Miller stage in Fig. 5.17.

g_m: The transconductance of the second stage bipolar transistor. For a collector current of 400μA, g_m = 15.06 mS.

r_π: Base-emitter resistance of BJT transistor, $r_\pi = 5355\Omega$.

C_μ: Collector-Base capacitance of BJT transistor, C_μ = 9.34fF.

C_π: The BJT's C_π, C_π = 0.21pF.

R_o: The output resistance of the second stage. Parallel of the output resistance of the BJT and PMOS cascode active load, R_o = 52KΩ.

C_o: The loading capacitance of the second stage. Primarily determined by the input capacitance of the next stage transconductor, C_o = 0.506pF.

C_m: The Miller capacitance, $C_m = 0.8pF$.

R_z: The Miller resistance at the maximum Q, R_z = 776.2 Ω.

The open loop amplifier frequency response *i.e.* when $R_z \rightarrow \infty$ (no external Miller feedback) can easily be obtained by substituting C_m with C_μ in (C-3). The Poles and RHP zero with no Miller capacitance are

$$p_1 = -2.41 \text{ MHz}, p_2 = -331.5 \text{ MHz and } z_1 = +258.0 \text{ GHz}. \quad \text{(C-4)}$$

and with Miller capacitance are when $R_z = 0$

$$p_1 = -46.48 \text{ KHz}, p_2 = -2.86 \text{ GHz and } z_1 = +3.0 \text{ GHz}. \quad \text{(C-5)}$$

As these numerical values show the effect the Miller capacitance C_m is to reduce p_1 significantly (producing a dominant pole) and to increase p_2. Hence, the Miller capacitor is sometimes called a pole-splitting capacitor [], [] too. As will be shown p_1 is the entire TC-amp dominant pole which can be expressed in terms of the input transconductance and the overall TC-amp DC gain parameters. Assuming $g_\pi \gg g_o$ and $C_m \geq C_o$ from (3) one can show

$$p_1 = -\frac{g_o \cdot g_\pi}{g_m C_m}. \quad \text{(C-6)}$$

The differential DC gain of the TC-amp shown in Fig. 5.17 is equal to

$$A_{dc} = \frac{v_{o+}}{v_{i-}} = \frac{v_{o+} - v_{o-}}{v_{i+} - v_{i-}} = (g_{m1} \cdot R_{o1}) \cdot (g_m R_o) \approx (g_{m1} \cdot r_\pi) \cdot \left(g_m \cdot \frac{1}{g_o}\right) \quad \text{(C-7)}$$

where $g_{m1} = i/v_i$ is the input stage transconductance[1] in Fig. 5.17 and R_{o1} the output impedance of the first stage including the effect of the input impedance of the second stage amplifier. The latter is approximated with r_π of the second stage amplifier. Recall

1. Since the input NMOS transistors are working in the triode regime and usually the small signal parameters given in the HSPICE output file are not calculated very accurately for these devices, the g_{m1} was directly measured from simulation.

from Sec. 5.1.1 that the differential transconductance is defined as $G_m = i/(v_{i+} - v_{i-}) = g_{m1}/2$. So from (C-6) and (C-7) it is straight forward to show that

$$p_1 = \frac{g_{m1}}{A_{dc}C_m} = \frac{2G_m}{A_{dc}C_m} \tag{C-8}$$

It should be noted because of the cross coupling in the transconductor shown in Fig. 5.10 the total differential transconductor and DC gain of the entire cross-coupled circuit represented by G'_m and A'_{dc} are twice as large as G_m and A_{dc} respectively. So one may write the dominant pole versus the cross-coupled parameters

$$p1 = \frac{2G'_m}{A'_{dc}C_m} = \frac{\omega_o}{A'_{dc}} \tag{C-9}$$

This is what was explained earlier as an important feature of a TC-amp which produces a very dominant pole due to its high DC gain. For example, for the simulated TC-amp with a differential DC gain of 66.3 dB and unity-gain frequency 85.41 MHz it turns out that $p_1 = 41.35$ KHz which is close to the result given in (C-5).

As mentioned a high DC gain with a low frequency dominant pole provides an almost flat –90° phase and a –20 dB/decade gain frequency response in a very wide frequency range as shown in Fig. 5.15. However, the second pole p_2 (at –2.86 GHz) in (C-5) produces another –90° phase shift and the RHP zero z_1 (at +3.0 GHz) in (C-5) contributes more in the integrator phase lead which deteriorates the integrator performance at the desired high frequencies further.

C.2 Effect of Miller Resistor (RHP zero to LHP)

It is well known that a resistor in series with Miller capacitance moves the RHP zero to the LHP, and can be used to overcome the excess phase produced by the second pole p_2 []. Taking into account C_μ and R_z effects shown in Fig. C.1. The $\boldsymbol{A}$, $\boldsymbol{v}$ and $\boldsymbol{i}$ in (C-1) become

$$\boldsymbol{A} = \begin{bmatrix} s(C_\pi + C_m) + g_\pi + g_z & -g_z & -sC_\mu \\ -g_z & g_z + sC_m & -sC_m \\ -sC_\mu g_m & -sC_m & s(C_m + C_o + C_\mu) + g_o \end{bmatrix} \tag{C-10}$$

$$\boldsymbol{v} = \begin{bmatrix} V_1 & V_2 & V_o \end{bmatrix}, \qquad \boldsymbol{i} = \begin{bmatrix} I & 0 & 0 \end{bmatrix}$$

This is a third order system producing three poles and two zeros. The transmission zeros can be found by applying Cramer's rule to (C-10) or by inspection from Fig. C.1. We find

$$I_m + I_\mu = g_m \cdot V_1 \Rightarrow V_1\left(sC_\mu + \frac{1}{R_z + 1/(sC_m)}\right) = g_m \cdot V_1$$

which implies

$$s^2 + \frac{1 + C_\mu C_m - g_m R_z}{R_z C_\mu} s - \frac{g_m}{R_z C_m C_\mu} = 0 \tag{C-11}$$

From (C-11) it can be shown that

$$\begin{aligned} z_1 &= -\frac{g_m}{C_m(g_m R_z - (1 + C_\mu / C_m))} \\ z_2 &= \frac{g_m R_z - (1 + C_\mu / C_m)}{R_z C_\mu} \end{aligned} \tag{C-12}$$

where one can calculate the numerical values for the zeros of TC-amp integrator:

$z_1 = -280.6$ MHz and $z_2 = +235.0$ GHz.

Both zeros are real where one is in the LHP another in the RHP. However, the effect of the very high frequency RHP zero is negligible. The effect of R_z on a TC-amp integrator is then creating a new LHP zero and moving the RHP zero from its previous location (C-5) to a much higher RHP frequency (recall that without R_z the RHP zero was at +3.0 GHz). Therefore, one may simply say that the Miller resistor moves the RHP zero (having just a Miller capacitance) to the LHP, as mentioned in this section's title.

This way one may exploit the new LHP zero phase lead to adjust the required phase

characteristic of a TC-amp integrator to produce a desired Q performance for a resonator.

Another effect of R_z as shown in (C-10) is increasing the order of system, creating a third pole. For low values of R_z, (C-5) can still be used for the first and second poles and the third pole can be approximated by a high frequency LHP real pole at

$$p_3 = -\frac{1}{R_z}\left(\frac{1}{C_m}+\frac{1}{C_\pi}+\frac{1}{C_o}\right). \tag{C-13}$$

The root locus of the this system (the second stage Miller amplifier) with respect to R_z variation is shown in Fig. C.2. Two poles of the amplifier without the Miller capacitor

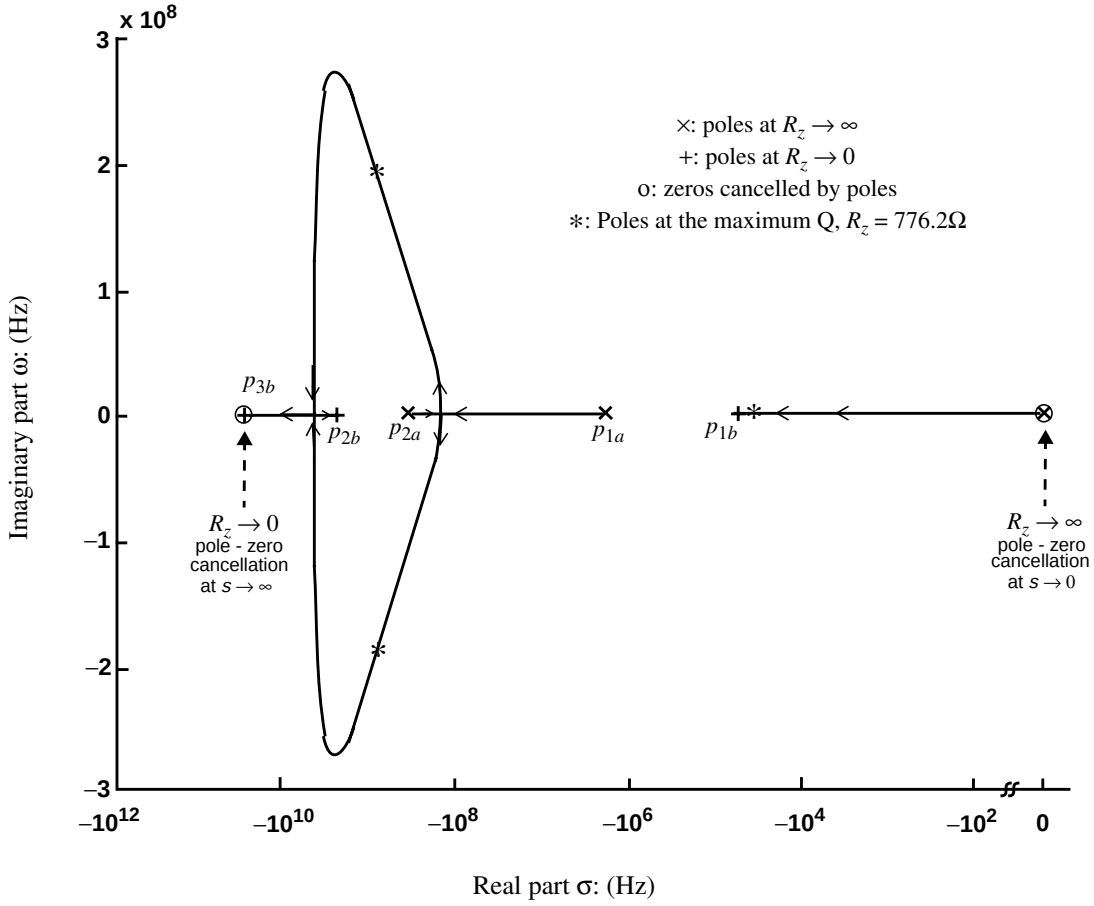

Figure C.2 : Root locus of the second stage amplifier with respect to R_z variation.

($R_z = \infty$) are shown by p_{1a} and p_{2a} respectively represented by "×" in Fig. C.2. The root locus shown in Fig. C.2 is obtained from the solution of the third-order system given in (C-10) for finite R_z values. The equations (C-1) and (C-3) demonstrate a second-order system for $R_z = \infty$ which is a special case of the third-order system.

At $R_z = \infty$ ($g_z = 0$) as shown in Fig. C.2 the equation (C-10) results in a pole at DC ($s = 0$) which is cancelled out by a zero at $s = 0$. From (C-12) it can be observed that at $R_z = \infty$, z_1 would be zero. This pole-zero cancellation in the third-order equation (C-10) refers to the second-order response with no Miller capacitor case given in (C-1) when C_m is replaced by C_μ.

As R_z decreases from some high finite values the real pole moves from $s = 0$ towards some negative real LHP pole represented by p_{1b} (for $R_z = 0$). At the same time the real poles represented by p_{1a} and p_{2a} first merge at some point in the real axis then depart to a complex conjugate pair on the trajectory shown in Fig. C.2. Finally they approach real poles represented by p_{2b} and p_{3b} at $R_z = 0$. Again it should be noted that at $R_z = 0$ the third pole given in (C-13) and the zero shown by z_2 in (C-12) both would be infinity at LHP. This indicates another pole-zero cancellation when $R_z \to 0$ which is shown in Fig. C.2 too. Therefore there are only two poles at $R_z = 0$ obtained from (C-3) and calculated in (C-5) represented by p_{1b} and p_{2b} in Fig. C.2. It should be noted that the three poles for the maximum Q ($R_z = 776.2\Omega$ shown in Fig. 5.14) are represented by '∗' in Fig. C.2.

The zero locus of the second stage circuit respect to R_z variation is shown in Fig. C.3. As shown in the figure the second stage zeros are always real. At two limits *i.e.* $R_z \to \infty$ and $R_z \to 0$ as shown in Fig. C.2 and Fig. C.3 there are pole-zero cancellation at $s \to 0$ and $s \to -\infty$ respectively which leaves the second stage with one zero: g_m/C_μ at $R_z = \infty$ and $g_m/(C_m + C_\mu)$ at $R_z = 0$. As R_z decreases from infinity the LHP zero moves from $s = 0$ towards $-\infty$ and the RHP zero moves from g_m/C_μ to a final destination $g_m/(C_m + C_\mu)$ when $R_z = 0$. The two zeros for the maximum Q ($R_z = 776.2\Omega$ shown in Fig. 5.14) are represented by 'z∗' in Fig. C.3. As shown the RHP zero (RHP z∗) has not moved too much from its initial place (258 GHz → 235 GHz) while the LHP zero (LHP z∗) has made a significant move from origin to −280.6 MHz. As will be shown shortly this is the major effect of R_z for the excess phase adjustment in a TC-amp

integrator.

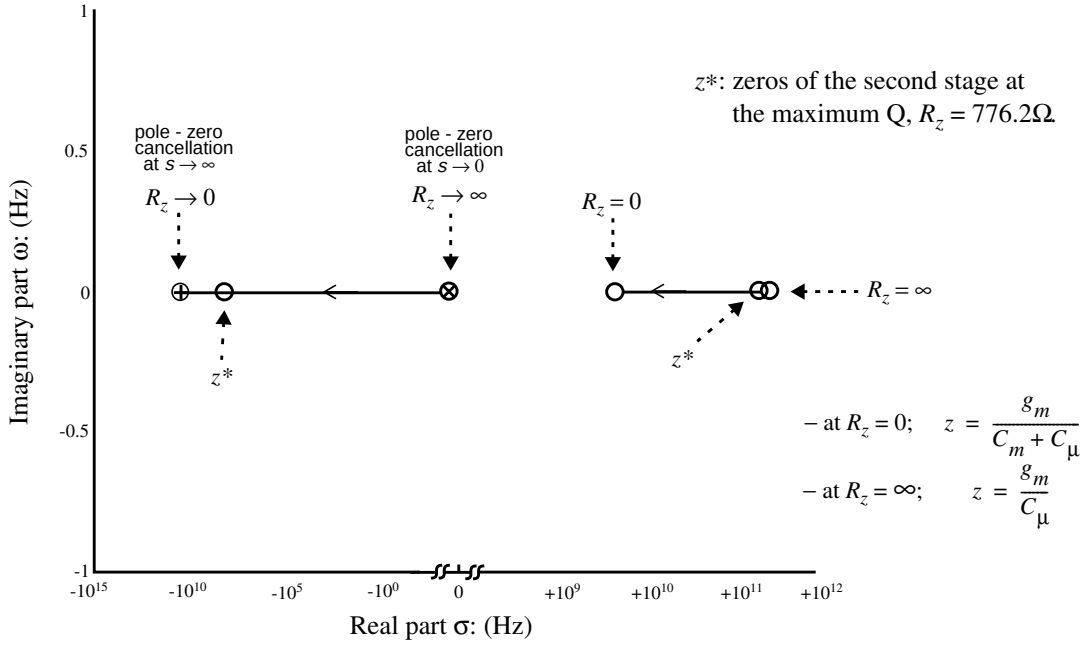

Figure C.3 : Zero locus of the second stage amplifier with respect to R_z variation.

C.3 First Stage Transconductor

So far we have presented a small signal analysis for the second stage amplifier. To get a complete understanding of the high frequency performance of the circuit we need to analyze the first stage transconductor too. A small signal model for the first stage transconductor shown back in Fig. 5.10 and Fig. 5.17 is shown in Fig. C.4. This small signal model shows the input NMOS–BJT cascode stage ignoring the BJT base resistance r_b. The current source $g_{mQ1} \cdot v_{be}$ can be replaced by a resistance $1/g_{mQ1}$ to simplify the circuit further. This resistance combined with the parallel resistance $r_{\pi 1}$ determines the resistance to ground from node "*e*" (in Fig. C.4): $r_{e1} \approx (1/g_{mQ1} \parallel r_{\pi 1}) \ll r_{ds}$.

It can be shown that the small signal transfer function of the first stage transconductor shown in Fig. C.4 is:

$$\frac{V_{o1}}{V_i} = \frac{sC_{gd1} - g_{m1}}{sC_2 + 1/r_{e1}} \tag{C-14}$$

where C_2 is the total capacitance to ground in node "*e*" emitter of the cascode BJT. If the

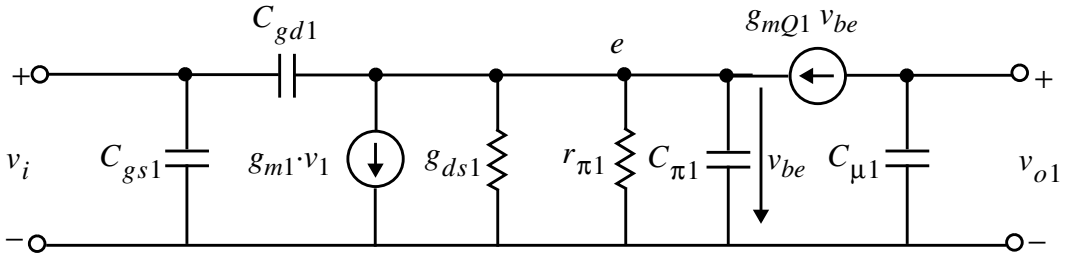

Figure C.4 : Simplified small signal model of the first stage transconductor.

input NMOS transistor gain is defined as $A_{v1} = v_e/v_i$ from Miller's theorem one can obtain that

$$C_2 = C_{\pi 1} + C_{gd1}(1 - 1/A_{v1}) .$$

Therefore the dominant pole and zero of the first stage transconductor are:

$$z_{11} = \frac{g_{m1}}{C_{gd1}}$$
$$p_{11} = -\frac{g_{mQ1} + g_{\pi 1} + g_{ds1}}{C_{\pi 1} + C_{gd1}(1 - 1/A_{v1})} \tag{C-15}$$

The numerical values of the parameters in this model obtained from HSPICE simulations of the realized BiCMOS transconductor are as follows:

g_{mQ1}: The transconductance of the cascode bipolar transistor. For a collector current of 1.58 mA, g_{mQ1} = 56.31 mS.

$r_{\pi 1}$: Base-emitter resistance of BJT cascode transistor, $r_{\pi 1}$ = 1336 Ω.

$C_{\mu 1}$: Collector-Base capacitance of cascode BJT transistor, $C_{\mu 1}$ = 10.6 fF.

$C_{\pi 1}$: The cascode BJT's C_π, C_π = 0.664 pF.

g_{m1}: The transconductance of the input NMOS transistor. For a DC operating point of V_{ds} of 77 mV, g_{m1} = 271.6 µS.

C_{gd1}: The drain to gate feedback capacitance of the input NMOS transistor, C_{gd1} = 71 fF.

C_{gs1}: The input gate capacitance of the input NMOS transistor, C_{gs1} = 72 fF.

g_{ds1}: The NMOS transistor drain to source admittance, g_{ds1} = 10.8 mA/V.

A_{v1}: The voltage gain from the gate of the NMOS transistor to its drain. A_{v1} = –44.5 dB.

From the given numerical parameter values the zero and pole of the first stage transconductor defined in (C-15) would be

$$p_{11} = -\,853.5 \text{ MHz and } z_{11} = +\,608.8 \text{ MHz.} \qquad \text{(C-16)}$$

Appendix D: Discrete-time to continuous-time state space transformation

Recall 3.1.3 that a continuous-time sate space can be expressed as

$$\begin{aligned} u'(t) &= \boldsymbol{A}_c \boldsymbol{u}(t) + \boldsymbol{b}_c \hat{y}(t) \\ \hat{u}(t) &= \boldsymbol{c}_c^T \boldsymbol{u}(t) + d_c \hat{y}(t) \end{aligned} \quad . \tag{D-1}$$

From the linear differential equation theory one can find a solution for (D-1) as the following:

$$\boldsymbol{u}_c(t) = e^{\boldsymbol{A}_c(t-t_0)} \boldsymbol{u}_c(t_0) + \int_{t_0}^{t} e^{\boldsymbol{A}_c(t-\tau)} \boldsymbol{b}_c \hat{y}(\tau) d\tau \tag{D-2}$$

For a RZ hold input

$$\hat{y}(t) = \begin{cases} \hat{y}(nT) & nT \le t < nT + \dfrac{T}{2} \\ 0 & \text{otherwise} \end{cases} . \tag{D-3}$$

Substituting (D-3) into (D-2):

$$\begin{aligned} \boldsymbol{u}_c[(n+1)T] &= e^{\boldsymbol{A}_c T} \boldsymbol{u}_c(nT) + \int_{nT}^{\left(n+\frac{1}{2}\right)T} e^{\boldsymbol{A}_c[(n+1)T-\tau]} \boldsymbol{b}_c \hat{y}(nT) d\tau \\ &= e^{\boldsymbol{A}_c T} \boldsymbol{u}_c(nT) - \boldsymbol{A}_c^{-1} (e^{\boldsymbol{A}_c T/2} - e^{\boldsymbol{A}_c T}) \boldsymbol{b}_c \hat{y}(nT) \end{aligned} \tag{D-4}$$

By comparing (D-4) to the state space equations of the discrete-time equivalent system:

$$\begin{aligned} \boldsymbol{u}_d(n+1) &= \boldsymbol{A}_d \boldsymbol{u}_d(n) + \boldsymbol{b}_d y(t) \\ u(n) &= \boldsymbol{c}_d^T \boldsymbol{u}_d(n) + d_d y(n) \end{aligned} \tag{D-5}$$

quite easily for RZ hold input it can be shown that

$$\begin{aligned} \boldsymbol{A}_d &= \exp(\boldsymbol{A}_c T) & \boldsymbol{A}_c &= \frac{1}{T} \log_e(\boldsymbol{A}_d) \\ \boldsymbol{b}_d &= \boldsymbol{A}_c^{-1} (\boldsymbol{A}_d - \boldsymbol{A}_d^{1/2}) \boldsymbol{b}_c & \boldsymbol{b}_c &= (\boldsymbol{A}_d - \boldsymbol{A}_d^{1/2})^{-1} \boldsymbol{A}_c \boldsymbol{b}_d \end{aligned} \quad , \quad . \tag{D-6}$$