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Continuous-Time Delta-Sigma Modulators for Wireless Communication

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LUND INSTITUTE OF TECHNOLOGY
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To Lisa

Abstract

The ever increasing data rates in wireless communication require analog to digital converters (ADCs) with greater requirements on speed and accuracy, while being power efficient to prolong battery life. This dissertation contains an introduction to the field and five papers that focus on the continuous-time (CT) $\Delta\Sigma$ modulator (DSM) as ADC.

Paper I analyses the performance degradation of dynamic nonlinearity in the feedback DAC of the DSM, caused by V_{th} mismatch in the current-switching (differential) pair of a current-steering DAC. A model is developed to study return-to-zero (RZ) and non-return-to-zero (NRZ) feedback DACs, with and without data-weighted averaging (DWA), where an RZ DAC with DWA recovers the performance.

Paper II and III presents a feedback scheme for improved robustness against variations in loop delay. An RZ pulse, centered in the clock period, is used in the innermost feedback path which has the highest sensitivity to loop delay, while NRZ pulses are adopted in the outer feedback paths to reduce the sensitivity to clock jitter and lower the integrator slew rate requirements. Furthermore, the otherwise obligatory loop delay compensation path (e.g. an additional DAC and adder) could be omitted to reduce hardware complexity. A discrete-time model of the feedback scheme confirms a negligible loss in performance. The 3^{rd}-order CT DSM in 65 nm CMOS with 9 MHz LTE bandwidth achieves 69/71 dB SNDR/SNR and consumes 7.5 mW from a 1.2 V supply. Measurements with OFDM signals verify an improved tolerance to blockers outside the signal band of the DSM.

Paper IV and V present two filtering ADCs, where the DSM is merged into the channel select filter to suppress the noise from the DSM. The first and second prototypes provide a 2^{nd}- and 3^{rd}-order channel select filtering and improve the SNDR of the DSM by 14 dB and 20 dB, respectively, which in theory can be exploited to reduce the DSM power consumption by four to eight times.

The first prototype has a 288 MHz clock frequency, a 9 MHz LTE bandwidth, a 2^{nd}-order Butterworth filter response with 12 dB gain, an input-referred noise of $8.1\,\text{nV}/\sqrt{\text{Hz}}$, an in/out-of-band IIP3 of $11.5/27\,\text{dBV}_{\text{rms}}$, and a power consumption of 11.3 mW. The second prototype is clocked at 576/288 MHz with an 18.5/9 MHz LTE bandwidth, a Chebyshev filter response with 26 dB gain, a low input-referred noise of $5\,\text{nV}/\sqrt{\text{Hz}}$, and an in/out-of-band IIP3 of -8.5/20 dBV_{rms}, with a power consumption of 7.9/5.4 mW for 2xLTE20/LTE20 mode. The prototype was characterized for OFDM modulated blockers and essentially meets the cellular standard LTE Rel. 11. A delay, introduced by the feedback DAC, is compensated by adjusting the filter coefficients to restore the original Chebyshev filter function.

Both prototypes have state-of-the-art power efficiency compared to other filtering ADCs and are comparable or better than a stand-alone filter. Furthermore, the filtering ADC provides both filtering and A/D conversion, which suggests that the A/D conversion is included in a power efficient manner, broadly speaking ”for free”.

Populärvetenskaplig sammanfattning

Trådlös kommunikation mellan olika batteridrivna enheter såsom smarta telefoner, används dagligen i våra liv. Kommunikationen sker ofta via internet med högkvalitativa bilder, filmer och ljud, vilket kräver högre datahastigheter i den trådlösa mottagaren (radiomottagaren). Den högre hastigheten ökar prestandakraven på komponenterna i mottagarkedjan, vilket generellt kräver en högre strömförbrukning. Således är det viktigt att förbättra både prestanda och energieffektivitet i komponenterna, så att de högre datahastigheterna kan nås för en rimlig strömförbrukning.

En begränsande komponent i mottagarkedjan är analog-till-digital omvandlaren (ADC:n), som tar emot den analoga radio signalen och omvandlar den till en digital representation (ettor och nollor) som sedan avkodas i efterföljande block. Den här avhandlingen innehåller fem vetenskapliga artiklar om tekniker som förbättrar en vanligt förekommande typ av ADC i radiomottagare, nämligen delta-sigma modulatorn (DSM). En DSM är ett återkopplat system som i sig internt innehåller både en ADC och flera DAC:ar (digital-till-analog omvandlare). Varje DSM använder i storleksordningen 0.1mm^2 kiselyta vid tillverkning i en så kallad 65 nm CMOS process och förbrukar i storleksordningen 5-10 mW i effekt. De två viktigaste lösningarna som presenteras i avhandlingen beskrivs nedan:

Den första tekniken sänker känsligheten mot fördröjningar internt i DSM, vilket gör den mer robust mot variationer i tillverkningsprocessen och förenklar utvecklingsarbetet. Dessutom är det möjligt att ta bort en av de interna DAC:arna och på så sätt spara ström och yta på chipet. Lösningen använder en annan slags puls i en av DAC:arna och är verifierad med mätningar av ett chip.

Den andra tekniken flyttar analog-till-digital omvandlaren in i ett filter för att skapa en filtrerande ADC. Ett filter används ofta före ADC:n för att sänka prestandakraven på ADC:n och totalt sett ge en lägre effektförbrukning. Fördelen med den filtrerande ADC:n är att kraven på ADC:n blir ännu lägre, vilket möjliggör en sänkning av effektförbrukningen i ADC:n med mer än fyra gånger. Konceptet är verifierat med två tillverkade chip, där det andra chipet stödjer en av de senaste standarderna för mobilkommunikation, "long-term evolution" (LTE) release 11. Den filtrerande ADC:n har lika bra eller bättre energieffektivitet jämfört med andra publicerade filter, vilket indikerar att själva analog-till-digital omvandligen sker effektivt.

Doktorandtjänsten och kiseltillverkningen har finansierats av projekten Design Methods for Radio Architectures GOing Nanoscale (DRAGON), System-design-On-Silicon (SOS) och ST Microeletronics.

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Preface

This dissertation summarizes my academic work for a Ph.D degree in Circuit Design in the Mixed Signal Design group, at the Department of Electrical and Information Technology, Lund University, Sweden. The Ph.D studies took place from February 2009 until March 2014. The dissertation is divided into two parts, where the first part has six chapters that contains an introduction to the research field, followed by an appendix with supplementary results. The second part contains the included research papers, which are listed below.

Included Research Papers

The main contribution is derived from the following publications:

[1] M. Andersson, M. Anderson, P. Andreani, and L. Sundström, "Impact of MOS threshold-voltage mismatch in current-steering DACs for CT ΔΣ modulators," in *Proc. of IEEE International Symposium on Circuits and Systems, ISCAS'10*, Paris, France, May 30–Jun. 2 2010, pp. 4021–4024.

[2] M. Andersson, M. Anderson, L. Sundström, and P. Andreani, "A 7.5 mW 9 MHz CT ΔΣ Modulator in 65 nm CMOS With 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations," in *Proc. of IEEE A-SSCC*, Kobe, Japan, Nov. 12–14 2012, pp. 245–248.

[3] M. Andersson, L. Sundström, M. Anderson, and P. Andreani, "Theory and design of a CT ΔΣ modulator with low sensitivity to loop-delay variations," *Analog Integrated Circuits and Signal Processing*, vol. 76, no. 3, pp. 353–366, Sep. 2013.

[4] M. Andersson, M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A 9MHz Filtering ADC with Additional 2nd-order ΔΣ Modulator Noise Suppression," in *Proc. of 39th IEEE ESSCIRC 2013*, Bucharest, Romania, Sep. 16–20 2013, pp. 323–326.

[5] M. Andersson, M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A Filtering ΔΣ ADC for LTE and Beyond," *IEEE Journal of Solid-State Circuits, submitted (invited)*, July 2014.

Related publications

I have also co-authored the following papers, which are not considered as a part of this dissertation.

M. Anderson, R. Strandberg, S. Ek, L. Wilhelmsson, L. Sundström, M. Andersson, I. ud Din, J. Svensson, T. Olsson, and D. Eckerbert, "A

4.75 - 34.75 MHz Digitally Tunable Active-RC LPF for >60 dB Mean RX IRR in 65 nm CMOS," in *Proc. of 38th IEEE ESSCIRC 2012*, Bordeaux, France, Nov. 17–21 2012, pp. 470–473.

L. Sundström, M. Anderson, M. Andersson, and P. Andreani, "Harmonic Rejection Mixer at ADC Input for Complex IF Dual Carrier Receiver Architecture," in *RFIC*, Montreal, Canada, Jun. 17–19 2012, pp. 265–268.

Patent applications

M. Anderson, M. Andersson, S. Mattisson, and P. Andreani, "A frequency selective circuit configured to convert an analog input signal to a digital output signal," *International application*, No. PCT/EP2013/053424, 2013.

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I have been fortunate to have Dr. Martin Anderson as a co-supervisor from the academia and later from the industry. Thank you for introducing me to Ph. D studies and guiding me in the right direction when I was lost. You have always taken your time to generously share your knowledge and ideas for me. I appreciate your friendship, and the countless inspiring discussions on technical (and non-technical) matters during my studies.

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My strong interest in integrated circuits and analog circuit design is largely thanks to the inspiring undergraduate courses I took from Henrik Sjöland, Viktor Öwall and Bertil Larsson. In particular, I would like to thank Bertil for allowing me to teach in his courses and for the things you have taught me.

At Ericsson, several people have assisted me during different periods of my career. Thank you Sven Mattisson for being active in the project at the time when I needed it the most. I am also very thankful to Roland Strandberg and Jim Svensson for many reasons.

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Last but not least, I am very thankful to my friends and my family: Evald, Birgitta, Rickard, and Cecilia for always being there. Thank you Lisa for making the few hours outside the office so delightful with your love.

Mattias Andersson

Design is a funny word. Some people think design means how it looks.
But of course, if you dig deeper, it's really how it works.
– Steve Jobs –

List of Acronyms

A/D	Analog-to-digital
ADC	Analog-to-digital converter
BW	Bandwidth of desired A/D converted channel
CIFB	Cascaded integrators with feedback compensated loop filter
CIFF	Cascaded integrators with feedforward compensated loop filter
CMFB	Common-mode feedback
CMOS	Complementary metal oxide semiconductor
CP	Compression point
CSF	Channel-select filter
CT	Continuous time
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DC	Direct current
DR	Dynamic range
DSM	Delta-sigma modulator
DT	Discrete time
DWA	Data-weighted averaging
FOM	Figure of merit
FFT	Fast fourier transform
GBW	Gain band-width
GE	Gain error
HF	High-frequency
HP	High-pass
IB	In-band (inside the desired bandwidth)
IBN	Noise within the desired bandwidth
ICP	Input-referred compression point

IIPn	n-th order input-referred intercept point
IMn	n-th order intermodulation distortion
IPn	n-th order intercept point
IRN	Input-referred noise
ISI	Inter symbol interference
IF	Intermediate frequency
LF	Low-frequency
LHP	Left half plane
LNA	Low-noise amplifier
LP	Low-pass
LSB	Least significant bit
LTE	3GPP long-term evolution
LTE20	LTE with 20 MHz channel bandwidth at RF
NF	Noise figure
NRZ	Non-return-to-zero
NTF	Noise transfer function
OCP	Output-referred compression point
OFDM	Orthogonal frequency division multiplexing
OOB	Out-of-band
OSR	Oversampling ratio
PAR	Peak-to-average ratio
PCB	Printed circuit board
PI	Proportional integrating
PM	Phase margin
PSD	Power spectral density
RF	Radio frequency
RFFE	RF front-end
RHP	Right half plane

RX	Receiver
RZ	Return-to-zero
SDR	Software defined radio
SFDR	Spurious-free dynamic range
S/H	Sample-and-hold
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SQNR	Signal-to-quantization-noise ratio
STF	Signal transfer function
TF	Transfer function
TX	Transmitter

List of Symbols

$A\beta$	Loop gain
A_t	Transfer function from source to load
$A_{t\infty}$	Ideal transfer function from source to load
α	Time instant where feedback DAC pulse starts
β	Time instant where feedback DAC pulse ends
Δ	Quantization step
HD_n	n^{th} order harmonic distortion
f_s	Clock/sampling frequency [Hz]
IM_n	n^{th} order intermodulation distortion
IP_n	n^{th} order (intermodulation) intercept point
IIP_n	Input-referred n^{th} order intercept point
k	Boltzmann's constant, $\approx 1.381 \times 10^{-23}$ [J/K]
NF	Noise figure
P_{1dB}	Input power where the IBN increases by 1 dB
T_s	Sampling period [s]
T	Temperature [k]
V_{th}	MOS transistor threshold voltage

Introduction

Chapter 1

Introduction

1.1 Motivation

Today, the major innovations in consumer electronics are demonstrated in portable, battery powered devices such as smartphones and tablets. These devices use a large data rate via a wireless communication link, and therefore require high performance radio receivers with wider bandwidths and/or higher signal-to-noise ratios. Moreover, a receiver with higher performance in general consumes more power, which shortens the battery life of the device. Thus, research is needed to improve the power efficiency and performance of the receiver, to be able to deliver a high data rate with reasonable power consumption. Furthermore, analysis of the circuits enables the designer to understand the performance limiting factors and invent better integrated circuits (chips). These chips are mass-produced and require robust solutions that have low sensitivity to process-variations from manufacture.

A key component in the radio receiver is the analog-to-digital converter (ADC), which provides an interface between analog (the world) and digital (the ones and zeroes). A popular type of ADC is the $\Delta\Sigma$ modulator (DSM), which was first invented in the early 1960s and commercially used for audio conversion in the late 80s. These high performance, low-speed data converters (often operating in discrete time) rely on oversampling and feedback to push the quantization noise out of the wanted band, a technique called noise shaping. The DSM contains analog integrators, an internal ADC with one or a few bits in the forward path, and internal DACs in the feedback paths. Although only a few bits are used in the ADC and DAC, the noise shaping enables the DSM to achieve a very high resolution (beyond 12 effective bits) with moderate requirements in component matching. During the last decade, the continuous-time (CT) DSM has been extensively used in high-speed wireless receivers due to speed/power advantages over its discrete-time counterpart and an anti-alias filtering that is included.

On the other hand, the CT DSM is sensitive to delays in the loop. These delays are to some extent unknown due to process-variations during manufacturing. A loop delay that differs from the nominal case must be taken care of to ensure a robust operating condition and avoid a performance degradation, or even instability of the modulator.

Furthermore, the DSM is sensitive to noise and distortion generated by the first DAC and integrator. These components are therefore highly interesting to analyze and improve, as they limit the performance of the DSM.

This dissertation addresses the above mentioned challenges to implement high performance continuous-time $\Delta\Sigma$ modulators that convert an analog input into a digital output, for the wireless cellular standard LTE. Moreover, the dissertation studies the concept of *filtering ADCs*, where a channel select filter and ADC are combined into a unit that offers significantly lower requirements on the ADC itself and enables an improved power/performance tradeoff in the radio receiver.

1.2 Research contributions

This section provides a list of the most important research contributions from this doctoral dissertation with the corresponding paper cited.

- Development of the filtering ADC concept, where the channel-select filter and A/D converter (DSM) are merged to provide additional shaping of noise and distortion coming from the DSM. The key benefit of the concept is significantly lower requirements on the DSM, which enables power savings [4, 5].

- A model and analysis of the filtering ADC to provide new coefficients that preserve the filter transfer function in presence of the feedback DAC [5].

- Two implementations of filtering ADCs (576/288 MHz clock frequency with 18.5/9 MHz bandwidth) for verification of the concept. The measurements include unconventional ADC parameters such as compression point and intermodulation distortion intercept point vs frequency [4, 5]. The second filtering ADC is verified against a blocker specification for LTE Rel. 11 using OFDM modulated blockers [5].

- An analysis of performance degradation due to V_{th} mismatch in the current-switching pair of the first current-steering DAC in the DSM. The results provide insight of how to improve the linearity of the DAC [1].

- A feedback scheme to: (i) Make the DSM more robust against variations in loop delay. (ii) To omit implementing the otherwise obligatory loop delay compensation path (e.g. an additional DAC and adder) to reduce hardware complexity [2].

- Model and analysis of the new feedback scheme. The results provide a tool for the designer to evaluate and predict the impact on stability and performance of a modulator that implements the technique [3].
- Implementation and measurement verification of the new feedback scheme in a 7.5 mW, 288 MHz CT DSM with 69 dB SNDR for 9 MHz bandwidth [2]. The overload behavior of the DSM to out-of-band blockers was studied by measurements with OFDM modulated signals [3].
- A frequency compensation technique that boosts the loop gain of the integrator in-band [4].
- Use of a phantom-zero frequency compensation of the last integrator in the loop filter to improve the phase margin without loss in bandwidth, or increase in power consumption [5].
- An AC-coupled push-pull output stage to improve the linearity of the amplifier and deliver a large dynamic current needed to sink high frequency blockers, to improve the power efficiency of the amplifier [4, 5].

1.3 Outline

The dissertation provides an introduction to the field, as a base for appreciating the main contributions of the included papers. For more in-depth understanding, the author recommends reading the excellent books of [6–8]. The chapters and papers included in this dissertation are listed below, together with a brief explanation of their contents.

Chapter 1 presents a motivation for the dissertation, followed by a list of the research contributions and finally the organization.

Chapter 2 introduces a radio receiver system and commonly used performance metrics.

Chapter 3 describes the architecture level aspects of CT DSMs. Here, the concept of filtering ADCs is introduced, along with a performance comparison to previous work.

Chapter 4 presents the circuit-level implementation aspects.

Chapter 5 gives summaries and conclusions of the included papers along with the author's contribution.

Chapter 6 provides a discussion with suggestions for future work.

Appendix A contains additional measurement results that were not included in paper V.

Appendix B extends the analysis of the positive feedforward/feedback frequency compensation in paper IV.

Paper I analyses the impact of mismatch in the switching transistors, that are part of a unit-current cell, used in a current-steering feedback DAC.

Paper II presents the implementation and measurements of a DSM that is more robust against variations in loop delay.

Paper III extends paper II with theory of the proposed approach and additional measurements with OFDM signals.

Paper IV presents the implementation and measurements of the first of two filtering ADCs, where a 2^{nd}-order filter is merged with a 3^{rd}-order DSM.

Paper V presents the theory, implementation and measurements of the second filtering ADC, that has an improved selectivity and better performance, targeting LTE Rel. 11 [9], 3GPP compliance with support for two contiguous channels (2xLTE20).

Chapter 2

The radio receiver

This chapter describes the radio receiver system and introduces common performance metrics.

2.1 Introduction

A commonly used radio receiver in wireless communication is the homodyne receiver, also known as zero-IF or direct converting receiver, Fig. 1. The receiver contains an antenna filter, low-noise amplifier (LNA) for amplification, mixers to down-convert the signal from RF frequencies to baseband, channel-select filters (CSFs) and A/D converters (ADCs), the latter shown as $\Delta\Sigma$ modulators (DSMs). It is also possible to directly feed the RF signal into a bandpass DSM [10] or a DSM with mixers in the feedback loop [11]. The digital baseband after the ADC performs demodulation of the received signal.

The worst sensitivity scenario is when the receiver is far away from the basestation, where the received wanted signal is very weak and a strong interfering signal called a blocker is present, situated outside the channel bandwidth, out-of-band (OOB)[1]. These signals appear at the input of the CSF, after amplification by the LNA and down-conversion to zero-IF by the mixers, as indicated in Fig. 1. The CSF attenuates the strong blocker by its low-pass characteristic, to relax the dynamic range (DR) requirements on the ADC (i.e. the difference between the strongest and weakest signal), which allows fewer bits to be used in the ADC to decrease the power consumption. The attenuation of the blocker allows the filter to amplify the weak wanted signal, without causing clipping at the output of the filter, to relax the noise requirements of the ADC as the input referred ADC noise is reduced by the gain of the filter.

The chosen filter characteristic is a trade off between CSF and ADC complexity, where a higher order CSF leads to a lower power consumption in the ADC, but more power in the CSF. To summarize, there is in principle no re-

---

[1] Since this dissertation concerns ADC design, the term band refers to the desired channel, e.g. in-band noise (IBN) is used instead of in-channel noise (ICN). The term band has a different definition in radio receivers, where a band typically contains several channels.

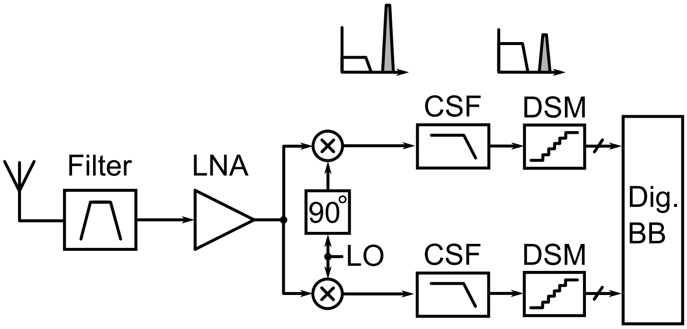

Figure 1: The homodyne receiver architecture with cascade of CSF and DSM.

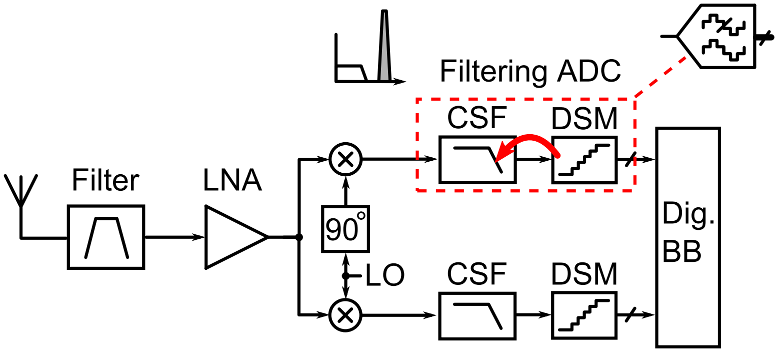

Figure 2: The homodyne receiver architecture with filtering ADC.

quirement to have a filter prior to the ADC, other than to improve the overall power efficiency, or to make the ADC design easier[2].

The ADC can be merged into the CSF to create a filtering ADC as illustrated in Fig. 2. Since the input signals to the filtering ADC and CSF in Fig. 1 are identical, the requirements in dynamic range for the filtering ADC are similar to those of the CSF. The filtering ADC is briefly described in chapter 3 and more thoroughly in [4, 5], with complementary measurement results in Appendix A.

---

[2] In general, an anti-alias filter is needed to avoid folding of high-frequency interferers on top of the wanted signal. However, the CT DSM has implicit anti-alias filtering that may be sufficient to eliminate the filter.

2.2 Characterization of receiver blocks

This section describes the main parameters that are used to characterize the behavior of circuit blocks in receivers. The main parameters are input referred

- Noise
- Compression point (clipping)
- Intermodulation intercept point (linearity)

In essence, the minimum input signal the receiver can detect is determined by the noise of the circuit, while the maximum allowed signal is limited by the ADC clipping level, often set near the supply voltage. In addition, due to limits imposed by receiver linearity, large OOB blockers may degrade the performance by generating intermodulation products that mask the wanted signal.

2.2.1 Input referred representation

In this dissertation, the input referred metrics are used, e.g. input referred 3^{rd}-order intercept point (IIP3). The input referred quantity is as usual found by moving a source at the output back to the input by division of the transfer function. Depending on the transfer function, the input referred quantity can be represented as a voltage, current or power. The performance parameters of the filtering ADCs are represented with a voltage quantity due to its voltage-mode interface.

For example, the input referred intermodulation distortion (IM) product or intercept point (IP) is found by referring the IM at the output back to the input via division by the in-band gain (IBG, typically equal to the DC gain) of the filter,

$$IIMn = OIMn - IBG, \tag{1}$$

where all quantities are in dB units.

2.2.2 Noise

The input referred noise sets a lower bound on the required input signal level for the receiver to successfully demodulate the data. The input referred noise is often given in [dBV_{rms}] or as a voltage spectral density in [$\text{nV}/\sqrt{\text{Hz}}$] in baseband circuits with a voltage interface [12, 13].

In the radio receiver, the input referred noise is represented by the noise figure (NF), which is a measure of how much noise the circuit adds to the receiver. The highest noise requirement is at the first stage of the receiver (the LNA), as the input referred noise contribution from the following circuits is diminished by the gain of the preceding blocks. The relationship between noise

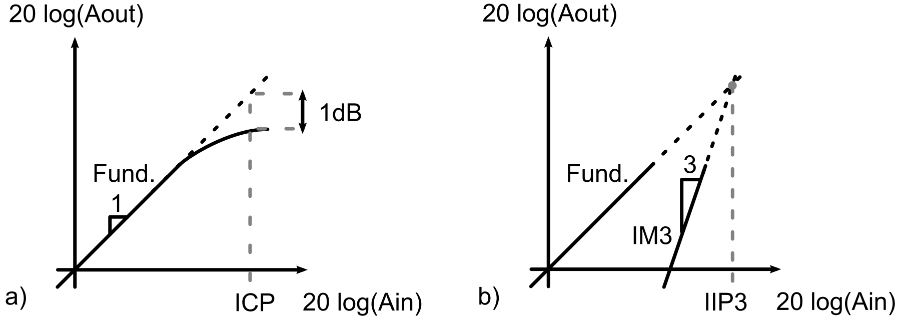

Figure 3: a) Input referred compression point. b) 3^{rd}-order intercept point.

figure and noise factor (F) is NF=10log(F), where the noise factor is given by [14,15]

$$F = \frac{N_{tot}}{N_s}. \tag{2}$$

N_{tot} is the total noise power of the receiver including that of the source (e.g. $N_{tot} = N_{rx} + N_s$) and N_s is the noise solely from the source. In all practical cases, the circuit adds noise, resulting in a NF larger than 0 dB.

2.2.3 Compression point, $\mathrm{P}_{1\mathrm{dB}}$ and CP

In the filtering ADC, the maximum allowed input signal is characterized by a metric called P_{1dB}. We have defined $\mathrm{P}_{1\mathrm{dB}}$ as the input signal level that yields a 1 dB increase in in-band noise (IBN). The filtering ADC has a P_{1dB} and dynamic range that improve with increasing frequency, due to the lowpass attenuation of high frequency signals.

In radio front-ends, the compression point (CP) specifies the maximum linear input signal. For small input tones, the input-output characteristic is linear and the amplitude of the fundamental output tone increases linearly with 1 dB/dB increase of the input signal, as illustrated in Fig. 3a. The compression point is found where the gain of the fundamental output tone drops by 1 dB compared with the extrapolated linear dashed line, and it can be either input referred (ICP) or output referred (OCP).

2.2.4 Intermodulation intercept point

The 2^{nd}- and 3^{rd}-order intercept point, IP2 and IP3 respectively, are commonly used to characterize the linearity of a circuit. When two tones are present at the input with frequencies f_1 and f_2, a nonlinear circuit exhibits harmonic distortion at integer multiples of f_1 and f_2, and intermodulation distortion

(IM) at linear combinations for integer multiples of f_1 and f_2 at the output. The second order IM (IM2) is found at $f_1 - f_2$ and $f_1 + f_2$, while IM3 is found at $2f_1 - f_2$ and $2f_2 - f_1$. The IM caused by strong OOB blockers may appear in-band, on top of the wanted signal for certain frequencies of f_1 and f_2. For example, the IM2 measurements in this dissertation were carried out at various offset frequencies f_o, with the two tones placed at $f_1 = f_o + f_{im}/2$ and $f_2 = f_o - f_{im}/2$, such that the IM always appears in-band with f_{im}=1 MHz. In general, an OOB blocker with wide bandwidth will due to IM2 generate components in-band that potentially masks the wanted signal.

The amplitude of an IM3 product versus one of the two, equal in power, input tones is sketched in Fig. 3b. The dashed lines show the linearly extrapolated curves of the fundamental tone (1 dB/dB) and the IM3 product (3 dB/dB). The input referred IP3 (IIP3) is the input amplitude where the two extrapolated curves intersect with each other, as indicated by the graph. The benefit of characterizing linearity for a circuit with IP is that the IP is independent of amplitude, while an IM product should be specified together with the corresponding amplitude.

The IP can be extrapolated from a single point instead of using several data points with [12, 14]

$$IIP2 = 2P_{in} - IIM2, \tag{3}$$

and

$$IIP3 = \frac{3P_{in} - IIM3}{2} \tag{4}$$

where $IIMn$ is the input referred n-th order IM product and all variables are in dB units (e.g. dBm or dBV$_{\mathrm{rms}}$). The equations should be applied in the region where the IM product varies by n dB/dB when calculating IPn.

As an example, a two-tone measurement of the circuit in [5] is shown in Fig. 4. For low input amplitudes, the IM3 product follows the expected 3 dB/dB increase, resulting in an extrapolated IIP3 that is essentially constant with amplitude, while the IM3 product rises quickly at large input amplitudes due to higher-order nonlinearities becoming significant as the circuit approaches compression.

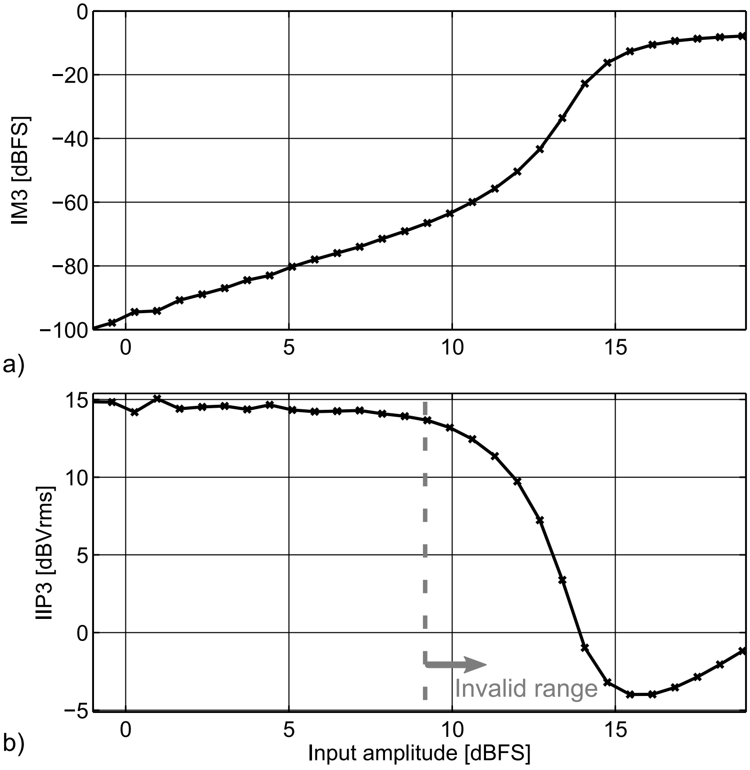

Figure 4: Measured IIM3 and IIP3 vs input amplitude of [5] for two tones with equal power at 86 and 43.5 MHz. 2×LTE20 mode.

Chapter 3

Continuous-time $\Delta\Sigma$ modulators

This chapter starts by defining common terminology used in the context of CT DSMs and then continues with a brief introduction to filtering ADCs including an overview of previous work and performance comparisons. The remaining part of this section describes non-idealities in the feedback DACs of the CT DSM.

3.1 Introduction

The DSM is a feedback system with a quantizer that operates in discrete-time (DT) on samples. A general DT DSM can be represented with the schematic in Fig. 5a that contains a linear DT loop filter L, an n-bit ADC, and an n-bit feedback DAC. During the last decade, the attention has increased towards DSMs with CT loop filters (Fig. 5b), due to an inherent anti-aliasing, absence of kT/C noise and benefits in speed compared with its DT counterpart [7]. The design of the CT modulator is often based on a DT reference modulator, that for example can be synthesized using Schreiers toolbox in Matlab [16].

The noise transfer function (NTF) contains the closed loop poles of the DSM, which determines the maximum signal-to-quantization noise ratio (SQNR) and the stability of the DSM. The NTF from quantization noise injected at node Y to the output V of the DSM, assuming a unity quantizer gain, is from linear analysis,

$$NTF(z) = \frac{V(z)}{E(z)} = \frac{1}{1 - L_1(z)}. \tag{5}$$

The NTF of the DT and CT DSM (Fig. 5a and b, respectively) can be made identical with the impulse invariant transform, to present the same impulse response at the input of the quantizer at the sampling instants. The (time domain) impulse response is the inverse Laplace or Z-domain of the transfer function from the output of the quantizer V back to the input Y. Equivalence between the two systems yields [3, 6, 17–19],

$$\mathcal{L}^{-1}\left\{DAC(s)L1(s)\right\}|_{t=nT_s} = \mathcal{Z}^{-1}\left\{L1(z)\right\}, \tag{6}$$

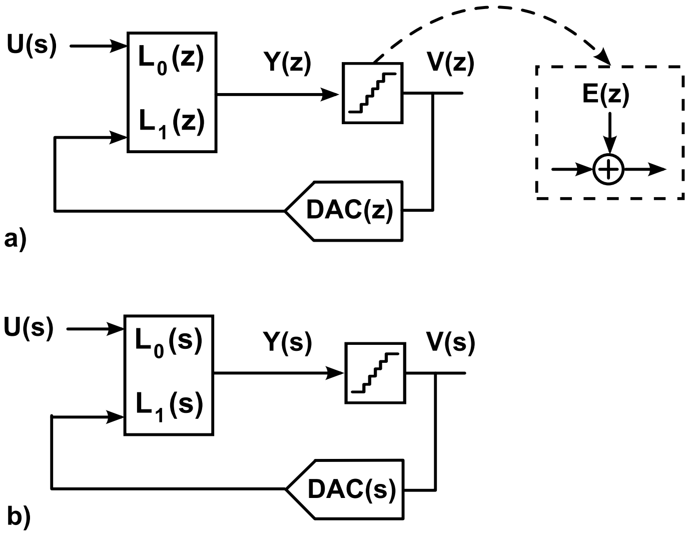

Figure 5: General representation of a) DT modulator as reference. b) CT modulator.

that enables to find the CT loop filter coefficients in $L_1(s)$ analytically. Alternatively, the coefficients can be found with numerical impulse response matching [20] for arbitrary DAC waveforms.

The signal transfer function (STF) from the input signal X to the output V of the DT DSM is

$$STF(z) = \frac{U(z)}{Y(z)} = \frac{L_0(z)}{1 - L_1(z)} = L_0(z)NTF(z). \tag{7}$$

The STF for the CT DSM is a mixture between CT and DT operation [6,7,21],

$$STF(s) = \frac{L_0(s)}{1 - L_1(z)} = L_0(s)NTF(z) \tag{8}$$

where $z = e^{sT_s}$, with a sampling period T_s. From this it is clear that even if a direct path exists from U to Y ($L_0(s) = 1$), $STF(s)$ has anti-alias filtering thanks attenuation by $NTF(z)$.

3.2 Basics of filtering ADCs

In this section, the concept of filtering ADCs is very briefly explained, as more details are given in the included papers in this dissertation.

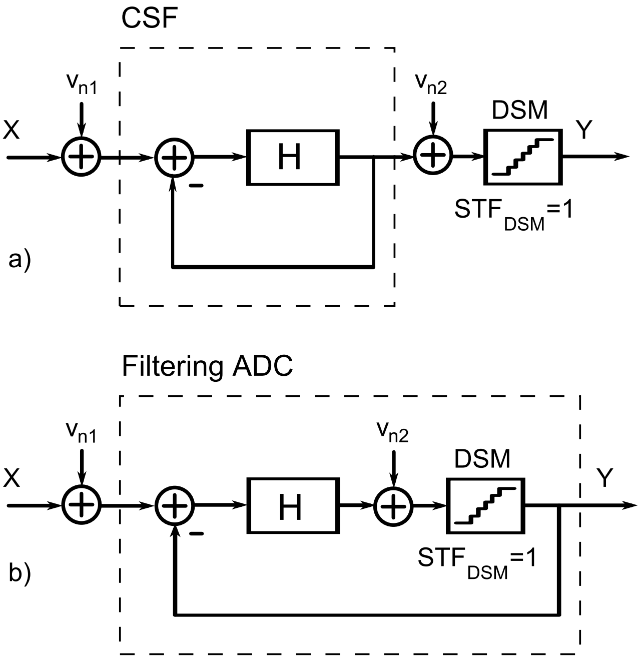

Figure 6: Simplified architecture of a) CSF and DSM in cascade. b) Filtering ADC.

In the filtering ADC, the DSM is incorporated inside the global feedback loop of the CSF, resulting in a suppression of flicker and thermal noise, distortion and quantization noise from the DSM. This is the key benefit compared with having the CSF and DSM in a cascade. The resulting filtering ADCs in this dissertation are equivalent to high-order DSMs [4, 5].

This additional noise suppression principally enables three design choices: if both CSF and DSM are kept unchanged, the overall noise and linearity of the analog baseband is improved by the noise suppression. Alternatively, the overall performance can be kept constant and the DSM redesigned with a suitably lower performance to save power. Finally, if the DSM is kept unchanged, the CSF can be redesigned with a higher noise contribution and a lower power consumption. In any case, the filtering ADC provides an improved trade-off between noise and power consumption.

To demonstrate the noise suppression, the CSF-DSM cascade and the filtering ADC are modeled as shown in Fig. 6a and b, respectively. The input referred noise of the CSF and the DSM, are represented with V_{n1} and V_{n2}, respectively. The transfer functions from the input X and the noise sources

V_{n1}, V_{n2} to the output Y for the two systems in Fig. 6 are easily found as,

$$Y = \frac{H}{H+1}X + \frac{H}{H+1}V_{n1} + V_{n2} \tag{9}$$

for the CSF-DSM cascade and

$$Y = \frac{H}{H+1}X + \frac{H}{H+1}V_{n1} + \frac{V_{n2}}{H+1} \tag{10}$$

for the filtering ADC. First note that the filter transfer function from X to Y is the same in both systems as a first order approximation, with $\mathrm{STF}_{\mathrm{DSM}}$=1. More importantly, (10) shows the advantage of the filtering ADC, as the noise source V_{n2} is suppressed by a factor $(H+1)$ with $H \gg 1$ in the filtering ADC, while V_{n2} is directly seen at the output for the CSF-DSM cascade. The noise suppression improves the SNDR of the DSM by 14 dB and 20 dB, respectively, in the included papers [4, 5]. This leads to very relaxed requirements on the DSM and allows for power savings or improved performance in the analog baseband, as previously mentioned.

The ADC is here shown as a DSM, but can in principle be anything from a simple flash ADC to an n^{th}-order DSM. The main limitation is that an STF_{DSM} of unity is desired (no attenuation and zero phase shift) in order to preserve the filter transfer function. More details about methods for mitigating deviations from the ideal $\mathrm{STF}_{\mathrm{DSM}}$ and design of filtering ADCs is described in [4, 5].

3.2.1 The term filtering ADC

The term filtering ADC is ill defined, since all lowpass DSMs (both discrete-time and continuous-time) have a loop filter (H) which in general provides some filtering at high frequencies. Traditionally, the DSM is designed with high-frequency poles for the NTF to maximize SQNR, at the expense of reduced filtering for the adjacent channels. While these ADCs present some high-frequency filtering, they do not qualify as filtering ADCs, as they implement no filtering of adjacent channels (sometimes these channels are even amplified). In this dissertation, we define a filtering ADC as a DSM where the positions of some poles have been compromised to yield a specific transfer function, different from the transfer function obtained for a purely SQNR optimized DSM[3].

3.2.2 Previous work

This section contains an overview of previous work that acknowledge the importance of the OOB STF for low-pass DSMs. In many applications, the OOB

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[3] The filtering ADCs in this thesis have both the conventional high-frequency poles to provide a sufficiently high SQNR and a few low-frequency poles for channel-select filtering (that provides the additional noise suppression mentioned previously).

STF may not matter, while in wireless communication systems it is of utmost importance due to the typically rather hostile radio environment with strong blockers.

NTF and STF trade-offs

It is well-known that CT DSMs with feedback-compensated loop filters (CIFB) can provide a sharp filtering of high-frequency blockers by the proper design of their STF [22, 23]. However, a fundamental issue in a filtering DSM is that its STF and its noise transfer function (NTF) share the same poles [23, 24]; therefore, the more aggressive the filtering, the poorer the NTF in-band quantization-noise shaping. In the filtering ADC of [23,25], this is circumvented by inserting a 1st-order low-pass filter in the forward path, while stability is preserved by a corresponding high-pass filter in the feedback path. While this approach provides the necessary filtering, the presence of both a high-pass and a low-pass filter results in an NTF with no net improvement in terms of noise shaping. Furthermore, the complexity of the high-pass filter increases when a higher-order transfer function (TF) is desired.

Feed-forward modulators

A vast amount of research has also been devoted to improve control of the STF in feedforward compensated modulators [26–31], which have a favorable power consumption but tend to display a pronounced high-frequency STF overshoot (STF peaking), which is undesirable in applications where large OOB blockers are expected. Starting with [26], a mix between feedback and feedforward modulator is used to achieve lower STF peaking than a feedforward modulator. This structure is used by [24] when blocker levels are low; however, when blockers are present, the DSM adaptively reconfigures the loop-filter based on a blocker detector, to operate as a conventional feedback modulator for improved selectivity.

In [28, 29, 31], a filtering STF is achieved for the feedforward modulator by using negative feed-in paths. These feed-in paths implement signal cancellation, which is sensitive to process variations [28,31]. For improved robustness, [28,30] suggests to omit the feed-in paths, add a second DAC and add a path from the output of the first integrator to the input of the other integrators. With this structure, the lowpass STF of a conventional feedback modulator is achieved, with fewer DACs. Although the design has a peaking free STF with good anti-alias filtering, there is no filtering of adjacent channels next to the wanted band.

The selectivity can be improved with a complex impedance in parallel with the output of the first integrator in the loop filter, to shunt the signal to ground at a specific frequency [32]. This technique is however limited to notching out

Table 1: Comparison of low-pass filtering ADCs. *Calculated from data in [25].

Parameter	[5]	[4]	[23]	[33]
BW (MHz)	**18.5**	**9**	1	6
fs (MHz)	**576**	**288**	64	405
SNDR (dB)	**56.4**	**68.4**	59	74.6
f_{-3dB} (MHz)	**25.0**	**16.9**	3	–
IRN ($\text{nV}/\sqrt{\text{Hz}}$)	**5.1**	**8.1**	280*	–
In-band IIP3 (dBV_{rms})	**-8.5**	**11.5**	19*	–
Tech. (nm)	**65**	**65**	180	90
Vdd (V)	**1.2**	**1.2**	1.8	1.2-1.8
Power (mW)	**7.9**	**11.3**	2	54
DR at BW×4 (dB)	**82**	**80**	65	90
FOM1 at BW×4 (fJ/conv. step)	**21**	**77**	700	180
FOM2 (fJ)	**0.32**	**0.075**	1.98	–

certain blockers local in frequency and is not a general remedy for improved selectivity.

Improved selectivity and noise shaping

As a further step toward improved selectivity with higher-order noise shaping, the DSM can instead be incorporated into a Rauch filter to create a filtering ADC [33, 34]. The key benefit is that the global feedback loop of the CSF provides a first order noise shaping of the noise from the DSM, to improve the performance and relax the requirements on the DSM itself, compared with a conventional CSF-DSM cascade. The designs presented in this dissertation were obtained in a similar manner; more details are found in [4, 5].

3.3 Performance comparison of filtering ADCs

This section presents an overview and performance comparison of filtering ADCs. While a survey of state-of-the-art ADCs can be found in [35], the concept of filtering ADCs is a quite new approach with only a few implementations reported in the literature. These implementations are compared in Table 1 for power efficiency figure-of-merits (FOMs) FOM1 and FOM2, defined in [5]. It is seen that [4, 5] achieve state-of-the-art FOMs, where a lower FOM is better.

The FOM1 is calculated based on the OOB performance of the filtering ADC, since it is not fair to base a comparison on the in-band performance, for the following reason. Consider a lowpass filter that is placed in front of an ADC: the filter adds noise, non-linearity and consumes power, which worsens the in-band performance of the overall chain. On the other hand, the filter

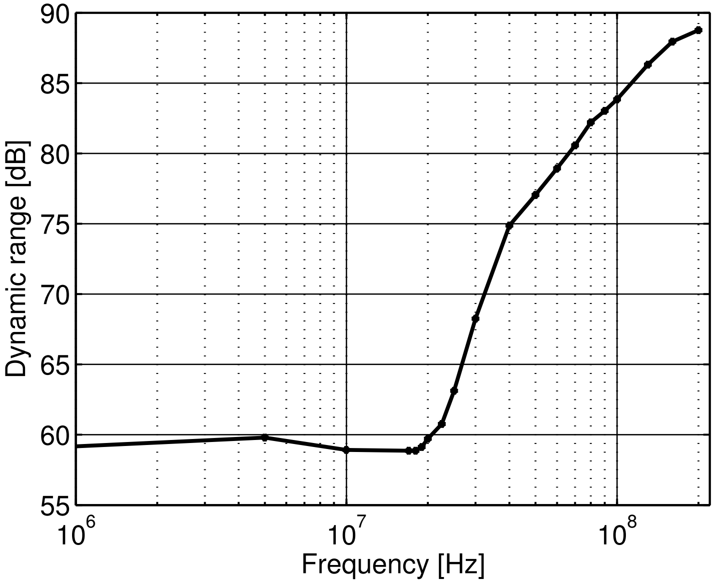

Figure 7: Measured dynamic range (P_{1dB}-IBN) for filtering ADC [5].

improves the OOB dynamic range, which is not captured using conventional ADC FOMs that are based on the in-band performance.

For comparison with Table 1, consider also the example of using a stand-alone ADC that targets 2xLTE20[4], connected directly after the RX mixers, with the assumptions on the RF front-end in [5]. The ADC needs a baseband bandwidth of 18.5 MHz and a DR in excess of 85 dB, which is very challenging to implement. Furthermore, these requirements translate into a power consumption beyond 25 mW, assuming the DSM can be implemented with a state-of-the-art FOM of 50 fJ/conv.step and has a frequency independent DR. On the other hand, the frequency dependent DR of the filtering ADC in [5], shown in Fig. 7, is tailored for 2xLTE20 support and exploits the low IB and high OOB DR requirements in the LTE receiver.

3.3.1 Comparison with filters

This section compares a stand-alone filter (without ADC) against the filtering ADC, which behaves like a filter with a digital output.

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[4] 2xLTE20 means that the receiver supports two contiguous LTE channels with 20 MHz bandwidth each at RF.

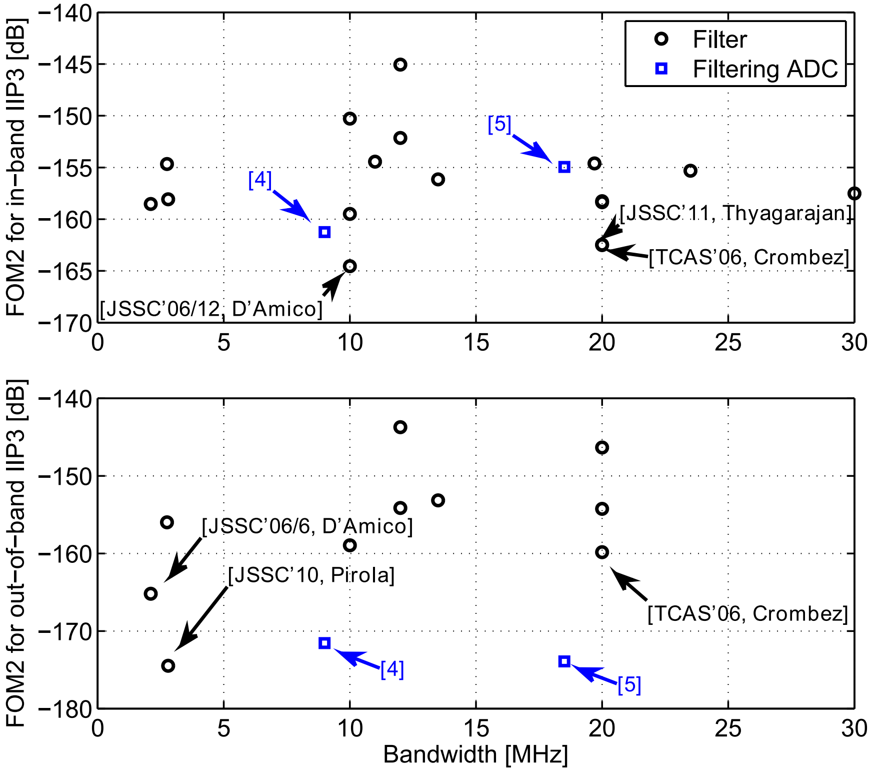

Figure 8: State-of-the-art CMOS active filters and the filtering ADCs in [4,5] evaluated for in-band IIP3 (top) and out-of-band IIP3 (bottom).

A performance comparison for state-of-the-art CMOS active filters is shown in Fig. 8, based on a survey by Saari [12] with the recently published filters added. The comparison uses the well-known filter FOM [36] (denoted FOM2 in [4,5]), evaluated for both in-band IIP3 and the maximum OOB IIP3[5], with the top three filters in both cases highlighted [37–41][6]

It is interesting to note that the power efficiency of the filtering ADC compares well against the filters in in-band performance and exceeds several in

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[5] The filtering ADCs uses the OOB IIP3 at TX duplex distance, which is the relevant IIP3 test case for FDD systems, although a higher IIP3 was recorded at higher offset frequencies. Furthermore, the offset frequency is not standardized and not reported for all filters. Also note that fewer filters report the OOB IIP3.

[6] FOM2 is calculated for the channel BW (band edge), as the 3dB BW contains noise that is removed by the following digital decimation filters.

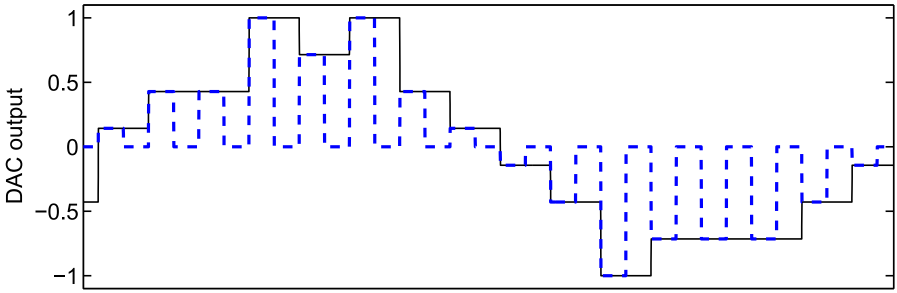

Figure 9: Time domain DSM output of an 8-level feedback DAC, normalized to V_{ref}, for a sine wave input. Solid black: NRZ DAC. Dashed blue: RZ DAC.

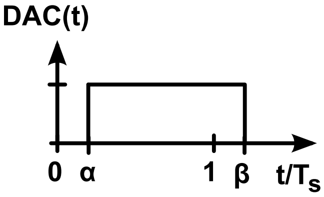

Figure 10: Rectangular feedback DAC pulse from α to β.

OOB performance. Furthermore, the filtering ADC provides both filtering and A/D conversion, which indicates that the A/D conversion is included in a power efficient manner, loosely speaking ”for free”.

As already mentioned, the filtering ADCs in this dissertation are equivalent to high-order CT DSMs. The following sections describes non-idealities of the feedback DACs in the DSM.

3.4 Feedback DAC pulse

The CT DSM (previously shown in Fig. 5b) is sensitive to the accuracy of the feedback DAC pulse in both time and magnitude. The feedback DACs often use a rectangular non return-to-zero (NRZ) and/or return-to-zero (RZ) pulse, which are illustrated in Fig. 9. There exist also various alternative pulse shapes that reduce the sensitivity to clock jitter, such as the switched capacitor with resistor DAC [20, 42].

The rectangular DAC pulse is specified with the parameters α and β as a fraction of the clock period (Fig. 10), where the NRZ pulse has a pulse width

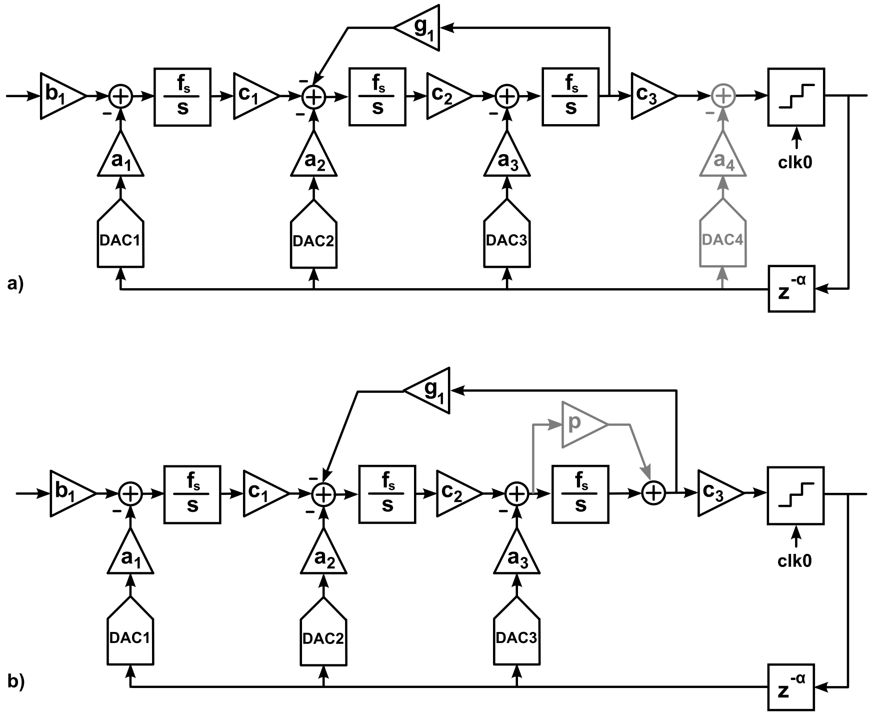

Figure 11: Third order CT DSM with CIFB loop filter. g_1 shifts the NTF zeros from DC to in-band with a resonator path. a) DAC4 and a_4 compensate for loop delay. b) p compensates for loop delay.

of $\beta - \alpha = 1$ and the RZ pulse has $\beta - \alpha < 1$, with a transfer function of

$$DAC(s) = \frac{1}{s}\left(e^{-s\alpha T_s} - e^{-s\beta T_s}\right). \tag{11}$$

From this, it is clear that if α and β vary (the DAC pulse width and position), the NTF of the DSM is affected via the CT impulse response, given by (6). The following sections describe why an intentional delay of α is commonly used and how the DSM can be made more robust against variations in α.

3.4.1 Fixed loop delay

A conventional third order CT DSM with cascade of integrators feedback (CIFB) [7] loop filter is shown in Fig. 11. A delay of the DAC pulse is known as loop delay and may come from the regeneration time in the flash ADC, delay in the feedback network of for example dynamic element matching circuits [2–5], internal delays in the DACs, delay in the loop filter due to integrators with finite GBW, and delay in the preamplifiers in the flash ADC. The exact value of these delays are to some extent unknown and affect the impulse response, which can lead to a performance degradation or even instability if not accounted for in the design [18, 43–48].

The uncertainty of the delay from the flash ADC output to the DAC input is often removed by intentionally clocking the DACs with a delayed clock that is a fixed amount of the clock period, to allow the digital signal to settle before rising edge of the DAC clock. The delay α is modeled by the $z^{-\alpha}$ element shown in Fig. 11. For the commonly used NRZ pulse, a delay causes the pulse to extend into the next clock period ($\beta > 1$), which in general requires an additional path directly from the output to the input of the flash ADC, to nominally compensate for loop delay. The components for loop delay compensation are a_4, DAC4, and the adder illustrated in grey in Fig. 11a.

An alternative compensation technique is a PI loop delay compensation [5, 45, 48, 49] shown in Fig. 11b. A proportional path is added to bypass (feedforward) an integrator in the signal-flow graph to create an LHP zero in the integrator transfer function. The zero is implemented by adding a series resistor with the integrator capacitor, as shown in Section 4.3.3. This technique avoids the additional DAC and adder, and preserves the NTF of the DSM, while the STF is affected by the feedforward path, i.e. a zero appears in L_0 of (8). A summary of the most popular loop delay compensation techniques is presented in [45].

The above methods nominally compensate for the fixed delay caused by intentionally clocking the DACs with a delayed clock. The following section shows how the sensitivity to delay from the DAC, finite integrator GBW, and preamplifier can be reduced.

3.4.2 Variations in loop delay

This section graphically illustrates how an RZ pulse that is centered in the clock period can reduce the sensitivity to variations in loop delay.

Consider first Fig. 12a where an NRZ pulse with a quarter clock period fixed loop delay, $\alpha = 0.25$, $\beta = 1.25$. The solid line shows the initial position of the NRZ pulse in the time domain and the first order integration of the pulse, i.e. the impulse response of the DAC3 path in Fig. 11. If the pulse is delayed by T_a as shown by the dashed line, the first sample of the impulse response sees an error, as indicated by the two circles. The error occurs due to the incomplete integration of the pulse, as it extends beyond the first sample into the next clock period.

The same procedure is illustrated with an RZ pulse centered in the clock period ($\alpha = 0.25$, $\beta = 0.75$) in Fig. 12b. In this case, the integration finishes within the sampling period and the two integrals coincide prior to the first

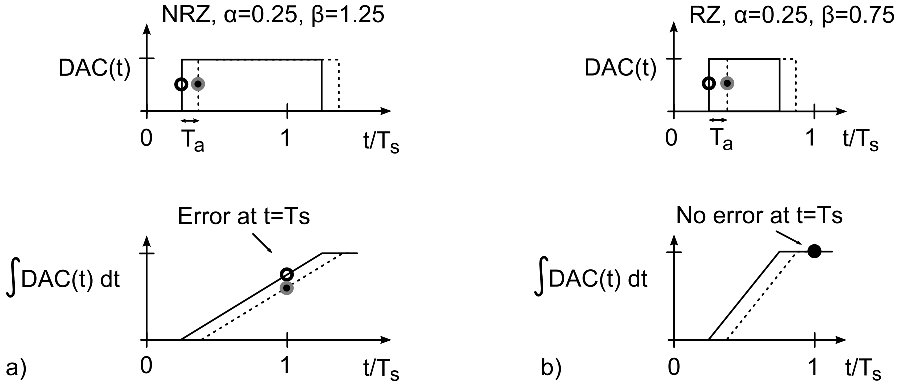

Figure 12: Impulse response of path with first order integration, with the DAC pulse in nominal position and delayed by T_a for a) NRZ pulse. b) RZ pulse.

sample with no error. Consequently, the DSM becomes more robust against variations in loop delay by using an RZ pulse in particular for the inner most loop [2, 3]. Another benefit is that the loop delay coefficient (a_4 in Fig. 11) reduces significantly and may even be omitted in the implementation to reduce hardware complexity.

The following section analytically confirms the above mentioned benefits.

3.4.3 z-domain analysis of loop delay variations

This section provides an extended analysis of the results in [2,3]. It applies the method in [18] to study how the z-domain NTF poles vary with loop delay for the third order DSM in Fig. 11 for three cases: First, the quarter clock period delayed NRZ pulse is used in all DACs, to illustrate that DAC3 has the highest sensitivity to loop delay. Secondly, the sensitivity is reduced with an RZ pulse that is centered in the clock period in DAC3. Thirdly, the NRZ/NRZ/RZ feedback scheme in [2–4], where DAC4 is omitted, is studied.

A DT model of the CT DSM is developed to show the pole-zero locations of the NTF and perform fast Matlab simulations with Schreiers toolbox [16]. The DT model was found by transforming the CT loop filter in Fig. 11 into a DT representation with the impulse invariant transform [6, 18, 19, 50], repeated in Table 2 for convenience. The output spectrum (8192-point FFT) for a -6dBFS input tone with 32 times averaging is recorded, together with the pole-zero locations in the NTF.

Table 2: z-domain representation of s-domain integration [50]. Rectangular DAC pulse from α to β.

s-domain	z-domain
$1/s$	$\frac{y_0}{z-1}$, $y_0 = \beta - \alpha$
$1/s^2$	$\frac{y_1 z + y_0}{(z-1)^2}$ $y_1 = \frac{1}{2}\left(\beta(2-\beta) - \alpha(2-\alpha)\right)$, $y_0 = \frac{1}{2}(\beta^2 - \alpha^2)$
$1/s^3$	$\frac{y_2 z^2 + y_1 z + y_0}{(z-1)^3}$ $y_2 = \frac{1}{6}(\beta^3 - \alpha^3) - \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$ $y_1 = -\frac{1}{3}(\beta^3 - \alpha^3) + \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)$, $y_0 = \frac{1}{6}(\beta^3 - \alpha^3)$

DAC with highest sensitivity

For the nominal pulse position in Fig. 13 ($\alpha = 0.25$, $\beta = 1.25$), the three zeroes are located at $z = 1$ and the three poles are scattered around the origin, as expected. The figure also shows two additional simulations when DAC1 or DAC3 is delayed by $T_a = 0.1T_s$ from the nominal pulse positions, resulting in an additional pole and zero that increases the order of the DSM. It is clear that DAC3 is much more sensitive to the delay than DAC1, as the poles have shifted by a larger amount and peaking is seen in the output spectrum. It is also seen that the z-domain linear model (in green) shows excellent agreement with the FFT.

Reduced sensitivity

The above analysis was repeated for a CT DSM with an RZ pulse in DAC3, for a nominal case ($\alpha = 0.25$, $\beta = 0.75$) and with all DACs delayed by $T_a = 0.1T_s$ in Fig. 14. The nominal result is as expected identical to the previous result in Fig. 13, while the poles are much less affected by the additional delay in this case. This illustrates the benefit of using an RZ pulse that is centered in the clock period, in the innermost DAC (DAC3) [2,3].

For completeness, the NRZ/NRZ/RZ feedback scheme in [2–4] where DAC4 is omitted, is presented in Fig. 15. Already in the nominal case, the absence of DAC4 increases the order of the DSM, as seen by the left half plane pole and the zero in origin [2,3]. More importantly, also this DSM shows a reduced sensitivity to loop delay variations, as is clear from the pole zero plot and the output spectrum. As a final remark, the poles remain inside the unit circle for $T_a = \pm 0.25T_s$, as expected from the simulations in [2,3].

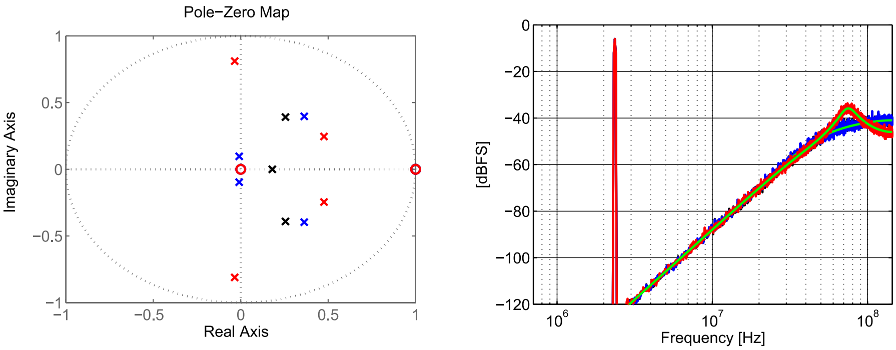

Figure 13: Pole-Zero plot and FFT. NRZ DAC1-4. Black: Nominal case. Blue: DAC1 delayed by $0.1T_s$. Red: DAC3 delayed by $0.1T_s$.

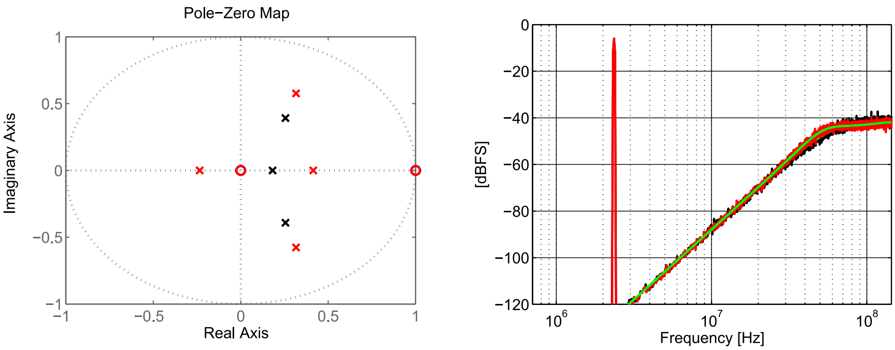

Figure 14: Pole-Zero plot and FFT. NRZ DAC1,2,4; RZ DAC3. Black: Nominal case. Red: All DACs delayed by $0.1T_s$.

3.4.4 Feedback DAC non-linearity

A critical component in the DSM is the feedback DAC, since its errors are not shaped (contrary to the ADC). The non-linearity of a feedback DAC can be divided into a static and a dynamic non-linearity. The static non-linearity is caused by mismatch in the DAC output levels, often represented by integral non-linearity (INL) and differential non-linearity (DNL) in Nyquist converters [51]. The variability of the output levels comes from mismatch in the unit elements comprising the DAC, e.g. the current sources in a current-mode DAC. The linearity is often improved with a dynamic-element matching (DEM) method, such as data-weighted averaging (DWA) [52].

The dynamic non-linearity occurs at the switching event of the DAC and

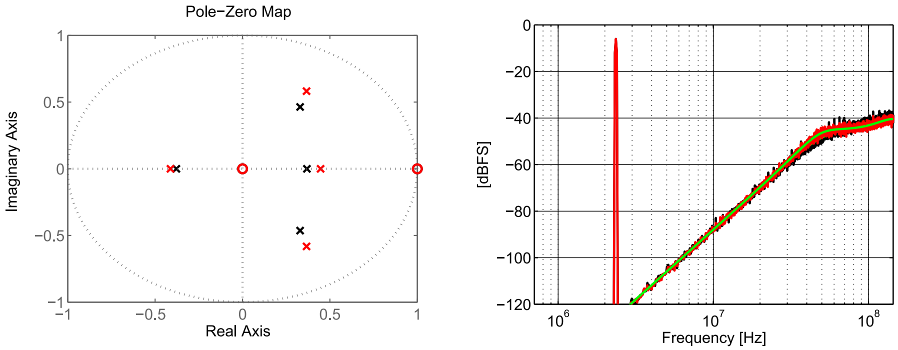

Figure 15: Pole-Zero plot and FFT. NRZ DAC1,2; RZ DAC3; DAC4 omitted. Black: Nominal case. Red: All DACs delayed by $0.1T_s$.

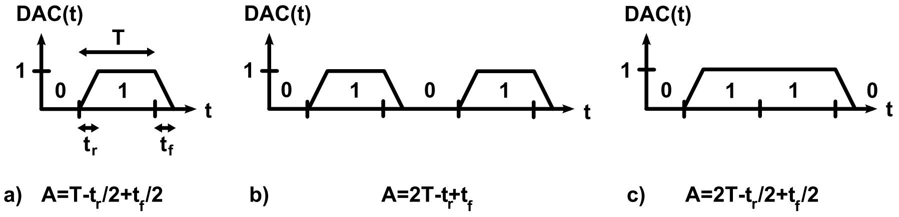

Figure 16: DAC output for code: a) ’01’. b) ’0101’. c) ’0110’.

is therefore problematic for high sampling speeds, or for extreme linearity requirements [53]. To illustrate dynamic non-linearity, a DAC output with the corresponding area (charge) for digital codes ’01’, ’0101’ and ’0110’ is illustrated in Fig. 16a, b and c respectively. In case the rise and fall times differ, the DAC output in Fig. 16b and c are not identical, i.e. the output depends on the previous code. This is known as inter-symbol-interference (ISI), which is a well-known challenge with NRZ feedback DACs. It is clear from the figure that the rise and fall time should be identical to preserve linearity in the DAC [54].

In a differential implementation of the DAC, the output has inherently a symmetric rise and fall time (as a first order approximation), even if the output is constructed by two asymmetric signals [55, 56]. However, it has later been shown that the output of a differential current-steering DAC may be asymmetric, due to second-order effects. For example, the two transistors in the differential switch pair may inject a different amount of charge, or have a V_{th} mismatch that in combination with a tail capacitor results in an asymmetric pulse [1, 57]. This ISI effect, in combination with DWA, results in even order distortion [1, 53, 57–61].

A common solution to avoid ISI is to use an RZ DAC, at the expense of increased clock jitter sensitivity [6]. The jitter sensitivity can be reduced by implementing an effective NRZ pulse with two RZ pulses within the clock period [62], assuming that the fall time of the first and rise time of the second RZ pulse are derived from the same clock edge. While this approach require twice the clock frequency to generate the RZ pulses, [63] use two parallel signal paths with DWA and a full clock period RZ pulse in an interleaved fashion to implement the effective NRZ pulse.

Recently, a more elegant approach has been presented which mitigate the ISI with an ISI shaping dynamic-element matching [53]. The algorithm turns the static and dynamic non-linearity of the DAC into noise with a mismatch shaping loop and an ISI shaping loop, respectively.

Chapter 4

Circuit level considerations

This chapter describes some of the design considerations at circuit level for CT DSMs. The section compares the resistive feedback DAC with the current-steering DAC with respect to output impedance and noise. It also contains an analysis of the active-RC integrator.

4.1 Feedback DAC

The unit cells of three common NRZ current-mode DACs are shown in Fig. 17. The DACs in Fig. 17a and b are current-steering and contain a constant current source together with switches to direct the unit current I_u to the branches, depending on the digital code. The complementary resistive DAC in Fig. 17c switches the two resistors to V_{refp}/V_{refn} and V_{refn}/V_{refp} for a digital code of '1' and '0', respectively. The DAC has a differential unit current of

$$I_u = \frac{V_{refp} - V_{refn}}{2R_u}, \tag{12}$$

where R_u is the unit resistor value. Assuming that V_{refp} and V_{refn} are centered around the common-mode voltage, the current into the CMFB is zero.

The unit current flows according to the figure for a digital input of b='1'. In the two complementary DACs, the complete signal current flows through the integrator, while in the differential DAC, half of the signal current is lost in the CMFB network. Thus, the differential DAC requires twice the unit current to provide the same load current, thereby implementing the same coefficient in the DSM.

4.1.1 Noise

As shown above, the differential DAC in Fig. 17a should have twice the unit current to provide the same current into the load and implement the same feedback coefficient as the complementary DAC in 17b. The noise current at the output of the differential and complementary DAC is the same for the following reason: the PMOS and NMOS current source of the complementary

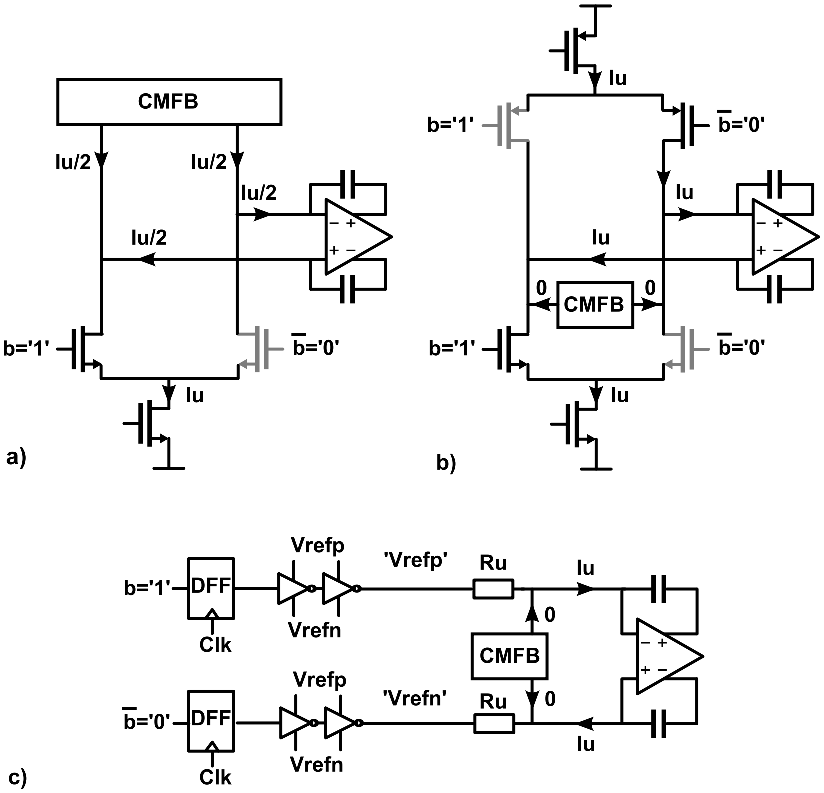
CMFB
Iu/2
Iu/2
Iu/2
Iu/2
b='1'
b̄='0'
Iu
a)
Iu
b='1'
b̄='0'
Iu
Iu
0
CMFB
0
b='1'
b̄='0'
Iu
b)
Vrefp
'Vrefp'
Ru
Iu
b='1'
DFF
Clk
Vrefn
0
CMFB
Vrefp
'Vrefn'
Ru
0
b̄='0'
DFF
Clk
Vrefn
Iu
c)

Figure 17: DAC architectures: a) Differential current-steering. b) Complementary current-steering. c) Complementary resistive.

DAC produce a total noise of $2S_{ID}$[7], while the differential DAC has a single NMOS current source with the same noise, $2S_{ID}$, since the unit current is doubled.

The main reason for using a resistive DAC is the lower thermal noise of the DAC itself, compared to a current-steering DAC [2,3,64]. This is clearly seen by inspecting the thermal current noise of a resistor and of a MOS current source, which are given by

$$S_{IR} = \frac{4kT}{R_u} = \frac{4kTI_u}{V_u}, \tag{13}$$

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[7] The PMOS and NMOS current source typically produce similar thermal noise, assuming the transconductances are matched to achieve comparable overdrive voltages.

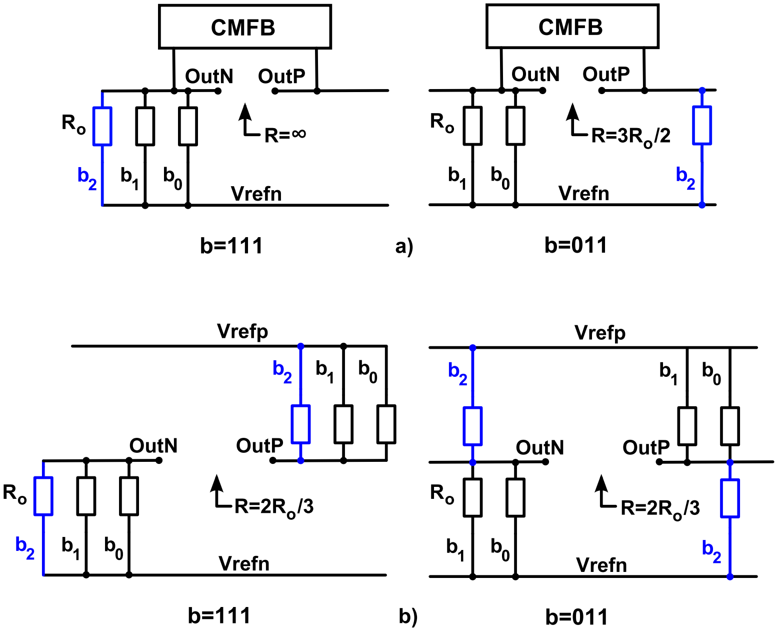
CMFB
OutN
OutP
R=∞
R_o
b_2
b_1
b_0
Vrefn
b=111
a)
CMFB
OutN
OutP
R=3R_o/2
R_o
b_1
b_0
b_2
Vrefn
b=011
Vrefp
b_2
b_1
b_0
OutN
OutP
R=2R_o/3
R_o
b_2
b_1
b_0
Vrefn
b=111
b)
Vrefp
b_2
b_1
b_0
OutN
OutP
R_o
R=2R_o/3
b_1
b_0
b_2
Vrefn
b=011

Figure 18: Differential output resistance for 2-bit a) differential DAC. b) Complementary DAC.

and

$$S_{ID} = 4kT\gamma g_m \tag{14}$$

respectively [15]. I_u is the unit current, V_u the voltage across the unit transistor or resistor, g_m the transconductance, k is Boltzmann constant, T the absolute temperature, and γ the channel noise factor. The noise is minimized with a small transconductance; however, the smallest transconductance for MOS current source is obtained at the boundary between the triode and active region with $V_{od} = V_{ds} = V_u$, resulting in $g_m = 2I_u/V_u$, assuming the long-channel equations are valid. The noise of the MOS current source is at least twice that of the resistor for a γ of unity in (14). Typically, the transconductance and noise power becomes 2-4 times larger for the MOS current source than for the resistor, as e.g. a cascode current source further reduces the voltage headroom for the transistor.

4.1.2 Output impedance

It is well-known that a signal dependent output impedance of a DAC, together with a non-zero load impedance, results in distortion of the signal [51,65]. For that reason, the output impedance of the DAC is often boosted with cascode transistors. As an example of signal dependent impedance, the differential output impedance of a 2-bit differential DAC is depicted for the codes b='111' and b='011' in Fig. 18a. As the varying impedance may degrade the performance due to distortion, it is not advisable to use this architecture in a low-impedance resistive DAC.

On the other hand, the complementary DAC in Fig. 18b is more suited for resistive DACs, as it has a constant output impedance with control word, which preserves the linearity although the impedance is low.

Also note that the complementary resistive DAC in Fig. 17c does not require a CMFB circuit. This is easily realized by observing that the DSM provides a short between Out_P and Out_N in Fig. 18b (the virtual ground of the integrator), that causes the common-mode to be centered between V_{refp} and V_{refn} if the unit resistors are identical.

4.2 Flash ADC

The requirements on the flash ADC are low since any errors injected in the ADC such as clock jitter, DC offset, thermal noise, and distortion are shaped by the loop. However, the flash ADC should have a low input capacitance to minimize the capacitive loading and loss in GBW of the last integrator.

Furthermore, the delay from the ADC input to the actual sampling event of the signal introduces a loop delay. This delay should be taken into account to preserve the loop dynamics (position of poles and zeroes in the NTF), by e.g. delaying the ADC clock with the same amount as the delay [30]. In case preamplifiers are used in the comparators, the delay can be reduced with a higher bandwidth in the input stage of the preamplifier.

4.3 Active-RC Integrators

DSMs often use active-RC integrators with an ideal, closed-loop integrator transfer-function of $A_{t\infty} = -1/sRC$, and an actual, non-ideal transfer-function of A_t which deviates from $A_{t\infty}$. This section examines these deviations in A_t based on a model of the integrator.

The active-RC integrator has an active part and two passives R, C that performs the voltage-to-current conversion and integration, respectively, shown in Fig. 19a. The active part is modelled by a single transconductance g_m, but may contain multiple, frequency dependent amplifier stages that will add additional poles to the circuit (e.g. g_m is frequency dependent). The input and output capacitance c_i and c_o, and the output resistance r_o, model the impedances seen at those nodes[8].

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[8] For example, r_o models both the output conductance of the amplifier and the load resistance from the input resistors of the following integrator; c_i includes the capacitance

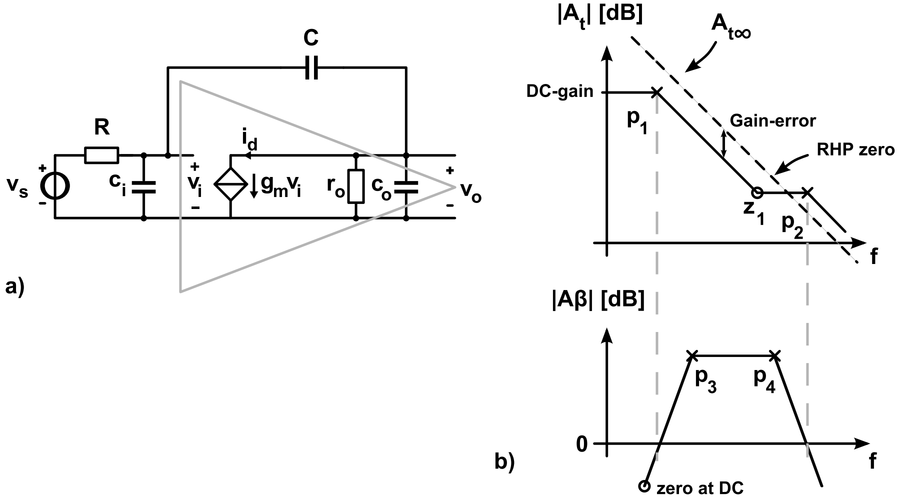

Figure 19: a) Active-RC integrator modelled with g_m and r_o. b) Sketch of integrator transfer function A_t, compared against $A_{t\infty}$ and the loop gain $A\beta$.

For a qualitative understanding, the integrator transfer function A_t is sketched together with the loop gain (described in section 4.3.1) in Fig. 19b. The following unwanted deviations from $A_{t\infty}$ can be identified due to the finite transconductance:

- Finite DC gain (p_1)
- Gain error at intermediate frequencies
- RHP zero (z_1)
- High-frequency pole (p_2)

The finite DC gain causes the integrator pole to shift from its ideal position at DC to p_1, which reduces the suppression of quantization noise in the DSM [51]. The limited loop gain at intermediate frequencies introduces a gain error that decreases the gain of the integrator by a factor GE, i.e. $A_t = GE \times -1/sRC$. At high frequencies, an extra high-frequency pole p_2 is present. The LHP pole mainly causes a phase retardation in A_t, equivalent to a delay of the feedback pulses, which will alter the NTF. Both the gain error and p_2 are not desired in the integrator transfer function and can be modelled and compensated with the approach in [47, 48].

The RHP zero z_1 introduces a phase retardation in A_t. z_1 may almost cancel with p_2 in the magnitude response of the transfer function A_t. However, they

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from the amplifier input and DAC output.

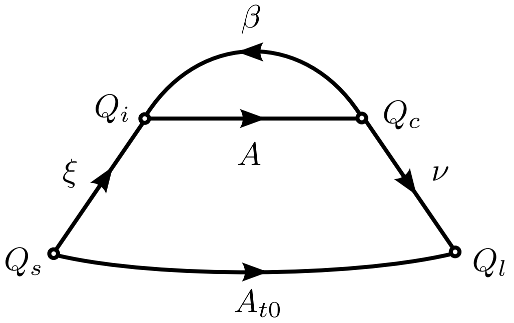

Figure 20: Superposition feedback model.

do not cancel in the phase response as they are located in different s-domain half-planes. The zero appears due to the non-inverting direct path from input to output of the integrator, via the integrator capacitor C (same effect as in a pole-split/Miller compensation). As usual, the RHP zero can be removed by inserting a small resistor in series with the integrator capacitor to move the zero towards infinity [66], also described in section 4.3.3.

It was qualitatively shown above that the deviations in A_t from $A_{t\infty}$ is caused by the limited loop gain of the integrator. For a quantitative understanding of the effects, an analytic expression for A_t is needed. While A_t can be found using straightforward nodal analysis of the integrator [67], this often results in large expressions in presence of more complex circuits that lack insight as to what design parameters are important. Thus, we proceed by introducing a method for calculating A_t that relates the loop gain $A\beta$ to A_t.

4.3.1 Superposition feedback model

This section describes how the integrator transfer function A_t can be found using the superposition feedback model [68–75] shown in the signal flow graph of Fig. 20, also referred to as return-ratio analysis [76, 77]. Moreover, the method is used in the stability analysis of the positive feedforward/feedback frequency compensation, described in Appendix B.

The superposition model describes the transfer from the source Q_s to the load Q_l, where the quantities Q represent either voltages or currents in the circuit. The model includes input and output circuit loading, ξ and ν respectively, and a direct path A_{t0} from the source to the load, that typically occurs via the bilateral feedback network[9]. Q_i and Q_c are the input and output of the controlled source, respectively, that provides the gain A and has a feedback path β. The transfer function from the input source to the controlled source is ξ and from the controlled source to the load is ν. For example, in Fig. 19a, $\{Q_s, Q_l, Q_i, Q_c, A, \beta\} = \{v_s, v_o, v_i, i_d, g_m, v_i/i_d\}$.

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[9] E.g. for A=0, there exists a transfer from source to load (contrary to Blacks feedback model [78] which assumes a unilateral feedback network).

In general, the closed loop transfer function can be written as

$$A_t = \frac{v_o}{v_s} = \underbrace{\left(A_{t0} - \frac{\nu\xi}{\beta}\right)}_{A_{t\infty}} \frac{-A\beta}{1 - A\beta} + \frac{A_{t0}}{1 - A\beta}, \tag{15}$$

where A and β form the feedback loop with loop gain $A\beta$, also known as the return ratio [76][10]. The second term in (15) includes the direct path A_{t0} and can in many cases be neglected, as shown later.

$A_{t\infty}$ is found by calculating the transfer from source to load with $A \to \infty$[11]. Using this approach, the transfers ξ, ν, and A_{t0} do not need to be calculated individually, as they are already included in $A_{t\infty}$. As is clear from (15), a large loop gain is desired (at all frequencies) for A_t to approach the ideal integrator transfer function $A_{t\infty}$.

A high loop gain is also desired to terminate the current-mode feedback DACs in the DSM with a low impedance node. The impedance at the virtual ground of the amplifier can be found using Blackman's impedance formula [76],

$$Z_i = Z_i|_{A=0} \frac{1 - A\beta|_{sc}}{1 - A\beta|_{oc}} \tag{16}$$

where $Z_i|_{A=0}$ is the impedance at the virtual ground node for zero gain in the amplifier, and $A\beta|_{sc}$ and $A\beta|_{oc}$ are the loop gain for a shorted and open circuited node, respectively ($A\beta|_{sc} = 0$ for the active-RC integrator in Fig. 19).

4.3.2 Transfer function

This section uses the method from the previous section to analytically show the loop gain and the integrator transfer function, as previously illustrated in Fig. 19b.

The super-position feedback model applied to Fig. 19a yields the loop gain,

$$A\beta = \frac{-sRCg_m r_o}{s^2(RCr_oc_i + RCr_oc_o + r_oc_oRc_i) + s(RC + r_oC + r_oc_o + Rc_i) + 1} \tag{17}$$

which confirms the zero at DC (caused by the integrator capacitor) and the two poles sketched in Fig. 19b.

The integrator transfer function is

$$A_t = \frac{-g_m r_o(1 - sC/g_m)}{s^2(RCr_oc_i + RCr_oc_o + Rc_ir_oc_o) + s(RC + RCg_m r_o + r_oC + r_oc_o + Rc_i) + 1} \tag{18}$$

---

[10] Return ratio should not be confused with the return difference, F=1-$A\beta$.

[11] $A_{t\infty}$ is (usually) not equal to $1/\beta$, and the β here must not be confused with the β in Blacks feedback model. For the special case of unity ξ, and ν and zero A_{t0}, the superposition model coincides with Blacks feedback model [78] and $A_{t\infty} = 1/\beta$.

with a DC gain of $g_m r_o$ and an RHP zero given by

$$z_1 = \frac{g_m}{C}. \tag{19}$$

The direct path A_{t0} in (15) contributes to (18) with only the zero in the numerator. The remaining part of (18) (e.g. the finite DC gain, the poles, and the gain error) is given by the first term of (15) (i.e. neglecting A_{t0}). It is therefore in many cases sufficient to only study the loop gain and $A_{t\infty}$ when analysing A_t.

The gain error is found by the ratio between A_t and $A_{t\infty}$ at intermediate frequencies,

$$GE = \frac{g_m r_o RC}{RC + RCg_m r_o + r_o C + r_o c_o + Rc_i} \approx \frac{g_m R}{1 + g_m R} \tag{20}$$

It is seen that the gain error is mainly caused by the input resistor that loads the integrator output via the integrator capacitor (assuming it acts as a short at intermediate frequencies). Thus, the input resistor should be chosen as large as possible, without degrading the thermal noise [6] of the integrator.

The poles in A_t are (assuming the poles are well separated in frequency[12])

$$p_1 = -\frac{1}{RC + g_m r_o RC + r_o C + r_o c_o + Rc_i} \approx -\frac{1}{g_m r_o RC}, \tag{21}$$

and,

$$p_2 = -\frac{RC + g_m r_o RC + r_o C + r_o c_o + Rc_i}{RCr_o c_i + RCr_o c_o + Rc_i r_o c_o} \approx -\frac{g_m C}{Cc_i + Cc_o + c_i c_o}. \tag{22}$$

p_1 moves towards the ideal position of zero with a higher output resistance r_o, leading to a higher DC gain of the integrator. A large DC gain is desired to reduce the quantization noise, as previously mentioned.

It is interesting to note that a large integrator capacitor C is desired to push p_2 to higher frequencies, for less phase shift (in particular, C larger than c_i and c_o is beneficial). This is also intuitively clear as the integrator feeds back more signal, that enlarges the loop gain (yields a higher β), which increases the unity loop gain frequency for the integrator. Also note that increasing g_m of the input stage by means of more current and larger devices, increases the input capacitance c_i that may in the end reduce p_2.

4.3.3 Series resistor R_z with integrator capacitor

This section describes the usage and impact of the commonly used resistor in series with the integrator capacitor. It also briefly describes how a phantom-zero can be used to improve the phase margin of such an integrator.

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[12] Typically, $|p_2| >> |p_1|$. p_1 and p_2 are then found from identification between the denominator of (18) and $s^2/(p_1 p_2) + s(-1/p_1 - 1/p_2) + 1 \approx s^2/(p_1 p_2) + s(-1/p_1) + 1$.

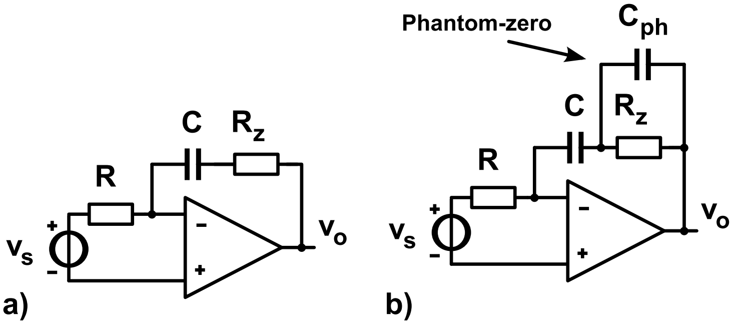

Figure 21: Active-RC integrator with a) series resistor. b) series resistor and phantom-zero compensation.

Active-RC integrators with a series resistor R_z (Fig. 21a) are frequently used in DSMs for two reasons: either the resistor can cancel the RHP zero (z_1) in A_t [66], for the same reason that a series resistor is often used in a Miller/pole-split frequency compensation. In this case, R_z is in general small, as it is chosen based on the transconductance of the amplifier that may be very large. Alternatively, R_z can be large to implement an LHP zero in A_t, to realize a PI loop-delay compensation of the DSM, already described in Section 3.4.1. The LHP zero enables to compensate for the fixed loop delay that is caused by intentionally clocking the feedback DACs with a delayed clock.

In both cases, R_z is used to preserve the system-level performance of the DSM by in the former case cancel an RHP zero (applied in [2, 3]), and in the latter case implement a wanted LHP zero in A_t for loop-delay compensation (applied in [5]). The following section shows how R_z impacts the performance of the integrator itself.

Impact on loop gain and phantom zero compensation

A loop gain simulation (Fig. 22) with Spectre STB-analysis of the fifth integrator in [5] shows that R_z decreases both the unity loop gain frequency (GBW) and the phase margin, from 1.5 GHz and 46° to 1.1 GHz and 26°, respectively. The decreased unity loop gain frequency leads to more delay in the integrator, from the lower unwanted high-frequency pole in the integrator transfer function (e.g. p_2 in Fig.19b).

By including R_z in the previous loop gain analysis given in (17), it can be shown that R_z reduces the frequency of the poles (i.e. p_3 and p_4 in the loop gain of Fig.19b), and introduces an additional high-frequency pole that retards the phase margin, also observed in [79]. The loss in GBW from R_z is intuitively explained by the increased feedback network impedance, which

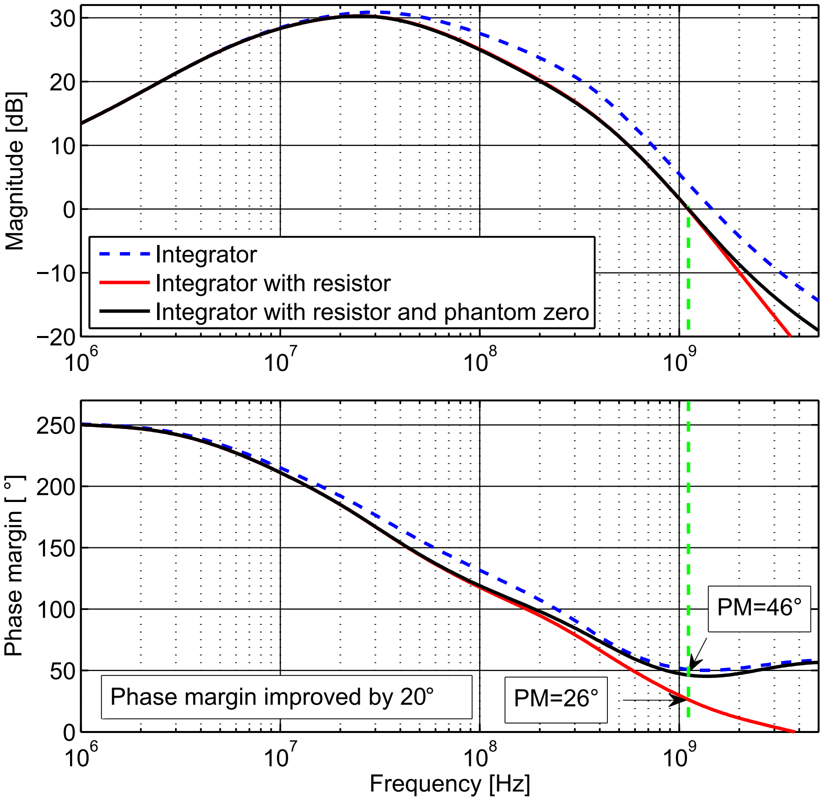

Figure 22: Spectre STB loop gain simulation of active-RC integrator. Pure integrator, integrator in Fig. 21a, and b.

reduces the amount of signal that is fed back (less β), thereby decreasing the loop gain.

The phase retardation can be counteracted with a capacitor in parallel with R_z as shown in Fig. 21b, referred to as phantom-zero frequency compensation [70–73, 80]. The capacitor implements a high-frequency zero at 1.2 GHz in the loop gain that restores the PM to 46°, as seen in Fig. 22.

Chapter 5

Paper Summary and Conclusions

This chapter presents a summary and conclusion of the results obtained in the research papers. The author's contributions to each paper are also stated.

5.1 Summary

Paper I analyses the impact of transistor threshold voltage mismatch in current-steering feedback DACs, often used within DSMs. It is well-known that mismatch between MOS current sources in current steering DACs affects the static linearity of the DAC and degrades SNDR. However, this paper shows that the current-switching pair (directing the current source) is sensitive to mismatch and degrades the dynamic performance of the DAC, causing a loss in SNDR (in the order of 10 dB). The $\mathrm{V_{th}}$ mismatch in the current-switching pair gives an asymmetric feedback pulse when switching from zero to one and vice versa. When switching, the source node of the current-switching pair sees a voltage step with amplitude equal to the $\mathrm{V_{th}}$ mismatch. This voltage-step is then converted into a current pulse by the source node capacitance, similar to the flicker noise up-conversion [81] in active mixers. A model of the mismatch is derived using a small-signal circuit analysis and implemented in VerilogA. The effect of mismatch is studied for a 3^{rd}-order, 3-bit CT DSM with simulations of the VerilogA model, investigated both for return-to-zero (RZ) and non-return-to-zero (NRZ) feedback DACs, with and without dynamic element matching (data-weighted averaging, DWA).
Conclusion: All cases except RZ DAC with DWA show a large degradation in both SNDR and SFDR performance, while an RZ DAC with DWA almost recovers the ideal performance of the modulator. The SNDR degradation can be reduced by minimizing the product between the source node capacitance and the offset caused by mismatch. The transconductance of the current-switching pair does not affect SNDR, as it only changes the form of the pulse but not the area. A VerilogA DAC model was developed that shows excellent agreement with component-level spectre simulations, and enables a fast exploration of the design space.

Contribution: I did the analysis, modeling, simulations, and manuscript writing.

Paper II describes a method to improve the robustness against variations in loop delay in the DSM. A loop delay that differs from the nominal case can give performance degradation and instability of the circuit. The loop delay varies due to e.g. process variations of the delay in the feedback DAC, the GBW of the amplifiers in the loop filter, or the delay in the flash ADC (e.g. the preamplifiers).

An RZ pulse is used in the innermost feedback path which has the highest sensitivity to loop delay, while NRZ pulses are adopted in the outer feedback paths to reduce the sensitivity to clock jitter and lower the integrator slew rate requirements. The RZ pulse allows to omit an additional DAC for loop delay compensation. In addition, a quadrature clock enables to center the RZ pulse in the middle of the sampling period to make the DSM more robust against loop delay variations, compared with a conventional NRZ pulse.

The concept was implemented in a 3^{rd}-order, 3-bit CT DSM in a 65 nm CMOS process for an LTE radio receiver, where it achieves an SNR of 71 dB and an SNDR of 69 dB over a 9 MHz bandwidth, for a power consumption of 7.5 mW from a 1.2 V supply. The quadrature clock required to center the RZ pulse is included in the power consumption, and was generated using an on-chip frequency divider. The multibit feedback DACs are complementary resistive instead of current-steering to reduce the thermal noise from the DAC.

Conclusion: The NRZ/NRZ/RZ feedback scheme is introduced and a 288 MHz, 3^{rd}-order, 3-bit, CT $\Delta\Sigma$ prototype is measured. The RZ pulse, centered in the clock period, improves the robustness to loop delay variations and removes the need for an additional DAC for loop-delay compensation in the modulator.

Contribution: I did the modeling, simulations, implementation, most of the layout, measurements, and manuscript writing.

Paper III extends the results of paper II with more analysis and measurement results.

The proposed NRZ/NRZ/RZ scheme causes a small error in the first sample of the impulse response that is modelled with a discrete-time model. An expression for the error is derived for arbitrary rectangular pulses with less than one clock period loop delay. The discrete-time model is used to analyze the impact on performance and stability of the modulator with time domain simulations using Schreiers toolbox and with a pole-zero plot using linear analysis, respectively. The analysis shows that the modulator performance and stability are negligibly affected.

The modulator was measured with OFDM modulated signals to analyze the overload behavior and tolerance to out-of-band LTE blockers.

Conclusion: The NTF, STF, SNDR, and stability are negligibly affected with

the NRZ/NRZ/RZ feedback scheme. Measurements verify that the lowpass characteristic of the feedback modulator improves the tolerance to out-of-band OFDM blockers.
Contribution: I did most of the analysis, measurements, and manuscript writing.

Paper IV presents the first of two filtering ADCs. A 3rd-order CT DSM is incorporated into a 2nd-order Tow-Thomas low-pass channel select filter (CSF) to create a filtering ADC. The key advantage of the filtering ADC is that the DSM noise is now suppressed by the global feedback loop of the CSF. The design provides an additional 2nd-order suppression of noise and distortion from the DSM, that improves the SNDR of the DSM by 14 dB. This allows using a much simpler DSM, or to benefit from the improved noise performance. The suppression occurs below the CSF cutoff frequency, and attenuates quantization noise, thermal and flicker noise, and distortion coming from the DSM. The filtering ADC behaves like the CSF and DSM cascade typically used in radio receivers, with the added benefit of noise suppression.

A two-stage amplifier with AC-coupled push-pull output stage is used to obtain a large loop gain with improved linearity (IM3 improved by 15 dB), and to deliver a high dynamic current to accommodate the strong out-of-band blockers present in the LTE receiver. A positive feedforward/feedback frequency compensation enables boosting the loop gain in the signal band by having imaginary loop poles. The unity loop-gain frequency is improved compared to the Miller compensation, and a robust phase response with a plateau at 70 degrees phase margin is achieved. Design equations are given.

The input referred noise, compression point, and 2nd- and 3rd-order intercept point are measured to characterize the circuit as a filter. The 65 nm CMOS prototype is clocked at 288 MHz and has a 9 MHz LTE bandwidth, an input-referred noise of $8.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 12 dB gain, and an in/out-of-band IIP3 of $11.5/27\,\mathrm{dBV_{rms}}$, with a power consumption of 11.3 mW, resulting in state-of-the-art FOMs compared with other filtering ADCs.
Conclusion: A filtering ADC was implemented that enables an additional 2nd-order suppression of DSM noise and distortion, compared to having the CSF and DSM in a cascade. The in-band noise is suppressed by 14 dB which enables using a DSM with four times lower power consumption. A high linearity is achieved using amplifiers with push-pull output stages and positive feedforward/feedback compensation. The concept was verified by measurements of a 288 MHz filtering ADC having a 2nd-order Butterworth characteristic and in total 5th-order noise shaping.
Contribution: I did the analysis, modeling, simulations, implementation, layout, measurements, and manuscript writing.

Paper V presents the second filtering ADC. A 2nd-order DSM is merged with a 3^{rd}-order CSF, to provide a 3^{rd}-order additional noise suppression which improves the SNDR of the DSM by nearly 20 dB. The higher noise suppression is achieved by shifting two of the three zeros in the CSF from DC to the CSF band edge. Compared with the previous prototype, this design has better selectivity, lower input-referred noise, twice the bandwidth and clock frequency, and significantly lower power consumption.

When the DSM is merged with the CSF, the Chebyshev filter function is affected by the delay of the DSM and feedback DAC. The delay mainly causes a bandwidth expansion in the Chebyshev function, which is analytically compensated by adjusting the CSF coefficients to restore the original Chebyshev filter function.

In the loop filter, a phantom-zero frequency compensation improves the phase margin of the last active-RC integrator, without a loss in bandwidth or increase in power consumption. The AC-coupled push-pull amplifier is power-efficiently biased with a DC current less than the strong, high-frequency TX-leakage current.

Three chips were measured, and show very similar performance in terms of blocker tolerance, linearity and noise. The 65 nm CMOS prototype is clocked at 576/288 MHz with an 18.5/9 MHz LTE bandwidth, and has 26 dB gain, an input-referred noise of $5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and an in/out-of-band IIP3 of -8.5/20 dBVrms, with a power consumption of 7.9/5.4 mW for 2xLTE20/LTE20 mode. The three 576/288 MHz prototypes are benchmarked against 3GPP requirements for LTE Rel. 11 with measurements of OFDM modulated blockers, and support for two contiguous channels (2xLTE20).

Conclusion: A filtering ADC with 3^{rd}-order Chebyshev filter function, and 5^{th}-order overall noise shaping is implemented, and verified by measurements. The fundamental filter properties are kept, such as the sharp 3^{rd}-order Chebyshev response, the low input referred noise, and an IIP2, IIP3, and blocker tolerance rising with frequency. The SNDR requirement of the DSM is relaxed by 20 dB, which in theory allows using a DSM with eight times less power. An improved phase margin was achieved with a phantom zero frequency compensation.

Contribution: I did the analysis, modeling, simulations, implementation, layout, measurements, and manuscript writing.

Chapter 6

Discussion and Future Work

This dissertation has presented several high performance data converters together with analysis of the proposed ideas; nevertheless, improvements are possible. This section presents concluding remarks, challenges, and ideas that are left for future researchers to pursue that the author did not have the opportunity to carry out himself.

The power efficiency of the third-order DSM (first prototype) can be further improved by for example using the two-stage push-pull amplifier instead of a folded-cascode. These amplifiers are much more linear, and can tolerate a larger voltage swing at the output from dynamic range scaling, which relaxes the noise requirements of the following integrators and allows their power consumption to be scaled down.

The dissertation shows that a NRZ/NRZ/RZ feedback scheme, where an RZ pulse in the innermost DAC, centered in the clock period, reduces the sensitivity to loop delay variations. Furthermore, simulations have shown that the RZ pulse also reduces the GBW requirements of the last amplifier by a factor two, as expected from the reduced loop-delay sensitivity; However, it is well known that a finite GBW anyway can be compensated by adjusting the CT coefficients. For that reason, it would be interesting to study whether the NRZ/NRZ/RZ feedback scheme enables to compensate for lower GBWs than an all NRZ feedback scheme.

In systems where twice the clock frequency is not available, it is desired to generate the RZ pulse without a frequency divider. For the NRZ/NRZ/RZ feedback scheme, the RZ DAC is located in the innermost path, where the requirements in clock jitter and linearity are very low due to shaping of the loop. Furthermore, the position of the pulse in the clock period does not have to be accurately generated. The low requirements of the RZ pulse suggests that it could be generated in a power efficient way, where a simple approach is to use an inverter delayed version of the reference clock, or possibly a delay-locked loop (DLL) locked to the same reference clock.

The DWA dynamic-element matching technique is successfully used in all of the implemented chips to linearize the feedback DACs. Although the measurements show no indication of problems but rather improvements with DWA, it is known that DWA in combination with NRZ pulses produces even order tones in presence of ISI. For that reason, it would be interesting to study the ISI shaping proposed by Risbo [53] to reduce the burden on the analog design and layout.

The concept of filtering ADCs has been successfully verified with two chips, where both designs achieve state-of-the-art performance and the second filtering ADC essentially meets the requirements for the cellular standard LTE Rel. 11. Nevertheless, it is interesting to study how the power consumption of the A/D converting part (the DSM) can be further reduced to fully exploit the low requirements on the DSM.

Further investigation is also needed on how to improve the chip-to-chip variations of the signal transfer function in the filtering ADC. Measurements of the second filtering ADC in Appendix A suggests that the variations come from the second order $\Delta\Sigma$ modulator.

A resistive input was used for the first integrator to emulate the LNA-mixer interface. While this is a reasonable model, the filtering ADC concept should be verified by measurements of a complete receiver chain that includes the LNA and mixer; a project that is ongoing at the department of electrical and information technology in Lund University.

Appendix A

Additional measurement results

This appendix contains measurement results for the filtering ADC in [5], that were not included in the paper due to limitations in length. The measurements consist of an FFT of the output signal, the blocker tolerance at the duplex distance for an 18 MHz modulated blocker, and further measurements of the chip-to-chip variations in the STF.

The filtering ADC was implemented in ST 65 nm CMOS process, with the die wire-bonded in a CQFP 44 package for testing. The design can operate in 2×LTE20 or LTE20 mode with 18.5 MHz or 9 MHz bandwidth, respectively. The DSM loop-filter coefficients can be configured for f_s=576/288MHz independently of LTE mode, where in normal operation the sampling frequency (roughly) tracks the LTE BW of 18.5/9 MHz.

The input signal is generated by a Rohde & Schwarz SMU 200A vector signal generator, with a Mini-Circuits SLP-2.5+ filter for in-band linearity measurements. The clock is generated by an HP E4432B RF signal generator, and the 3-bit output data is collected with an Agilent 16962A logic analysis module with differential probes, triggered by the clock output from the chip. The signal spectra were obtained by FFTs in Matlab, after Hann windowing and averaging. Three different chips have been tested for both 2×LTE20 and LTE20 mode.

A.1 FFT

An example of output signal spectrum is shown in Fig. 23 for a −1 dBFS, 2.0 MHz CW input. The thermal noise of the 1st CSF integrator dominates the noise floor, masking the 3rd-order suppression of DSM noise.

A.2 Blocker tolerance

To investigate the tolerance to blockers, the in-band noise vs. blocker power is measured. The performance is characterized by P_{1dB}, which we define as the input power for which the in-band noise rises by 1 dB compared to its zero-input level.

Depending on the type of interference specified in the 3GPP [9], P_{1dB} was measured using either a modulated blocker or a CW input. In addition to

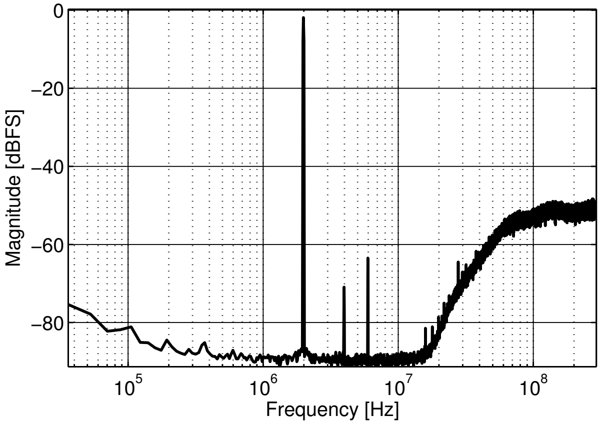

Figure 23: 32768-point FFT for a −1.0dBFS input tone. HD2 is −68.9 dBc and HD3 is −61.5 dBc. 2×LTE20 mode.

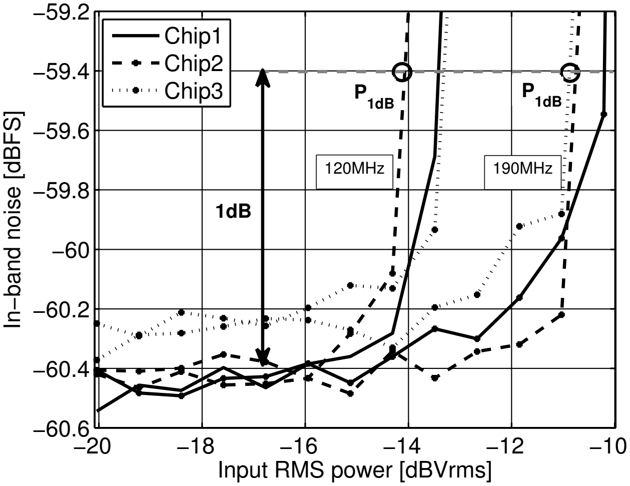

Figure 24: In-band noise vs. input power for an 18 MHz SC-FDMA signal at 120 MHz and 190 MHz. 2×LTE20 mode.

the measurements in [5] with 5 MHz modulated blocker, the tolerance to TX leakage was measured with an 18 MHz uplink blocker (modulated with SC-FDMA, based on QPSK, having a baseband PAR of 8 dB) located at either

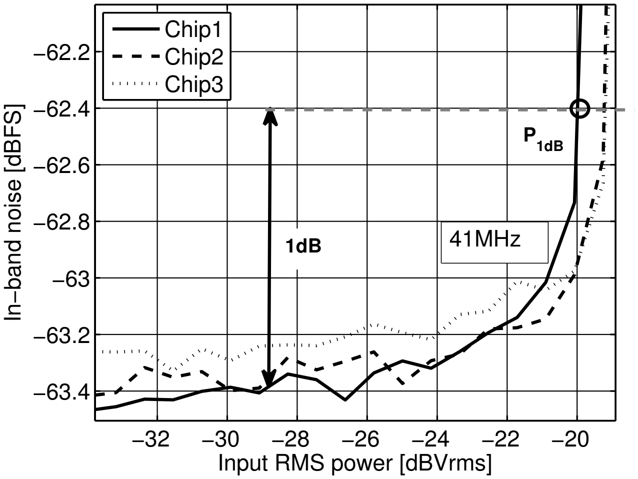

Figure 25: In-band noise vs. input power for an 18 MHz SC-FDMA signal at 41 MHz. LTE20 mode.

120 MHz or 190 MHz for band 7 and 20, respectively in 2×LTE20 mode, and at 41 MHz for band 20 in LTE20 mode. As shown in Figs. 24 and 25, $\mathrm{P_{1dB}}$ is $-14\,\mathrm{dBV_{rms}}$ at 120 MHz, $-11\,\mathrm{dBV_{rms}}$ at 190 MHz, and $-20\,\mathrm{dBV_{rms}}$ at 41 MHz.

As already mentioned in [5], the expected maximum TX leakage is $-18\,\mathrm{dBV_{rms}}$, which indicates that the TX leakage performance is 2 dB short for the worst LTE20 case, band 20.

A.3 Chip-to-chip variations

The measurements in [5] reported transfer function variations at intermediate frequencies between the filtering ADC chip 1 on one hand and chip 2 and 3 on the other. The largest variations are seen at the same frequency relative to the channel bandwidth in both 2×LTE20, and LTE20 mode, i.e. at a frequency around $f = 3 \times BW$ in both cases. The results for LTE20 mode are repeated for convenience in Fig. 26a.

The filtering ADC was also measured with the DSM operating at twice the clock frequency, while the CSF is left in LTE20 mode, see Fig. 26b. In this case, the variations are shifted up in frequency by roughly a factor two, centered around $f = 6 \times BW$. This suggests that the variations are related to the DSM, that operates at twice the clock frequency.

For completeness, the DSM was also measured stand-alone by disabling, and bypassing the CSF-part of the filtering ADC, Fig. 27. It is seen that chip

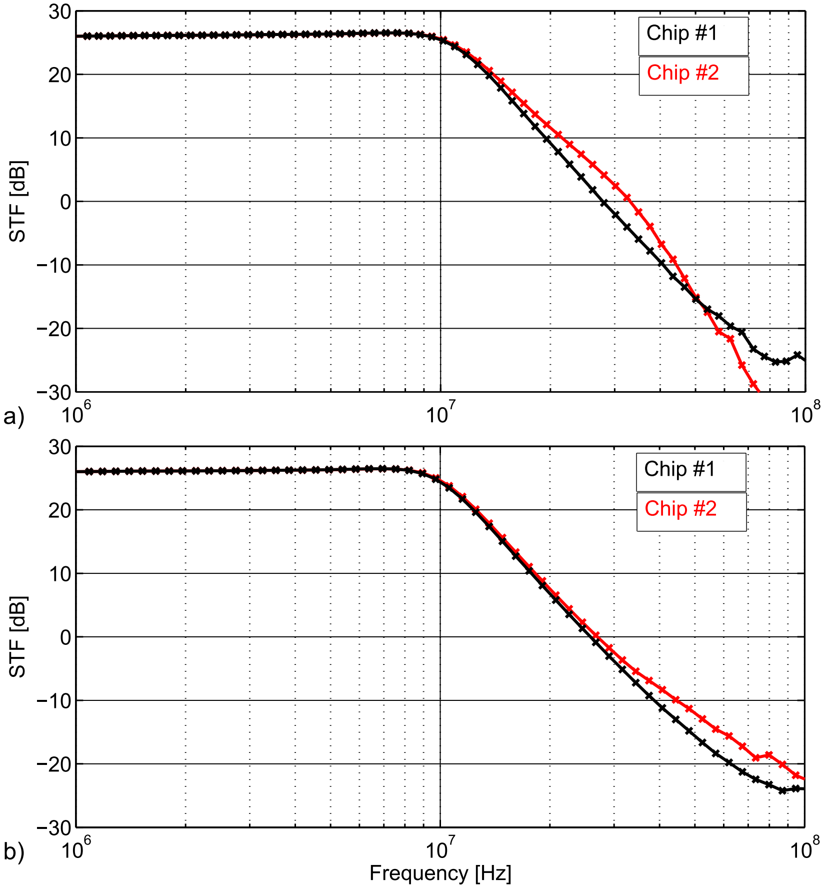

Figure 26: Measured transfer function of filtering ADC, BW=9MHz. a) f_s=288MHz. b) f_s=576MHz.

2 and 3 have similar transfer function, while chip 1 displays large deviations with slightly more peaking, and a much wider bandwidth with less phase shift in the band of interest.

It should be noted that no tuning or RC-calibration was performed on the different chips.

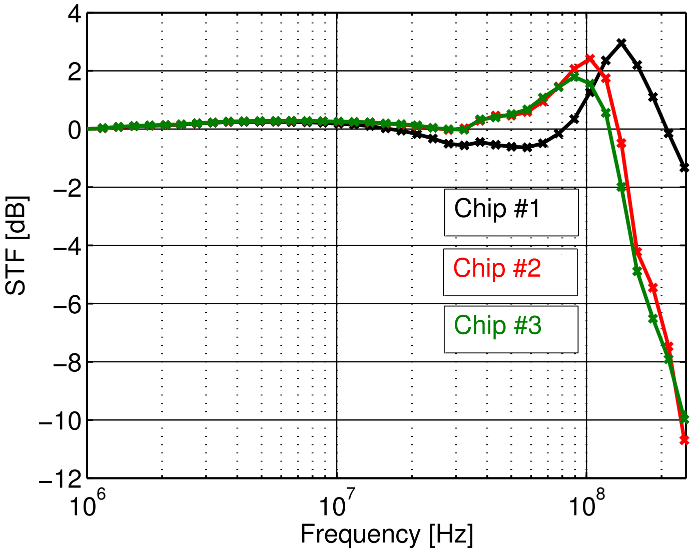

Figure 27: Measured transfer function of stand-alone DSM for f_s=576MHz.

Appendix B

Positive feedforward/feedback compensation

This appendix extends the analysis of the positive feedforward/feedback frequency compensation (PFC) of the amplifier, applied in [4]. The frequency compensation is performed by placing the high-frequency poles of A_t in the LHP with an appropriate Q value, where A_t is found from the loop gain of the integrator.

B.1 Overview

For convenience, the two-stage amplifier with AC-coupled push-pull output stage is repeated in Fig. 28. C_{pf} acts as a positive feedforward/feedback compensation [82] (PFC), and connects the positive output back to the positive input of the input stage as indicated by the signs in Fig. 28a. The bidirectional nature of C_{pf} results in both a positive feedforward and feedback path. The positive feedback loop acts as an anti pole-split [83–86] that causes the two loop poles to attract, and eventually become imaginary with increasing values of C_{pf}. Thus, the loop gain in the signal band is boosted by the imaginary loop poles. The positive feedforward path through C_{pf} yields an LHP zero in the loop gain, due to the non-inverting forward signal path (contrary to pole split/Miller compensation which presents an RHP zero). The feedforward path performs the frequency compensation, and stabilizes the amplifier by bending the root locus into the LHP, as illustrated in Fig. 28b. Thus, the closed loop poles in A_t can be positioned in the LHP, although the loop poles may reside in RHP from the beginning.

The compensation capacitor C_{pf} alters both the poles and the zero in the loop gain, which complicates the stability analysis. Furthermore, the two loop poles can not be estimated using a dominant pole approximation, as the poles are typically closely spaced due to the anti pole split mentioned previously. The following section analyses the compensation technique.

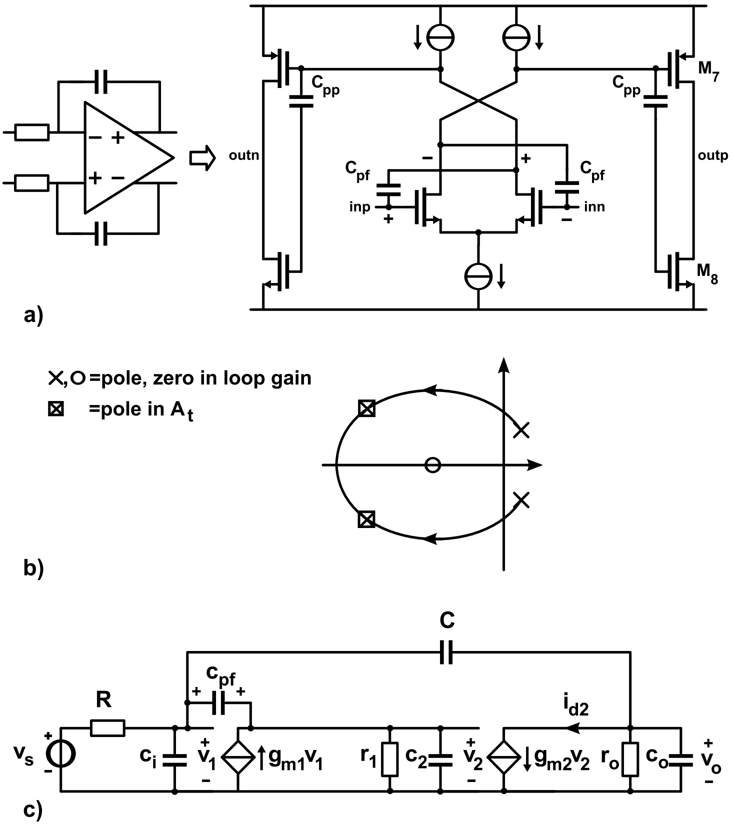
a)
C_pp
C_pp
M_7
M_8
outn
outp
C_pf
C_pf
inp
inn
X,O =pole, zero in loop gain
⊠ =pole in A_t
b)
C
C_pf
R
i_d2
v_s
c_i
v_1
g_m1v_1
r_1
c_2
v_2
g_m2v_2
r_o
c_o
v_o
c)

Figure 28: a) Amplifier with positive feedforward/feedback compensation via c_{pf}. b) Sketch of root-locus. c) Small-signal model.

B.2 Analysis

The integrator transfer function $A_{t\infty} = -1/(sRC)$ is found with $A = g_{m2} \to \infty$ in Fig. 28c and calculating the transfer from source to load[13].

The closed loop poles are found from the loop gain of the circuit, which is calculated assuming a large integrator capacitor compared with c_2 and c_3 (a realistic case)

$$A\beta = \frac{-g_{m2}r_1r_2(sc_{pf}+g_{m1})}{s^2r_1r_2\left[c_2c_3+c_{pf}(c_2+c_3)\right]+s\left[r_1(c_2+c_{pf})+r_2(c_3+c_{pf}(1-g_{m1}r_1))\right]+1} \qquad (23)$$

where $c_3 = c_o||c_i$, $r_2 = R||r_o$. It is clear that an LHP zero exists in the loop gain, located at $-g_{m1}/c_{pf}$.

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[13] This simple expression for $A_{t\infty}$ is a result of using g_{m2} instead of g_{m1} (that has local feedback) as forward gain A.

The closed loop poles in A_t are found using (15) and well predicted without the direct path A_{t0}. Identification with the denominator of a second order transfer function with a Q value and natural frequency ω_0, $s^2 + s\omega_0/Q + \omega_0^2$, yields

$$\omega_0 = \sqrt{\frac{1 + g_{m1}g_{m2}r_1r_2}{r_1r_2(c_2c_3 + c_{pf}(c_2 + c_3))}} \tag{24}$$

$$\begin{aligned} Q &= \frac{r_1r_2(c_2c_3 + c_{pf}(c_2 + c_3))\omega_0}{r_1c_2 + r_2c_3 + c_{pf}(r_1 + r_2 + r_1r_2(g_{m2} - g_{m1}))} \\ &\approx \frac{(c_2c_3 + c_{pf}(c_2 + c_3))\omega_0}{(g_{m2} - g_{m1})c_{pf}} \end{aligned} \tag{25}$$

From (25), it is seen that the closed loop poles can be placed in the LHP if $g_{m2} > g_{m1}$ (Q is positive). The approximate value of the compensation capacitor c_{pf} that provides a stable amplifier is found from (24), and (25),

$$c_{pf} \approx \frac{g_{m1}g_{m2}(c_2 + c_3)}{Q^2(g_{m2} - g_{m1})^2}, \tag{26}$$

where c_2 represents the total capacitance at the internal node of the amplifier, and c_3 the sum of the load and input capacitance of the amplifier (assuming a large integrator capacitor); g_{mi} are the transconductances in Fig. 28. For example, $Q = 1/\sqrt{2}$ yields two Butterworth closed loop poles, equivalent to a phase margin of 67° [87]. Note that the transconductances of the input and output stages may not be equal for a finite capacitor value, as clearly seen in the denominator of (26).

Finally, as mentioned previously, the loop gain can be boosted by having imaginary loop poles. As an example, the maximum loop gain is achieved if the loop poles are exactly on the imaginary axis, with

$$c_{pf} = \frac{r_1c_2 + r_2c_3}{(g_{m1}r_1 - 1)r_2 - r_1} \approx \frac{r_1c_2 + r_2c_3}{r_1(g_{m1}r_2 - 1)} \tag{27}$$

where a successful implementation is possible for $g_{m1}r_2 > 1$, to yield a positive value of c_{pf}.

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Paper I

Paper I

Impact of MOS Threshold-Voltage Mismatch in Current-Steering DACs for CT $\Delta\Sigma$ Modulators

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Impact of MOS Threshold-Voltage Mismatch in Current-Steering DACs for CT $\Delta\Sigma$ Modulators

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***Abstract*— This paper studies the impact of MOS threshold-voltage (V_{th}) mismatch in the switch pairs of the current-steering DAC used in the feedback path of continuous-time (CT) $\Delta\Sigma$ modulators. The V_{th} mismatch causes an asymmetric feedback pulse, whose effect is investigated both for return-to-zero (RZ) and non-return-to-zero (NRZ) feedback DACs, with and without dynamic element matching (data-weighted averaging, DWA). All cases except RZ DAC with DWA show a large degradation in both SNDR and SFDR performance, while a RZ DAC with DWA displays an (almost) ideal performance. A mismatch-aware DAC model has been developed in VerilogA, showing an excellent agreement with component-level spectre simulations and enabling a fast exploration of the design space.**

I. INTRODUCTION

Current steering DACs are often used in the feedback path of multi-bit CT $\Delta\Sigma$ modulators, where the CT integration demands a very accurate output from the feedback DAC connected to the integrators (in particular, to the integrator at the modulator input). In many cases, the area of the feedback pulse is more important than its exact position in time [1], [2]. Compared with RZ, a NRZ DAC is desirable because of reduced sensitivity to jitter, lower thermal noise, and relaxed slew rate requirements for the integrators. A drawback of NRZ modulators, on the other hand, is the sensitivity to inter-symbol interference (ISI) that may be caused by asymmetrical switching errors in the DAC [3].

This paper investigates the impact of the unavoidable V_{th} mismatch between the two MOS transistors in each DAC current-switching pair. The static performance of a current-steering DAC including mismatch effects, as well as its dynamic performance without mismatch effects, has been investigated in [4]. In the present paper, we show that also the dynamic performance of the DAC is affected by mismatches in each current-switching pair, where the V_{th} mismatch is particularly relevant. Such mismatch has an unexpectedly strong impact on the SNDR/SFDR of the $\Delta\Sigma$ modulator, even if the current sources are perfectly matched to each other (which will be assumed in the following).

A model of the mismatch is derived using a small-signal circuit analysis and further implemented in VerilogA, enabling both fast and accurate simulations.

A 3rd order, 3-bit CT $\Delta\Sigma$ modulator is simulated with both RZ and NRZ feedback DACs, both with and without DWA [5]. The RZ DWA modulator displays a superior behavior in terms of SNDR and SFDR.

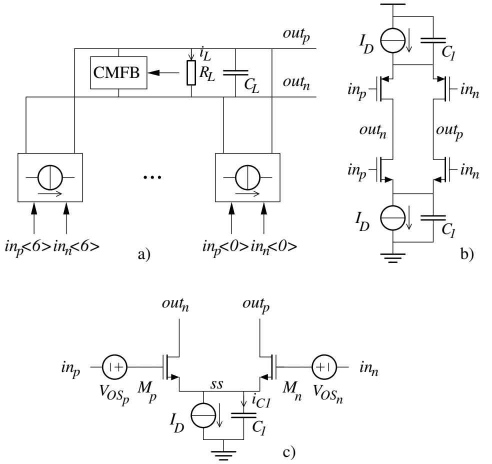

Fig. 1. (a) Block schematic of current-steering DAC with common-mode feedback and 7 unit current cells; (b) unit current cell in NRZ DAC with parasitic capacitor C_1; (c) NMOS current cell with C_1 and DC offsets V_{OS_p}, V_{OS_n}, accounting for the threshold-voltage mismatch between M_p and M_n.

II. VERILOGA MODEL OF THE CURRENT CELL

An N-bit current-steering DAC uses 2^N-1 thermometer-coded unit cells in parallel (Fig. 1.a), where each cell contains a PMOS and an NMOS current cell (Fig. 1.b). The NMOS current cell (Fig. 1c) contains the switch pair M_n, M_p, and a current source I_D with a parasitic capacitor C_1 in parallel. The switch pair is driven by a digital signal with limited swing, to operate the transistors in the saturation region. In the balanced state ($in_p = in_n$), I_D flows equally through M_p and M_n, and the transistors operate as a differential stage. In the switched state, all current flows through e.g. M_p, which then operates as a current follower for I_D and as a voltage follower for in_p to ss, with a DC shift of V_{GS}.

The different threshold voltages of M_p and M_n are modeled by the DC offsets V_{OS_p} and V_{OS_n} at the input of an ideal switch pair. For e.g. $V_{OS_n} = -V_{OS_p}$, the gate voltage of M_p

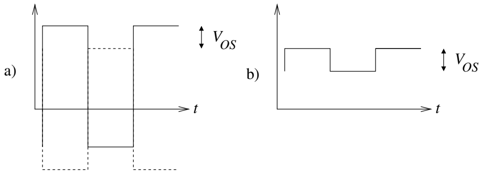

Fig. 2. (a) Solid: voltage at M_p gate; dashed: voltage at M_n gate; (b) Resulting signal at node ss.

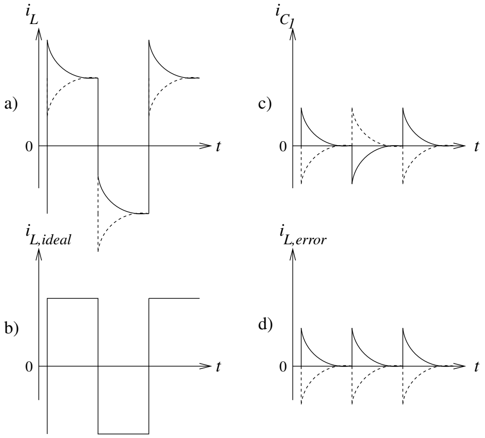

Fig. 3. Currents in one NMOS cell. Solid lines are for positive V_{OS}, dashed for negative. a) DAC differential output current i_L; b) ideal i_L (i.e., for $V_{OS} = 0$); c) Current i_{C1} through C_1; d) rectified i_{C1} as error current $i_{L,error}$ superimposed on $i_{L,ideal}$.

shifts up by V_{OS_p}, whereas the gate voltage of M_n shifts down (Fig. 2.a). For a periodic alternation between the two switched states, node ss becomes a square wave with an amplitude of $V_{OS} = V_{OS_p} - V_{OS_n}$ (Fig. 2.b). This square wave is then converted into current pulses by C_1. Depending on the sign and magnitude of V_{OS}, the current pulses shape the unit cell output current in different ways, see Fig. 3.a. As a consequence, the output current becomes asymmetric, causing the area of a '+1' pulse to differ from the area of a '-1' pulse.

To see how, we separate the DAC output current (Fig. 3.a) into two components: the ideal square wave current (Fig. 3.b), and the current pulses i_{C_1} generated by C_1 (Fig. 3.c). The switching pair alternately changes the sign of i_{C_1}, presenting the rectified error current $i_{L,error}$ at the cell output (Fig. 3.d). Thus, the DAC output current is the superposition of the current waveforms in (Fig. 3.b) and (Fig. 3.d). Interestingly, a very similar analysis was performed in [6] in the study of flicker noise up-conversion in active mixers.

The current generated by V_{OS} is calculated in a straightforward way by merging the two switched states of the cell into a single state [6], with e.g. M_p biased at $max(in_p)$ and M_n turned off (Fig. 4.a). The effect of V_{OS} is then modeled by the square-wave signal source v_s switching between V_{OS_p} and V_{OS_n}. The corresponding first-order small-signal model (V_{OS} being indeed small) is shown in Fig. 4.b. In the NRZ case, the transfer function from v_s to the output current i_o is

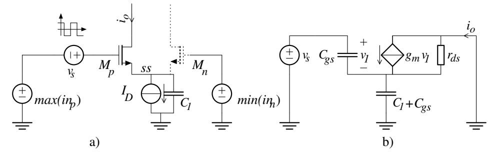

Fig. 4. a) Model of the NMOS current cell in presence of V_{th} mismatches V_{OS_p} and V_{OS_n}; b) Small-signal model (we assume for simplicity that M_n and M_p introduce identical C_{gs}, even if M_n is off and M_p is on).

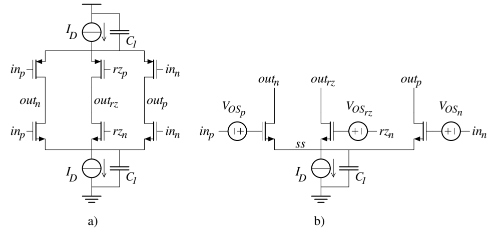

Fig. 5. a) Unit current cell in the RZ DAC with parasitic capacitor C_1; b) NMOS current cell with V_{th} mismatches V_{OS_p}, V_{OS_n}, $V_{OS_{rz}}$.

$$A_{t_{NRZ}}(s) = \frac{i_o}{v_s} \approx \frac{s(C_1 + C_{gs})}{1 + s(C_1 + 2C_{gs})/g_m}. \qquad (1)$$

For an applied unit step of V_{OS}, the current cell injects a charge (area) error Q_e equal to

$$Q_e = \int_0^\infty \mathcal{L}^{-1}\left(\frac{V_{OS}}{s}A_{t_{NRZ}}(s)\right) dt = (C_1 + C_{gs})V_{OS}. \quad (2)$$

It is noteworthy that the transistor transconductance g_m only affects the form of the current pulse i_L, but not the error charge Q_e, as clear from (2). Hence, to minimize Q_e, it is the product $(C_1 + C_{gs})V_{OS}$ that should be minimized. As a first-order approximation, C_1 is proportional to the transistors width W (including that of the devices implementing I_D), while C_{gs} is proportional to the transistors area WL (where L is the transistors length). On the other hand, it is well known that V_{OS} is proportional to $1/\sqrt{WL}$. There are therefore optimal values for W, L minimizing Q_e; these optimal values, however, are strongly process-dependent.

A RZ current cell has also been implemented to further investigate the effect of V_{th} mismatches, see Fig. 5. All transistors operate in the saturation region and node out_{rz} is biased at $V_{dd}/2$. The additional offset $V_{OS_{rz}}$ introduces a third voltage level at node ss during RZ mode. Analogously to (1), the small-signal analysis of Fig. 5.b yields

$$A_{t_{RZ}}(s) \approx \frac{s(C_1 + 2C_{gs})}{1 + s(C_1 + 3C_{gs})/g_m} \qquad (3)$$

When the circuit goes into RZ mode, i_{C1} is discharged to out_{rz} and does not affect the output. However, when returning

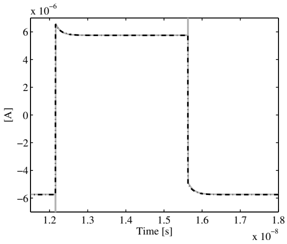

Fig. 6. Transient output current of the NRZ current cell for a logic input of +1,-1 (V_{OS_p}=5mV, V_{OS_n}=-5mV). Grey (solid): component-level simulation; black (dashed): VerilogA model.

TABLE I

COMPONENT PARAMETERS

Parameter	Value
NMOS (W/L)	$1\mu m/0.2\mu m$
PMOS (W/L)	$2\mu m/0.2\mu m$
I_D	5.75μA
C_1	10fF
$\sigma(V_{OS_{p,n}})$	7mV

back from RZ mode, a voltage step of $V_{OS_p} - V_{OS_{rz}}$ (or $V_{OS_n} - V_{OS_{rz}}$) occurs at node ss, depending on the input signal. This results in a current pulse with a signal-dependent charge error of

$$Q_e = \begin{cases} (C_1 + 2C_{gs})(V_{OS_p} - V_{OS_{rz}}) & \text{for } in_p > in_n, \\ -(C_1 + 2C_{gs})(V_{OS_n} - V_{OS_{rz}}) & \text{for } in_p < in_n. \end{cases}$$

Again, Q_e is independent of g_m, as in the NRZ case. Contrary to NRZ operation, however, a RZ DAC resets all current cells at every clock cycle. It will be clear that this has a momentous impact on the behavior of the modulator.

A 3-bit NRZ DAC has been modeled using VerilogA, incorporating the mismatch of the switch pairs. The DAC model contains two vectors of offset voltages and one vector for the internal node ss. Each offset pair and ss node correspond to a switch pair in the DAC. The voltage at each ss node generates the corresponding current $i_{L,error}$ (via the inverse Laplace transform of (1)), which is added to the ideal DAC output current (in our case, half of $i_{L,error}$ flows through the load, and the other half into the CMFB circuit).

A similar model for the RZ DAC was implemented using the transfer function in (3). In this case, a third offset vector is used for the RZ phase.

III. NRZ DAC RESULTS

The current-steering NRZ DAC (Fig. 1.a) has been implemented at the component level in a 65nm CMOS process, with component values given in Table I. The value of the parasitic capacitor C_1 accounts for both the implementation of the ideal current source I_D and the layout parasitics at node ss. The gaussian-distributed offset vectors accounting for $V_{OS_{n,p}}$ are generated through Monte Carlo spectre simulations on $M_{n,p}$, resulting in a standard deviation $\sigma(V_{OS_{n,p}})$ of approx. 7 mV.

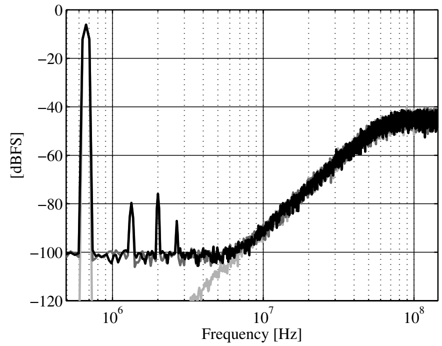

Fig. 7. 8192 points Hann-windowed FFT for the NRZ DAC $\Delta\Sigma$ modulator. Light grey: ideal signal (SNDR = 74 dB). Dark grey: component-level simulations with $\sigma(V_{OS_{n,p}}) = 7$ mV (SNDR = 66 dB). Black: VerilogA-model simulations with the same $\sigma(V_{OS_{n,p}})$ (SNDR = 66.2 dB).

The DAC VerilogA model contains the same offset vectors as the component-level DAC, allowing a direct comparison of the outputs. The g_m and C_{gs} values in the VerilogA model are derived from the DC operation point simulation of the component-level DAC. As clear from Fig. 6, VerilogA simulations match component-level simulations very well, apart from a large but very narrow switching spike that is otherwise of no consequence. In fact, the value of Q_e is practically the same in both simulations.

The DAC VerilogA model is also verified by including it inside a CT $\Delta\Sigma$ modulator model. To isolate the mismatch effects, all blocks except the DAC feeding into the integrator at the modulator input are ideal. The modulator has a 3rd-order loop with 3-bit DACs, 288 MHz sampling frequency, and an OSR of 16, resulting in an SNDR of 74 dB in the ideal case. A comparison between VerilogA-model DAC and component-level DAC is shown in Fig. 7, with $\sigma(V_{OS_p}) = 7$ mV. The two cases display an SNDR difference below 0.5 dB, and harmonic tones matching within 1 dB, proving the accuracy of the VerilogA model. Even more importantly, it is clear that the modulator performance is greatly affected by the threshold-voltage mismatches, with large distortion tones appearing and the SNDR dropping by 8 dB compared to the ideal case.

The verilogA-model-DAC modulator is further simulated without and with DWA for four different random seed values for the mismatch vectors, with results shown in Fig. 8 and Fig. 9, respectively. The SNDR is degraded by at least 10 dB in both cases, irrespectively of the use of DWA.

IV. RZ DAC RESULTS

The component values for the RZ DAC cell in Fig. 5 are still as in Table I. Again, VerilogA-model DAC and component-level DAC yield almost identical simulation results for the modulator, and the VerilogA model is used to assess the usefulness of DWA in the RZ DAC modulator, exploring the design space in a time-efficient way.

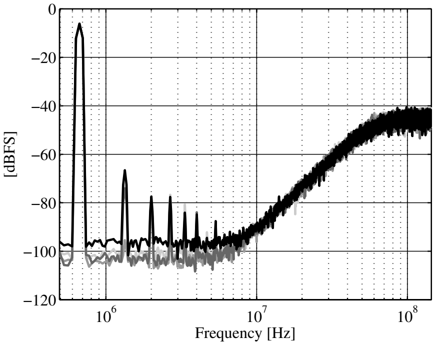

Fig. 8. 8192 points Hann-windowed FFT for the $\Delta\Sigma$ modulator with NRZ DAC without DWA (four simulations with different mismatch seeds).

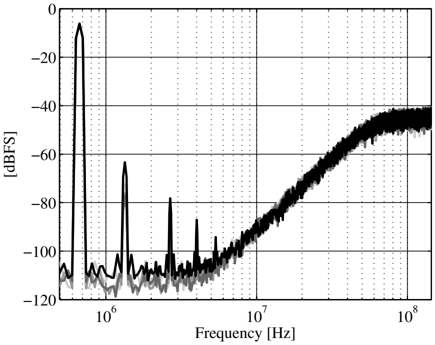

Fig. 9. 8192 points Hann-windowed FFT for the $\Delta\Sigma$ modulator with NRZ DAC with DWA (four simulations with different mismatch seeds).

Also in this case, we show the simulation outcome for four different seed values for the mismatch vectors, both without and with DWA. Without DWA, mismatches cause again an increased in-band noise and large distortion harmonics of the input signal (Fig. 10). The RZ DAC in combination with DWA, however, is very successful in reducing the effect of mismatch, as shown in Fig. 11, where harmonic distortion (almost) disappears, and an SNDR of at least 73.7 dB (i.e., only 0.3 dB from the ideal) is recovered.

V. CONCLUSION

The V_{th} mismatch in the switch pairs of a current-steering DAC, in combination with a parasitic tail capacitance, introduces asymmetrical DAC pulses that deteriorate the SNDR in a CT $\Delta\Sigma$ modulator. Several simulations run on an accurate VerilogA model of the DAC show that a NRZ DAC (either with or without DWA dynamic element matching) is greatly affected by V_{th} mismatches, as is a RZ DAC without DWA.

A RZ DAC employing DWA, on the contrary, is able to recover the full performance of the modulator.

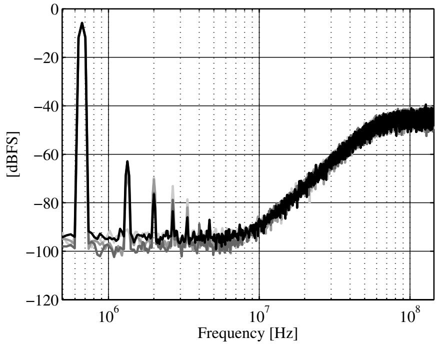

Fig. 10. 8192 points Hann-windowed FFT for the $\Delta\Sigma$ modulator with RZ DAC without DWA (four simulations with different mismatch seeds).

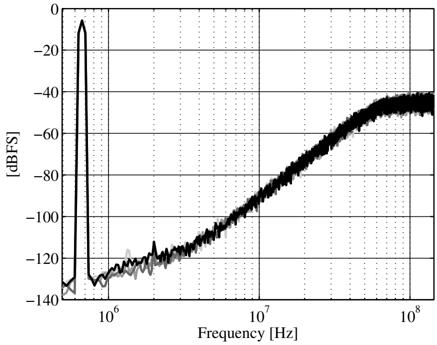

Fig. 11. 8192 points Hann-windowed FFT for the $\Delta\Sigma$ modulator with RZ DAC with DWA (four simulations with different mismatch seeds).

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Paper II

Paper II

A 7.5 mW 9 MHz CT ΔΣ Modulator in 65 nm CMOS With 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations

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A 7.5 mW 9 MHz CT $\Delta\Sigma$ Modulator in 65 nm CMOS with 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations

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***Abstract*—This paper presents a 3^{rd}-order, 3-bit continuous-time (CT) $\Delta\Sigma$ modulator for an LTE radio receiver. By adopting a return-to-zero (RZ) pulse in the innermost DAC, the modulator shows a reduced sensitivity to loop-delay variations, and the additional loop delay compensation usually needed in CT modulators can be omitted. The modulator has been implemented in a 65 nm CMOS process, where it occupies an area of 0.2 mm × 0.4 mm. It achieves an SNR of 71 dB and an SNDR of 69 dB over a 9 MHz bandwidth with an oversampling ratio of 16, while consuming 7.5 mW from a 1.2 V supply.**

I. INTRODUCTION

The increasing data rates in cellular communications demand a wider bandwidth analog-to-digital converter (ADC) in the radio receiver, e.g. 9 MHz in LTE. The low-pass nature of the signal transfer function (STF) provided by the feedback CT $\Delta\Sigma$ modulator (Fig. 1 (a)) is particularly attractive in cellular receivers. Furthermore, there is no peaking at the pass-band edge of the STF, where strong interferers may be present.

Non return-to-zero (NRZ) pulses in the feedback DACs are highly desirable for their reduced sensitivity to clock jitter and a lower integrator slew rate requirement [1]. The pulses are often intentionally delayed by a fixed fraction of the sampling period to give time for the quantizer and data-weighted averaging (DWA) circuits to settle. On the other hand, a delay shifts a NRZ pulse into the next sampling period, which requires an additional feedback path (i.e., DAC4 in Fig. 1 (a)) to restore the ideal modulator behavior [2]. Numerous alternative ways of implementing this additional path have been proposed.

In this paper, a NRZ / NRZ / RZ feedback scheme is proposed for a 3^{rd}-order CT $\Delta\Sigma$ modulator. A RZ pulse, centered in the middle of the sampling period, is used in the innermost feedback path (DAC3), while NRZ pulses extending into the following sampling period are adopted in the outer feedback paths. Besides the already mentioned advantages of NRZ feedback, which is kept for the more sensitive outer paths, the NRZ / NRZ / RZ feedback scheme has two main benefits. Firstly, the direct feedback path through DAC4 can be omitted, thanks to the DAC3 RZ pulse, which is fully contained within the sampling period. Secondly, centering the DAC3 RZ pulse in the middle of the sampling period makes the modulator more robust against loop delay variations, as will be shown in the following. A RZ pulse in the innermost feedback path was used in [3], together with a fixed loop delay of $1/2$ sampling period – this combination, however, does not result in a reduced sensitivity to loop delay variations. Furthermore, the current-steering DACs widely used in high-speed converters are replaced with resistive DACs [4] to reduce thermal noise.

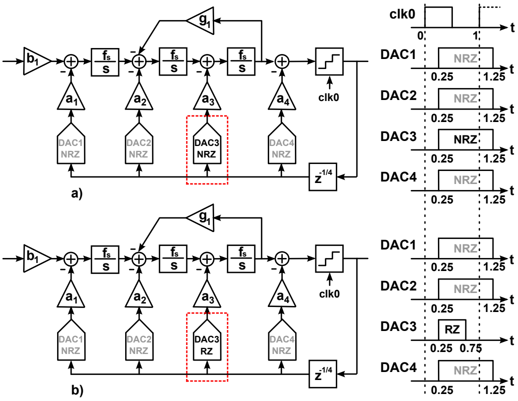

Fig. 1. 3^{rd}-order feedback CT $\Delta\Sigma$ modulator with $1/4$ sampling period fixed loop delay, compensated by DAC4: a) NRZ modulator; b) NRZ in DAC1,2,4, RZ in DAC3.

II. SELECTION OF FEEDBACK DAC PULSES

Starting from a reference 3^{rd}-order discrete-time (DT) modulator designed with Schreier's toolbox, the coefficients a_i of the corresponding CT modulator are found with the impulse-invariant transformation [5], which makes the sampled open-loop impulse response $h_{ct}(n)$ of the CT modulator equal the open-loop impulse response $h_{dt}(n)$ of the reference DT modulator. This yields identical noise transfer functions (NTF) for the two modulators.

The 3^{rd}-order CT modulator with all NRZ DACs is shown in Fig. 1 (a) with a fixed loop delay of $1/4$ sampling period, to allow the quantizer and DWA circuits to settle. The loop delay is compensated by the additional, 4^{th} feedback path with coefficient a_4, which injects its feedback signal into the last, memoryless node of the loop filter. Consequently, DAC4 only corrects the first sample ($h_{ct}(1)$) of the impulse response, as is shown in Fig. 2 (a) (where the sampling frequency is normalized to unity). Also note that a delay of DAC3 has much larger impact on the first sample, than a delay of DAC2 and

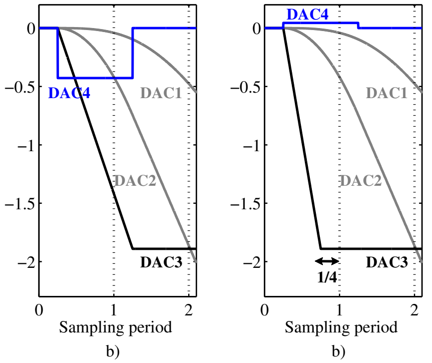

Fig. 2. Open-loop impulse responses for the individual DACs in the modulator of: a) Fig. 1 (a), and b) Fig. 1 (b).

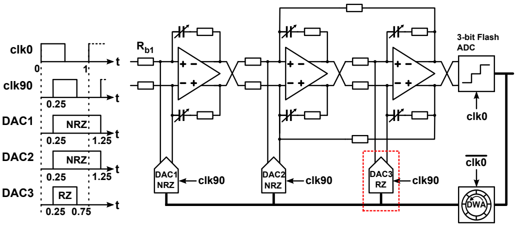

Fig. 3. CT $\Delta\Sigma$ modulator with the NRZ / NRZ / RZ feedback scheme (DAC4 omitted). Timing diagram and simplified schematic view.

DAC1. In the following, the modulator in Fig. 1 (a) is referred to as the NRZ modulator.

If instead DAC3 employs a RZ pulse, the pulse becomes centered and fully contained within the sampling period (see Fig. 1 (b)). The resulting impulse response is shown in Fig. 2 (b) where two benefits can be observed: Firstly, DAC3 can be delayed $1/4$ sampling period without affecting the impulse response at the sampling instants. This reduces the sensitivity to loop delay variations. Secondly, the coefficient for DAC4 (a_4) is substantially reduced. In fact, it is now possible to omit a_4 altogether, at the price of only a small error in $h_{ct}(1)$. A DT model has shown that such an error causes a behavior very similar, but not identical, to when all DAC pulses are delayed from their nominal positions [5]. The difference is that a delay affects all samples in the impulse response, while omitting DAC4 only affects the first sample.

In addition to the 1/4 sampling period fixed loop delay, there are other sources of delay in the loop to be compensated with a_4. One source is the finite gain-bandwidth product (GBW) of the active-RC integrators in the loop filter, which results in a high-frequency parasitic pole in the integrator. The pole can be modeled as an additional loop delay for all DAC pulses preceding that integrator [6]. This delay can be compensated by recalculating the CT coefficients a_i in presence of the delayed DAC pulses. It was shown in [7] that a GBW as low as $1.2\,f_s$ (where f_s is the sampling frequency) is feasible in the third integrator, which has the toughest GBW requirements.

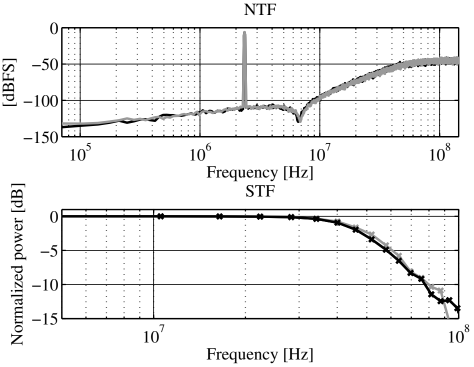

Fig. 4. NTF and STF for, Black: NRZ modulator (GBW$=\infty$), Grey: NRZ / NRZ / RZ modulator with GBW$= f_s$ for the third integrator.

A. Impact of loop delay and loop delay variations

The NRZ / NRZ / RZ modulator without the additional DAC4 path is shown in Fig. 3. This modulator has been optimally compensated for two sources of loop delay: the mentioned fixed $1/4$ sampling period delay, and as an example, a finite GBW$= f_s$ in the third integrator. The NTF and STF for this modulator are shown in Fig. 4, together with the NTF and STF of the ideal (i.e., with integrator GBW$=\infty$) NRZ modulator in Fig. 1 (a). It is clear that the NRZ / NRZ / RZ modulator with loop delay has essentially the same performance as the ideal NRZ modulator, even if the DAC4 path has been removed. To repeat, this is allowed by the adoption of a RZ pulse in DAC3, which substantially reduces the value of a_4.

In order to show the robustness of the proposed NRZ / NRZ / RZ modulator, its performance is simulated in presence of the loop delays described above, together with an additional uncompensated loop delay T_d (normalized to the sampling period T_s). As shown in Fig. 5, the NRZ / NRZ / RZ modulator displays almost full SNDR performance for delay deviations up to ± 0.24, while the ideal NRZ modulator only tolerates a deviation of ± 0.1. This is also confirmed analytically, by applying the theory in [5] to plot the z-domain NTF poles for the modulators versus deviation in delay.

As mentioned in the Introduction, there are alternative ways of implementing the additional DAC4 path in the NRZ modulator. A popular and very attractive approach is to replace DAC4 with a feed-forward loop delay compensation, implemented with a resistor in series to the integrating capacitor in the third integrator [8]. As shown again in Fig. 5, a very similar sensitivity to deviations in loop delay was obtained with this solution (with GBW$=\infty$ for all integrators), compared to the DAC4 path compensation.

Repeating the same simulations in presence of the commonly used $1/2$ sampling period fixed delay, the NRZ modulator displays a sensitivity to an additional loop delay very similar to the one with in Fig. 5(a).

The above results show improved robustness against additional sources of loop delay for the proposed NRZ / NRZ / RZ

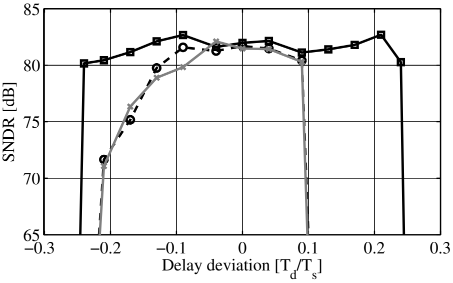

Fig. 5. SNDR vs. delay deviation (additional uncompensated delay). Dashed: NRZ modulator of Fig. 1 (a) (GBW $= \infty$). Black: NRZ / NRZ / RZ modulator of Fig. 3 with GBW $= f_s$ for the third integrator. Grey: NRZ modulator with feed-forward loop delay compensation (GBW $= \infty$).

modulator, where a delay of $1/4$ sampling period was used to center the RZ DAC3 pulse in the middle of the sampling period. This choice leaves $1/4$ of the sampling period for the quantizer and DWA circuits to settle, which is more than sufficient for the presented application. A drawback of the RZ DAC3 pulse is that its peak current is doubled, compared with a NRZ pulse. However, the linearity requirement for the third integrator is relaxed by its 3rd-order high-pass transfer function to the modulator output, while the power consumption of DAC3 is only very marginally affected.

The quadrature clock phases used in the clocking scheme in Fig. 3 can be generated by frequency division of the high frequency local oscillator, which is already available in the LTE radio receiver.

III. CIRCUIT IMPLEMENTATION

The target application for the modulator is the ADC in a cellular receiver for the LTE standard, which has a 9 MHz signal bandwidth at baseband. A relatively low oversampling ratio (OSR) of 16 is chosen, resulting in a clock frequency of 288 MHz. A 576 MHz external clock is buffered and divided-by-two on-chip, to generate the 288 MHz quadrature clock phases clk0 and clk90 (Fig. 3).

The loop filter in the modulator is built with active-RC integrators for high linearity. The amplifiers in the integrators make use of a folded-cascode topology (although more power efficient solutions exist [9]) with unity loop-gain frequencies of $\mathrm{Amp}_{1,2,3}=\{1.6, 1.2, 0.8\}$GHz. Each integrating capacitor is split into a 3-bit MIM capacitor array for tunability of the time constants in the loop filter. The differential full-scale input amplitude was set to $\mathrm{V}_{\mathrm{fs}} = 600\,\mathrm{mV}_{\mathrm{pk}}$, which, together with the differential input resistance R_{b1} of $7.85\,\mathrm{k}\Omega$, sets the full-scale input current to $\mathrm{I}_{\mathrm{fs}} \approx 76\,\mu\mathrm{A}$. The right-half-plane zero in the frequency response of each integrator is compensated with a resistor in series with the integrator capacitor.

The quantizer is a 3-bit flash ADC with a differential input range of ± 480 mV. An external voltage is buffered on-chip and fed to a resistive ladder to generate the reference voltages for the comparators. A Gray-Lewis differential dynamic comparator is used in the quantizer. The capacitive loading from the quantizer of the third integrator is kept small by using minimum-length transistors in the input pair of the comparator.

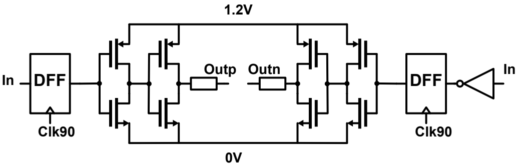

Fig. 6. Unit NRZ DAC cell using a complementary resistive topology.

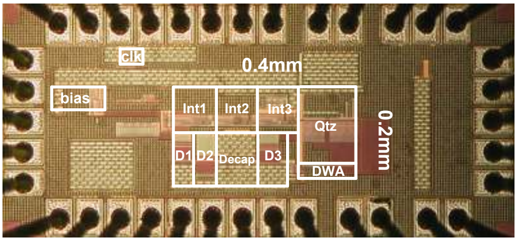

Fig. 7. Die photograph of the CT $\Delta\Sigma$ modulator prototype, with an active area of 400μm $\times$ 200μm.

The design includes data-weighted averaging (DWA) with a 3-bit binary input. The DWA pointer is updated on the falling edge of clk0, providing an additional half sampling period for the operation of the 3-bit adder in the DWA.

A. *Resistive multi-bit DACs*

A resistive multi-bit DAC [4] (Fig. 6) was chosen, as it produces lower thermal noise than the current-steering DAC. In general, a resistor is less noisy than a MOS transistor working in the active region for the same current, assuming a channel noise factor of unity.

The resistive DAC has a low output impedance, which in a multi-bit implementation may cause distortion due to the code-dependent output impedance in a differential implementation. However, in a complementary implementation, such as the one portrayed in Fig. 6, the output DAC impedance is constant with the control word, and therefore, linearity is retained.

The NRZ DAC cell in Fig. 6 was implemented with poly-silicon resistors and low-V_{th} devices as switches. The resistor matching requirements are relaxed by the DWA algorithm to about 1%. The RZ DAC cell has a similar implementation as the NRZ DAC cell, with transmission gates added to provide RZ operation, while a non-overlapping clock generator is used to avoid short-circuiting the common-mode voltage reference to power supply or ground.

IV. MEASUREMENT RESULTS

The modulator occupies an active chip area of $400\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$ (Fig. 7). The die was bonded in a CQFP 44 package for testing. The measured signal spectra were calculated in Matlab using Hann windowing and averaging.

The output spectra of a 2.36 MHz sine wave with a -2.4 dBFS input amplitude is shown in Fig. 8. The DWA algorithm is very effective, reducing the 2nd- and 3rd-order

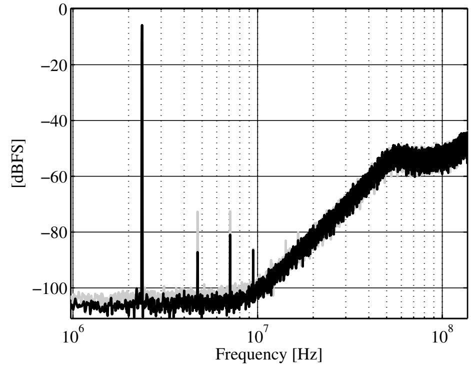

Fig. 8. 32768-point FFT with -2.4 dBFS input signal at 2.36 MHz, with DWA (black) and without DWA (grey). With DWA enabled, SNDR=69.2 dB, HD2=-81.4 dB and HD3=-75.2 dB.

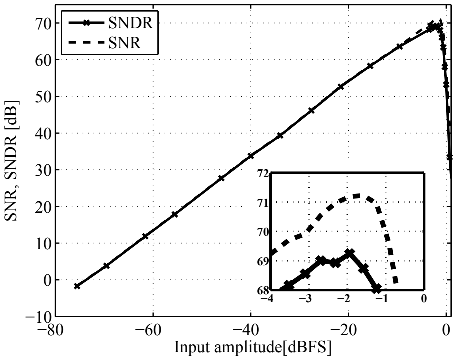

Fig. 9. SNR and SNDR over 9 MHz bandwidth vs. input amplitude for a 2.36 MHz sine wave. Peak SNR is 71 dB and peak SNDR is 69 dB.

harmonic distortion by 13 dB and 8 dB, respectively, and the noise floor by 2.5 dB. The intrinsic resistor matching is better than expected, as Monte Carlo simulations predicted an SNDR of 55 dB without DWA. The SNR and SNDR vs. input amplitude are shown in Fig. 9. The peak SNR and SNDR are 71 dB and 69 dB, respectively, and occurs at -2.0 dBFS input amplitude.

The total power consumption, including clock buffers, DAC reference voltages, frequency dividers and bias-current generators, is 7.5 mW from a 1.2 V power supply. The well-known figure-of-merit, $\mathrm{FoM} = \mathrm{P}/(2^{\mathrm{ENOB}} \cdot 2\,\mathrm{f_B})$, where $\mathrm{ENOB} = (\mathrm{SNDR} - 1.76)/6.02$, yields a FoM of 181 fJ / conv. The measured performance of the modulator is summarized in Table I.

V. Conclusions

A 3rd-order, 3-bit, continuous-time $\Delta\Sigma$ modulator with a NRZ / NRZ / RZ feedback scheme implemented in 65 nm CMOS has been presented. The modulator, clocked at 288 MHz with a quadrature clock, displays an SNDR of 69 dB over 9 MHz bandwidth, and consumes 7.5 mW from a 1.2 V power supply. The usually necessary loop-delay compensation is avoided with a RZ pulse for the innermost feedback DAC, and the sensitivity to additional uncompensated loop-delay is reduced. Finally, the commonly used current-steering DAC was replaced by a multi-bit resistive DAC, with improved thermal noise performance.

TABLE I
Comparison with state-of-the-art CT $\Delta\Sigma$ modulators

Parameter	**This work**	**[10] 06**	**[7] 12**	**[11] 10**	**[9] 12**	**[12] 12**	**[13] 10**
fs (MHz)	**288**	640	500	640	3600	600	1152
BW (MHz)	**9**	20	25	10	36	10	9
SNR (dB)	**71**	76	69.1	–	76.4	79.1	76
SNDR (dB)	**69**	74	67.5	65	70.9	78	72
DR (dB)	**72**	80	72	67	83	83.5	-
Power (mW)	**7.5**	20	8.5	6.8	15	16	17
Area (mm^2)	**0.08**	1.2	0.23	0.4	0.12	0.36	0.07
Tech. (nm)	**65**	130	90	90	90	90	65
Vdd (V)	**1.2**	1.2	1.2	1.2	1.2	-	1.2/2.5
FoM (fJ/c.)	**181**	122	88	240	73	125	290

VI. Acknowledgement

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Paper III

Paper III

Theory and Design of a CT $\Delta\Sigma$ Modulator with Low Sensitivity to Loop-Delay Variations

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Theory and design of a CT ΔΣ modulator with low sensitivity to loop-delay variations

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Abstract This paper presents a 3rd-order, 3-bit continuous-time (CT) ΔΣ modulator for an LTE radio receiver. A return-to-zero (RZ) pulse, centered in the sampling period by a quadrature clock, is used in the innermost DAC to reduce the sensitivity to loop-delay variations in the modulator, and omit implementing the additional loop delay compensation usually needed in CT modulators. The performance and stability of the NRZ/NRZ/RZ feedback scheme is thoroughly analysed using a discrete-time model. The modulator has been implemented in a 65 nm CMOS process, where it occupies an area of 0.2 × 0.4 mm^2. It achieves an SNR of 71 dB and an SNDR of 69 dB over a 9 MHz bandwidth with an oversampling ratio of 16, and a power consumption of 7.5 mW from a 1.2 V supply.

Keywords Delta sigma · Return-to-zero · RZ · Loop delay · Sensitivity · Quadrature clock

1 Introduction

The increasing data rates in cellular communications demand a wider-bandwidth analog-to-digital converter (ADC) in the radio receiver, e.g. 9 MHz in LTE. Delta-sigma modulators (DSMs) with continuous-time (CT) loop filters have gained popularity in battery-powered user equipment due to speed advantages over their discrete-time (DT) counterparts, enabling a higher clock rate or a lower power consumption [1, 2]. Furthermore, the low-pass nature of the signal transfer function (STF) provided by the feedback-compensated CT DSM, with no peaking at the pass-band edge, is particularly attractive in cellular receivers, where strong interferers are present in nearby receive channels [2, 3]. In addition, non return-to-zero (NRZ) (Fig. 1(a)) as opposed to return-to-zero (RZ) DAC pulses (Fig. 1(b)) are desirable for their reduced sensitivity to clock jitter and a lower integrator slew rate requirement [4].

A well-known issue in CT DSMs is the sensitivity to loop-delay variations, and in particular to the signal-dependent delay of the quantizer, which can cause serious performance degradation and even instability [5, 6]. As a consequence, many modulators [7–12] are designed with a fixed delay of 1/2 sampling period in the feedback path, which is easily generated via a differential clock. This allows the flash ADC and dynamic element matching circuits such as data-weighted averaging (DWA) to settle within a 1/2 sampling period. The fixed loop delay shifts the NRZ pulse into the next sampling period, as shown in Fig. 1(c) with T_{fix}, which requires an additional direct-path DAC to compensate for the delay, thereby restoring the ideal modulator behavior [13]. On top of the fixed loop delay, there are additional sources of loop delay, e.g. internal delays in the DACs, flash ADC [14] and loop filter [7] that further delays the NRZ pulse, indicated by T_a in Fig. 1(d). Although this delay can be optimally compensated, process variations yield an uncertainty in the exact value of the loop delay, which can lead to performance degradations and instability [6].

The implementation of the loop delay compensation typically requires an extra DAC (DAC4 in Fig. 2(a)) and a differential summing amplifier with high unity gain-bandwidth (GBW) [15]. The adder can be avoided by first doing

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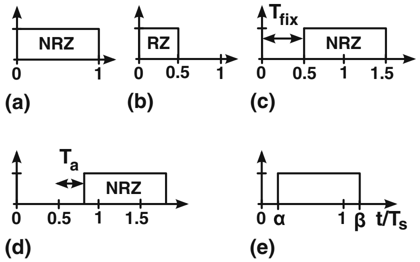


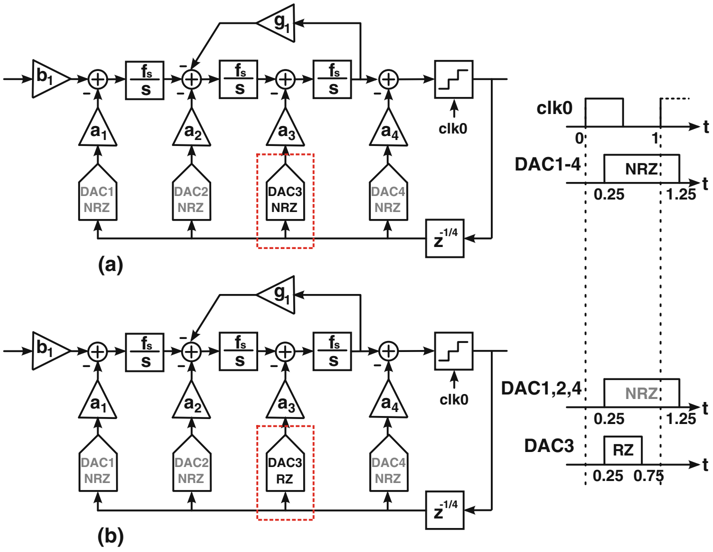
Fig. 1 DAC pulses: **a** NRZ. **b** NRZ with fixed loop delay. **c** NRZ with fixed, and additional loop delay. **d** Arbitrary pulse from α to β

digital differentiation, followed by using the last integrator for integration [8]. While this scheme has lower GBW requirements than the direct-path DAC approach, an additional DAC is still required. The additional DAC can be removed by compensating entirely in the digital domain [9], with the drawback that additional levels in the quantizer are needed to achieve an optimal performance. This may be difficult to implement, if the quantizer is already multi-bit. Finally, the direct-path DAC may be replaced with a feed-forward path across the last integrator, which is easily implemented by a resistance in series with the integrator capacitance, creating a left-half-plane zero [10]. This approach is attractive, since it avoids additional DACs and has a relatively moderate requirement on the integrator GBW [15].

In this paper, an NRZ/NRZ/RZ feedback scheme is proposed for a 3rd-order CT DSM. An RZ pulse is used in the innermost feedback path (DAC3 having $\alpha = 0.25$, $\beta = 0.75$ in Fig. 1(e)), while NRZ pulses extending into the following sampling period are adopted in the outer feedback paths ($\alpha = 0.25$, $\beta = 1.25$). Besides the already mentioned advantages of NRZ feedback, which is kept for the more sensitive outer paths, the NRZ/NRZ/RZ feedback scheme has two main benefits. Firstly, the direct feedback path through DAC4 can be omitted, thanks to the DAC3 RZ pulse, which is fully contained within the sampling period ($\beta \leq 1$). Secondly, quadrature clocking enables to center the DAC3 RZ pulse in the middle of the sampling period. This makes the modulator more robust against loop delay variations, as will be shown in the following. An RZ pulse in the innermost feedback path was used in [16], together with a fixed loop delay of 1/2 sampling period—this combination, however, does not result in a reduced sensitivity to loop delay variations.

The paper is organized as follows: Sect. 2 presents the reduced sensitivity to loop delay and the impact of omitting DAC4 on the modulator, while Sect. 3 shows how the DAC pulses are individually chosen for the three DACs, to meet the required modulator performance. A theoretical analysis of the NRZ/NRZ/RZ feedback technique using a DT model, including the maximum SNR degradation caused by an arbitrary combination of rectangular DAC pulses and loop delay, is presented in Sect. 4 The resulting implementation of a 3rd-order 3-bit CT DSM with a fixed loop

Fig. 2 3rd-order feedback CT DSM with 1/4 sampling period fixed loop delay, compensated by DAC4: **a** NRZ modulator; **b** NRZ in DAC1,2,4, RZ in DAC3



delay of 1/4 of the sampling period and NRZ/NRZ/RZ feedback is presented in Sect. 5, including the adoption of resistive DACs [17] to reduce the thermal noise, replacing the more common current-steering DACs. Measurement results, showing an SNDR of 69 dB in a 9 MHz bandwidth, are discussed in Sect. 6, while conclusions are drawn in Sect. 7 Finally, an Sect. 9 contains the mathematical derivations used in Sect. 3.

2 Benefits of using RZ in DAC3

Typically, a DT DSM is used as reference to determine the coefficients a_i of the CT loop filter, employing the so-called impulse-invariant transformation [6]. This makes the open-loop impulse response $h_{ct}(n)$ of the CT loop filter, sampled at the input of the quantizer, identical to the open-loop impulse response $h_{dt}(n)$ of the DT loop filter. This operation results in identical noise transfer functions (NTF) for the two modulators.

The 3rd-order CT modulator with NRZ DACs, referred to as the NRZ modulator, is shown in Fig. 2(a). A fixed loop delay of 1/4 sampling period allows the quantizer and DWA to settle before the data is fetched by the DACs. The loop delay shifts the NRZ pulse into the next sampling period, which is compensated [13] using an additional 4th feedback path with coefficient a_4, which injects a feedback signal into the last, memoryless node of the loop filter. Thus, the DAC4 path only corrects the first sample of the impulse response ($h_{ct}(1)$), as seen in Fig. 3(a). It can be shown that DAC3 is the dominant source of sensitivity to loop delay compared with DAC2 and DAC1, using the theory in [6] to plot the z-domain poles versus loop delay. It is therefore interesting to examine DAC3, while DAC1 and DAC2 are kept as NRZ DACs.

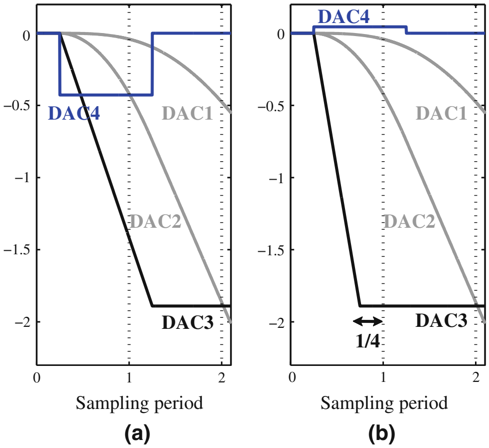


Fig. 3 Open-loop impulse responses for the individual DACs in the modulator of: **a** Fig. 2(a), and **b** Fig. 2(b)

If DAC3 is RZ, the pulse is centered and fully contained within the sampling period, see Fig. 2(b). This results in an impulse response according to Fig. 3(b), which has two benefits: Firstly, DAC3 tolerates an additional loop delay of ±1/4 sampling period without affecting the impulse response at integer sampling instants. This significantly reduces the sensitivity to loop delay variations for the overall DSM, since DAC3 has the highest sensitivity to loop delay among the DACs. Secondly, the coefficient for DAC4 (a_4) is about ten times smaller. This in fact enables removing DAC4, which results in a small error in $h_{ct}(1)$ that can affect the performance and stability of the modulator, thoroughly analysed in Sect. 4.

On top of the fixed loop delay of 1/4 sampling period, there are additional sources of delay in the loop to be compensated with a_4, e.g. delay in the DAC DFFs, in the preamplifiers of the flash ADC and in the loop filter. In the loop filter, the finite gain-bandwidth product (GBW) of the active-RC integrators introduces a high-frequency pole in the transfer function of the integrator. The pole is equivalent to an additional loop delay of all DAC pulses preceding that integrator [18]. The delay can be compensated by recalculating the CT coefficients a_i in presence of the delayed DAC pulses. A low GBW of $1.2f_s$ (where f_s is the sampling frequency) was successfully compensated in [19] in the third integrator, which has the highest GBW requirements.

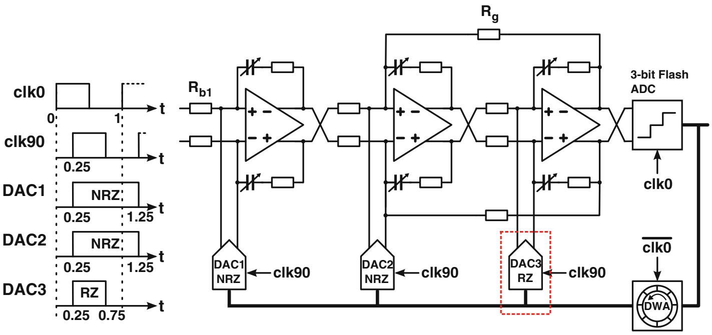
2.1 Effects of loop delay and loop delay variations

The proposed modulator with RZ in DAC3, and without the additional DAC4 path is shown in Fig. 4, referred to as the NRZ/NRZ/RZ modulator. Two sources of loop delay have been optimally compensated in the modulator: the fixed delay of 1/4 sampling period described earlier, and, as an example, a GBW $= f_s$ in the third integrator.

The NTF and STF for the proposed NRZ/NRZ/RZ modulator are shown in Fig. 5, together with the NTF and STF of the ideal (i.e., with integrator GBW $= \infty$) NRZ modulator in Fig. 2(a). It is clear that the NRZ/NRZ/RZ modulator with loop delay has very similar NTF and STF compared with the ideal NRZ modulator, although the DAC4 path is omitted. Again, this is enabled by using RZ in DAC3, which significantly lowers the value of a_4, as previously shown in Fig. 3.

In order to show the robustness of the proposed NRZ/NRZ/RZ modulator, its performance is simulated in presence of the loop delays described above, together with an additional uncompensated loop delay T_d (normalized to the sampling period T_s). As shown in Fig. 6, the NRZ/NRZ/RZ modulator displays almost full SNDR performance for delay

Fig. 4 Proposed CT DSM with the NRZ/NRZ/RZ feedback scheme where DAC4 is omitted. Timing diagram and simplified schematic



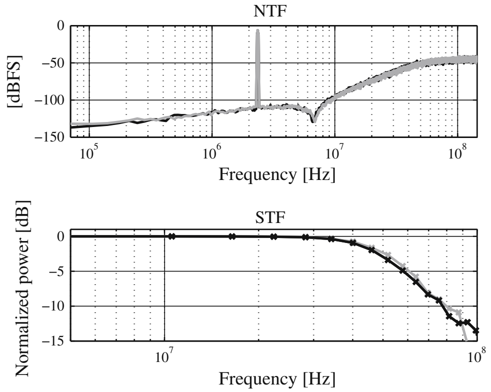


Fig. 5 NTF and STF for *Black* NRZ modulator (GBW $= \infty$), *Grey* NRZ/NRZ/RZ modulator (GBW $= f_s$ for 3rd integrator)

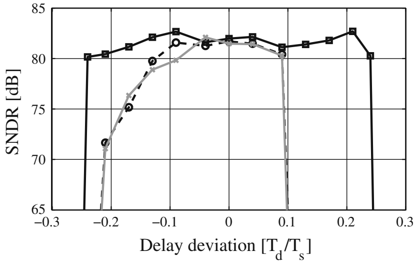


Fig. 6 SNDR versus delay deviation (additional uncompensated delay). *Solid* NRZ/NRZ/RZ modulator of Fig. 4 (GBW = f_s for 3rd integrator). *Dashed* NRZ modulator of Fig. 2(a) (GBW $= \infty$). *Grey* NRZ modulator with feed-forward loop delay compensation (GBW $= \infty$)

deviations up to ±0.24, while the ideal NRZ modulator only tolerates a deviation of ±0.1. This is also confirmed analytically, by applying the theory in [6] to plot the z-domain NTF poles for the modulators versus deviation in delay.

As mentioned in the Sect. 1, there are alternative ways of implementing the additional DAC4 path in the NRZ modulator. A popular and very attractive approach is to replace DAC4 with a feed-forward loop delay compensation, implemented with a resistor in series to the integrating capacitor in the third integrator [10]. As shown again in Fig. 6, a very similar sensitivity to deviations in loop delay was obtained with this solution (with GBW $= \infty$ for all integrators), compared to the DAC4 path compensation.

For completeness, the same simulations was repeated in presence of the commonly used 1/2 sampling period fixed delay. The NRZ modulator shows a very similar sensitivity to uncompensated delay as the NRZ modulator with 1/4 sampling period fixed delay in Fig. 6.

The above results show improved robustness against additional sources of loop delay for the proposed NRZ/NRZ/RZ modulator, which is a result of using an RZ pulse that is centered in the sampling period, in the path most sensitive to loop delay.

3 Determination of direct-path coefficient

In the following, an expression for the CT coefficient a_4 in the DAC4-path as a function of the DAC pulse shape and delay is derived. The goal is to determine DAC pulses that yield a small a_4, to allow omit implementing the coefficient. It is worth reminding that $h_{ct}(n)$ and $h_{dt}(n)$ can be matched exactly (i.e., with $a_4 = 0$), if all DAC pulses are contained within the first sampling period, i.e. if $\beta \leq 1$ in Fig. 1(e), neglecting additional sources of loop delay. Thus, the coefficient a_4 corrects the first sample of the impulse response, and is calculated[1] with individually delayed DAC pulses, where the DACi pulse ($i = 1, 2, 3$)

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[1] The analysis is vastly simplified by disregarding the feedback path g_1 in the resonator (see Fig. 2(a)), which is allowed by the fact that such a path has an utterly negligible impact on $h_{ct}(1)$ for any realistic value of g_1.

starts at $t/T_s = \alpha_i$ and ends at $t/T_s = \beta_i = 1 + \alpha_i$ (Fig. 1(e)), and T_s is the sampling period. The coefficient is calculated in the Sect. 9, which yields

$$\begin{aligned} a_4 = {} & a_{3dt}\left(1 - \frac{\gamma_3 - \alpha_3}{\beta_3 - \alpha_3}\right) \\ & - a_{2dt}\left[\frac{\gamma_3 - \alpha_3}{\beta_3 - \alpha_3}\left(\frac{\alpha_2 + \beta_2 - 2}{2}\right) + \frac{\gamma_2 - \alpha_2 + \frac{\alpha_2^2 - \gamma_2^2}{2}}{\beta_2 - \alpha_2}\right] \\ & - a_{1dt}\left\{\frac{\gamma_3 - \alpha_3}{\beta_3 - \alpha_3}\left[1 - \frac{1}{6}(\alpha_1^2 + \alpha_1\beta_1 + \beta_1^2)\right.\right. \\ & \left. + \frac{1}{4}(\alpha_2 + \beta_2)(\alpha_1 + \beta_1 - 3)\right] \\ & + \frac{\gamma_2 - \alpha_2 + \frac{\alpha_2^2 - \gamma_2^2}{2}}{2(\beta_2 - \alpha_2)}(\alpha_1 + \beta_1 - 3) \\ & \left. + \frac{1}{2(\beta_1 - \alpha_1)}\left[(\gamma_1 - \alpha_1) + (\alpha_1^2 - \gamma_1^2) + \frac{\gamma_1^3 - \alpha_1^3}{3}\right]\right\} \end{aligned} \tag{1}$$

where, a_{1dt}, a_{2dt}, and a_{3dt} are given in Table 1, and γ_i is defined as $\min(\beta_i, 1)$. Equation (1) was investigated for many DAC pulses of varying widths, of which two realistic cases are presented: (1) All three DAC pulses are NRZ and equally delayed by $\alpha_1 = \alpha_2 = \alpha_3 = \alpha$ into the next sampling period; (2) The pulses from DAC1 and DAC2 are NRZ and delayed by $\alpha_1 = \alpha_2 = \alpha$ into the next sampling period, while the pulse from DAC3 is RZ and completely contained within the current sampling period (i.e., $\beta_3 < 1$). As shown in Fig. 7, in the first case a_4 rises very quickly with α, which means that only a very small delay is acceptable to avoid a performance degradation from omitting DAC4 (e.g. an $\alpha = 1/4$ yields $a_4 = 0.43$, which results in an unstable modulator), as will be clear in Sect. 4.

In the second case, the absolute value of a_4 is much smaller and grows much more slowly with α. It is therefore very convenient to use $\alpha = 1/4$, and NRZ pulses for DAC1 and DAC2, while an RZ pulse is chosen for DAC3. The RZ pulse is fully contained in the period, which, according to Fig. 7, significantly reduces a_4 from 0.43 to -0.045 (observed already in Fig. 3(a), (b)). This enables omitting the DAC4 path with a negligible impact on STF and NTF, as previously shown in Fig. 5. In addition, this centers the RZ pulse in the sampling period, resulting in 1/4 period for the quantizer and DWA circuits to settle, which is more than sufficient for the presented application, and 1/4 sampling period of margin against additional loop delay, as was presented in Fig. 6. The differential phases of the local oscillator (LO) synthesized by the PLL in the radio receiver can be used to generate the quadrature clock phases required by the modulator via frequency division.[2]

Table 1 DT loop filter coefficients

Coefficient	a_{1dt}	a_{2dt}	a_{3dt}	b_{1dt}	g_{1dt}
Value	0.5779	1.9238	2.3056	0.5779	0.023

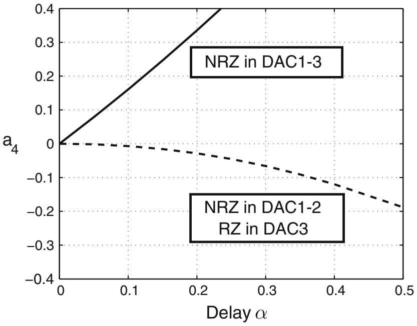

Fig. 7 CT coefficient a_4 versus loop delay α for two combinations of DAC pulses: *Solid* NRZ pulses for DAC1-3. *Dashed* NRZ pulses for DAC1-2, and RZ pulse in DAC3

A drawback of the using RZ in DAC3 is that its peak current is doubled, compared with an NRZ pulse. However, the linearity requirements for the third integrator are relaxed by its 3rd-order high-pass transfer function to the modulator output, while the power consumption of DAC3 is only very marginally affected.

4 Analysis of NRZ/NRZ/RZ feedback scheme

In this section, the impact of removing the DAC4 path on the stability and performance of the modulator is studied for various values of a_4 with a DT model. As mentioned previously, DAC4 only affects the first sample ($h_{ct}(1)$) of the CT impulse response ($h_{ct}(n)$) in Fig. 3(a). Thus, if the DAC4 path is not implemented, $h_{ct}(n)$ can be written as

$$h_{ct}(n, \epsilon) = h_{dt}(n) + \epsilon\delta(n - 1) \tag{2}$$

where $\delta(n)$ is the Dirac delta, $h_{dt}(n)$ is the reference DT impulse response, and ϵ is the error caused by not implementing the DAC4 path (as we will show in the Sect. 9, ϵ coincides with a_4). The z-domain expression of (2) becomes

$$H_{ct}(z, \epsilon) = H_{dt}(z) + \epsilon z^{-1}. \tag{3}$$

In the following, the impact of ϵ on the modulator will be investigated.

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[2] Of course, the LO frequency varies with the frequency of the receive channel, which means that the modulator is clocked with slightly different frequencies according to the receive channel. The transition from the variable-clock domain in the modulator to the fixed-clock domain in the digital base-band can be performed with a Farrow interpolator [20, 21].

4.1 A linear analysis of $NTF_{ct}(z,\epsilon)$

Assuming a linear quantizer model with unity gain, $NTF_{ct}(z,\epsilon)$ can be calculated from $H_{ct}(z,\epsilon)$ as

$$\begin{aligned} NTF_{ct}(z,\epsilon) &= \frac{1}{1-H_{ct}(z,\epsilon)} = \frac{1}{1-(H_{dt}(z)+\epsilon z^{-1})} \\ &= \frac{1}{1-\left(\frac{NTF_{dt}(z)-1}{NTF_{dt}(z)}+\epsilon z^{-1}\right)}, \end{aligned} \qquad (4)$$

where the coefficients of $H_{dt}(z)$ in Table 1, have been found with Schreier's Delta-Sigma Matlab Toolbox [22].

Compared to $NTF_{dt}(z), NTF_{ct}(z,\epsilon)$ presents an additional zero in the origin and an additional pole, which increases the modulator order by one. The zeroes are unaffected by ϵ, while the poles are shifted from their original positions. We might incorrectly conclude that this behavior is identical to a loop delay, where all DAC pulses are delayed from their nominal positions [6]. However, a loop delay affects all samples in the impulse response, while omitting DAC4 (as here) only affects the first sample, $h_{ct}(1)$.

The stability of the modulator is investigated by plotting poles and zeros of $NTF_{ct}(z,\epsilon)$ versus ϵ, as shown in Fig. 8. For $-0.26 \leq \epsilon \leq 0.32$, the poles are within the unit circle and the system is stable, while outside this range the linear model predicts an unstable system. In our case, the poles are moved only by a negligible amount, due to the small $a_4 = \epsilon = -0.05$.

4.2 Time-domain simulations

The z-domain expression of $NTF_{ct}(z,\epsilon)$ in (4) allows us to run fast and accurate Matlab simulations for various values of ϵ, to investigate the impact of ϵ on the modulator performance.

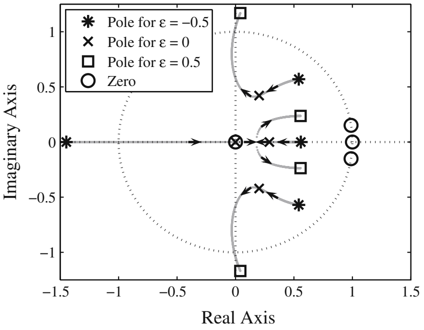

Fig. 8 Pole-zero plot for the CT NTF, with $-0.5 \leq \epsilon \leq 0.5$. The *poles* are within the unit *circle* for $-0.26 \leq \epsilon \leq 0.32$

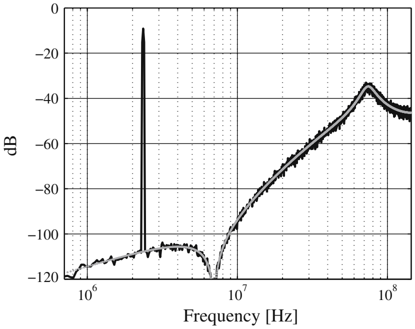

Fig. 9 FFT of CT DSM output for $\epsilon = 0.2$. *Black* Matlab time-domain simulations. *Grey* linear model of CT NTF from (4)

Figures 9 and 10 show the spectra of the modulator output for $\epsilon = \pm 0.2$, together with $NTF_{ct}(z,\epsilon)$ from the linear analysis for comparison. The agreement between time-domain simulation and linear analysis is excellent.[3] Clearly, these values of ϵ affect the out-of-band quantization noise shaping, resulting in a pronounced spectral peak close to the Nyquist frequency. This confirms that the DSM is close to instability for these values of ϵ, as predicted by the linear model. The in-band noise, however, increases only very marginally, i.e. by less than 1 dB.

To assess the impact of ϵ on the modulator performance, the maximum stable amplitude (MSA), the in-band noise (IBN), and the maximum SNDR have been plotted for several ϵ values in Fig. 11 (negative ϵ values) and 12 (positive ϵ values), where MSA, IBN and SNDR have been normalized to their respective values when $\epsilon = 0$. For large absolute values of ϵ, IBN increases and MSA decreases, resulting in a lower SNDR (similarly to what previously observed in presence of loop delay [6]). On the other hand, Figs. 11 and 12 also show that if ϵ is small (e.g. below ±0.1), the SNDR degradation is well below 1 dB and therefore negligible in our case.

5 Circuit implementation

A 3rd-order, 3-bit, CT DSM based on the NRZ/NRZ/RZ feedback scheme has been designed in a 65 nm CMOS process based on the simplified block schematic of the

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[3] For higher absolute values of ϵ, the time-domain behavior shows an increasing discrepancy with the linear model, which predicts a lower in-band noise. This is because the signal-dependent quantizer gain, assumed to be unity in the linear analysis, drops below unity in the time-domain simulation [23]. However, by adjusting the quantizer gain in the linear model to the effective quantizer gain found in the time-domain simulation [24], the agreement between time-domain simulations and the linear analysis is recovered almost completely.

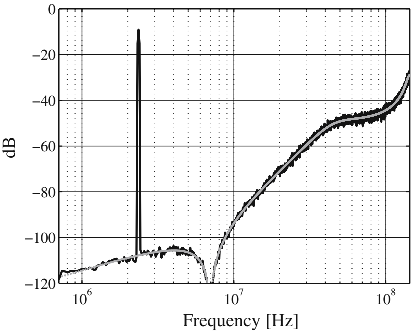


Fig. 10 FFT of CT DSM output for $\epsilon = -0.2$. *Black* Matlab time-domain simulations. *Grey* linear model of CT NTF from (4)

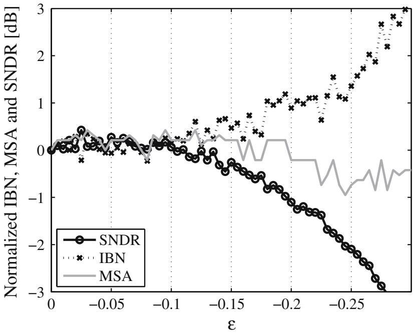


Fig. 11 Matlab simulation of IBN, MSA, and SNDR for a growing negative ϵ

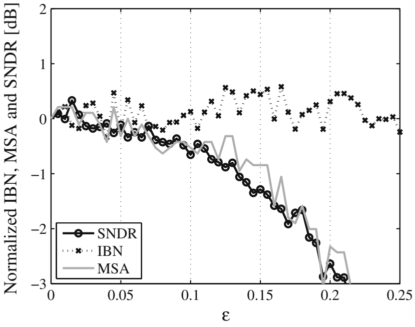


Fig. 12 Matlab simulation of IBN, MSA, and SNDR for a growing positive ϵ

modulator in Fig. 4 [25]. The target application is the ADC in a cellular receiver for the LTE standard, which has a 9 MHz signal bandwidth at baseband. A relatively low oversampling ratio (OSR) of 16 is chosen, resulting in a clock frequency of 288 MHz. A 576 MHz external clock is buffered and divided-by-two on-chip, to generate the 288 MHz quadrature clock phases clk0 and clk90.

5.1 Loop filter, quantizer and DWA

The loop filter in the modulator is built with active-RC integrators for high linearity. The amplifiers in the integrators make use of a folded-cascode topology [26] (although more power efficient solutions exist [27]) with unity loop-gain frequencies of $\text{Amp}_{1,2,3} = \{\ 1.6, 1.2, 0.8\ \}$ GHz. Each integrating capacitor is split into a 3-bit MIM capacitor array for tunability of the time constants in the loop filter.

The differential full-scale input amplitude was set to $V_{fs} = 600\ \text{mV}_{pk}$, which, together with the differential input resistance R_{b1} of 7.85 kΩ, sets the full-scale input current to $I_{fs} \approx 76\ \mu$ A. The right-half-plane zero in the frequency response of each integrator is compensated with a resistor in series with the integrator capacitor [28].

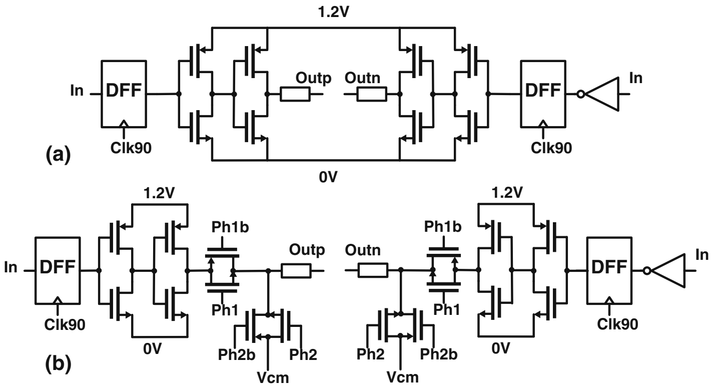
The quantizer is a 3-bit flash ADC with a differential input range of ±480 mV. An external voltage is buffered on-chip and fed to a resistive ladder to generate the reference voltages for the comparators. As described previously, a delay of $0.25T_s$ has been allocated for the quantizer latches, drivers, and DWA circuitry to settle. A Gray-Lewis differential dynamic comparator with a regenerative latch is used in the quantizer [29], together with an SR latch. The capacitive loading of the quantizer on the third integrator is kept small by using minimum-length transistors in the input pair of the comparator.

The DWA block has a 3-bit binary input and consists of an adder, a register and a shifter [30]. Data shifting in the DWA is performed by transmission gates configured as a logarithmic shifter. The DWA pointer is updated on the falling edge of clk0, providing an additional half sampling period for the operation of the 3-bit DWA adder.

5.2 Resistive feedback DAC

The current-steering DAC is widely used in multi-bit high-speed modulators, appearing in e.g. [7–12, 31–34]. Apart from the input resistors, DAC1 and the first integrator are the main contributors of thermal noise in the modulator [10]. To minimize the DAC noise, it is well-known that the overdrive voltage V_{od} of the MOS transistors implementing the current sources should be maximized. However, in a low-V_{DD} design like the one described here, the highest feasible V_{od} is still low, resulting in DAC1 dominating the overall noise budget. For this reason, a resistive multi-bit

Fig. 13 Unit DAC cell using a complementary resistive topology. **a** NRZ. **b** RZ



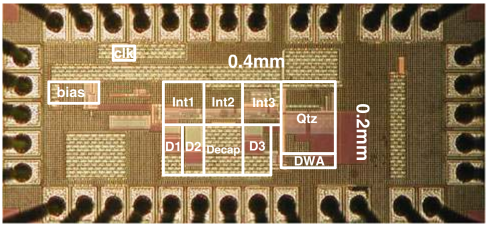


Fig. 14 Die photograph of the CT DSM prototype, with an active area of 400 × 200 μm^2

DAC [17] (Fig. 13a)) was chosen, which produces a lower thermal noise than the current-steering DAC.[4]

The resistive DAC has a lower output impedance than the current-steering DAC, which may cause distortion due to the signal-dependent output impedance in a differential implementation [34]. However, in a complementary implementation such as the one displayed in Fig. 13, the output DAC impedance is constant with the control word, and linearity is preserved.

The resistive DAC cell in Fig. 13 was implemented with poly-silicon resistors and low-threshold-voltage devices as switches. The reference voltages V_{refp} and V_{refn} were maximized to power supply (1.2 V) and ground, respectively, to minimize the current noise from the resistors. Since the switches are connected directly to supply and ground, a low on-resistance is achieved with small switches. The resistor matching requirements are relaxed by the DWA circuit to about 1%. The RZ DAC cell in Fig. 13(b) has a similar implementation as the NRZ DAC cell, with transmission gates added to provide RZ operation, while a non-overlapping clock generator is used to avoid short-circuiting the common-mode voltage reference to power supply or ground.

6 Measurement results

The 3rd-order, 3-bit, CT DSM was implemented in a 65 nm CMOS process, with an active chip area of 400 × 200 μm^2 (Fig. 14). The die was bonded in a CQFP 44 package for testing. The 3-bit output data was collected with an Agilent 16962A logic analysis module with differential probes, triggered by the clock output from the chip. An AFQ-100A I/Q signal generator from Rohde and

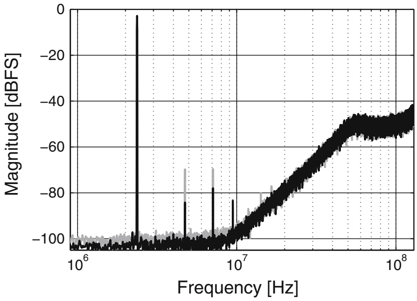


Fig. 15 32768-point FFT with −2.4 dBFS input signal at 2.36 MHz, with and without DWA. With DWA enabled, the noise floor is lowered by 2.5 dB, while HD2 = −81.4 dB and HD3 = −75.2 dB

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[4] A resistor is less noisy than a MOS transistor working in the active region. In fact, if both must deliver a current I_{DAC} with a voltage drop of V_{od}, the admittance G of the resistor is simply I_{DAC}/V_{od}, while the transconductance g_m of the MOS current source is twice as high, i.e. 2 I_{DAC}/V_{od}. Assuming that the noise contributions are proportional to G and g_m, respectively, with the same proportionality constant (assuming a channel noise factor $\gamma = 1$ for the MOS device), the MOS current source has twice as large noise power spectral density, compared to the resistive current source. Component-level simulations confirm this prediction with good quantitative agreement.

Schwarz was used to generate the baseband input signal, biased at common mode by two ZFBT-6 GW bias tees. The measured signal spectra were calculated in Matlab using Hann windowing and averaging.

The output spectra of a 2.36 MHz sine wave with a −2.4 dBFS input amplitude is shown in Fig. 15. The DWA algorithm is very effective, reducing the 2nd- and 3rd-order harmonic distortion by 13 and 8 dB, respectively, and the noise floor by 2.5 dB. The intrinsic resistor matching is better than expected, as Monte Carlo simulations predicted an SNDR in the order of 55 dB without DWA. The SNR and SNDR versus input amplitude are shown in Fig. 16. The peak SNR is 71 dB and the peak SNDR is 69 dB, occurring at −2.0 dBFS input amplitude.

To resemble what an ADC for a cellular receiver will be exposed to in practice, the modulator was tested with an interfering OFDM signal with a bandwidth of 18 MHz centered at 20, 40, 60 and 130 MHz. As example, Fig. 17 shows the spectra of the modulator output with the OFDM input centered at 20 MHz, for an OFDM signal power of −8 dBFS.

The power of the OFDM signal, which had a peak-to-average ratio (PAR) of approximately 13 dB when measured separately on the I and Q components, was swept for each center frequency. As a reference, each measurement was repeated with a single tone placed at the same center frequency. In Fig. 18, the IBN (including distortion components) is plotted versus the input power of both OFDM signal and single tone for 20 and 40 MHz center frequencies (the maximum power of the OFDM signal is limited by the instrument used). Both OFDM signals are within the passband of the STF, and hence overload the modulator at approximately the same input power. This is also true for the tones, although (only) at a 7 dB higher level. This means that when accounting for the additional dynamic range headroom required by an OFDM signal over a single tone, 7 dB will suffice, instead of the difference in PAR, which

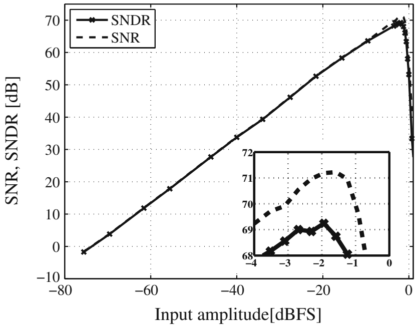

Fig. 16 SNR and SNDR versus input amplitude for a 2.36 MHz signal. Peak SNR is 71 dB and peak SNDR is 69 dB

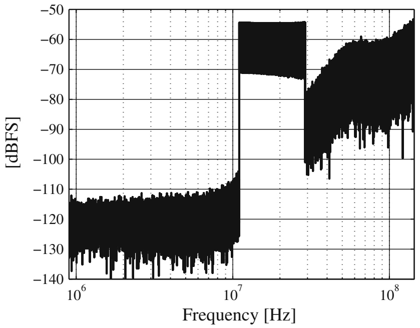

Fig. 17 1048576-point FFT with an 18 MHz OFDM signal centered at 20 MHz (i.e. in the adjacent receive channel) with −8 dBFS input power

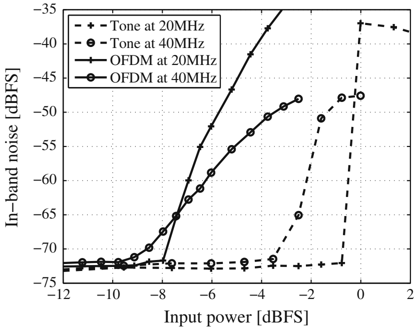

Fig. 18 In-band noise versus input power of a sine wave and an 18 MHz OFDM interferer centered around 20 and 40 MHz

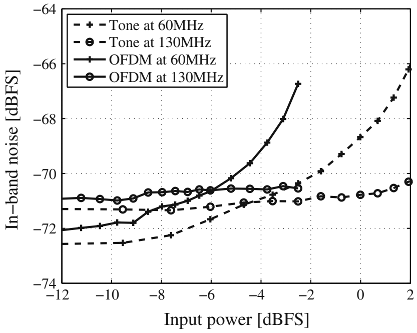

Fig. 19 In-band noise versus input power of a sine wave and an 18 MHz OFDM interferer centered around 60 and 130 MHz

Table 2 Comparison with state-of-the-art CT DSM having similar bandwidth

Ref.	fs (MHz)	BW (MHz)	SNR (dB)	SNDR (dB)	DR (dB)	P (mW)	Area (mm^2)	Tech. (nm)	FoM (fJ/c.)
[35]	640	18	–	73.6	78.1	3.9	0.08	28	28
[36]	300	10	–	70	70.6	2.57	0.05	40	50
[37]	1300	20.3	70	69	71	11.5	0.075	65	123
[38]	250	20	61.6	60	68	10.5	0.15	65	321
[39]	2560	20	63	61	63	7	0.08	65	191
[19]	500	25	69.1	67.5	72	8.5	0.23	90	88
[12]	640	10	–	65	67	6.8	0.4	90	240
[27]	3600	36	76.4	70.9	83	15	0.12	90	73
[40]	600	10	79.1	78	83.5	16	0.36	90	125
[41]	185	7	78.2	76.9	80	13.7	1.3	130	166
[42]	640	20	67.9	63.9	68	58	1.17	130	1133
[43]	1000	15.6	64.5	59.8	67	4	0.38	130	161
[44]	800	16	67	65	75	47.6	0.68	180	1002
This work	288	9	71	69	72	7.5	0.08	65	181

would predict $13 - 3 = 10$ dB (the PAR of a sinusoidal signal being 3 dB). It is also worthwhile to note that while a tone leads to an overload behavior with a rather abrupt IBN increase, degradation is more graceful in the case of an OFDM signal. For the tone, the IBN increases from -72 to -37 dBFS over a single measurement step ($\approx$0.75 dB of input power increment), whereas the same IBN degradation occurs over a range of 4 dB for the OFDM signal.

Figure 19 shows the corresponding results for interferers at 60 and 130 MHz. An extended dynamic range of the modulator is observed thanks to the lowpass nature of the STF, which effectively attenuates far–out interferers. As seen in the figure, the IBN is not much degraded by a signal at 130 MHz having a peak power far above full scale.

The total power consumption, including clock buffers, DAC references, frequency dividers and bias-current generators, is 7.5 mW from a 1.2 V power supply. The well-known figure-of-merit, $\mathrm{FoM} = \mathrm{P}/(2^{\mathrm{ENOB}} \cdot 2\mathrm{f_B})$, where ENOB = (SNDR − 1.76) / 6.02, is used to compare the modulators in Table 2.

7 Conclusions

A 3rd-order, 3-bit, continuous-time DSM with an NRZ/NRZ/RZ feedback scheme has been presented. By using an RZ current pulse in the innermost feedback DAC, the usually necessary loop-delay compensation in the modulator is avoided. The quadrature clock enables to center the RZ pulse in the sampling period, which significantly reduces the sensitivity to additional uncompensated loop-delay. Finally, the commonly used current-steering DAC was replaced by a resistive DAC, with improved thermal noise performance. The resulting modulator, integrated in a 65 nm CMOS process, displays an SNDR of 69 dB for a power consumption of 7.5 mW.

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Appendix

In this Appendix, the loop filter coefficients $a_{i,ct}$ of a 3rd-order CT DSM are derived from the loop filter coefficients $a_{i,dt}$ of a 3rd-order DT DSM. It is assumed that the DAC pulses (either NRZ or RZ) in the CT modulator can be delayed by up to one sampling period. The employed method is the impulse-invariant transformation [6, 45], in which the open-loop impulse response $h_{ct}(n)$ of the CT loop filter, sampled at the input of the quantizer, is mapped to the open-loop impulse response $h_{dt}(n)$ of the DT loop filter. The modulator sampling period T_s is normalized to unity.[5]

The $a_{i,ct}$ coefficients are needed to derive the general analytical expression for a_{4ct}, defined in (1) and used in Sects. 2 and 3.

The open-loop transfer function $H_{dt}(z)$ of the DT modulator is immediately found from Fig. 20, disregarding the g_1 feedback path[6], as

$$H_{dt}(z) = -\frac{a_{3dt}}{z-1} - \frac{a_{2dt}}{(z-1)^2} - \frac{a_{1dt}}{(z-1)^3}, \tag{5}$$

resulting in the time-domain open-loop impulse response of the DT loop filter equal to

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[5] In the special case of identical DAC pulses for all feedback paths, the loop filter coefficients are found in a straightforward manner following the approach proposed by Pavan [46].

[6] As already explained in Sect. 3. footnote 1, this path has no impact on $h_{dt}(1)$, which is the only sample compensated by a_4.

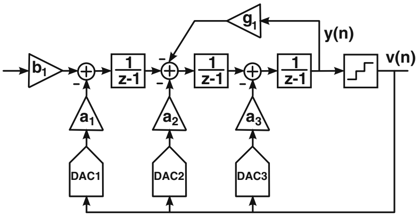

Fig. 20 3rd-order DT DSM serving as a reference for the CT DSM

$$h_{dt}(n) = -a_{3dt} - a_{2dt}(n-1) - a_{1dt}\left(\frac{n^2}{2} - \frac{3}{2}n + 1\right). \tag{6}$$

For the CT modulator, the DACs are assumed to deliver rectangular pulses $r_{\alpha,\beta}(t)$ of unit height, lasting from $t/T_s = \alpha$ to $t/T_s = \beta$ (Fig. 1(e)). Thus, $r_{\alpha,\beta}(t)$ is defined by

$$r_{\alpha,\beta}(t) = \begin{cases} 1, & \alpha \le t/T_s < \beta \\ 0, & \text{otherwise.} \end{cases} \tag{7}$$

It is assumed that the current pulse starts in the first sampling period for all three DACs, and stops in the following sampling period at the latest, i.e.

$$0 \le \alpha_i < 1$$
$$0 < \beta_i \le 2$$
$$\alpha_i < \beta_i$$

In the Laplace domain, $r_{\alpha\_i,\beta\_i}(t)$ becomes [6]

$$R_{\alpha_i,\beta_i}(s) = \frac{1}{s}\left(e^{-s\alpha_i} - e^{-s\beta_i}\right). \tag{8}$$

We proceed by deriving $H_{ct}(s)$, after which its inverse Laplace transform $h_{ct}(t)$ is computed and sampled at $t = nT_s$. If $\beta_i > 1$ for any of the DAC pulses, an additional parameter, $\gamma_i = \min(\beta_i, 1)$, is needed to handle correctly the first sample $h_{ct}(1)$ of the CT impulse response (i.e., for a DAC pulse with $\beta_i \le 1$, γ_i is equal to β_i; otherwise $\gamma_i = 1$).

Following the same procedure as in [6], and referring to Fig. 2(b), the sampled impulse responses for DAC4, DAC3, DAC2, and DAC1 are

$$\begin{aligned} h_{DAC4}(n) &= \mathcal{L}^{-1}\left\{-\frac{a_{4ct}}{s}\left(e^{-s\alpha_4} - e^{-s\beta_4}\right)\right\} \\ &= \begin{cases} -a_{4ct} & n = 1 \\ 0 & n \ge 2 \end{cases} \end{aligned} \tag{9}$$

$$\begin{aligned} h_{DAC3}(n) &= \mathcal{L}^{-1}\left\{-\frac{a_{3ct}}{s}\left(e^{-s\alpha_3} - e^{-s\beta_3}\right)\frac{1}{s}\right\} \\ &= \begin{cases} -a_{3ct}(\gamma_3 - \alpha_3) & n = 1 \\ -a_{3ct}(\beta_3 - \alpha_3) & n \ge 2 \end{cases} \end{aligned} \tag{10}$$

$$\begin{aligned} h_{DAC2}(n) &= \mathcal{L}^{-1}\left\{-\frac{a_{2ct}}{s}\left(e^{-s\alpha_2} - e^{-s\beta_2}\right)\frac{1}{s^2}\right\} \\ &= \begin{cases} -a_{2ct}\left[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}\right] & n = 1 \\ -a_{2ct}\left[(\beta_2 - \alpha_2)n + \frac{\alpha_2^2 - \beta_2^2}{2}\right] & n \ge 2 \end{cases} \end{aligned} \tag{11}$$

$$\begin{aligned} h_{DAC1}(n) &= \mathcal{L}^{-1}\left\{-\frac{a_{1ct}}{s}\left(e^{-s\alpha_1} - e^{-s\beta_1}\right)\frac{1}{s^3}\right\} \\ &= \begin{cases} -\frac{a_{1ct}}{2}\left[(\gamma_1 - \alpha_1) + \right. & \\ \left. +(\alpha_1^2 - \gamma_1^2) + \frac{\gamma_1^3 - \alpha_1^3}{3}\right] & n = 1 \\ -\frac{a_{1ct}}{2}\left[(\beta_1 - \alpha_1)n^2 + \right. & \\ \left. +(\alpha_1^2 - \beta_1^2)n + \frac{\beta_1^3 - \alpha_1^3}{3}\right] & n \ge 2 \end{cases} \end{aligned} \tag{12}$$

Obviously, $h_{ct}(n)$ is the sum of (9), (10), (11) and (12), which yields

$$\begin{aligned} h_{ct}(1) = {} & -a_{4ct} - a_{3ct}(\gamma_3 - \alpha_3) - a_{2ct}\left[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}\right] \\ & - \frac{a_{1ct}}{2}\left[(\gamma_1 - \alpha_1) + (\alpha_1^2 - \gamma_1^2) + \frac{\gamma_1^3 - \alpha_1^3}{3}\right], \end{aligned} \tag{13}$$

valid only for the first sample, $n = 1$, and

$$\begin{aligned} h_{ct}(n) = {} & -a_{3ct}(\beta_3 - \alpha_3) - a_{2ct}\left[(\beta_2 - \alpha_2)n + \frac{\alpha_2^2 - \beta_2^2}{2}\right] \\ & - \frac{a_{1ct}}{2}\left[(\beta_1 - \alpha_1)n^2 + (\alpha_1^2 - \beta_1^2)n + \frac{\beta_1^3 - \alpha_1^3}{3}\right] \end{aligned} \tag{14}$$

valid for the remaining samples, $n \ge 2$.

The CT coefficients $a_{1ct} - a_{3ct}$ can now be found by setting $h_{ct}(n)$ in (14) equal to $h_{dt}(n)$ in (6), resulting in

$$\begin{aligned} a_{1ct} &= \frac{a_{1dt}}{\beta_1 - \alpha_1} \\ a_{2ct} &= \frac{a_{2dt} + \frac{a_{1dt}}{2}(\alpha_1 + \beta_1 - 3)}{\beta_2 - \alpha_2} \\ a_{3ct} &= \frac{a_{3dt}}{\beta_3 - \alpha_3} + \frac{a_{2dt}}{\beta_3 - \alpha_3}\left[\frac{1}{2}(\alpha_2 + \beta_2) - 1\right] \\ &\quad + \frac{a_{1dt}}{\beta_3 - \alpha_3}\left[1 - \frac{1}{6}(\alpha_1^2 + \alpha_1\beta_1 + \beta_1^2)\right. \\ &\quad \left. + \frac{1}{4}(\alpha_2 + \beta_2)(\alpha_1 + \beta_1 - 3)\right] \end{aligned} \tag{15}$$

while a_{4ct} is found by setting $h_{ct}(1)$ in (13) equal to $h_{dt}(1)$ in (6):

$$a_{4ct} = a_{3dt} - a_{3ct}(\gamma_3 - \alpha_3) - a_{2ct}\left[(\gamma_2 - \alpha_2) + \frac{\alpha_2^2 - \gamma_2^2}{2}\right] - a_{1ct}/2\left[(\gamma_1 - \alpha_1) + (\alpha_1^2 - \gamma_1^2) + \frac{\gamma_1^3 - \alpha_1^3}{3}\right] \quad (16)$$

It is clear that the extra, fourth coefficient a_{4ct} is needed to match $h_{ct}(n)$ and $h_{dt}(n)$ at $n = 1$. Thus, the error ϵ mentioned in Sect. 4 coincides exactly with a_{4ct}. In this work, $\alpha_i = 0.25$, and an RZ pulse for DAC3 well contained within the first sampling period ($\beta_3 = 0.75$) is chosen, which makes a_{4ct} small enough to be omitted without compromising the modulator performance. The general analytical expression for a_{4ct} is found by inserting $a_{1ct} - a_{3ct}$ from (15) into (16), which yields (1).

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Paper IV

Paper IV

A 9MHz Filtering ADC with Additional 2nd-order $\Delta\Sigma$ Modulator Noise Suppression

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A 9 MHz Filtering ADC with Additional 2^{nd}-order $\Delta\Sigma$ Modulator Noise Suppression

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***Abstract*—This paper presents a filtering ADC for the LTE standard, where a Delta-Sigma modulator (DSM) is merged into the channel-select filter (CSF) of the LTE radio receiver. The CSF introduces an additional 2^{nd}-order suppression of both quantization and thermal DSM noise, while the CSF transfer function is essentially maintained. The 65 nm CMOS prototype is clocked at 288 MHz with a 9 MHz LTE bandwidth, and has an input-referred noise of 8.1 nV/$\sqrt{\mathrm{Hz}}$, 12 dB gain, and an in/out-of-band IIP3 of 11.5/27 dBV$_{\mathrm{rms}}$, with a power consumption of 11.3 mW, resulting in state-of-the-art figure-of-merits (FOMs) for filtering ADCs.**

I. INTRODUCTION

To reduce the power consumption of the ADC in a radio receiver, its dynamic range requirements are relaxed by a CSF attenuating the strong out-of-band interferers prior to A/D conversion. The amount of receiver noise contributed by the ADC is reduced thanks to the gain of the CSF and RF front-end. By incorporating the DSM ADC into the CSF [1], [2], the overall noise performance can be further improved, compared with the conventional CSF-DSM cascade. As an example, the 2^{nd}-order Rauch CSF in [2] provides a 1^{st}-order high-pass noise suppression, thereby reducing the noise of the DSM itself, contained inside the CSF.

This paper presents a filtering ADC, where a 3^{rd}-order continuous-time (CT) DSM is incorporated into a 2^{nd}-order Tow-Thomas low-pass CSF, which results in an additional 2^{nd}-order suppression of noise and distortion originating from the DSM. The relaxed requirements on the DSM afford significant power and area savings in an LTE receiver, and even more so in radios supporting carrier aggregation [3] and MIMO streams, where the number of analog baseband chains increases linearly with the number of simultaneously received independent channels. Thus, the filtering ADC is a very attractive alternative to the widespread CSF-DSM cascade in the design of modern radio receivers.

This paper is organized as follows: the benefits of the filtering ADCs are explained in detail in section II, while the design techniques to preserve the original CSF transfer function in the filtering ADC are described in Section III. Section IV presents a push-pull amplifier capable of linearly delivering large currents for handling strong out-of-band blockers, while a positive-feedback frequency compensation boosts the loop gain in the signal band; finally, several measurements on a fabricated prototype are presented in Section V.

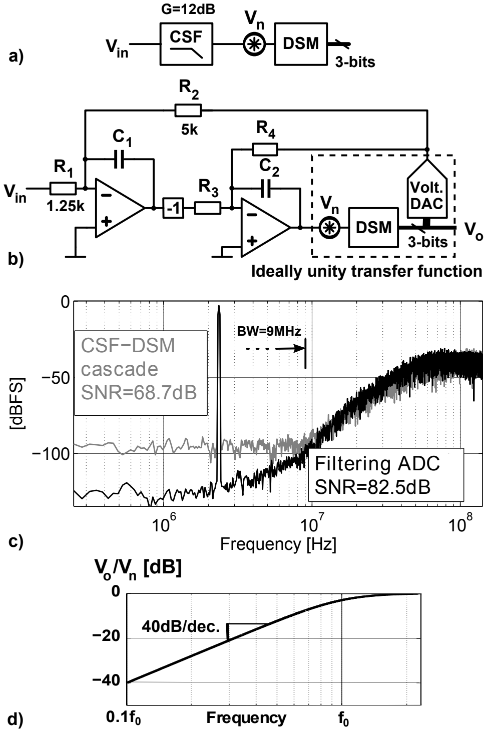

Fig. 1. a) CSF-DSM in cascade. b) Filtering ADC: DSM incorporated into 2^{nd}-order Tow-Thomas CSF. c) FFT of filtering ADC and CSF-DSM cascade with white noise from v_n. d) 2^{nd}-order suppression of v_n.

II. FILTERING ADC

Instead of the conventional cascade of CSF and DSM in Fig. 1a, the DSM is moved into the CSF, as shown in Fig. 1b. This requires in principle an additional voltage-mode DAC to convert the digital output back into an analog signal, shown in Fig. 1b. The CSF transfer function is not affected by this operation, provided the DSM-DAC cascade has a signal transfer function (STF) equal to 1 [V/V] well beyond the CSF cutoff frequency f_0. The key advantage of the filtering ADC is that the DSM noise is now suppressed by the global feedback loop of the CSF. The benefit is demonstrated in Fig. 1c, where both the conventional CSF-DSM cascade and filtering ADC are simulated with the white noise source v_n representing the

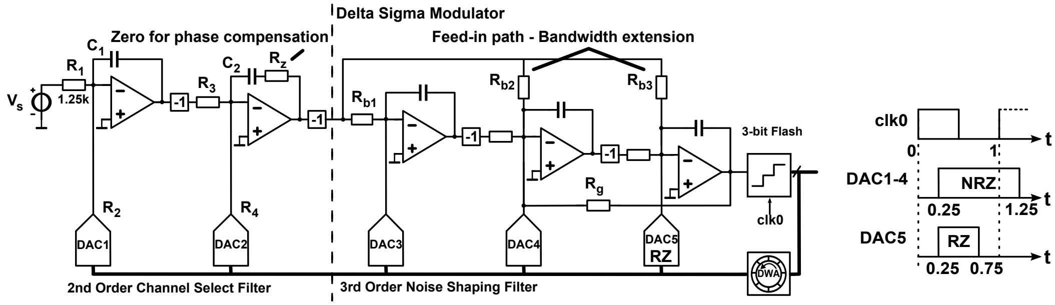

Fig. 2. Simplified schematic of the filtering ADC.

thermal noise of the DSM input. A 13.8 dB additional noise suppression over the 9 MHz LTE channel is obtained in the filtering ADC, compared to the CSF-DSM cascade. Distortion, quantization noise and flicker noise from the DSM are also 2^{nd}-order suppressed.

The 2^{nd}-order suppression enables three design choices: if both CSF and DSM are kept unchanged, the overall noise and linearity of the analog baseband is improved by the noise suppression. Alternatively, the overall performance can be kept constant and the DSM redesigned with a suitably lower performance, saving power (by roughly a factor four in the present case, based on the definition of FOM1, see Table I). Power can saved by a reduced order of the DSM, lower OSR, or fewer bits in the quantizer. Finally, if the DSM is kept unchanged, the CSF can be redesigned with a higher noise contribution and a lower power consumption. This is the approach taken in this work.

In any case, the filtering ADC provides an improved trade-off between noise and power consumption, and thus, the conventional CSF-DSM cascade appears as a less attractive choice.

The filtering ADC uses the Tow-Thomas filter of Fig. 1b, which provides a 2^{nd}-order suppression of DSM noise. This is a consequence of damping the 2^{nd} integrator [4] instead of the 1^{st}, which is more common. The filtering ADC has a total of 5 poles: 2 low-frequency Tow-Thomas poles performing filtering, and 3 high-frequency DSM poles providing a 3^{rd}-order quantization-noise shaping. The suppression of DSM noise is active below the CSF cutoff frequency f_0, as shown in Fig. 1d; the in-band quantization noise is as low as -95 dBFS, due to its overall 5^{th}-order shaping. At frequencies above f_0, the low CSF gain disables the operation of the outer loops (through R_2 and R_4 in Fig. 1b), causing the quantization noise at the filtering ADC output to be essentially the same as that of the 3^{rd}-order DSM itself.

III. CIRCUIT DESIGN

A single-ended version of the filtering ADC is shown in Fig. 2. The CSF is chosen as a 2^{nd}-order Butterworth with 12 dB in-band gain and -3dB cutoff frequency of 13.2 MHz, which yields a 0.8 dB droop at 9 MHz. The differential full-scale signal at the DSM input is $600\,\text{mV}_{pk}$, while the full-scale signal at the filtering ADC input is $150\,\text{mV}_{pk}$ due to the 12 dB gain. Current-mode DAC1 and DAC2 implement the cascade voltage-mode DAC and feedback resistors R_2 and R_4 in Fig. 1b. The area overhead from the 3-bit DACs DAC1 and DAC2 is small, due to the relaxed component matching requirements allowed by data-weighted averaging (DWA) dynamic element matching. The thermal noise from the DACs is reduced by adopting a switched-resistor architecture [**?**] instead of the more commonly used current-steering DAC.

The sensitivity to loop-delay variations in the DSM is greatly decreased by adopting a $1/4$-clock-cycle fixed loop delay, in combination with a return-to-zero (RZ) pulse in the inner-most feedback path in the DSM, see Fig. 2. In addition, the otherwise obligatory direct-feedback DAC for loop delay compensation can be omitted [5].

A. Compensation of DSM-DAC transfer function

A 3^{rd}-order low-pass CT DSM cascaded with a DAC (dashed part in Fig. 1b) displays a non-negligible STF phase shift already at frequencies close to the CSF cutoff frequency, due to the low OSR of 16. This phase shift causes a large peaking in the overall transfer function of the filtering ADC. The problem is counteracted by introducing two extra signal feed-in paths in the DSM through resistors R_{b2} and R_{b3}, as shown in Fig. 2. These paths effectively increase the bandwidth of the DSM and thus almost restore the original CSF Butterworth transfer function.

A further improvement is obtained by inserting an additional zero in the STF through the resistance R_z in the 2^{nd} CSF integrator, providing additional phase compensation. The remaining STF phase shift is exploited in the filtering ADC to compensate the 0.8 dB signal droop introduced by the CSF at the edge of the 9 MHz signal band. The -3dB cutoff frequency of the filtering ADC is 17.4 MHz, with a droop of only 0.2 dB at 9 MHz.

IV. PUSH-PULL AMPLIFIER WITH POSITIVE FEEDBACK COMPENSATION

The two-stage amplifier with AC-coupled push-pull output stage in Fig. 3 is used to obtain a large loop gain with improved linearity, and to deliver a high dynamic current to accommodate the strong out-of-band blockers present in the LTE receiver. IM3 simulations show improvements in the order of 15 dB when the push-pull output is enabled via C_{pp}, and the gain of the output stage increases as M_7 and M_8 operate in parallel above 2 MHz (set by R_b and C_{pp}).

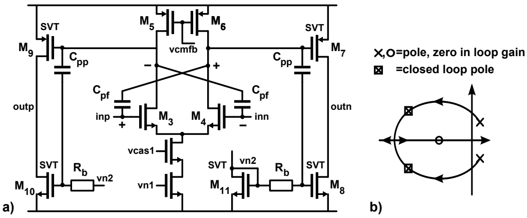

Fig. 3. a) Schematic of amplifier. b) Sketch of root-locus for PFC.

C_{pf} enables a positive feedback compensation [6] (PFC), connecting the positive output back to the positive input of the input stage, as indicated by the signs in Fig. 3a. A feed-forward path also exist through C_{pf}, resulting in a left half-plane (LHP) zero, instead of the right-half-plane (RHP) zero of Miller compensation. Thus, C_{pf} alters the positions of both zero and poles in the loop gain. The positive feedback path enables boosting the loop gain in the signal band by having imaginary loop poles, which may even appear in the RHP. However, the closed loop poles of the integrator can still be in the LHP, since the LHP zero and the feedback via the integration capacitor moves the closed-loop poles into the LHP, as illustrated by the root locus of Fig. 3b.

To show the effectiveness of the PFC, the loop gain for the first integrator in the CSF is simulated in Spectre without frequency compensation, with Miller compensation, and with PFC having imaginary loop poles, see Fig. 4. All three loop-gain plots converge to zero at DC, due to the capacitive feedback around the amplifier. As expected, the imaginary poles created by the PFC boost the loop gain above the uncompensated case in the signal band. The unity loop-gain frequency is improved from 820MHz to 1.25GHz, compared to the Miller compensation. The phase response starts at -90° due to the integration, and the LHP zero provides a robust phase response by creating a plateau around -290° (where -360° denotes the limit for instability). The unity loop-gain frequency and phase margin vary over 1.1-1.53 GHz and within ±5°, respectively, using process variations with slow-slow and fast-fast MOS device corners, $\mathrm{C_{min}}$-$\mathrm{C_{max}}$ MIM capacitor corners, and a temperature variation from -20 to 80 degrees. Simulations varying the value of C_{pf} confirm that its exact value is not critical for stability. If the transconductance of the push-pull stage is larger than that of the input stage, the approximate value of C_{pf} is

$$C_{pf} \approx \frac{g_{m4}(g_{m7}+g_{m8})(c_1+c_2)}{Q^2(g_{m7}+g_{m8}-g_{m4})^2}, \tag{1}$$

where c_1 represents the total capacitance at the internal node of the amplifier, and c_2 the sum of the load and input capacitance of the amplifier (assuming a large integration capacitor); g_{mi} is the transconductance of transistor M_i; and Q is the desired Q-value of the two closed-loop poles (e.g., $Q = 1/\sqrt{2}$ yields two Butterworth closed-loop poles).

V. MEASUREMENT RESULTS

The filtering ADC occupies 0.11 mm^2 in 65 nm CMOS (Fig. 5) and consumes 9.4 mA from a 1.2 V supply, including bias-current generators, clock buffers and frequency divider to generate quadrature clock phases, and DAC reference voltages. An FFT of the output signal is shown in Fig. 6(a) for a -3.5 dBFS, 2.0 MHz input, resulting in HD2 = -85 dB and HD3 = -79 dB. The thermal noise of the 1$^{\mathrm{st}}$ CSF integrator dominates the noise floor, masking the 2$^{\mathrm{nd}}$-order suppression of DSM noise. The peak SNR and SNDR in Fig. 6(b) are 69.0 dB and 68.4 dB, respectively, resulting in an input-referred noise of only 8.1 nV/$\sqrt{\mathrm{Hz}}$.

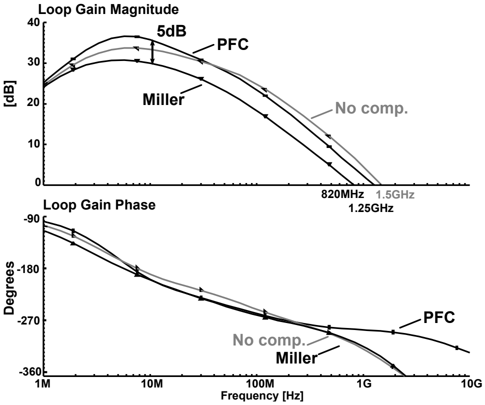

Fig. 4. Loop gain simulation of first integrator.

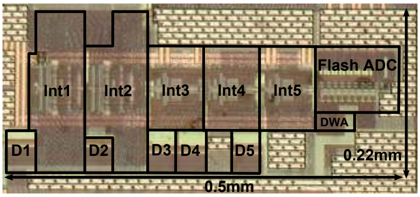

Fig. 5. Die photo (0.5mm×0.22mm active area).

Fig. 7 displays the lowpass STF of the filtering ADC, with a 0.15 dB droop at 9 MHz and a -3 dB cutoff frequency of 16.9 MHz, in very good agreement with simulations. If the feed-in paths via R_{b2} and R_{b3} are disabled, a very large peak appears in the STF close to the CSF cutoff frequency, as expected.

The dynamic range (DR) of the filtering ADC is defined as the difference between the maximum tolerated input signal before going unstable (maximum stable amplitude, MSA) and the in-band noise (-73.5 dBFS). The DR is highly improved by the CSF for frequencies beyond the CSF cutoff frequency, see Fig. 8. Above 60 MHz, the DR is limited to 93 dB by the ESD protection of the input pad. In a real-life application, it is also important to quantify the impact of an out-of-band interferer on the in-band noise; for this reason, we define $\mathrm{A_{1dB}}$ as the input signal for which the in-band noise rises by 1 dB. The $\mathrm{A_{1dB}}$ of the filtering ADC is plotted in Fig. 8.

Fig. 9(a) shows the spectra for two intermodulation (IM) measurements with two 0 dBFS input tones: the 2$^{\mathrm{nd}}$-order IM product (IM2) with input tones at f_1, f_2 = [40.2, 41.8] MHz is -96 dBFS, and the 3$^{\mathrm{rd}}$-order IM product (IM3) with input

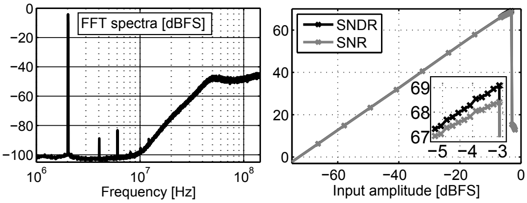

Fig. 6. (a) 32768-point FFT. (b) SNR, SNDR vs. input amplitude.

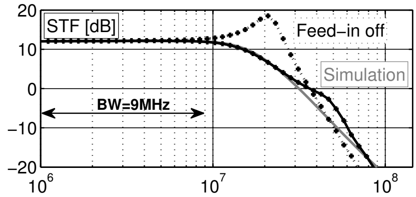

Fig. 7. Signal transfer function.

tones at $f_1, f_2 = [21.1, 41]$ MHz is -99 dBFS.

The linearity is characterized by the input-referred 2^{nd}- and 3^{rd}-order intercept point (IIP2 and IIP3), plotted in Fig. 9(b). The filtering ADC displays a high linearity, with in-band IIP2 and IIP3 of 55 $\mathrm{dBV_{rms}}$ and 11.5 $\mathrm{dBV_{rms}}$ respectively. The out-of-band IIP2, measured with two tones at 40 MHz and 41 MHz, is 72 $\mathrm{dBV_{rms}}$, while the out-of-band IIP3, with two tones at 40 MHz and 20.5 MHz, is 27 $\mathrm{dBV_{rms}}$. Fig. 9(b) shows IIP2 and IIP3 vs. frequency, with IM products always falling at 1 MHz.

As the filtering ADC is a combination of a filter and ADC, two FOMs are evaluated in Table I, where FOM1 is commonly used for ADCs, and FOM2 is often adopted for filters. FOM1 is here evaluated at four times the 9 MHz channel bandwidth (following the approach in [2]) to accommodate the effect of filtering. The DR includes the in-band noise, but not distortion, as the harmonics of the test tone fall out-of-band. However, FOM2 includes both the noise and intermodulation distortion of the filtering ADC. The performance is summarized in Table I, where state-of-the art FOMs are achieved compared to other filtering ADCs.

TABLE I
COMPARISON WITH FILTERING ADCS

Parameter	**This work**	[1]	[2]	[7]	[8]
BW (MHz)	**9**	1	6	6.5	5
fs (MHz)	**288**	64	405	96	160
SNDR (dB)	**68.4**	59	74.6	70.9	69.5
f_{-3dB} (MHz)	**16.9**	3	–	–	–
Gain (dB)	**12**	0-40	–	–	–
IRN (nV/$\sqrt{\mathrm{Hz}}$)	**8.1**	280*	–	–	–
In-band IIP3 ($\mathrm{dBV_{rms}}$)	**11.5**	19*	–	–	–
Out-of-band IIP3 ($\mathrm{dBV_{rms}}$)	**27**	–	–	–	–
Tech. (nm)	**65**	180	90	180	130
Vdd (V)	**1.2**	1.8	1.2-1.8	1.8	1.2
Power (mW)	**11.3**	2	54	122**	6
DR at BW×4 (dB)	**80**	65	90	–	–
FOM1 at BW×4 (fJ/c.)	**77**	700	180	–	–
FOM2, (fJ)	**0.075**	1.98	–	–	–

FOM1=$\mathrm{P/(2^{ENOB+1}BW)}$, ENOB=(DR-1.76)/6.02.
FOM2=$\mathrm{P/(N \cdot BW \cdot 10^{2/3(IIP3-P_{noise})/10}}$, $\mathrm{P_{noise}} = 10\log(\mathrm{IRN}^2 \cdot \mathrm{BW})$
*Calculated from data in [1]. **Complex filtering.

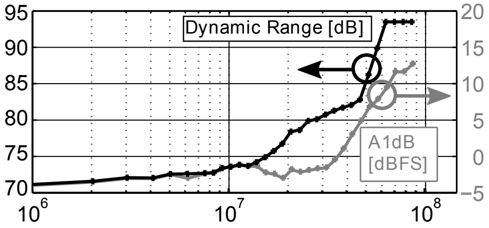

Fig. 8. Dynamic range and $\mathrm{A_{1dB}}$.

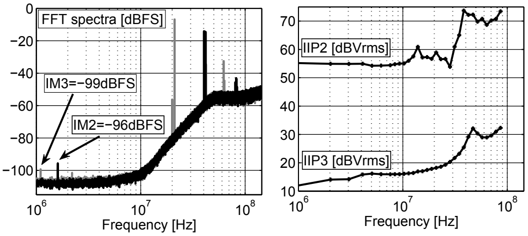

Fig. 9. (a) 131072-point FFT. Grey: IM3. Black: IM2. (b) IIP2 and IIP3 vs. frequency (IM products fall at 1MHz).

VI. CONCLUSIONS

A filtering ADC has been presented that enables an additional 2^{nd}-order suppression of DSM noise, compared to the conventional CSF-DSM cascade. A prototype, implemented in a 65 nm CMOS process, displays an input-referred noise as low as 8.1 nV/$\sqrt{\mathrm{Hz}}$, for a DSM noise suppression of 14 dB. A high linearity has been achieved using operational amplifiers with push-pull output stages and positive feedback compensation, obtaining a highly improved dynamic range in presence of strong out-of-band signals. The filtering ADC, targeted for the LTE communication system, shows state-of-the-art FOMs.

VII. ACKNOWLEDGEMENT

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Paper V

Paper V

A Filtering ΔΣ ADC for LTE and Beyond

M. Andersson, M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A Filtering ΔΣ ADC for LTE and Beyond," *IEEE Journal of Solid-State Circuits, submitted (invited)*, July 2014.

A Filtering $\Delta\Sigma$ ADC for LTE and Beyond

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***Abstract*—This paper presents a filtering ADC for the LTE communication standard, where a 2$^{\text{nd}}$-order Delta-Sigma modulator (DSM) is incorporated into the 3$^{\text{rd}}$-order Chebychev channel-select filter (CSF) of the radio receiver. The CSF introduces an additional 3$^{\text{rd}}$-order suppression of both thermal and quantization DSM noise, while the CSF transfer function is maintained. A design method for the filtering ADC accounting for unavoidable DSM-DAC delays is developed and experimentally demonstrated. The 65 nm CMOS prototype is clocked at 576/288 MHz with an 18.5/9.0 MHz LTE bandwidth, has an in-band gain of 26 dB, an SNDR of 56.4/58.1 dB, an input-referred noise of 5 nV/$\sqrt{\text{Hz}}$, and an out-of-band (half-duplex) IIP3 of 20/12 dBV$_{\text{rms}}$, with a power consumption of 7.9/5.4 mW.**

***Index Terms*—Continuous-time, delta sigma modulator, A/D converter, Channel-select filter, STF, Filtering A/D converter.**

I. INTRODUCTION

The power efficiency of the analog baseband of the (cellular) radio receiver (RX) is witnessing a renewed research effort, driven by the increased number of simultaneously received channels with carrier aggregation (CA) and/or MIMO, supported by upcoming releases of 3GPP LTE to meet the demand for higher data rates [1], [2]. The most challenging baseband condition is when the received signal mainly consists of strong out-of-band interferers, so-called blockers, while the desired signal is weak. Consequently, the dynamic range (DR) requirement (and thereby the power consumption) of the RX analog-to-digital converter (ADC) is relaxed by preceding it with a channel-select filter (CSF) to attenuate the blockers, as shown in Fig. 1a.

It is well-known that CT DSMs with feedback-compensated loop filters (CIFB) can provide a sharp filtering of high-frequency blockers by the proper design of their signal transfer function (STF) [3], [4]. However, a fundamental issue in a filtering DSM is that its STF and its noise transfer function (NTF) share the same poles [4]–[6]; therefore, the more aggressive the filtering, the poorer the in-band NTF.

While a vast amount of research has also been devoted to improving the STF in feedforward-compensated [7]–[11] and complex DSMs [12], a fundamental step toward a CSF-like selectivity combined with higher-order noise shaping was taken by Sosio *et al.*, who incorporated the DSM into a Rauch CSF to create a filtering ADC [13], [14]. The key benefit of this approach is that the global feedback loop of the Rauch CSF provides an additional 1$^{\text{st}}$-order noise shaping of the DSM noise, relaxing the noise requirements on the DSM itself, compared to a conventional CSF-DSM cascade. A more aggressive filtering ADC uses a 2$^{\text{nd}}$-order inverse follow-the-leader CSF topology [15], improving the additional DSM noise shaping from a few dB to above 10 dB.

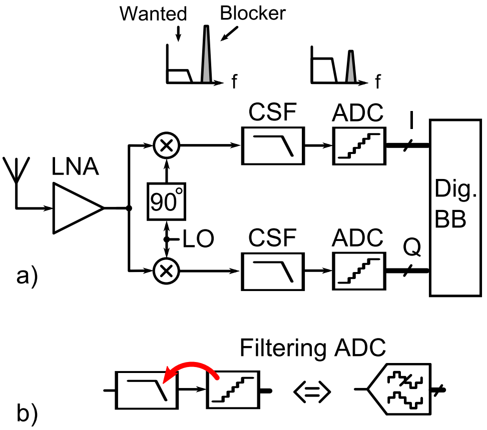

Fig. 1. a) Direct-conversion receiver. b) ADC merged into CSF to create a filtering ADC.

More in general, placing the DSM inside the CSF feedback affords the same advantages as a filter making use of global feedback: the noise from all integrators after the first is suppressed by the gain of the preceding integrators[1]. In a filter consisting of a cascade of biquads, on the other hand, the noise from the first integrator in all biquads remains unshaped [16], and the same is true for the DSM noise in a CSF-DSM cascade.

This paper presents a continuous-time (CT) filtering $\Delta\Sigma$ modulator (DSM) capable of providing an improved DR for out-of-band blockers. Thanks to this property, and to a low input-referred noise, this power-efficient circuit can replace the traditional CSF-ADC cascade in the RX, as graphically illustrated in Fig. 1b. While the work in [15] proved the

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[1] It should be noticed, though, that such a suppression becomes less effective close to the filter cut-off frequency, which is therefore advantageous to select in (slight) excess of the signal bandwidth. Alternatively, or additionally, gain should be developed by the first filter integrator, to suppress the noise from all following integrators (see Section III-B).

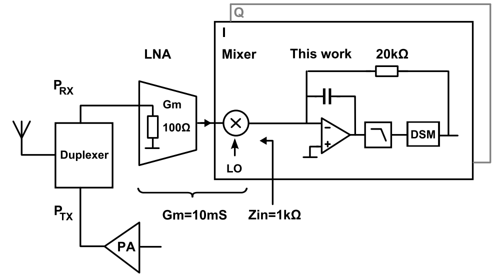

Fig. 2. Example of direct-conversion receiver.

feasibility of higher-order additional DSM noise shaping, this work targets the wideband LTE standards with RF bandwidths of 20 MHz and 2×20 MHz, the latter addressing contiguous CA (these RF bandwidths translate to baseband bandwidths of 9.0 MHz and 18.5 MHz, respectively). The filtering ADC is built with a 2^{nd}-order DSM embedded inside a 3^{rd}-order Chebychev CSF, where the 3^{rd}-order CSF transfer function (TF) contributes three zeros to the overall 5^{th}-order NTF of the filtering ADC. A frequency shift of the CSF poles, caused by the delay introduced by the DACs of the filtering ADC, is counteracted by adjusting the values of the CSF coefficients after a detailed theoretical analysis. The 65 nm CMOS prototype of the filtering ADC supports the 2×LTE20/LTE20 mode tailored for LTE Rel. 11 at a clock rate of 576/288 MHz, with a low power consumption and an overall state-of-the art performance.

II. RECEIVER CHAIN AND BLOCKERS

The filtering ADC is designed to operate in the assumed RX chain in Fig. 2 (single-ended representation for simplicity). The RX uses a transconductance LNA with a differential input impedance of 100Ω and a passive current-mode mixer terminated by the virtual ground of the (transimpedance) filtering ADC. The overall transconductance and noise figure (NF) of the LNA-mixer cascade are (reasonably) assumed to be 10 mS and 1.8 dB, respectively. The filtering ADC has a transimpedance of 20 kΩ, resulting in an overall RX voltage gain of 46 dB from LNA input to filtering ADC output. To simplify the standalone testing of the filtering ADC, the time-variant impedance of the RX front-end is replaced by a 1k Ω resistor. With this choice, the filtering ADC has a voltage gain of 26 dB.

In addition to the desired signal, the filtering ADC is subject to blockers entering the RX; in particular, the strong blocker generated by an FDD radio's own transmitter (TX) appears at the RX due the a limited TX-to-RX isolation in the antenna duplexer. Far away from the base station, the RX desired signal is weak, while the blockers (in particular the TX leakage) may be very strong. The RX linearity requirements for out-of-band signals are thus very high, to handle the out-of-band blockers without producing excessive distortion that folds on top of the weak desired signal. In particular, a low 2^{nd}- and 3^{rd}-order intermodulation distortion is required at the TX-to-RX (duplex) distance, where the strong TX leakage is situated.

The filtering ADC converts a single (LTE20), or two contiguous LTE channels (2×LTE20). The FDD-mode 2×LTE20 is adopted in band 1 (B1) and band 7 (B7) [1], while LTE20 is used in several bands, where B20 has the toughest TX leakage requirements, since this band has the lowest ratio of duplex distance to channel bandwidth. As a consequence, the CSF portion of the filtering ADC provides the lowest TX leakage attenuation in B20.

The receiver must meet several different test cases specified by 3GPP [1], as shown in Fig. 3: reference sensitivity (REFSENS), adjacent channel selectivity (ACS), narrow-band blockers (NBB), in-band blockers (IBB), out-of-band blockers (OBB), and intermodulation distortion (IMD). The REFSENS case specifies the minimum power of the desired signal, and varies with both band and channel bandwidth. The remaining test cases add a specific value to the REFSENS power level. According to 3GPP, a blocker is specified either as an unmodulated continuous-wave (CW) tone, or as a SC-FDMA QPSK modulated signal with a 5 MHz bandwidth and 8 dB peak-to-average ratio (PAR) at baseband.

The duplexer is assumed to attenuate the following at different frequencies: 2 dB for REFSENS, 2 dB for OBB1, 26 dB for OBB2, 27 dB for OBB3, and 54 dB at the duplex distance. The blocker power vs. frequency for 2×LTE20 (B1 and B7) and LTE20 (B20) at the RX input is shown in Fig. 3a and Fig. 3b, respectively.

The blockers in the first 25 MHz in Fig. 3b originate from ACS, NBB, and IBB test cases. NBB is specified for a CW tone, while ACS and IBB are modulated blockers. ACS1 is specified for the highest REFSENS in B1, B7 and B20. Above 25 MHz, the OBB requirements are defined for a CW tone, and must be fulfilled for frequencies from OBB1 to OBB2, from OBB2 to OBB3, and from and above OBB3. OBB2 has a lower power at the RX input than OBB1, due to the mentioned duplexer attenuations. In addition to individual blockers, the two signals testing IMD are a CW blocker at f_{int} and a modulated blocker at $2f_{int}$.

The remaining blocker test is due to the TX leakage for the REFSENS case, shown in Fig. 3 as TXL for the highest TX power of 26 dBm at the P_{TX} output in Fig. 2. It is clear that the TX leakage is the strongest blocker, which is a well-known challenge in FDD radio systems. The worst-case duplex distance for the CA case is 120 MHz (2×LTE20, B7), and 41 MHz for the single-carrier case (LTE20, B20).

III. THE FILTERING ADC

The purpose of this work is to merge the cascaded CSF and DSM of Fig. 4a into the single block of Fig. 4b, decreasing the overall power consumption without impairing performance. We start, however, by treating the general case.

A. A general model of the filtering ADC

A general model of the filtering ADC is shown in Fig. 5. It is well-known that the STF of a CT DSM (and of a filtering ADC, which is topologically identical, as discussed in Section V) is a mix of DT and CT TFs [16], [17]. However, at frequencies well below Nyquist, where the CSF poles

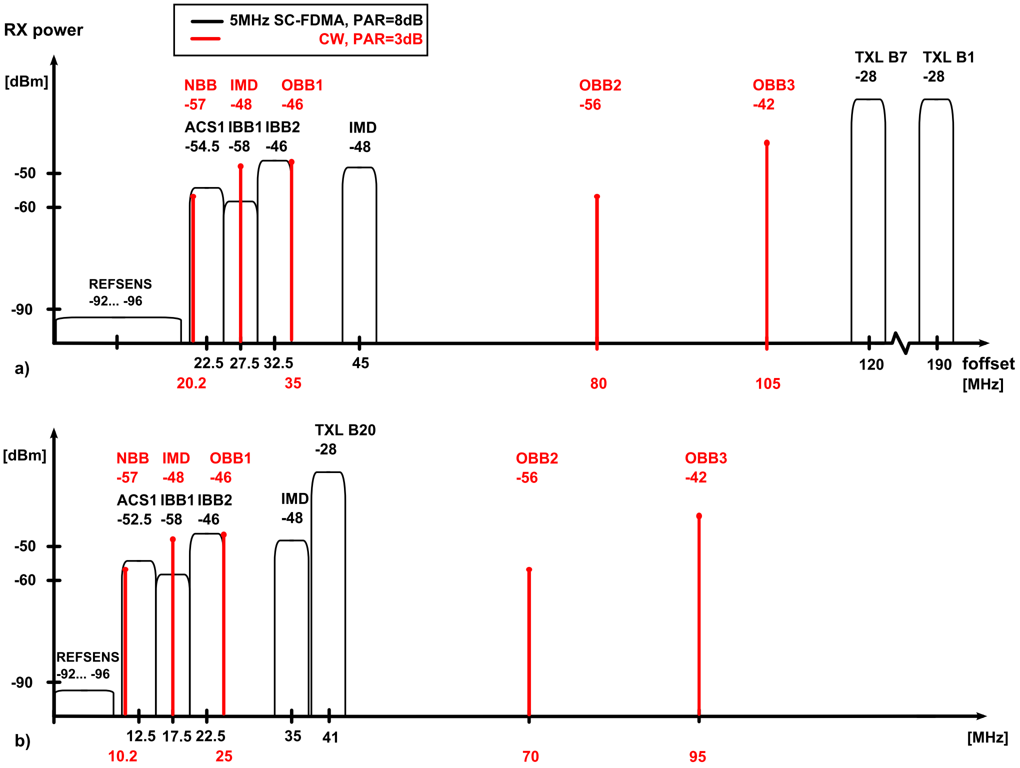

Fig. 3. Blocker test cases at the RX input for a) 2×LTE20; b) LTE20. A TX-to-RX attenuation of 54 dB is assumed.

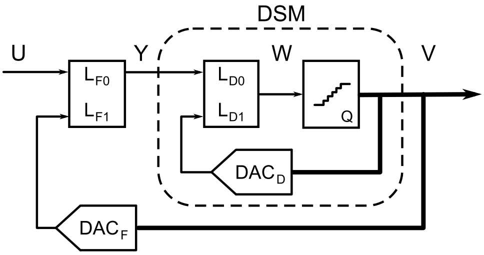

Fig. 5. Generic block diagram of a filtering ADC.

reside, a simplified s-model for all blocks in Fig. 5 can be used [18], [19]. Both CSF and DSM are modeled as two-input systems [16] through the two TFs $L_{F0}(s)$ and $L_{F1}(s)$ for the CSF, and $L_{D0}(s)$ and $L_{D1}(s)$ for the DSM. The respective feedback DACs have TFs $DAC_F(s)$ and $DAC_D(s)$. It is well known that the STF of the DSM, $STF_{DSM}(s)$, is

$$STF_{DSM}(s) = \frac{L_{D0}(s)}{1 - L_{D1}(s)\, DAC_D(s)}, \tag{1}$$

while the STF of the filtering ADC, $STF_a(s)$, is

$$STF_a(s) = \frac{L_{F0}(s)\, STF_{DSM}(s)}{1 - L_{F1}(s)\, DAC_F(s)\, STF_{DSM}(s)} \tag{2}$$

Clearly, if $STF_{DSM}(s) = DAC_F(s) = 1$, $STF_a(s)$ reduces to the TF of the CSF alone, i.e. $L_{F0}(s)/(1 - L_{F1}(s))$. In reality, $STF_{DSM}(s)$ and $DAC_F(s)$ are frequency dependent, which will be accounted for in section IV and in the Appendix.

The NTF of the filtering ADC, $NTF_a(s)$, is

$$NTF_a(s) = \frac{1}{1 - L_{F1}(s)\, L_{D0}(s)\, DAC_F(s)\; - L_{D1}(s)\, DAC_D(s)}, \tag{3}$$

and shows two fundamental properties. First, its denominator contains the product of $L_{F1}(s)$ and $L_{D0}(s)$, both (very) large at low frequencies, resulting in a higher-order noise shaping, compared to what is given by $L_{D0}(s)$ alone. As an example, in the filtering ADC of Fig. 4, $L_{F1}(s)$ implements three (low frequency) poles (i.e. those for CSF filtering), while $L_{D0}(s)$ implements two (high-frequency) DSM poles for standard 2^{nd}-order quantization-noise shaping. This yields an overall 5^{th}-order quantization-noise shaping for $NTF_a(s)$. Furthermore, and equally important, the noise (white or $1/f$) present at the DSM input is suppressed by $L_{F1}(s)$.

Secondly, at high frequencies NTF_a reduces to the NTF of the DSM itself, as the CSF provides no loop gain at frequencies well above the CSF cut-off frequency f_c. Thus, at high frequencies the quantization noise of the filtering ADC is essentially the same as for the DSM. More importantly, the stability properties of the DSM are not dependent on the CSF,

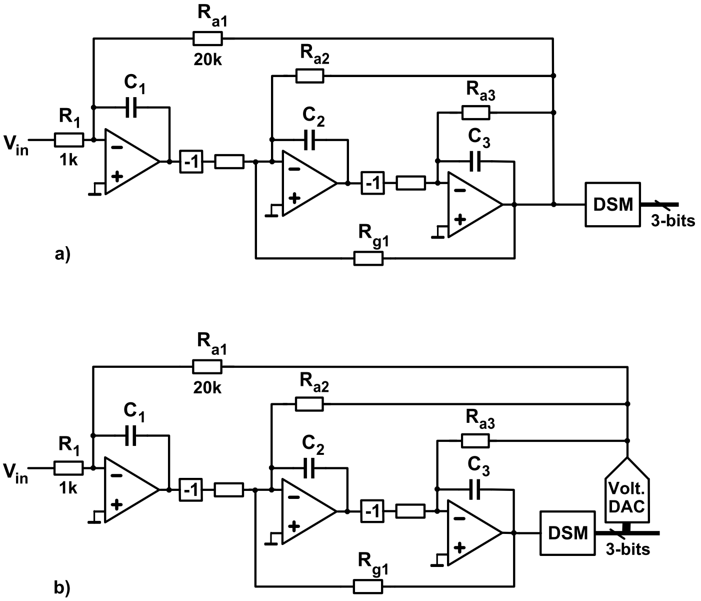

Fig. 4. a) Conventional CSF and DSM in cascade. b) Proposed filtering ADC: DSM merged into the CSF.

since f_c is much lower than the unity gain frequency of the DSM. Therefore, the DSM can be designed independently of the CSF, which highly simplifies the design of the filtering ADC.

B. Implementation of the filtering ADC

The filtering ADC of Fig. 4b requires an additional voltage-mode DAC to convert the digital DSM output back into an analog signal to close the loop around the CSF. In fact, the cascade of voltage-mode DAC and feedback resistors R_{a1}-R_{a3} is more easily implemented with current-mode DACs, as shown later.

A 3$^{\text{rd}}$-order Chebychev filter is used with 18.5 MHz/9.0 MHz bandwidth for 2×LTE20/LTE20, and an in-band ripple of 0.1 dB. Furthermore, such a CSF choice has the advantage of presenting a (relatively) high loop gain also close to the band limit, which, as remarked in the Introduction, is very beneficial for a high additional suppression of DSM noise.

The in-band gain from CSF input to DSM input is set to 26 dB, and is implemented by the ratio of R_{a1} to R_1. This relatively high gain, mainly developed by the first CSF integrator, strongly reduces the impact of a number of noise sources: all integrators after the first (where the second is the most prominent), the outermost feedback DAC (corresponding to the noise from the outermost feedback resistor R_{a1} in the CSF), the DAC reference voltage, and the clock circuitry driving the DAC, since the clock signal may display a relatively large amount of jitter.

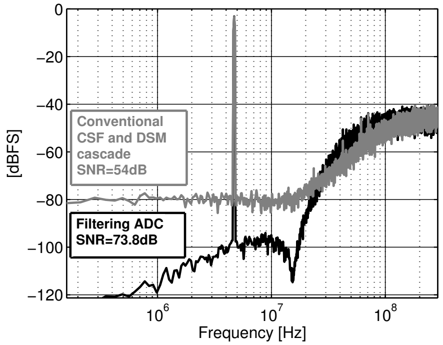

Fig. 6. Simulated spectra with white noise at the DSM input for: filtering ADC (black), and CSF-DSM cascade (grey).

C. Additional DSM noise shaping

The advantage of the filtering ADC is forcefully demonstrated in Fig. 6, where both the conventional CSF-DSM cascade and the filtering ADC (both with the aforementioned CSF gain of 26 dB) are simulated in the presence of a white noise source at the DSM input. Two of the three NTF_a zeros corresponding to the CSF poles are shifted from DC to the edge of the signal band by the local feedback loop created by R_{g1} (a standard technique in DSM design), creating the deep notch in Fig. 6. The CSF TF, however, is also affected by such a local feedback loop, which must be accounted for with a modification of the CSF coefficients. In total, a 19.8 dB suppression of DSM white noise over the 18.5 MHz

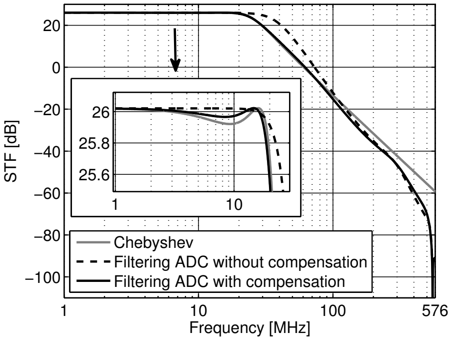

Fig. 7. Simulated STF of the filtering ADC. The STF with uncompensated delays shows a bandwidth expansion, while the STF with compensated delays is very close to the nominal STF.

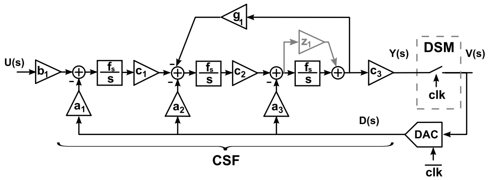

Fig. 8. Model of filtering ADC.

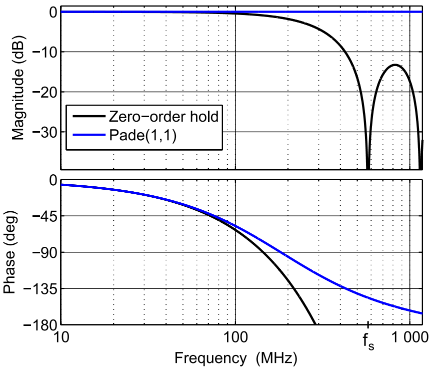

Fig. 9. Transfer function of zero-order hold with a half a sampling period delay, and Pade(1,1) approximations. Sampling frequency f_s is 576 MHz.

LTE channel is obtained in the filtering ADC, compared to the CSF-DSM cascade, while the quantization noise is much below the white noise level. DSM $1/f$ noise and distortion are also suppressed in the same way. Finally, we notice that noise shaping is no longer effective at frequencies above f_c, as expected.

The DSM noise suppression by 19.8 dB enables the adoption of a DSM with a much relaxed performance, saving power (roughly by a factor of eight, according to the Walden figure-of-merit [20]). Specifically, the DSM can have a lower order, a lower oversampling ratio, fewer quantizer levels, or allow more noise and distortion from its integrators. In general, the filtering ADC can be designed with a performance tracking that of the stand-alone CSF, but with a reduced power consumption compared to the CSF-DSM cascade.

IV. CSF DESIGN

The 3$^{\text{rd}}$-order CSF in Fig. 4a employs the so-called cascade-of-integrators-in-feedback (CIFB) architecture, often used in DSM design [16]. When the DSM is merged into the CSF, the CSF TF is affected by the delay of the DSM-DAC cascade, which mainly causes a bandwidth expansion, as is clear from Fig. 7. In the following, and more in detail in the Appendix, we show how the DSM-DAC delay is compensated by adjusting the CSF coefficients, recovering the original CSF TF.

A model of the filtering ADC of Fig. 4b is drawn in Fig. 8, which contains three sections: CSF, DSM, and non-return-to-zero (NRZ) feedback DAC. To begin with, $STF_{DSM} = 1$ is assumed, which is implicit when the DSM is modeled as the ideal sampling circuit in Fig. 8. This captures well the first-order behavior of the low-order DSM used here. The DAC is allocated a time $T_d = T_s/2$ for its input to settle, where T_s is the sampling (clock) period.

It is well-known that a NRZ DAC is a zero-order hold (ZOH) circuit, with transfer function

$$ZOH(s) = \frac{1 - e^{-sT_s}}{sT_s} = e^{-sT_s/2}\,\mathrm{sinc}(sT_s/2) \qquad (4)$$

The DAC TF is therefore, including the delay T_d, given by

$$DAC(s) = e^{-sT_d}\,ZOH(s) = e^{-sT_s}\,\mathrm{sinc}(sT_s/2) \qquad (5)$$

which, for signal frequencies much lower than the sampling frequency f_s, reduces to a pure delay of T_s.

A plot of (5) is shown in Fig. 9. The magnitude response has less than 1 dB attenuation up to f_s/4, which is far above f_c. Thus, it is sufficient to find an approximation of (5) that has a flat amplitude response of 0 dB, and a phase response that follows (5) for frequencies well above f_c. Ignoring the sinc term in (5), we mimic the pure delay T_s with a Pade(1, 1) [21] approximation:

$$e^{-sT_s} \approx \frac{1 - sT_s/2}{1 + sT_s/2} \qquad (6)$$

It is clear from Fig. 9 that the pole-zero pair follows closely (5) in magnitude and phase well beyond f_c. As shown in detail in the Appendix, the pole-zero approximation of (5) given by (6) is used to recalculate the CSF coefficients, producing an almost ideal Chebychev TF for the filtering ADC (Fig. 7).

The analysis above accounts for the unavoidable DAC delays in the filtering ADC, for an ideal DSM with $STF_{DSM} = 1$. In reality, the 2$^{\text{nd}}$-order DSM in section V has a frequency-dependent STF_{DSM} with a phase shift that affects the CSF TF in a similar manner as the T_s delay. This additional phase shift is compensated by adding a left half-plane (LHP) zero at $f_s/2$ in the CSF TF through the grey path z_1 in Fig. 8.

The STF of the complete filtering ADC, with and without overall delay compensations, is shown in Fig. 7. The bandwidth extension is very effectively counteracted by the techniques described above, and STF_a follows closely the

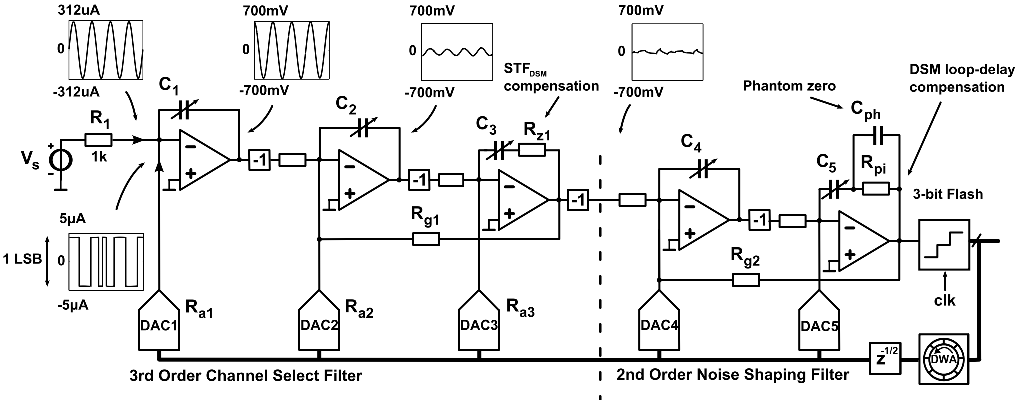

Fig. 10. Single-ended schematic of the filtering ADC. Voltages/currents show a 120 MHz tone emulating the maximum expected TX leakage in B7.

nominal Chebyshev TF, with an in-band ripple of slightly less than the nominal 0.1 dB, while the discrepancy at higher frequencies is due to the f_s notch typical of CT DSMs (see also Fig. 9).

V. CIRCUIT DESIGN

A single-ended version of the filtering ADC is shown in Fig. 10, where the first three integrators belong to the CSF and the last two to the DSM.

Looking at Fig. 10, it is clear that the filtering ADC is topologically identical to a 5$^{\text{th}}$-order DSM. However, and crucially, in a 5$^{\text{th}}$-order DSM all five poles are placed at high frequencies to aggressively minimize the in-band quantization noise, but providing no filtering at frequencies close to baseband. In our filtering ADC, on the other hand, three low-frequency CSF poles (mainly) perform filtering and two high-frequency DSM poles accomplish an optimized 2$^{\text{nd}}$-order shaping of the quantization noise, which, most importantly, is further suppressed by the three low-frequency CSF poles. Obviously, a 5$^{\text{th}}$-order DSM would provide a much lower in-band quantization noise than the filtering ADC, since the former's poles are optimized for such performance, but this, besides the lack of filtering, would be an unnecessary overkill: the key advantage of the filtering ADC is not that its CSF poles implement an *optimal* noise shaping, but rather that they offer a *substantial additional* noise shaping *for free*[2], without deteriorating the filtering capability of the filtering ADC.

The graphs in Fig. 10 exemplify the time-domain node voltages and branch currents with the largest anticipated blocker at the input of the filtering ADC, caused by TX leakage. A transient simulation with Spectre was carried out with a 120 MHz tone with the same peak amplitude and frequency as the TX leakage in B7. The TX leakage at the DSM input is highly suppressed by the CSF filter, as in a conventional CSF-DSM cascade, while the first CSF integrator sinks the largest part of the TX leakage current without causing distortion. Consequently, the DAC feedback current to the first integrator essentially contains only 1 LSB of quantization noise.

The filtering ADC operates in either 2×LTE20 or LTE20 mode by reconfiguring the integrator capacitors in CSF and DSM, to support 576/288 MHz clock frequency for an 18.5/9.0 MHz CSF cutoff frequency. The differential full-scale DSM input is 600 mV$_{pk}$, while the differential full-scale filtering-ADC input is 30 mV$_{pk}$, yielding the already mentioned 26 dB in-band gain. The resistor R_{z1} implements the z_1 compensation path in Fig. 8. The internal DSM quantizer and the feedback DACs are 3-bit, and all DACs are NRZ with a fixed delay of $T_s/2$ to allow the quantizer and DWA circuitry to settle. The 3-bit switched-resistor DAC from [22] implements the feedback resistors R_{a1}-R_{a3} of Fig. 4a with the same low noise level [23].

The discrete-time (DT) coefficients of the 2$^{\text{nd}}$-order CIFB DSM are found for an out-of-band gain of 2.5, resulting in an SQNR of 62 dB. The CT DSM coefficients are calculated for a total DSM loop delay that includes the fixed $T_s/2$ DAC delay, the finite switching DAC speed, and the limited gain-bandwidth product (GBW) of the integrators [24]. Thereafter, the DSM loop delay is compensated by inserting resistor R_{pi} in series with C_5 [25] (Fig. 10).

A. Push-pull operational amplifiers

The two-stage operational amplifier with AC-coupled push-pull output stage [15], [26] in Fig. 11a obtains a large gain with improved linearity, and delivers a high dynamic current for the strong out-of-band blockers. Simulations of 3$^{\text{rd}}$-order intermodulation distortion (IM3) show an improvement of 15 dB when the push-pull output is enabled via C_{pp}.

The bias currents for the 1$^{\text{st}}$ and 2$^{\text{nd}}$-5$^{\text{th}}$ amplifiers are shown by the black and grey numbers in Fig. 11a, respectively. The push-pull stage allows to use a quiescent current of only 180 μA, which is significantly less than the TX leakage of 312 μA$_{pk}$ (see Fig. 10), without clipping.

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[2] Or, more precisely, almost for free, since it costs more area and slightly more power to implement feedback DACs than resistors.

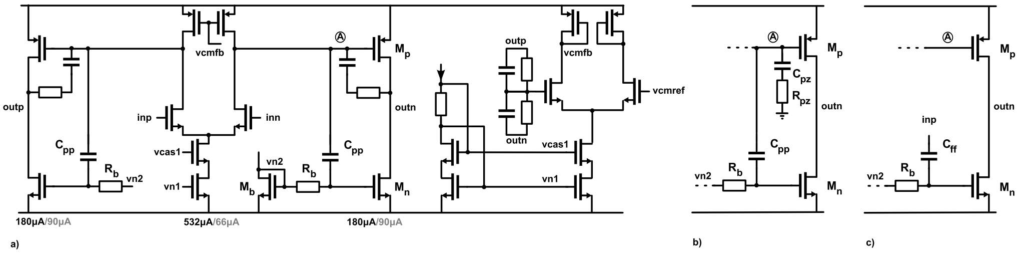

Fig. 11. a) Schematic of the operational amplifier, with push-pull output stage and pole-split frequency compensation; b) frequency compensation with pole-zero cancellation; c) feed-forward frequency compensation.

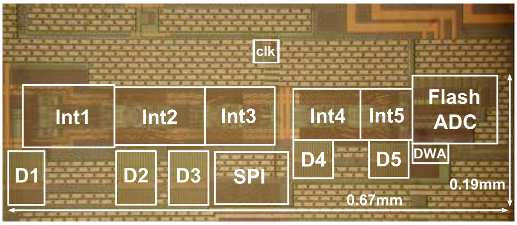

Fig. 12. Die photograph (0.67 mm× 0.19mm active area).

Three different frequency compensation techniques have been used in the amplifiers: pole-split in the 1st (Fig. 11a), pole-zero cancellation in the 2nd-4th (Fig. 11b), and feedforward path in the 5th. In the latter case, the speed requirement is highest [27], while the blockers have already been suppressed; thus, a push-pull output stage is not required. This enables a feedforward compensation [23] via capacitor C_{ff} (Fig. 11c), together with a phantom zero [28] created by C_{ph} (Fig. 10) to improve the phase margin to 46°, without impairing either GBW or power consumption.

VI. MEASUREMENT RESULTS

The filtering ADC was implemented in a 65 nm CMOS process, with a core area of 0.13 mm^2 (Fig. 12). Three different chips have been tested in 2×LTE20/LTE20 mode for 576/288 MHz clock rate, at a current consumption of 6.6/4.5 mA from a 1.2 V supply, including the current through the DAC reference voltages, clock input buffer, clock distribution, bias current generators, and common-mode voltage buffers.

A. Transfer function

The measured TFs of the filtering ADC for 2×LTE20 and LTE20 are shown in Fig. 13 and Fig. 14 respectively. The in-band gain is 26 dB, as expected, with an in-band ripple below 0.5/0.7 dB for 2×LTE20/LTE20. The worst-case frequency response at the alias frequencies in the vicinity of f_s is -43 dB for both 2×LTE20 and LTE20, resulting in an alias suppression of 69 dB, with small chip-to-chip variation.

At intermediate frequencies there is a chip-to-chip gain variation of up to 6 dB, with similar deviation in 2×LTE20 and LTE20 mode. This indicates that the deviation is not caused by an unaccounted delay in the loop, since this would have a larger impact at 576 MHz than at 288 MHz sampling frequency. From stand-alone measurements of the DSM STF (bypassing the CSF section), the DSM shows significantly higher bandwidth for Chip1, which displays the best overall system selectivity. However, and more importantly, these STF variations do not affect significantly the compression point

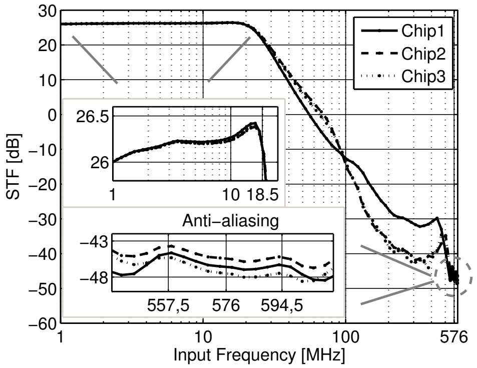

Fig. 13. Measured transfer function of filtering ADC. 2×LTE20 mode.

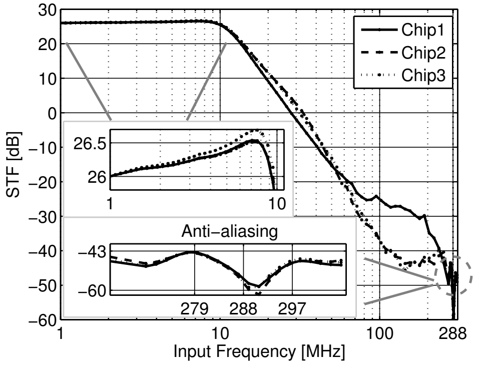

Fig. 14. Measured transfer function of filtering ADC. LTE20 mode.

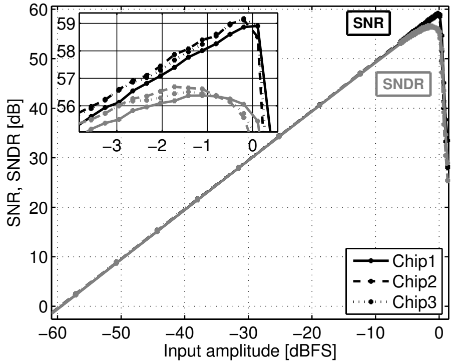

Fig. 15. SNR and SNDR, 2×LTE20 mode.

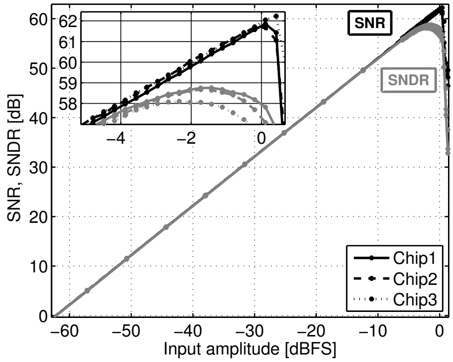

Fig. 16. SNR and SNDR, LTE20 mode.

of the filtering ADC, which is largely determined at high frequencies by the 1st CSF integrator.

The SNR and SNDR vs. input amplitude for a single in-band tone are shown in Fig. 15 and Fig. 16 for 2×LTE20 and LTE20, respectively. The worst-case peak SNR/SNDR are 58.9/56.4 dB for 2×LTE20, and 61.7/58.1 dB for LTE20.

The input-referred noise of the filtering ADC is $5.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, where 65% of the noise power is contributed by the $1\,\mathrm{k}\Omega$ input resistor whose purpose is to facilitate measurements. In the current-mode receiver in Fig. 2, this resistor and its noise would not be present, thereby reducing the noise power to $2.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. With the assumptions on the RX front-end mentioned in Section II, the addition of the filtering ADC to the RX would result in an overall RX NF of 2.2 dB.

B. IIP2 and IIP3

The linearity is characterized by the input-referred 2^{nd}- and 3^{rd}-order intercept points (IIP2 and IIP3), plotted in Fig. 17 and Fig. 18 for 2×LTE20 and LTE20, respectively. Each individual IIP2 point is found by sweeping the amplitude of two CW tones centered around the specified frequency, while IIP3 is found with one tone at the specified frequency and another slightly above half the specified frequency (so-called half-duplex test, the most critical for IIP3). IIP2 and IIP3 are plotted vs. the input signal frequency (the highest of the two in the IIP3 case), while making sure that the intermodulation product is always falling at 1 MHz. A high linearity is achieved, with a half-duplex IIP3 of $20/12\,\mathrm{dBV}_{\mathrm{rms}}$ at the filtering ADC input for 2×LTE20/LTE20. The duplex-distance IIP2 is $64/61\,\mathrm{dBV}_{\mathrm{rms}}$ at the filtering ADC input for 2×LTE20/LTE20. As expected, the IIP2, which is largely determined by component matching, varies from chip to chip, while the IIP3 is very similar across the three chips.

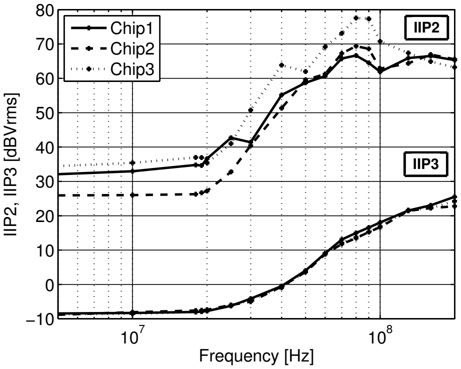

Fig. 17. IIP2 and IIP3 vs. frequency (with IM products always falling at 1 MHz). 2×LTE20 mode.

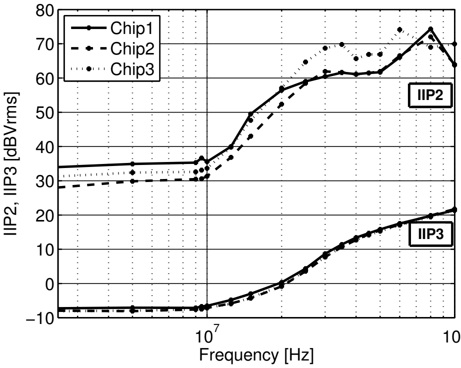

Fig. 18. IIP2 and IIP3 vs. frequency (with IM products always falling at 1 MHz). LTE20 mode.

C. Blocker tolerance

To investigate the tolerance to blockers (Fig. 3), the in-band noise vs. blocker power is measured. The performance is characterized by $\mathrm{P}_{1\mathrm{dB}}$, which we define as the blocker power for which the in-band noise rises by 1 dB compared to its zero-input level.

$\mathrm{P}_{1\mathrm{dB}}$ vs. frequency was found with a 5 MHz blocker (modulated with SC-FDMA with a baseband PAR of 8 dB) [1]

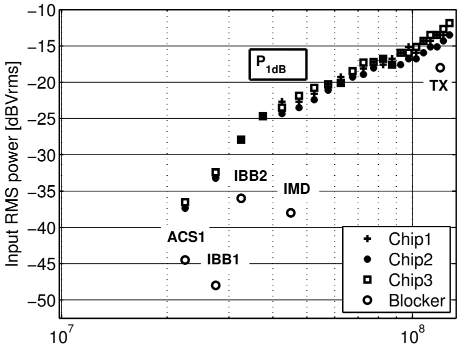

Fig. 19. P_{1dB} and blockers vs. frequency for a blocking 5 MHz SC-FDMA signal at 22.5... 127.5 MHz in 5 MHz steps. 2×LTE20 mode.

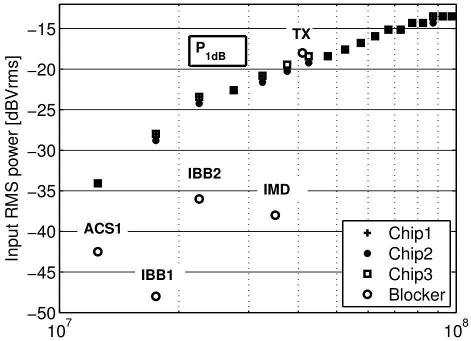

Fig. 20. P_{1dB} and blockers vs. frequency for a blocking 5 MHz SC-FDMA signal at 12.5... 97.5 MHz in 5 MHz steps. LTE20 mode.

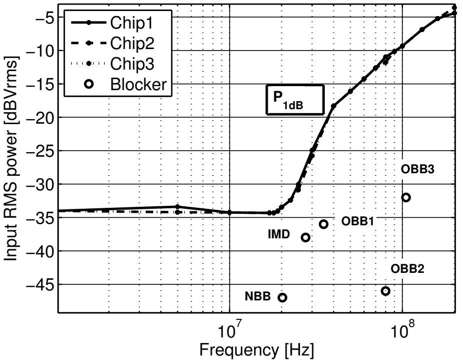

Fig. 21. P_{1dB} and blockers vs. frequency for a blocking CW tone. 2×LTE20 mode.

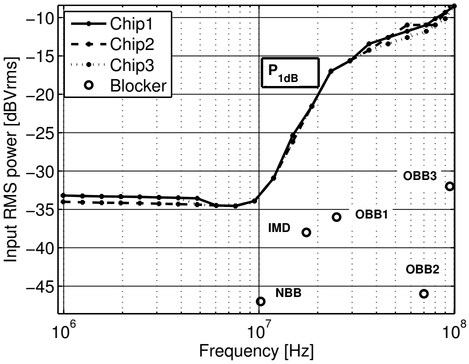

Fig. 22. P_{1dB} and blockers vs. frequency for a blocking CW tone. LTE20 mode.

centered at different frequencies. The results, together with the blocker levels from Fig. 3, are shown in Figs. 19 and 20 for 2×LTE20 and LTE20, respectively. In particular, the tolerance to TX leakage was measured at a duplex frequency of 120 MHz for 2×LTE20, and of 41 MHz for LTE20; P_{1dB} is $-15\,\mathrm{dBV_{rms}}$ and $-20\,\mathrm{dBV_{rms}}$, respectively. A very similar performance was achieved with an 18 MHz SC-FDMA blocker.

With the aforementioned RX front-end, the power in $\mathrm{dBV_{rms}}$ at the filtering ADC input (P_a) can be referred to the RX input (P_RX) in dBm by the simple relation

$$P_\mathrm{RX}[\mathrm{dBm}] = P_\mathrm{a}[\mathrm{dBV_{_{rms}}}] - 10 \tag{7}$$

Thus, the worst-case 2×LTE20 P_{1dB} of $-15\,\mathrm{dBV_{rms}}$ caused by TX leakage translates to -25 dBm at the RX input. This figure should be compared with the maximum TX leakage of -28 dBm (Fig. 3), which indicates that the TX leakage performance in 2×LTE20 mode is met with 3 dB margin. In LTE20 mode, the same performance is 2 dB short, due to the small duplex distance of 41 MHz in B20. Since the main culprit is the high-gain first CSF integrator, the issue can be solved straightforwardly by scaling down the voltage swing at this integrator output, with only a minor noise and power penalty.

P_{1dB} for a single tone was measured in the same fashion, and is displayed in Figs. 21 and 22 for 2×LTE20 and LTE20, respectively. The filtering ADC handles all tones and modulated blockers in 2×LTE20 and LTE20, except the TX leakage in LTE20, as explained above.

It is interesting to note that P_{1dB} varies much less from chip to chip than the TF at intermediate frequencies, as expected from the discussion in VI-A.

D. Figures of merit

The usual ADC figure-of-merit (FoM) focus on the in-band performance, and can not take into account the filtering of out-of-band blockers. Thus, we employ two other FoMs:

$$\begin{aligned}\mathrm{FOM1} &= P/(2^{(DR-1.76)/6.02}\cdot 2\,BW) && (8)\\ \mathrm{FOM2} &= P/(N\cdot BW\cdot 10^{2/3(\mathrm{IIP3}-\mathrm{P_{noise}})/10}) && (9)\end{aligned}$$

where P is the total power consumption, $P_\mathrm{noise} = 10\log(\mathrm{IRN}^2\cdot\mathrm{BW})$ is the input-referred noise in $\mathrm{dBV_{rms}}$,

IRN is the input-referred noise power spectral density, BW is the bandwidth of the desired signal, and N is the number of filter poles.

FOM1 is the Walden FoM [20], where the out-of-band (instead of in-band) DR is used to account for filtering. The DR is here defined as the ratio of P_{1dB} to P_{noise}; furthermore, the DR is measured at four times the channel bandwidth [14], where the worst-case strong TX leakage is present. The increased in-band noise caused by the TX leakage is captured by the DR, while distortion is not, since the harmonics of the out-of-band blockers fall out-of-band as well. FOM2, on the other hand, includes both noise and intermodulation distortion performance, and is frequently used when evaluating filters [29]. The excellent performance of the filtering ADC, quantified by FoM1 and FoM2, is summarized in Table I.

VII. CONCLUSIONS

This paper has presented a filtering ADC, where the channel-select filter (CSF) and the $\Delta\Sigma$ modulator (DSM) have been merged. The filtering ADC yields an additional shaping of DSM noise and distortion, which can be exploited to save power. The CSF properties are kept, such as the sharp 3rd-order Chebyshev response, the low input-referred noise, and the blocker tolerance, IIP2 and IIP3 rising with frequency. The filtering ADC consumes only 7.9/5.4 mW for a signal bandwidth of 18.5/9.0 MHz, with a state-of-the-art performance.

VIII. ACKNOWLEDGEMENTS

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TABLE I
WORST-CASE PERFORMANCE SUMMARY FOR THE FILTERING ADC

Parameter	BW=18.5MHz	BW=9.0MHz
fs (MHz)	**576**	**288**
SNR (dB)	**58.9**	**61.7**
SNDR (dB)	**56.4**	**58.1**
Gain (dB)	**26**	**26**
f_{-3dB} (MHz)	**25.0**	**12.1**
In-band ripple (dB)	**0.5**	**0.7**
Anti-aliasing (dB)	**69**	**69**
IRN (nV/$\sqrt{\mathrm{Hz}}$)	**5.1**	**5.1**
In-band IIP2 (dBV$_{\mathrm{rms}}$)	**26**	**28**
In-band IIP3 (dBV$_{\mathrm{rms}}$)	**-8.5**	**-8**
IIP2 at duplex (dBV$_{\mathrm{rms}}$)	**64**	**61**
IIP3 at duplex (dBV$_{\mathrm{rms}}$)	**20**	**12**
Tech. (nm)	**65**	**65**
Vdd (V)	**1.2**	**1.2**
Power (mW)	**7.9**	**5.4**
Area (mm^2)	**0.13**	**0.13**
DR at BW×4 (dB)	**82**	**84**
FOM1 at BW×4 (fJ/c.)	**21**	**23**
FOM2 (fJ)	**0.32**	**0.26**

IX. APPENDIX

In this section, we find the correct values of the CSF coefficients a_1-a_3 in the filtering ADC, which compensate for the DAC delay discussed in Section IV. With reference to Fig. 8, the path z_1 will be disregarded since it has a very minor effect on the final result, while the analysis is considerably simplified. From Fig. 5 with $STF_{DSM} = 1$, the expression of STF_a for a general $DAC_F(s)$ becomes

$$STF_{a,d}(s) = \frac{L_{F0}(s)}{1 - DAC_F(s)\, L_{F1}(s)} \tag{10}$$

With reference to Fig. 8, $L_{F0}(s)$ and $L_{F1}(s)$ are

$$L_{F0}(s) = \frac{b_1 c_1 c_2 c_3 f_s^3}{s(s^2 + g_1 c_2 f_s^2)}, \tag{11}$$

$$L_{F1}(s) = \frac{-c_3 f_s (s^2 a_3 + s a_2 c_2 f_s + a_1 c_1 c_2 f_s^2)}{s(s^2 + g_1 c_2 f_s^2)} \tag{12}$$

where a_i, g_i, and c_i are all positive. From (11), (12), and the pole-zero in (6), (10) becomes

$$STF_{a,d}(s) = \frac{(2/T_s + s) c_1 c_2 c_3 b_1 f_s^3}{D_{a,d}(s)}, \tag{13}$$

$$\begin{aligned} D_{a,d}(s) &= s^4 + s^3(2 - a_3 c_3 f_s T_s)/T_s \\ &+ s^2 f_s (c_2 f_s T_s (g_1 - a_2 c_3) + 2 a_3 c_3)/T_s \\ &+ s f_s^2 c_2 (2 g_1 + 2 a_2 c_3 - a_1 c_1 c_3 f_s T_s)/T_s \\ &+ 2 a_1 c_1 c_2 c_3 f_s^3 / T_s \end{aligned} \tag{14}$$

where we recall that $f_s = 1/T_s$. Thus, the effect of the DAC delay is to shift the three CSF poles to higher frequencies, as well as to introduce a high-frequency zero at $2/(2\pi T_s)$, and a high-frequency pole. Our strategy is now the following: we push the three low-frequency poles of $STF_{a,d}(s)$ back to their original CSF frequencies, while we disregard the fourth high-frequency pole, which will fall well out-of-band anyway, and possibly close to the high-frequency zero, which is disregarded as well. This amounts to forcing $STF_{a,d}(s)$ into the form

$$STF_a(s) = \frac{\omega_4}{s + \omega_4} H_{CSF}(s), \tag{15}$$

where ω_4 is unknown, and $H_{CSF}(s)$ is the ideal 3rd-order CSF TF, written in all generality as

$$H_{CSF}(s) = A \frac{\omega_r}{s + \omega_r} \cdot \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \tag{16}$$

with known values of A, ω_r, ω_0, and Q. Therefore, (15) becomes

$$STF_a = \frac{A \omega_0^2 \omega_r \omega_4}{D_a(s)}, \tag{17}$$

$$\begin{aligned} D_a(s) &= s^4 + s^3(\omega_0/Q + \omega_r + \omega_4) \\ &+ s^2(\omega_r \omega_0/Q + \omega_0^2 + \omega_4(\omega_r + \omega_0/Q)) \\ &+ s(\omega_r \omega_0^2 + \omega_4(\omega_0^2 + \omega_r \omega_0/Q)) \\ &+ \omega_4 \omega_r \omega_0^2 \end{aligned} \tag{18}$$

By equating the s-coefficients in (14) to the corresponding ones in (18), we obtain four equations in the four unknowns a_1-a_3 and ω_4, whose solution yields the desired result, as clear from Fig. 7.

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