Control of Distributed Generation Systems—Part I: Voltages and Currents Control

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***Abstract*—This paper discusses a digital control strategy for three-phase pulse-width modulation voltage inverters used in a single stand-alone ac distributed generation system. The proposed control strategy utilizes the perfect robust servomechanism problem control theory to allow elimination of specified unwanted voltage harmonics from the output voltages under severe nonlinear load and to achieve fast recovery performance on load transient. This technique is combined with a discrete sliding mode current controller that provides fast current limiting capability necessary under overload or short circuit conditions. The proposed control strategy has been implemented on a digital signal processor system and experimentally tested on an 80-kVA prototype unit. The results showed the effectiveness of the proposed control algorithm**

***Index Terms*—Digital signal processor (DSP), distributed generation system (DGS), pulse-width modulation (PWM) voltage inverters.**

I. Introduction

TECHNIQUES for producing low total harmonic distortion (THD) in pulse-width modulated (PWM) inverters (single-phase or three-phase) have been known to exist in several prior works. In the early days, the carrier-modulated PWM techniques such as the triangular wave comparison type PWM are very popular [1]–[3]. Microcomputer based techniques using preprogrammed PWM pattern have also been utilized [4]–[7], [22]. In these techniques, the PWM patterns are generated by computing the switching edges which satisfy specified performance requirements such as controlling the fundamental component and eliminating certain harmonics. Two main disadvantages of these techniques are slow voltage regulation response due to average voltage control, and phase displacement between the reference sine wave and the filter output varies with the load [15]. More recent techniques include the time optimal response switching PWM [8]–[10] and the real-time deadbeat-controlled PWM [11], [12]. These techniques have very fast response for load disturbances, but it is also known that these systems have a high THD for nonlinear load (crest-load).

The voltage control technique proposed here uses the perfect control of robust servomechanism problem [perfect robust servomechanism problem (RSP)] theory developed in [13] to ensure perfect tracking of the output voltages under unknown load by providing means for eliminating errors at specified harmonic and at the same time ensuring good transient response. The theory is based on the internal model principle, proposed in [14] which states that asymptotic tracking of controlled variables toward the corresponding references in the presence of disturbances (zero steady-state tracking error) can be achieved if the models that generate these references and disturbances are included in the stable closed loop systems. In other words, if we include the frequency modes of the references and the disturbances to be eliminated in the control loop, then the steady-state error will not contain these frequency modes. Applying the internal model principle into the output voltages control in a three-phase PWM inverter means that the fundamental frequency mode (50–60 Hz) has to be included in the controller since the references vary at this frequency. Elimination of the voltages errors due to the load currents at other harmonics frequency can then be achieved by including the frequency modes of these harmonics into the controller. The perfect RSP theory combines this internal model principle with optimal state feedback to guarantee stability of the closed loop system and providing arbitrary good transient response.

Similar techniques that use the internal model principle to achieve very low THD output voltage in single-phase PWM inverters have been reported recently in [15] and [16]. In these papers, the control development follows the repetitive control theory developed in [17]–[19]. Unlike the technique based on the perfect RSP that provides zero steady-state error for references or disturbances only at finite specified frequencies, the repetitive control guarantees zero steady-state error at all the harmonic frequencies less than half of the sampling period. However, the repetitive control is not easy to stabilize for all unknown load disturbances and cannot obtain very fast response for fluctuating load. In [15], the latter problem is solved by including a "one sampling ahead preview controller," and [16] enhances the stability result of [15] by providing an adaptive mechanism for unknown load disturbances.

The authors would like to point out here that, although the perfect RSP used in this paper only eliminates voltage harmonic at a finite specified frequencies, the perfect RSP control is still a very suitable control for a three-phase PWM inverters. It is to be emphasized that in a three-phase system, most of the voltage harmonics, the even harmonics, are either nonexistence and/or uncontrollable, or negligible in values. Therefore, not too many harmonics are left for the control to handle. Since the perfect RSP controller contains only poles at specific harmonic frequencies to be eliminated, the closed loop stability under unknown load is easier to achieve while providing a good transient response as compared to the repetitive control. The latter includes all the poles

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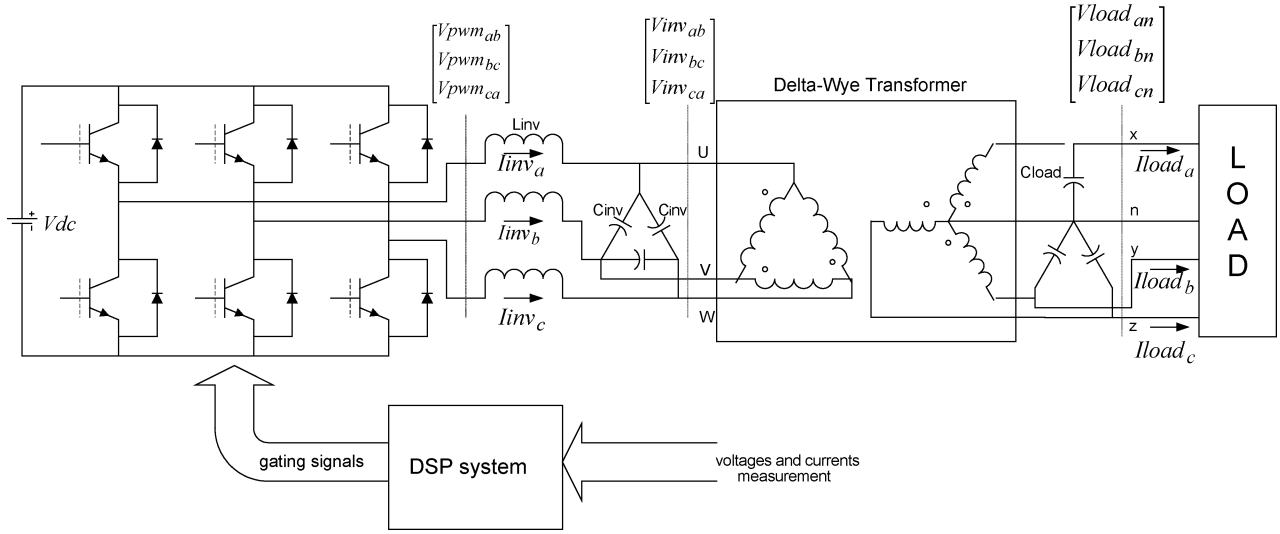

Fig. 1. Power converter system.

at frequencies up to half the sampling frequency, and the presence of these additional poles may affect the placement of the overall closed loop poles for achieving good transient response.

In this research, the authors have also successfully combined the perfect RSP control of the voltages harmonics with a fast current controller using a discrete time sliding mode controller [20] for limiting the inverter currents under overload condition. This is one of the important features necessary for a stand-alone DGS, which is not addressed in the repetitive control work of [15] and [16]. The discrete sliding mode controller has been chosen because of the fast and no-overshoot response that it provides. The current controller acts as an inner loop to the perfect RSP control of the output voltages in the outer loop. In this case, the perfect RSP voltage control has been designed by accounting for the extra dynamic introduced by the discrete time sliding mode controller. This way, the stability and robustness of the overall control system are still guaranteed.

This paper is organized as follows. Section II provides a description of the power converter system and its state space model development. Section III explains systematically the design of the voltage and current controllers using the two control techniques. Experimental results of the proposed control strategy are given in Section IV. Section IV also provides comparison between the proposed control with a commonly used synchronous reference frame control using a proportional integral (PI) controller.

II. Power Converter System

The power converter system used in this research consists of a typical three-phase PWM voltage inverter with LC output filter ($Linv$ and $Cinv$) and a delta-wye transformer that acts both as a potential transformer and electrical isolation to the load. Fig. 1 shows a circuit diagram of the system. Notice that the delta-wye transformer converts a three-wire (UVW) power system of the inverter to a four-wire (XYZ-N) system for the load. Small capacitors (denoted as $Cload$ in Fig. 1) are added at the load side of the transformer to provide further harmonics filtering and stabilization of the load voltages. A digital signal processor (DSP) system controls the operation of the power converter, providing required PWM gating signals to the power devices. Voltages and

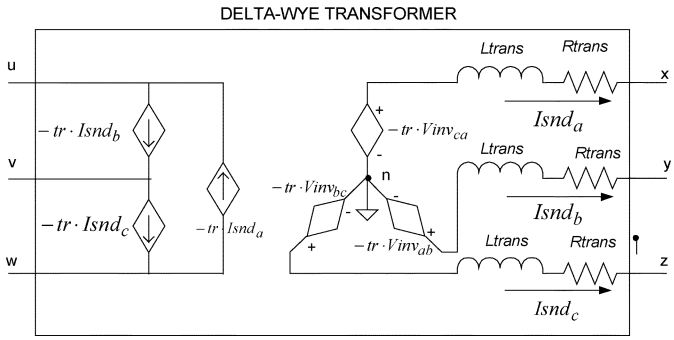

Fig. 2. Transformer model.

currents measured by the DSP system for control purposes are shown labeled in Fig. 1. The line-to-neutral load voltages (at points xyz-n in Fig. 1) are denoted as $Vload_{\rm an}$, $Vload_{\rm bn}$, and $Vload_{\rm cn}$, the load phase currents as $Iload_a$, $Iload_b$, and $Iload_c$, the line-to-line inverter filter capacitor voltages (at points uvw in Fig. 1) as $Vinv_{\rm ab}$, $Vinv_{\rm bc}$, and $Vinv_{\rm ca}$, the inverter phase currents as $Iinv_a$, $Iinv_b$, and $Iinv_c$.

For development of the control algorithm, a state space model of the system is needed. Each phase of the delta-wye transformer has been modeled as an ideal transformer with leakage inductance $Ltrans$ and series resistance $Rtrans$ on the secondary winding as shown in Fig. 2. The secondary transformer currents are denoted as $Isnd_a$, $Isnd_b$, and $Isnd_c$.

Using the transformer model in Fig. 2, the dynamic equations of the output filter circuit in Fig. 1 can be written as in

$$\frac{d\vec{V}inv_{\rm abc}}{dt} = \frac{1}{3\cdot C_{\rm inv}}\vec{I}inv_{\rm abc} - \frac{1}{3\cdot C_{inv}}Tr_i\cdot\vec{I}snd_{\rm abc} \quad (1a)$$

$$\frac{d\vec{I}inv_{\rm abc}}{dt} = \frac{1}{L_{\rm inv}}\vec{V}pwm_{\rm abc} - \frac{1}{L_{\rm inv}}\vec{V}inv_{\rm abc} \quad (1b)$$

$$\frac{d\vec{V}load_{\rm abc}}{dt} = \frac{1}{C_{\rm load}}\vec{I}snd_{\rm abc} - \frac{1}{C_{\rm load}}\vec{I}load_{\rm abc} \quad (1c)$$

$$\frac{d\vec{I}snd_{\rm abc}}{dt} = -\frac{R_{\rm trans}}{L_{\rm tran}}\vec{I}_{\rm snd} + \frac{1}{L_{\rm tran}}Tr_v \cdot \vec{V}inv_{\rm abc} - \frac{1}{L_{\rm tran}}\vec{V}load_{\rm abc} \quad (1d)$$

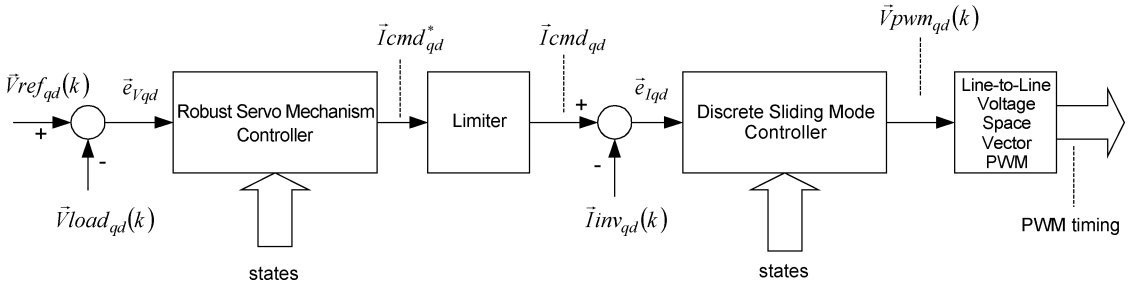

Fig. 3. Overall control system.

where the voltages and currents vectors are defined as in

$$\begin{aligned}
&\vec{V}inv_{\rm abc}\\
&\quad=[Vinv_{\rm ab}\quad Vinv_{\rm bc}\quad Vinv_{\rm ca}]^T\\
&\vec{V}load_{\rm abc}\\
&\quad=[Vload_a\quad Vload_b\quad Vload_c]^T\\
&\vec{I}load_{\rm abc}\\
&\quad=[Iload_a\quad Iload_b\quad Iload_c]^T\\
&\vec{I}snd_{\rm abc}\\
&\quad=[Isnd_a\quad Isnd_b\quad Isnd_c]^T\\
&\vec{I}inv_{\rm abc}\\
&\quad=[Iinv_{\rm ab}\quad Iinv_{\rm bc}\quad Iinv_{\rm ca}]^T\\
&\quad=[Iinv_a-Iinv_b\quad Iinv_b-Iinv_c\quad Iinv_c-Iinv_a]^T.
\end{aligned}\tag{2}$$

Matrices Tr_i and Tr_v in (1a) and (1d) denote the currents and voltages transformations of the delta-wye transformer. Denoting the transformer's turn ratio as tr, these matrices are given by

$$Tr_i = tr\cdot\begin{bmatrix}1 & -2 & 1\\ 1 & 1 & -2\\ -2 & 1 & 1\end{bmatrix},\quad Tr_v = tr\cdot\begin{bmatrix}0 & 0 & -1\\ -1 & 0 & 0\\ 0 & -1 & 0\end{bmatrix}.\tag{3}$$

To obtain a state space model of the system, the dynamic equations in (1) are transformed to the DQ0 stationary reference frame using the transformation

$$\vec{f}_{\rm qd0} = K_S\cdot\vec{f}_{\rm abc}\tag{4}$$

with

$$\begin{aligned}
K_S &= \frac{2}{3}\begin{bmatrix}1 & -0.5 & -0.5\\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}\\ 0.5 & 0.5 & 0.5\end{bmatrix}\\
f_{\rm qd0} &= [f_q,\ f_d,\ f_0]^T\\
f_{\rm abc} &= [f_a,\ f_b,\ f_c]^T
\end{aligned}$$

where $\vec{f}_{\rm abc}$ denotes the abc voltages and currents defined in (2), and $\vec{f}_{\rm qd0}$ the corresponding DQ0 stationary reference frame variables. The circuit dynamics can then be written as in

$$\begin{aligned}
\frac{d\vec{V}inv_{\rm qd}}{dt} &= \frac{1}{3\cdot C_{\rm inv}}\vec{I}inv_{\rm qd} - \frac{1}{3\cdot C_{\rm inv}}Tri_{\rm qd0}\\
&\quad\cdot\vec{I}snd_{\rm qd0}
\end{aligned}\tag{5a}$$

$$\frac{d\vec{I}inv_{\rm qd}}{dt} = \frac{1}{L_{\rm inv}}\vec{V}pwm_{\rm qd} - \frac{1}{L_{\rm inv}}\vec{V}inv_{\rm qd}\tag{5b}$$

$$\frac{d\vec{V}load_{\rm qd0}}{dt} = \frac{1}{C_{\rm load}}\vec{I}snd_{\rm qd0} - \frac{1}{C_{\rm load}}\vec{I}load_{\rm qd0}\tag{5c}$$

$$\begin{aligned}
\frac{d\vec{I}snd_{\rm qd0}}{dt} &= -\frac{R_{\rm tran}}{L_{\rm tran}}\bar{I}snd_{\rm qd0} + \frac{1}{L_{\rm tran}}Trv_{\rm qd}\\
&\quad\cdot\vec{V}inv_{\rm qd} - \frac{1}{L_{\rm tran}}\overline{V}load_{\rm qd0}
\end{aligned}\tag{5d}$$

where the matrices $Tri_{\rm qd0}$ and $Trv_{\rm qd}$ are defined as

$$\begin{aligned}
Tri_{\rm qd0} &= \left[K_s\cdot Tr_i\cdot K_S^{-1}\right]_{row\,1,2}\\
&= tr\cdot\frac{3}{2}\begin{bmatrix}1 & \sqrt{3} & 0\\ -\sqrt{3} & 1 & 0\end{bmatrix}
\end{aligned}\tag{6a}$$

$$\begin{aligned}
Trv_{\rm qd} &= \left[K_s\cdot Tr_v\cdot K_S^{-1}\right]_{col\,1,2}\\
&= tr\cdot\frac{1}{2}\begin{bmatrix}1 & -\sqrt{3}\\ \sqrt{3} & 1\\ 0 & 0\end{bmatrix}.
\end{aligned}\tag{6b}$$

Notice that, due to the three-wire system of the inverter and filter, the zero components of the inverter voltages ($\vec{V}\ inv_{\rm qd}$), the inverter currents ($\vec{I}inv_{\rm qd}$), and the input PWM voltages $\vec{V}\ pwm_{\rm qd}$ are trivial and they do not appear in (5).

III. Control System Development

To achieve fast current limiting capability for the inverter, the control strategy uses a two-loop control structure: an inner inverter currents loop and an outer load voltages loop as shown in Fig. 3. The outer loop regulates the load voltages ($\vec{V}\ load_{\rm qd}$) to follow 50/60-Hz balanced three-phase voltages references ($\vec{V}\quad ref_{\rm qd}$) and generates the inverter currents commands ($\vec{I}cmd_{\rm qd}$), which are limited. The inner loop in turn generates the PWM voltage commands to regulate the inverter currents to follow the inverter current command. A standard voltage space vector algorithm [21] is then used to realize these PWM command voltages. Notice that the zero-components of the load voltages are not regulated by the control, since it is uncontrollable.

Fig. 4 shows the timing diagram of the PWM gating signals generation in relation with the A/D sampling time of the DSP. It can be seen that there is a one-half PWM period delay between the time the signals are sampled by the A/D and the time the PWM control action is applied.

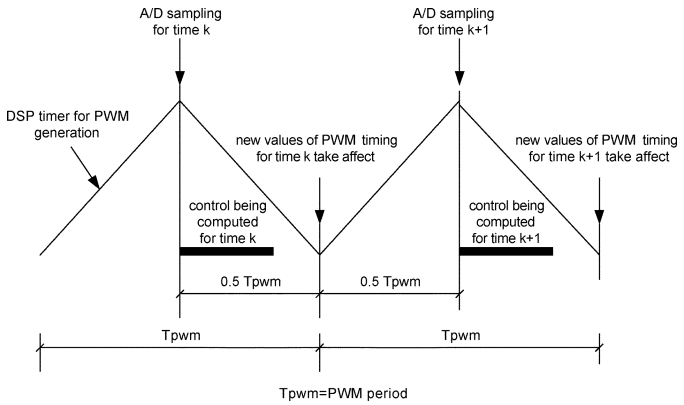

Fig. 4. Control timing diagram.

The next two subsections summarizes the development of the two control loops, the inner current loop using the discrete sliding mode controller and the voltage control loop using the robust servomechanism principles.

A. Discrete-Time Sliding Mode Current Controller

For designing the discrete time sliding mode current controller, consider the inverter and filter subsystem with no transformer and load dynamics

$$\frac{d\vec{V}inv_{\rm qd}}{dt} = \frac{1}{3\cdot C_{\rm inv}}\vec{I}inv_{\rm qd} - \frac{1}{3\cdot C_{\rm inv}}Tri_{\rm qd0} \cdot \vec{I}snd_{\rm qd0} \tag{7a}$$

$$\frac{d\vec{I}inv_{\rm qd}}{dt} = \frac{1}{L_{\rm inv}}\vec{V}pwm_{\rm qd} - \frac{1}{L_{\rm inv}}\vec{V}inv_{\rm qd}. \tag{7b}$$

Assuming the secondary transformer currents $\vec{I}snd_{\rm qd0}$ as disturbances, this subsystem can be written in state space form as

$$\begin{aligned}
\dot{\vec{x}}_1 &= A_1\vec{x}_1 + B_1\vec{u} + E_1\vec{d}_1 \\
\vec{A}_1 &= \begin{bmatrix} \vec{0}_{2\times2} & (3\cdot C_{\rm inv})^{-1}\cdot\vec{I}_{2\times2} \\ -(L_{\rm inv})^{-1}\cdot\vec{I}_{2\times2} & \vec{0}_{2\times2} \end{bmatrix} \\
\vec{B}_1 &= \begin{bmatrix} \vec{0}_{2\times2} \\ (L_{\rm inv})^{-1}\cdot\vec{I}_{2\times2} \end{bmatrix} \\
\vec{E}_1 &= \begin{bmatrix} -(3\cdot C_{\rm inv})^{-1}\cdot Tri_{\rm qd0} \\ \vec{0}_{2\times3} \end{bmatrix}
\end{aligned} \tag{8}$$

where the states are $\vec{x}_1 = [\vec{V}inv_{\rm qd}, \vec{I}inv_{\rm qd}]$, the inputs $\vec{u} = \vec{V}pwm_{\rm qd}$, and disturbances $\vec{d}_1 = \vec{I}snd_{\rm qd}$.

The discrete form of (8) can be calculated as

$$\vec{x}_1(k+1) = A_1^*\vec{x}_1(k) + B_1^*\vec{u}(k) + E_1^*\vec{d}_1(k)$$

where

$$\begin{aligned}
A_1^* &= \exp(A\cdot T_S) \\
B_1^* &= \int_0^{T_S} e^{A_1\cdot T_S}B_1 d\tau \\
E_1^* &= \int_0^{T_S} e^{A_1\cdot T_S}E_1 d\tau
\end{aligned}$$

and T_S is the A/D sampling time, which in this case is equal to the PWM period $T_{\rm pwm}$.

To force the inverter currents to follow their commands, the sliding mode surface is chosen as $\vec{s}(k) = C_1\cdot\vec{x}_1(k) - \vec{I}cmd(k)$ where $C_1\cdot\vec{x}_1(k) = \vec{I}inv_{\rm qd}(k)$, so that when discrete sliding mode occurs, we have $\vec{s}(k) = 0$ or $\vec{I}inv(k) = \vec{I}cmd(k)$. The existence of the discrete sliding mode can be guaranteed if the control is given [20]

$$u(k) = \begin{cases} \vec{u}_{\rm eq}(k), & \text{for } \|\vec{u}_{\rm eq}(k)\| \le u_0 \\ u_0\frac{\vec{u}_{\rm eq}(k)}{\|\vec{u}_{\rm eq}(k)\|}, & \text{for } \|\vec{u}_{\rm eq}(k)\| > u_0 \end{cases} \tag{9}$$

where the equivalent control input $\vec{u}_{\rm eq}(k)$ is calculated from

$$\vec{u}_{\rm eq}(k) = (C_1B_1^*)^{-1}\left(\vec{I}cmd_{\rm qd} - C_1A_1^*\vec{x}_1(k) - C_1E_1^*\vec{d}_1(k)\right) \tag{10}$$

and u_0 denotes the maximum value of the PWM voltage command realizable by the space vector algorithm.

Note that the secondary transformer currents are needed for the control, but these currents are not measured in the system (see Fig. 1). A linear Luenberger observer can be easily designed to estimate these currents for control purposes. However, in most practical cases we can approximate these currents with the load currents (i.e., $\vec{I}snd_{\rm qd} \approx \vec{I}load_{\rm qd}$) since the currents through the output capacitor filters are small. According to the authors' experience, the effect of using this approximation is unnoticeable in the control performance.

Due to the computation delay of the DSP, the control action given by (9) will result in undesirable overshoots during transients. This effect can be minimized, however, if the states $\vec{x}_1(k)$ and disturbances $\vec{d}_1(k)$ are replaced with their first order one-half step ahead predicted values given by

$$\begin{aligned}
\vec{x}_1^p(k) &= 1.5\cdot\vec{x}_1(k) - 0.5\cdot\vec{x}_1(k-1) \\
\vec{d}_1^p(k) &= 1.5\cdot\vec{d}_1(k) - 0.5\cdot\vec{d}_1(k-1).
\end{aligned} \tag{11}$$

Substituting $\vec{x}_1^p(k)$ and $\vec{d}_1^p(k)$ in (11) into $\vec{x}_1(k)$ and $\vec{d}_1(k)$ in (10), the equivalent control input $\vec{u}_{\rm eq}(k)$ then becomes

$$\vec{u}_{\rm eq}(k) = (C_1B_1^*)^{-1}\left(\vec{I}cmd_{\rm qd} - C_1A_1^*\vec{x}_1^p(k) - C_1E_1^*\vec{d}_1^p(k)\right). \tag{12}$$

B. Voltage Controller Design Using Discrete Perfect RSP

The voltage control loop designed in this paper is based on the discrete form of the technique developed in Davison [13]. To design the load voltages controller, let's first consider the entire plant system with the-0 components of the voltages and currents omitted as given in (13). As explained in Section II, these 0-components are completely decoupled and uncontrollable from the inputs, and therefore are not useful to be included in the design. In the system (13), an input delay of one-half the PWM period $(0.5T_{\rm pwm})$ has been explicitly included to account for the computation delay of the DSP, as seen in (13), shown at the bottom of the next page.

The states variables for the system (13) are chosen as $\vec{x}_p = [\vec{V}inv_{\rm qd}, \vec{I}inv_{\rm qd}, \vec{V}load_{\rm qd}, \vec{I}snd_{\rm qd}]$, with the inputs as $u = \vec{V}\ pwm_{\rm qd}$. System (13) can be transformed to a discrete-time system with sampling time $T_s = T_{\rm pwm}$ to yield

$$\vec{x}_p(k+1) = \Phi\cdot\vec{x}_p(k) + \Gamma_1\cdot\vec{u}(k-1) + \Gamma_2\cdot\vec{u}(k) \tag{14}$$

where

$$\Phi = e^{A_p T_S}, \quad \Gamma_1 = \int_{0.5T_S}^{T_S} e^{A_p \tau} B_p d\tau, \quad \Gamma_2 = \int_{0}^{0.5T_S} e^{A_p \tau} B_p d\tau.$$

Discrete time system (14) can be written in a standard discrete time state space equations by adding the extra states $\vec{x}_a(k) = \vec{u}(k-1) = \overrightarrow{V}\ pwm_{\rm qd}(k-1)$ to yield

$$\begin{bmatrix} \vec{x}_p(k+1) \\ \vec{x}_a(k+1) \end{bmatrix} = \begin{bmatrix} \Phi & \Gamma_1 \\ \vec{0}_{2\times 2} & \vec{0}_{2\times 2} \end{bmatrix} \cdot \begin{bmatrix} \vec{x}_p(k) \\ \vec{x}_a(k) \end{bmatrix} + \begin{bmatrix} \Gamma_2 \\ \vec{I}_{2\times 2} \end{bmatrix} \cdot \vec{u}(k) \tag{15}$$

so that the system can be written as

$$\vec{x}_p^*(k+1) = A_p^* \vec{x}_p^*(k) + B_p^* \vec{u}(k) \tag{16}$$

where

$$\vec{x}_p^*(k) = \begin{bmatrix} \vec{x}_p(k) \\ \vec{x}_a(k) \end{bmatrix}$$
$$A_p^* = \begin{bmatrix} \Phi & \Gamma_1 \\ \vec{0}_{2\times 2} & \vec{0}_{2\times 2} \end{bmatrix}$$
$$B_p^* = \begin{bmatrix} \Gamma_2 \\ \vec{I}_{2\times 2} \end{bmatrix}.$$

To design the voltage controller, we need to consider the true plant (16) and the discrete time sliding mode current controller as the equivalent "plant" as seen by the outer voltage loop. Using (10) and (16) the augmented true plant and discrete sliding mode current controller can be found as in

$$\vec{x}_p^*(k+1) = A_d \vec{x}_p^*(k) + B_d \vec{u}_1(k) \tag{17}$$

with $\vec{u}_1(k) = \vec{I}cmd_{\rm qd}^*(k)$, and

$$A_d = A_p^* - B_p^* (C_1 B_1^*)^{-1} (B_1^* C_{11} + E_1^* C_{12})$$
$$B_d = B_p^* (C_1 B_1^*)^{-1}$$
$$C_{11} = \begin{bmatrix} \vec{I}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} \\ \vec{0}_{2\times 2} & \vec{I}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} \end{bmatrix}$$
$$C_{12} = [\vec{0}_{2\times 2} \quad \vec{0}_{2\times 2} \quad \vec{0}_{2\times 2} \quad \vec{I}_{2\times 2} \quad \vec{0}_{2\times 2}].$$

Note that the augmented system given in (17) was found assuming the approximation $\vec{I}snd_{\rm qd} \approx \vec{I}load_{\rm qd}$ has been used.

Now, assume $\omega_i = 2\pi f_i\ i = 1, 2, \ldots n$ are frequencies of the reference voltages and harmonics to be eliminated. For a 60-Hz DGS system with desire to eliminate third, fifth, and seventh harmonics, for example, we use $\omega_1 = 2\pi \cdot 60$, $\omega_2 = 2\pi \cdot 3 \cdot 60$, $\omega_3 = 2\pi \cdot 5 \cdot 60$, and $\omega_4 = 2\pi \cdot 7 \cdot 60$. We can then choose the servo-compensator to be

$$\dot{\vec{\eta}} = A_c \vec{\eta} + B_c e_{\rm Vqd}$$
$$\vec{e}_{\rm Vqd} = \vec{V}ref_{\rm qd} - \vec{V}load_{\rm qd} \tag{18}$$

where

$$\vec{\eta} = [\vec{\eta}_1, \vec{\eta}_2, \cdots \vec{\eta}_n]^T \quad \vec{\eta}_i \in R^4, \quad i = 1, 2, \ldots n$$
$$A_c = \text{block diag}\,[Ac_1, Ac_2, \cdots, Ac_n]$$
$$B_c = [Bc_1, Bc_2, \cdots, Bc_n]^T$$

with

$$Ac_i = \begin{pmatrix} \vec{0}_{2\times 2} & \vec{I}_{2\times 2} \\ -\omega_i^2 \vec{I}_{2\times 2} & \vec{0}_{2\times 2} \end{pmatrix}, \quad i = 1, 2, \ldots n$$
$$Bc_i = (\vec{0}_{2\times 2} \quad \vec{I}_{2\times 2})^T \quad i = 1, 2, \ldots n.$$

Note that each of the blocks $\dot{\vec{\eta}}_i = Ac_1 \vec{\eta}_i + Bc_i \vec{e}_{\rm Vqd}$ represents a state space implementation of the continuous transfer function $1/(s^2 + \omega_i^2)$ for each of the qd-axis voltages errors.

The servo compensator (18) can be transformed to a discrete time system to yield

$$\vec{\eta}(k+1) = A_c^* \vec{\eta}(k) + B_c^* \vec{e}_{Vqd}(k)$$
$$\vec{e}_{\rm Vqd}(k) = \vec{V}ref_{\rm qd}(k) - \vec{V}load_{\rm qd}(k) \tag{19}$$

where

$$A_c^* = \exp(A_c \cdot T_S) \quad B_c^* = \int_0^{T_S} e^{A_1 \cdot (T_S - \tau)} B_c d\tau.$$

In the perfect robust servomechanism control [13], the controller uses linear state-feedback of the "plant" states $x_p^*(k)$ and servo compensator states $\eta(k)$ to form the controller input $\vec{I}cmd_{\rm qd}^*(k)$

$$\vec{u}_1(k) = \vec{I}cmd_{\rm qd}^*(k) = K_0 x_p^*(k) + K_1 \eta(k). \tag{20}$$

The gains $K = [K_0 \quad K_1]$ are then found by minimizing the discrete performance index

$$J_\varepsilon = \sum_{k=0}^{\infty} (z(k)' z(k) + \varepsilon \cdot u(k)' u(k))$$
$$z = \begin{bmatrix} x_p^* \\ \eta \end{bmatrix} \tag{21}$$

$$\dot{x}_p(t) = A_p \vec{x}_p(t) + B_p \vec{u}(t - 0.5T_{\rm pwm})$$
$$\vec{A}_p = \begin{bmatrix} \vec{0}_{2\times 2} & (3 \cdot C_{\rm inv})^{-1} \cdot \vec{I}_{2\times 2} & \vec{0}_{2\times 2} & -(3 \cdot C_{\rm inv})^{-1} \cdot \hat{T}ri_{\rm qd} \\ -(L_{\rm inv})^{-1} \cdot \vec{I}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} \\ \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & \vec{0}_{2\times 2} & (C_{\rm load})^{-1} \cdot \vec{I}_{2\times 2} \\ (L_{\rm inv})^{-1} \cdot \hat{T}rv_{\rm qd} & \vec{0}_{2\times 2} & -(L_{\rm inv})^{-1} \cdot \vec{I}_{2\times 2} & -R_{\rm trans}(L_{\rm trans})^{-1} \cdot \vec{I}_{2\times 2} \end{bmatrix}$$
$$\vec{B}_p = \begin{bmatrix} \vec{0}_{2\times 2} \\ (L_{\rm inv})^{-1} \cdot \vec{I}_{2\times 2} \\ \vec{0}_{2\times 2} \\ \vec{0}_{2\times 2} \end{bmatrix}, \quad \hat{T}ri_{\rm qd} = tr \cdot \frac{3}{2} \begin{bmatrix} 1 & \sqrt{3} \\ -\sqrt{3} & 1 \end{bmatrix} \quad \hat{T}rv_{\rm qd} = tr \cdot \frac{1}{2} \begin{bmatrix} 1 & -\sqrt{3} \\ \sqrt{3} & 1 \end{bmatrix} \tag{13}$$

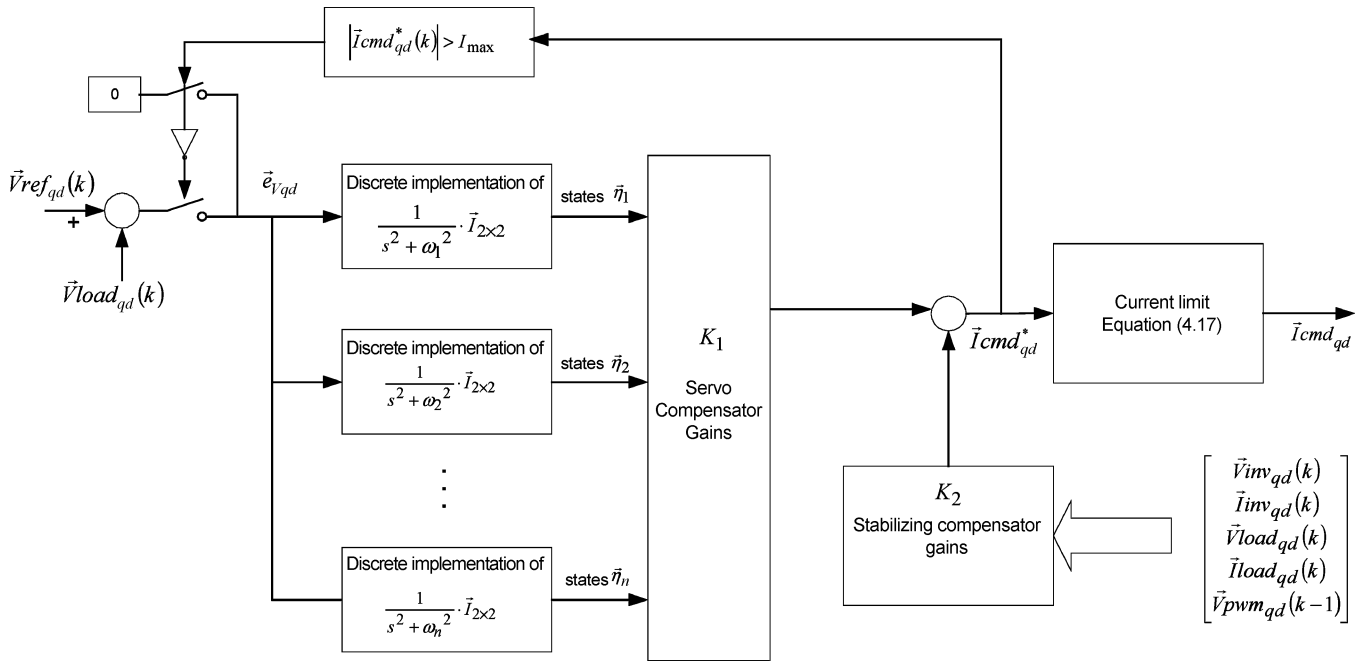

Fig. 5. Output voltages controller using robust servomechanism controller.

for the augmented "equivalent plant" (17) and the servo compensator (19)

$$\begin{bmatrix} \vec{x}_p^*(k+1) \\ \eta(k+1) \end{bmatrix} = \begin{bmatrix} A_d & 0 \\ -B_c^*C & A_c^* \end{bmatrix} \begin{bmatrix} \vec{x}_p^*(k) \\ \eta(k) \end{bmatrix} + \begin{bmatrix} B_d \\ -B_c^*D \end{bmatrix} u_1(k) \tag{22}$$

where $\varepsilon > 0$ is an arbitrarily small scalar. Solutions of (21) and (22) can be found easily using Matlab command *dlqr*.

Current Limit and Control Saturation Handling: The current command $\vec{I}cmd^*_{\rm qd}(k)$ generated by the robust servomechanism voltage controller above is limited in magnitude as in (23) to yield the current command $\vec{I}cmd_{\rm qd}(k)$, which will be implemented by the inner loop current controller

$$\vec{I}cmd_{\rm qd}(k) = \begin{cases} \vec{I}cmd^*_{\rm qd}(k), & \text{if } \left|\vec{I}cmd^*_{\rm qd}(k)\right| \le I_{\max} \\ \dfrac{\vec{I}cmd^*_{\rm qd}(k)}{\left|\vec{I}cmd^*_{\rm qd}(k)\right|} I_{\max}, & \text{if } \left|\vec{I}cmd^*_{\rm qd}(k)\right| > I_{\max}. \end{cases} \tag{23}$$

$I_{\max}$ represents the maximum allowable magnitude of the inverter currents. Equation (23) limits the magnitude of the current commands but maintains their vector directions in the qd-space.

The states $\vec{\eta}_i$ of the servo-compensator can be seen as sine wave signal generators that get excited by the harmonic contents of the error signals at frequency ω_i. When the control inputs of the robust servomechanism voltage controller saturate, i.e., $|\vec{I}cmd^*_{\rm qd}(k)| > I_{\max}$ the servo-compensator states will grow in magnitude due to the break in the control loop. This problem is similar to the integrator windup problem that occurs in an integral type controller. To prevent this, the servo-compensator in (19) can be modified as

$$\begin{aligned} \vec{\eta}(k+1) &= A_c^*\vec{\eta}(k) + B_c^*\vec{e}_1(k) \\ \vec{e}_1(k) &= \begin{cases} \vec{e}_{\rm Vqd}(k), & \text{if } \left|\vec{I}cmd^*_{\rm qd}\right| \le I_{\max} \\ 0, & \text{if } \left|\vec{I}cmd^*_{\rm qd}\right| > I_{\max}. \end{cases} \end{aligned} \tag{24}$$

TABLE I
SYSTEM PARAMETERS

DC Bus Voltages	
Vdc	*540 V* (nom.) 390V (min)
AC Output voltage	
Vload	208V(LL-RMS), 120V(LN)
f	60 *Hz*
Inverter filters	
C_{inv}	540 μF
L_{inv}	300 μH
Delta-Wye Transformer	
	245V:208V, 60Hz
L_{trans}	48 μH ($\approx$ 0.03 p.u)
R_{trans}	0.02 ohm
Output filter	
C_{grass}	90 μF

Using (24), during the current limit saturation, the servo compensator states will continue to oscillate at the harmonic frequency with constant magnitude. The resulting robust servomechanism controller structure is shown in Fig. 5.

IV. EXPERIMENTAL RESULTS

The effectiveness the proposed control strategy has been verified on an 80-kVA DGS unit with system parameters shown in Table I. The dc bus voltage is obtained from a six-pulse thyristor controlled rectifier in parallel with a 480-V battery system. The DSP control system used is based on the TMS320F240 fixed point DSP with control timing diagram as given in Fig. 5. The PWM timing is calculated through a standard space vector PWM [21] with switching frequency of 3.2 kHz ($T_{\rm pwm} = T_s = 320\ \mu$s). The experimental results presented in this paper have been obtained using the proposed control strategy with only the third, the fifth, and seventh harmonics being eliminated.

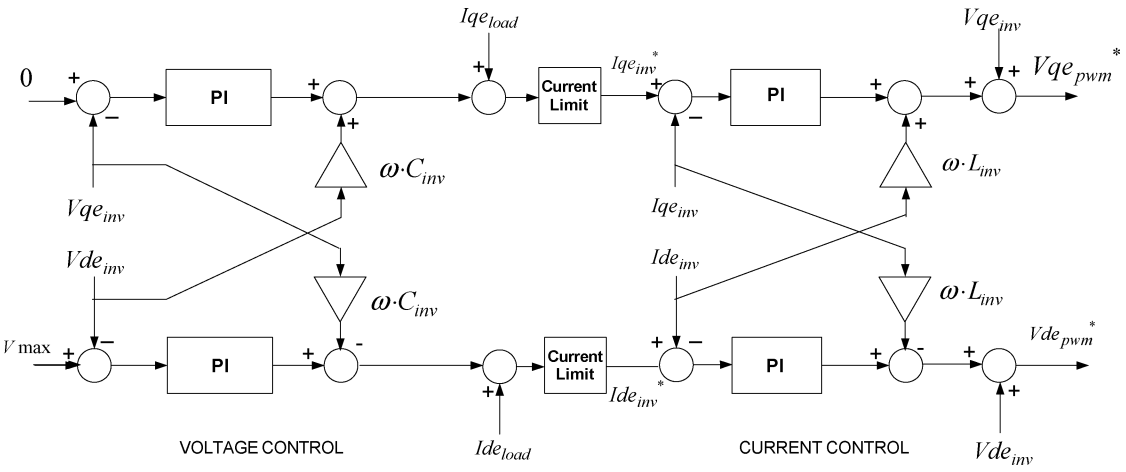

Fig. 6. Synchronous reference frame voltage and current control with PI controllers.

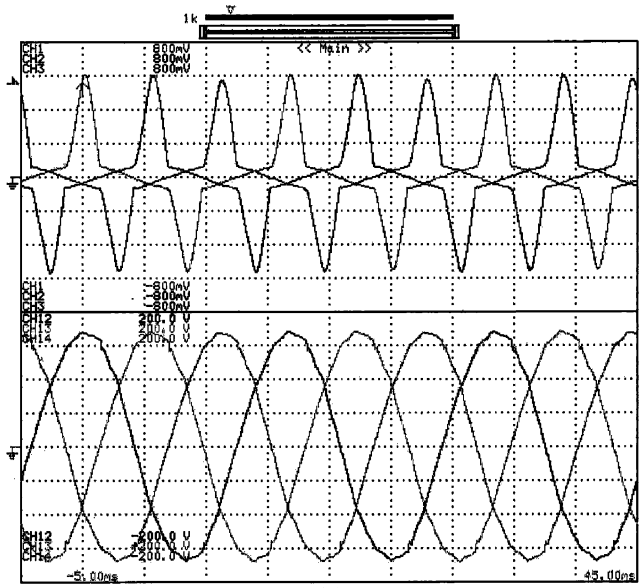

Fig. 7. steady-state performance comparisons under nonliner load (a) using proposed control and (b) PI controllers. Top: three phase load currents. Bottom: three-phase load voltages.

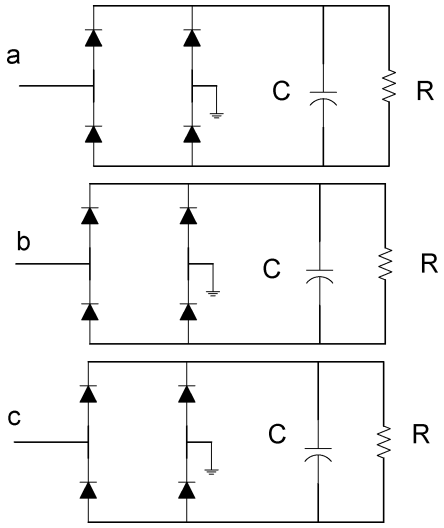

Fig. 8. Three single-phase diode rectifier as nonlinear loads.

Comparison With Synchronous Reference Frame Control With PI Controllers: It is instructive to compare the proposed control with commonly used PI controllers. To provide a fair comparison, the PI controls should preferably be performed in synchronous reference frame where perfect sinusoidal quantities will appear as dc quantities. Note that it is not necessary for the proposed control to be performed in the synchronous frame, since the proposed control can guarantee zero steady-state error for signals varying at fundamental frequency. Fig. 6 shows the synchronous reference frame control of the voltages and currents using the PI controllers. In this figure, the voltages and currents are expressed in the synchronous reference frame using transformation

$$f_{\mathrm{qe}} = f_{\mathrm{qs}} \cdot \cos \omega t - f_{\mathrm{ds}} \cdot \sin \omega t$$
$$f_{\mathrm{ds}} = f_{\mathrm{qs}} \cdot \sin \omega t + f_{\mathrm{ds}} \cdot \cos \omega t \tag{25}$$

where the qs and ds subscripts denote variables in the stationary reference frame, the qe and de denote the synchronous reference frame variables, and ωt represent the phase angle of the voltages references. Given three-phase balanced voltages references, it can be shown using (25) that the de and qe references

TABLE II
OUTPUT VOLTAGES REGULATION

TYPE OF LOAD	% Reg	N LD OUTPUT V			AVG	F LD OUTPUT V			AVG
V REG (100% RES LD)	0.031	120.23	120.07	120.16	120.15	120.17	120.03	120.15	120.12
V REG (100%, 0.8PF LD)	0.033	120.23	120.07	120.16	120.15	120.20	120.00	120.14	120.11
V REG (100%, 2.75:1CF LD)	0.019	120.23	120.07	120.16	120.15	120.14	120.11	120.14	120.13
V REG, 100% UNBAL RES LD (A)	0.019	120.23	120.07	120.16	120.15	120.59	119.59	120.21	120.13
V REG, 100% UNBAL RES LD (A&B)	0.028	120.23	120.07	120.16	120.15	120.67	119.97	119.72	120.12
		540VDC, OUTPUT V			AVG	390VDC, OUTPUT V			AVG
V REG, 100% RES LD ON BATT. @ 390VDC	-0.089	120.17	120.03	120.15	120.12	120.26	120.12	120.29	120.22

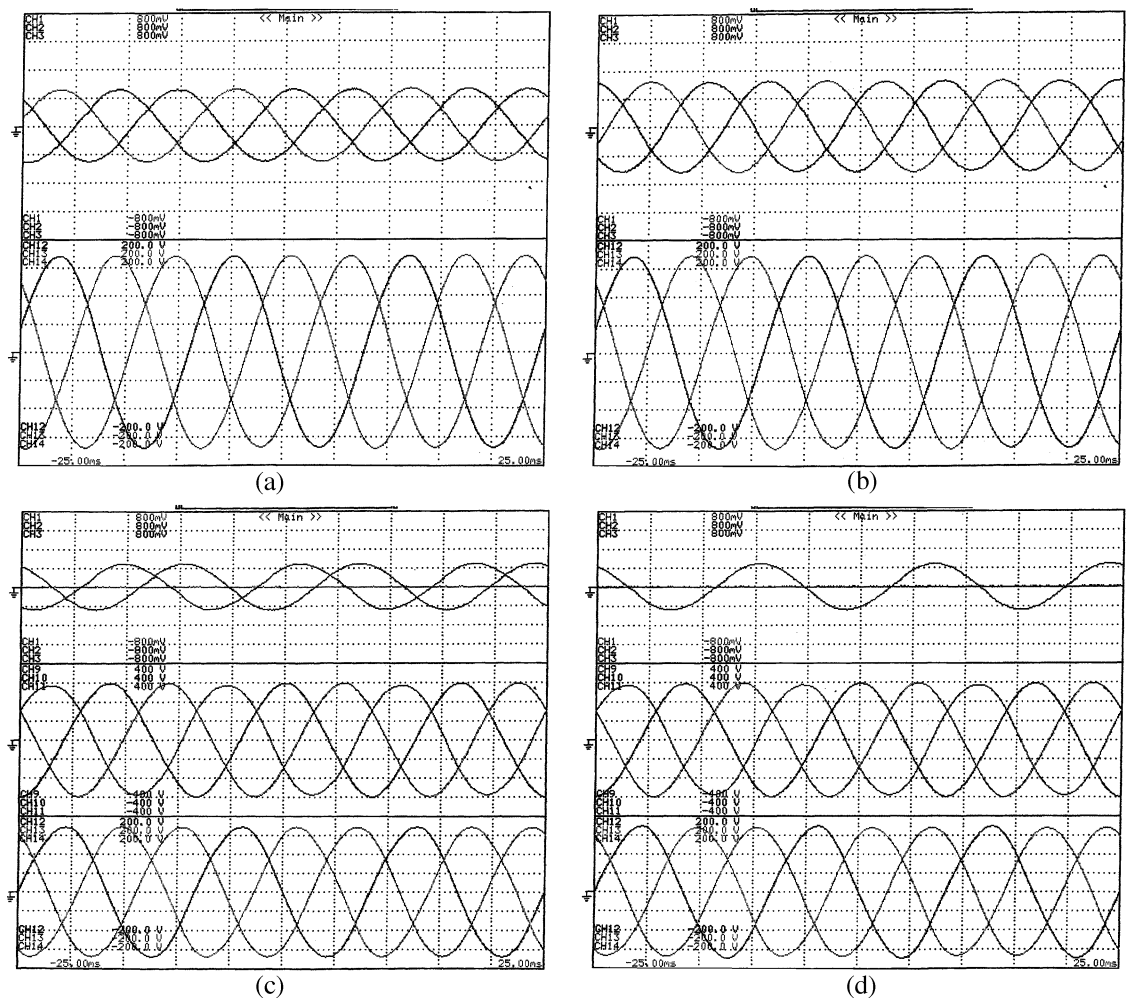

Fig. 9. Steady-state linear load: (a) 100% resistive balanced, (b) 100% 0.8 pf load, (c) 100% resistive unbalanced (phase A unloaded), and (d) 100% resistive unbalanced (phase A&B). Top: load currents; middle: load voltages; bottom: inverter voltages.

voltages in the synchronous reference frame are given by the maximum value of the reference voltage $Vmax$ and 0 respectively as shown in Fig. 6. The control shown in Fig. 6 also includes decoupling terms [11] that are used to compensate for the coupling of the d and q dynamics due to transformation (25), and feed forward terms used to improve transient performance.

It is worth noting that, if properly tuned, the control given in Fig. 6 can easily provide a good transient response for sudden load changes. Also, based on the internal model principle [14], since the PI controller includes an integral term $(1/s)$, the controller guarantees zero steady-state error for references and disturbances at zero frequency in synchronous reference frame, which in turn correspond to fundamental frequency references and disturbances in abc reference frame. Therefore, it is expected that the control in Fig. 6 would have a good steady-state voltage regulation and low THD voltage when only linear bal-

TABLE III
OUTPUT VOLTAGES THD

TYPES OF LOAD	Output voltages THD
No load	0.90%
100% balanced resistive load	1.30%
100% 0.8 pf load	1.32%
100% unbal. resistive (ph.A)	1.70%
100% unbal. resistive (ph.A&B)	1.89%
Crest load (3:1)	2.7%

anced loads are applied. However, when disturbances other than the zero frequency (in synchronous reference frame) exist, then the PI controller can no longer guarantee a perfect regulation at steady-state. Note that, even though unbalanced linear loads in *abc* reference frame (or stationary reference frame) vary at fundamental frequency, in synchronous reference frame they appear as signals varying at frequency other than zero as apparent from transformation (25). Therefore, the PI controllers shown in Fig. 6 would not yield satisfactory steady performance for nonlinear harmonics and unbalanced nonlinear and linear loads.

Fig. 7 shows experimental results showing the steady-state performances comparison between the proposed control and the control shown in Fig. 6 under 100% nonlinear load condition. Both controls are updated at the same control rate equal to the 3.2-kHz PWM switching frequency. The nonlinear load applied consists of three single-phase diode rectifiers with RC load as shown in Fig. 8 with small amount of linear load added to obtain 100% rated power. It can be seen that the proposed control yields output voltages with significantly lower THD than the PI controllers, which confirms the arguments of the preceding paragraph.

Other Performance Measures of the Proposed Control: Table II gives the steady-state RMS output voltages regulation under different types of loads. It can be seen that the control strategy provides good output voltages regulation in all cases. Note that, the deviations in the output voltages for unbalanced load are due to the uncontrollable zero-component of the load currents. However, as can be seen the effect is minimal showing the effectiveness of the LC filter at the output side of the transformer.

Fig. 9 shows the waveforms of the load currents, load voltages, and inverter voltages under various linear loads: resistive, inductive, balanced, and unbalanced load. Table III summarizes the output voltages THD under different types of loads showing the superior THD performance of the proposed control strategy. Better results may be obtained by including more harmonics to be eliminated into the robust servomechanism controller.

Figs. 10 and 11 show the responses of the load voltages on resistive load transients, zero–100% and 100%–zero, respectively. It can be seen that the load voltages recover within less than a cycle after the load is applied. Even though in both cases the output voltages exhibit slight overshoot due to the underdamped nature of the control, the output voltages magnitudes deviate less than 5% of the nominal. These results show that the perfect RSP controller provides fast transient recovery under load transients with minimal overshoot in the response.

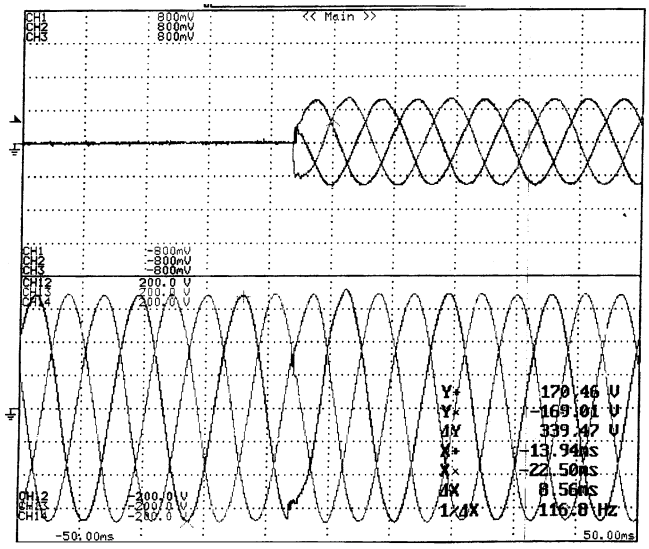

Fig. 10. Resistive load transient: 0% to 100%. Top: three-phase load currents, bottom: three-phase load voltages resistive load transient.

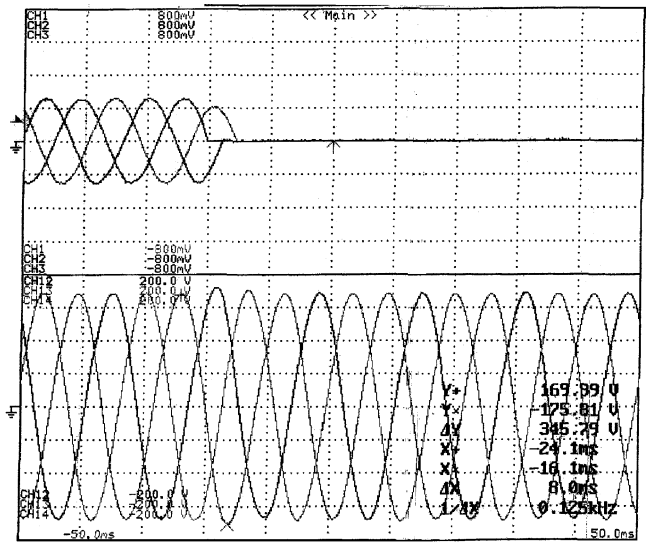

Fig. 11. Resistive load transient: 100% to 0% top: three-phase load currents, bottom: three-phase load voltages resistive load transient.

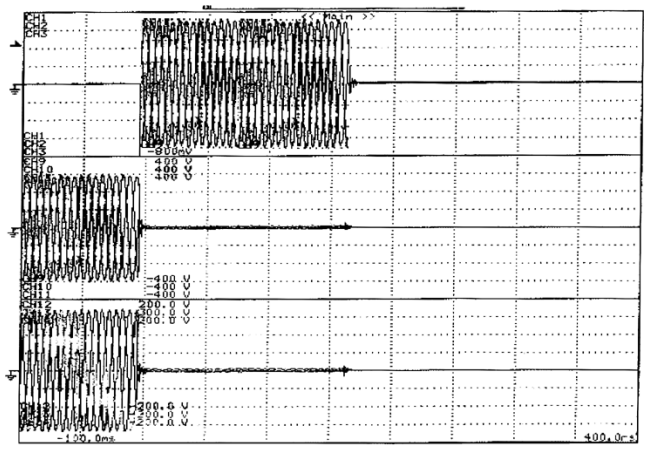

Fig. 12. Three-phase short-circuits on output terminals. Top: inverter currents, middle: load voltages, and bottom: inverter voltages.

Finally, the effectiveness of the current controller was verified by applying a sudden three-phase short circuit on the output load terminals. The current limit was set at 300% level, and the inverter was shutdown deliberately after ten cycles of short circuit condition. The results are shown in Fig. 12. It can be seen that the discrete sliding mode controller provides a fast and minimal overshoot on the inverter currents.

V. Conclusion

This paper has outlined the development of a digital control strategy for three-phase PWM inverters used in DGS applications. The control strategy combines the perfect RSP controller for low THD output voltages regulation and the discrete sliding mode current controller for fast over-current protection. The voltage controller was developed by including the dynamic of the current controller into the plant with the computation delay of the DSP accounted for. It was shown that by including the harmonic frequency mode to be eliminated into the perfect RSP controller, superior low THD performance could be achieved without sacrificing the transient recovery performance of the output voltages. The experimental results presented verified the effectiveness of the proposed control strategy both in providing low THD output voltages regulations and in providing protection under short circuit condition.

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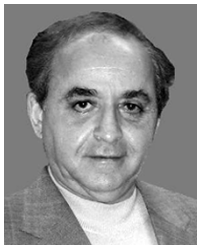

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