AIP Advances

Control of O-H bonds at a-IGZO/SiO_2 interface by long time thermal annealing for highly stable oxide TFT

Cite as: AIP Advances **7**, 125110 (2017); https://doi.org/10.1063/1.5008435
Submitted: 06 October 2017 • Accepted: 01 December 2017 • Published Online: 12 December 2017

Jae Kwon Jeon, Jae Gwang Um, Suhui Lee, et al.

ARTICLES YOU MAY BE INTERESTED IN

Heavily doped n-type a-IGZO by F plasma treatment and its thermal stability up to 600°C
Applied Physics Letters **112**, 162104 (2018); https://doi.org/10.1063/1.5007191

Hydrogen anion and subgap states in amorphous In–Ga–Zn–O thin films for TFT applications
Applied Physics Letters **110**, 232105 (2017); https://doi.org/10.1063/1.4985627

Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors
Applied Physics Letters **99**, 093507 (2011); https://doi.org/10.1063/1.3633100

AIP Publishing

AIP Advances
Mathematical Physics Collection
READ NOW

© 2017 Author(s).

AIP ADVANCES 7, 125110 (2017)

Control of O-H bonds at a-IGZO/SiO_2 interface by long time thermal annealing for highly stable oxide TFT

Jae Kwon Jeon, Jae Gwang Um, Suhui Lee, and Jin Jang[a]
Advanced Display Research Center (ADRC), Department of Information Display, Kyung Hee University, 26, Kyungheedae-ro, Dongdaemun-gu, Seoul 02447, Korea

(Received 6 October 2017; accepted 1 December 2017; published online 12 December 2017)

We report two-step annealing, high temperature and sequent low temperature, for amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT) to improve its stability and device performance. The annealing is carried out at 300 °C in N_2 ambient for 1 h (1st step annealing) and then at 250 °C in vacuum for 10 h (2nd step annealing). It is found that the threshold voltage (V_{TH}) changes from 0.4 V to -2.0 V by the 1st step annealing and to +0.6 V by 2nd step annealing. The mobility changes from 18 $cm^2V^{-1}s^{-1}$ to 25 $cm^2V^{-1}s^{-1}$ by 1st step and decreases to 20 $cm^2V^{-1}s^{-1}$ by 2nd step annealing. The V_{TH} shift by positive bias temperature stress (PBTS) is 3.7 V for the as-prepared TFT, and 1.7 V for the 1st step annealed TFT, and 1.3 V for the 2nd step annealed TFT. The XPS (X-ray photoelectron spectroscopy) depth analysis indicates that the reduction in O-H bonds at the top interface (SiO_2/a-IGZO) by 2nd step annealing appears, which is related to the positive V_{TH} shift and smaller V_{TH} shift by PBTS. © *2017 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* https://doi.org/10.1063/1.5008435

Amorphous oxide semiconductor (AOS) is getting more attention for its TFT application for displays. The amorphous indium-gallium-zinc oxide (a-IGZO) is the most popular AOS used for thin-film transistor (TFT) of active-matrix displays because of its advantages such as relatively high field-effect mobility (> 10 $cm^2V^{-1}s^{-1}$), low threshold voltage (< 1 V), low subthreshold swing (< 0.3 $Vdec^{-1}$), low-temperature process (< 200 °C) and optical transparency in visible region. Therefore, a-IGZO TFTs are being used for liquid-crystal display (LCD) and organic light-emitting diode (OLED) displays.[1–5] However, there are still many issues related to the control of threshold voltage and bias-induced degradation.[6–11] Therefore, there have been many studies on improving AOS TFT stability such as high-pressure oxygen annealing,[12] annealing in hydrogen environment,[13] O_2 plasma treatment,[14] suitable passivation materials,[15] long channel TFT[16] and long-time annealing, etc.[17]

Especially, the performance of a-IGZO TFT depends on channel length, and the TFTs with channel length less than 2 µm exhibit mostly depletion mode behavior.[18,19] Hence, the annealing technique to make the transfer shift to the positive gate voltage (V_G) is significant. However, it is also found that the threshold voltage (V_{TH}) of oxide TFT usually shifts to negative V_G by high-temperature annealing (> 300 °C).[20] Therefore, there are lots of studies on bias stability using relatively long channel TFTs (> 6 µm) under the NBIS (negative bias illumination stress) or PBTS (positive bias temperature stress) because the device with short channel length can be more easily affected by the electrical stress under the PBTS or NBTS (negative bias temperature stress).[16] Note that most of the oxide TFTs studied for improving stability have channel length longer than (> 6 µm) a-IGZO TFTs.

In this letter we studied the improvement of device performance and stability for relatively short channel (channel width/length = 20/4 µm) TFTs by introducing two-step annealing; 1st step is

[a]Author to whom correspondence should be addressed. Electronic mail: jjang@khu.ac.kr.

 © Author(s) 2017

annealing at 300 °C for 1 h in N_2 ambient, and 2nd step is annealing at 250 °C for 10 h in vacuum. Here we found that the device performance and bias-stability can be improved by 1st and subsequent 2nd step annealing. By XPS (X-ray photoelectron spectroscopy) depth analysis, it is found that O-H concentration at the top SiO_2/a-IGZO interface could be reduced significantly by 2nd step annealing. It is noted that the O-H bonds at the SiO_2/a-IGZO interface affect the device performance and stabilities.[15,21]

The a-IGZO TFT used in this study is a bottom gate, back-channel etched (BCE) structure as shown in Fig. 1(a), cross-sectional view, and (b) optical image. The fabrication process of the BCE TFTs appears elsewhere.[22] On glass substrate, 100 nm molybdenum (Mo) layer was deposited by DC sputtering and patterned as gate electrode. A bilayer of 100 nm SiN_x and 150 nm SiO_2 was deposited through plasma enhanced chemical vapor deposition (PECVD) as a gate insulator, followed by deposition of an a-IGZO by sputtering. Note that the gate dielectric and active layer were deposited in a cluster deposition system and thus impurity contamination could be reduced, supporting the device reproducibility. Following the active layer deposition and patterning, a 150 nm Mo layer was deposited and patterned to form source/drain (S/D) electrodes. Then, 300 nm SiO_2 layer was deposited by PECVD as a passivation layer. Finally, the post fabrication annealing was carried out at 250 °C in vacuum for 4 h. The channel width and length of the TFTs studied in this work are 20 μm and 4 μm respectively. The post-fabrication annealing for the TFT for 4h at 250 °C is called "as-fabricated" TFT. Note that this annealing step is a forming process because the TFT performance can be reproducible by this process.

To investigate the change in TFT performance by the annealing step, it was measured after 1st step annealing and then again after 2nd step annealing. All transfer curves are plotted at a drain voltage (V_{DS}) of 0.1 V. The threshold voltage (V_{TH}) is defined as the gate voltage giving drain current of I_{DS} = W/L x 10^{-11} (A), subthreshold swing (SS) is obtained from (d log (I_{DS})/d V_{GS})$^{-1}$ of the range 0.1 pA ≤ I_{DS} ≤ 10 pA with V_{DS} = 0.1 V and linear mobility (μ_{Lin}) from trans-conductance (g_M) $\partial I_{DS}/\partial V_{GS}$ at V_{GS} = 20 V and V_{DS} = 0.1 V.

The performance of "as-fabricated" TFT shown in Fig. 2 indicates that the V_{TH}, SS and μ_{Lin} are 0.4 V, 0.32 Vdec^{-1}, and 18 cm^{2}V^{-1}s^{-1}, respectively. It is found that the transfer curve shifts to negative V_{GS} direction, which makes mobility increases after 1st step annealing, resulting in V_{TH} shifts from 0.4 V to -2 V and μ_{Lin} from 18 cm^{2}V^{-1}s^{-1} to 25 cm^{2}V^{-1}s^{-1}. On the other hand, after the 2nd step annealing, the transfer curve shifts to the positive V_{GS} direction and V_{TH} shifts from -2.0 V to 0.6 V.

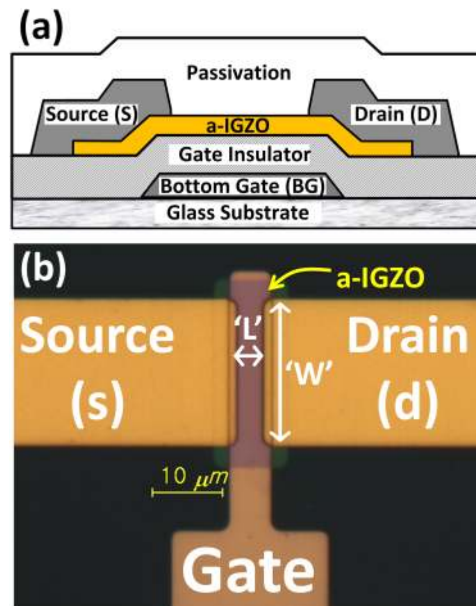

FIG. 1. The back channel etched (BCE) a-IGZO TFT fabricated for this work. (a) A cross-sectional view of a-IGZO TFT and (b) optical image of a-IGZO TFT. TFT channel width/length is 20 μm/4 μm.

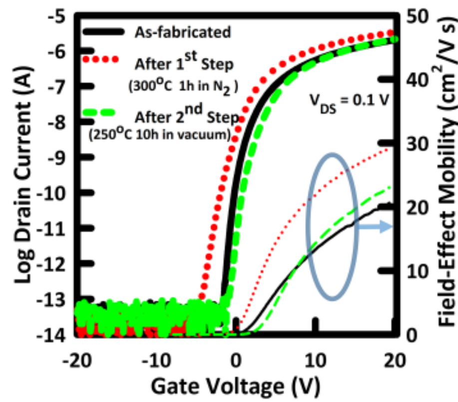

FIG. 2. Representative transfer characteristics of the a-IGZO TFTs according to annealing conditions; as-fabricated, 1st step annealing (300 °C in N_2 ambient for 1 h) and 2nd step annealing (250 °C in vacuum for 10 h).

The SS of the as-fabricated TFT is 0.32 $Vdec^{-1}$, and it changes to 0.60 $Vdec^{-1}$ by 1st step annealing, and 0.43 $Vdec^{-1}$ after 2nd step annealing.

The average value and standard deviation of the TFT parameters are shown in Fig. 3, obtained from the 10 TFTs fabricated simultaneously. The changes in V_{TH}, SS, linear mobility and saturation mobility are shown in (a), (b), (c) and (d), respectively. The V_{TH} shifts to the negative gate voltage by 1st step annealing.[16] On the other hand, 2nd step annealing makes the transfer shift back to the positive V_{GS} direction and thus TFT shows accumulation mode behavior, which is better for the application to gate driver.[5] Given that higher temperature (300 °C) for shorter annealing time might be attributed to the wider TFT parameter deviation after 1st step annealing. To investigate the stability of the TFTs, PBTS at 60 °C was measured by applying gate bias of +20 V with source/drain electrodes grounded. The evolution of transfer curves of the as-deposited TFT according to PBTS time exhibits

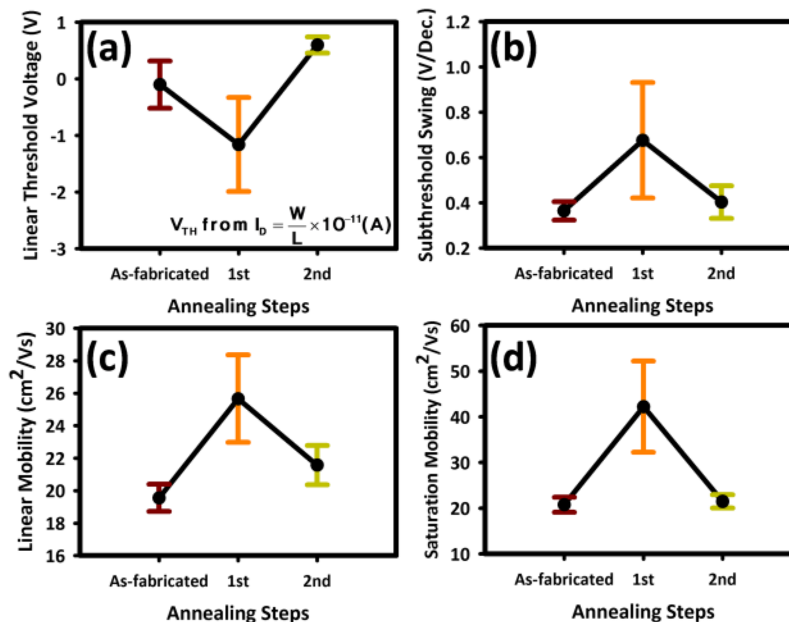

FIG. 3. Summary for the a-IGZO TFT parameters according to annealing step. (a) Constant current threshold voltage extracted at I_{DS} =W/L X 10^{-11} (A), (b) subthreshold swing ($Vdec^{-1}$), (c) linear mobility ($cm^2V^{-1}s^{-1}$) and (d) saturation mobility ($cm^2V^{-1}s^{-1}$) from the square root plot of drain currents for the 10 TFTs fabricated at the same preparation conditions.

significant shift toward positive V_{GS} direction, resulting in ΔV_{TH} of 3.6 V as shown in Fig. 4(a). The positive shift is due to the electron trapping at the gate insulator/active interface. The TFT after the 1st step annealing exhibits ΔV_{TH} of 1.7 V as shown in Fig. 4(b). Therefore, the PBTS stability can be improved by the 1st step annealing at 300 °C. Moreover, after the 2nd step annealing at 250 °C, the PBTS shows ΔV_{TH} of 1.3 V as shown in Fig. 4(c). The turn-on voltage shifts to the positive V_{GS} direction by 1.3 V. These results are beneficial to design the gate drivers because of its accumulation mode.

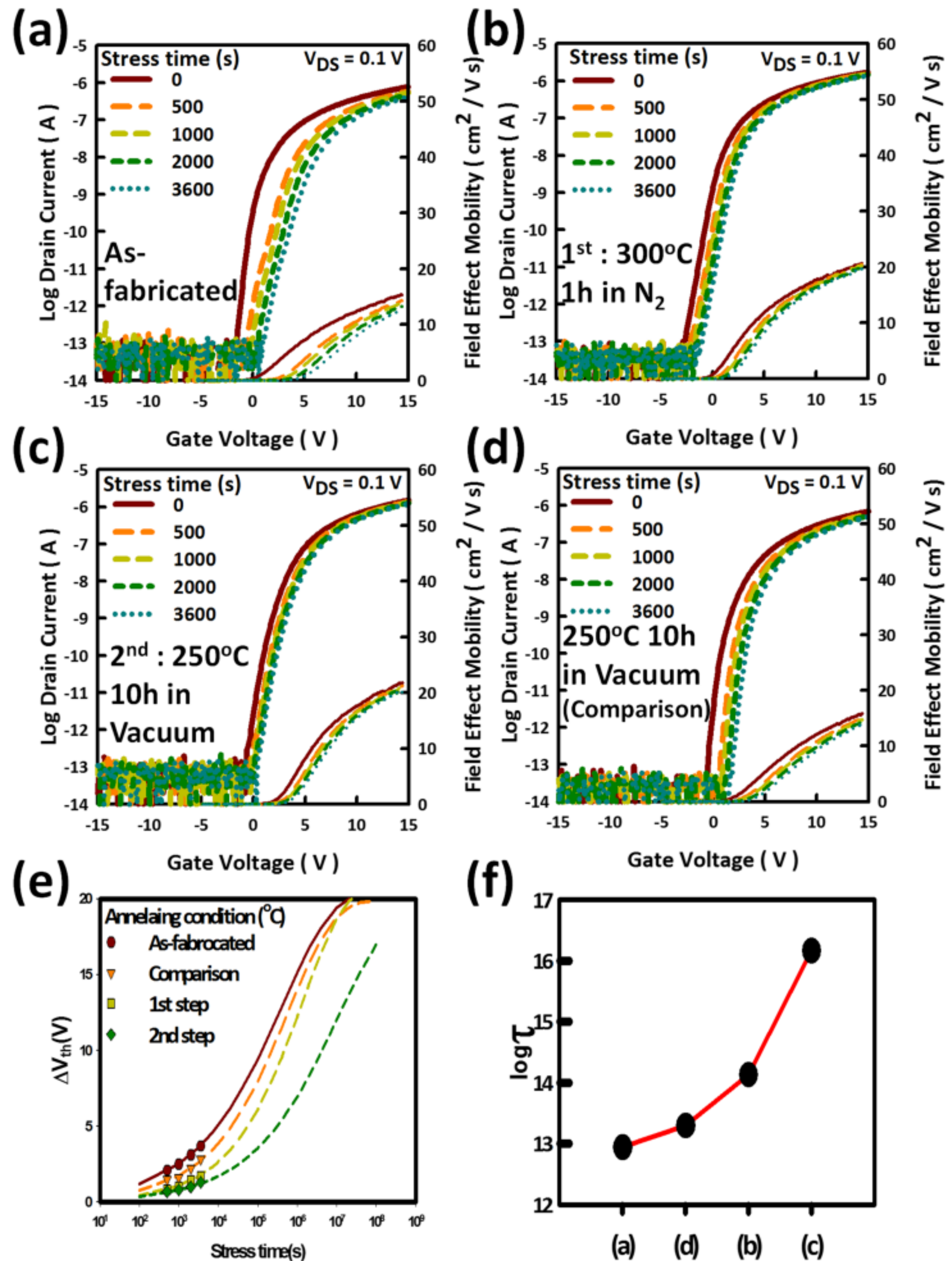

FIG. 4. The evolution of transfer characteristics under the positive bias temperature stress (PBTS) according to annealing step; (a) as-fabricated, (b) 1st step annealing and (c) 2nd step annealing. For comparison, the results for (d) the as-fabricated TFT annealed at 250 °C in vacuum for 10h are included. The PBTS was carried out at the gate bias stress = +20 V with source/drain = 0 V at 60 °C for 3600s. (e) Stretched exponential plots for the TFTs with different annealing conditions and (f) extracted Tau (τ) for the different annealing conditions (a) to (d).

The PBTS results of the TFT annealed for 10 h at 250 °C without 300 °C annealing appear in Fig. 4(d), indicating ΔV_{TH} of 2.4 V which is larger than that (ΔV_{TH} of 1.3 V) of the 1st and 2nd step annealed TFT. Note that the TFTs annealed in N_2 ambient shows better stability than that of vacuum ambient. The nitrogen can serve as an environmental shielding gas. The stretched exponential plots shown in Fig. 4(e) are used to evaluate a long-term stability; log τ is plotted in Fig. 4(f). The stretched exponential formula is expressed as,

$$|\Delta V_{TH}(\mathrm{t})| = V_0 \left\{ 1 - exp\left[-(\frac{t}{\tau})^{\beta} \right] \right\} \tag{1}$$

here, V_o is $|\Delta V_{TH}|$ at infinite time, τ is the time constant and β is the stretched exponential parameter.[23] Here, we found that the τ of the as-fabricated TFTs is 4.18 x 10^5s. Moreover, the τ for the 1st and 2nd step annealed TFTs are respectively 1.37 x 10^6s and 1.05 x 10^7s, indicating that the bias-stability of TFT is much improved by the 1st and 2nd step annealing. The β's for the as-prepared and 1st and 2nd annealing steps are 0.34, 0.41 and 0.34 respectively.

To study the effect of annealing on the top SiO_2/a-IGZO and bottom a-IGZO/SiO_2 interfaces, the XPS depth profile of SiO_2/a-IGZO/SiO_2 was measured. Fig. 5(a), (b) and (c) show the deconvolution of O1s intensity at the top interface. The three peaks are due to the metal-oxygen (M-O) bonds at 530 eV, oxygen vacancy (V_o) at 531 eV and oxygen-hydrogen (O-H) at 532 eV.[12] At the top interface, it is found the significant change of M-O concentration according to annealing step, from 43.7 % for as-fabricated, to 30.1 % after 1 step annealing, and to 41.5 % after second step annealing. Moreover, V_o concentration exhibits a slight change from 30.1 % to 28.4 % and to 27.3 %, O-H bonds change from 26.2 % to 41.5 % and to 31.3 %, respectively.

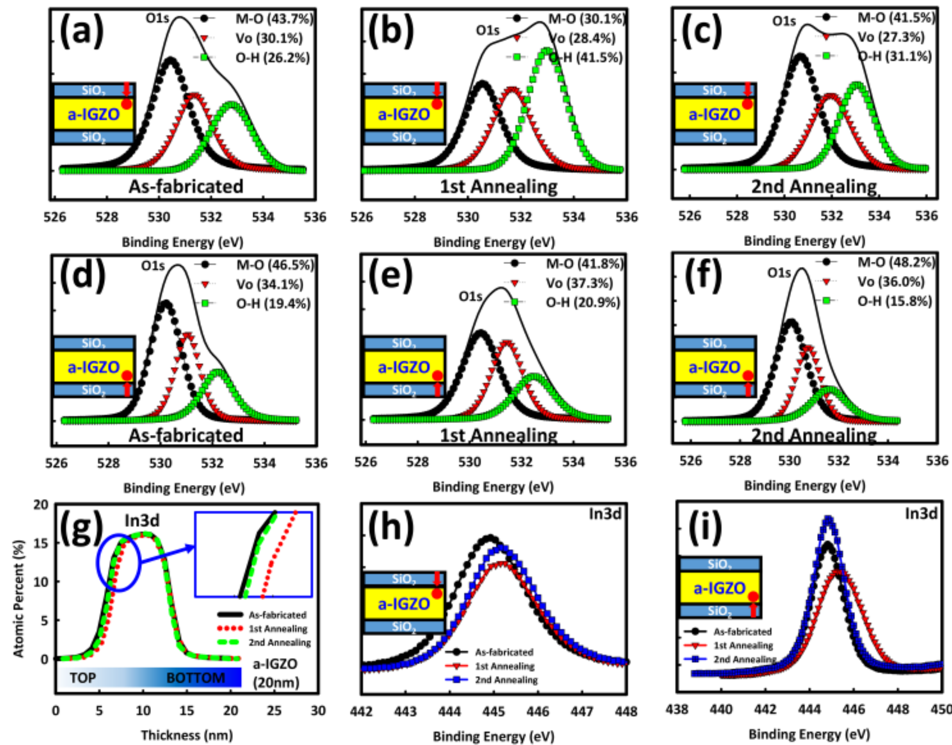

FIG. 5. Deconvolution of XPS O1s intensity at the top SiO_2/a-IGZO interface according to the annealing step; (a) as-fabricated, (b) 1st step annealing and (c) 2nd step annealing. Deconvolution of O1s intensity at the bottom interface between a-IGZO/bottom SiO_2; (d) as-fabricated, (e) 1st step annealing and (f) 2nd step annealing. (g) Depth profile of In3d intensity with inset which is an enlargement of the circled area and the deconvolution of In3d intensity at (h) the top interface and (i) bottom interface for the different annealing conditions.

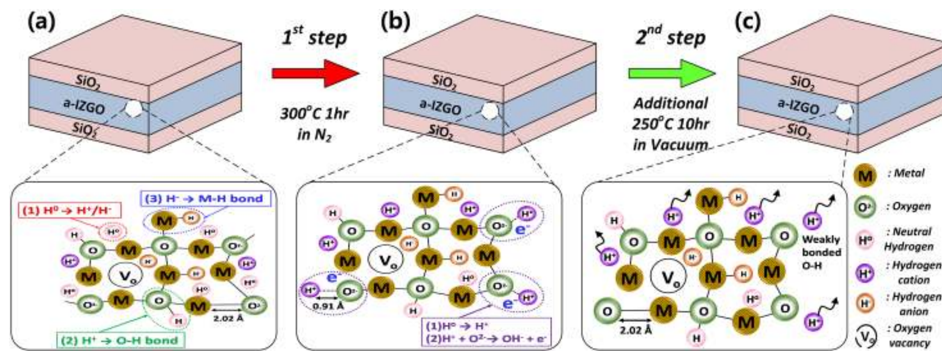

FIG. 6. The schematic of SiO_2/a-IGZO/SiO_2 structures at the top and bottom interfaces according to the annealing step. (a) As-fabricated, (b) 1st step annealing and (c) 2nd step annealing. Hydrogen absorption upon 1st step annealing and desorption after 2nd step annealing change the concentration of O-H bonds at the interfaces. Hydrogen exists as H^o, H^+, and H^- and the bond length of oxygen with hydrogen (O-H: 0.0911 nm) is shorter than In with oxygen (In-O = 0.20167 nm).

High O-H concentration at the top interface appears upon 1st step annealing, but its concentration decreases significantly by the 2nd step annealing, leading to more M-O bonds. On the other hand, the V_o concentration changes a little. On the other hand, the bottom interface of a-IGZO/SiO_2 changes a little as shown in Figure 5(d), (e) and (f), summarizing that M-O (46.5 %, 41.8 %, and 48.2 %), O-H (19.4 %, 20.9 %, and 15.8 %) and V_o (34.1 %, 37.3 %, and 36.0 %) for the three different steps. This is due to the stable bottom interface because the bottom SiO_2 is deposited at high temperature (380 °C) than top SiO_2 and thus makes a stable bottom a-IGZO/SiO_2 interface.[24] As a result, comparing Figure 5 (a), (b), (c) with (d), (e) and (f) reveals that the reaction with hydrogen is more active at the top interface. Fig. 5(g) shows the In3d atomic percentage as a function of etching time, indicating that In at the interface diffuses toward the a-IGZO after the 1st step annealing. It appears to be correlated with the hydrogen in a-IGZO with shorter O-H bond (0.0911nm) compared with In-O (0.20167nm).[25] This phenomenon is identified in Fig. 5 (h) and (i) showing In3d intensity at the top and bottom interfaces respectively. As shown in Fig. 5 (h), the InO_3 peak at the binding energy 444.6 eV shifts to In $(OH)_3$ peak at the binding energy 445.2 eV.

Fig. 6 shows the schematic diagram explaining the annealing effect for the a-IGZO TFT. The hydrogen in the a-IGZO can be in the states of H^0, H^+, and H^-. The H^- can be placed at the oxygen vacancy site and then form the metal-hydrogen bond (M-H) which is thermally stable.[26] Therefore, this does not change after annealing at 300 °C. On the other hand, H^+ in a-IGZO reacts with O^{2-} and donates one electron by the following reaction;

$$(H^+ + O^{2-} \rightarrow OH^- + e^-) \tag{2}$$

The H^+ in a-IGZO can react with O^{2-} during 300 °C annealing and then form O-H, leading to increase in O-H concentration as shown in Fig. 6 (b). The increase in O-H is confirmed by XPS result, and the generated free electrons according to eq. (2) decrease the V_{TH} and leads to negative shift of transfer curve.

The 2nd step annealing, long time annealing at 250 °C, the H in the weak O-H bonds formed during the 1st step annealing can diffuse out as shown in Fig. 6 (c). It leads to decrease in O-H concentration and to increase M-O bonds. This leads to the reduction in free electron and positive shifts of V_{TH} and transfer curve. By optimization of annealing steps, the a-IGZO TFT can have accumulation mode and stable operation under bias stress.

In summary, the two-step annealing for the a-IGZO TFTs is studied to improve the positive bias stability and to move V_{TH} into positive gate direction. The transfer curve shifts to the negative gate voltage by 1st step annealing at 300 °C for 1h. However, V_{TH} shifts to the positive gate voltage direction by 2nd step annealing at 250 °C for 10h. The mobility increases from 18 to 25 $cm^2V^{-1}S^{-1}$ by 1st step at 300 °C and to 20 $cm^2V^{-1}S^{-1}$ by 2nd step annealing. The better PBTS stability can be achieved through these two-step annealing process. It is found from the XPS analysis that the

diffusion of hydrogen in a-IGZO layer affects the threshold voltage shift. These results indicate that the threshold voltage of the TFT shifts to near zero and bias stability can be improved by two-step annealing, first at high temperature for a short time and then low-temperature long time.

The research was supported by the Korea Evaluation Institute of Industrial Technology (KEIT) Development of Core Technologies (Grant Number : 10070201) for Transportation Systems such as Green Car program funded by the Ministry of Trade, Industry and Energy (MOTIE).

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).
[2] T. Kamiya, K. Nomura, and H. Hosono, J. Disp. Technol. **5**, 273 (2009).
[3] T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11117**, 44305 (2010).
[4] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap. **45**, 4303 (2006).
[5] E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012).
[6] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park, and J. Chung, Appl. Phys. Lett. **90** (2007).
[7] B. Kim, E. Chong, D. Hyung Kim, Y. Woo Jeon, D. Hwan Kim, and S. Yeol Lee, Appl. Phys. Lett. **99**, 062108 (2011).
[8] M. Mativenga, S. Hong, and J. Jang, Appl. Phys. Lett. **102**, 023503 (2013).
[9] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, Appl. Phys. Lett. **95**, 063502 (2009).
[10] P. Migliorato, M. D. H. Chowdhury, J. Gwang Um, M. Seok, and J. Jang, Appl. Phys. Lett. **101** (2012).
[11] K. Nomura, T. Kamiya, and H. Hosono, ECS J. Solid State Sci. Technol. **2**, P5 (2013).
[12] K. H. Ji, J. I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, C. S. Hwang, D. Lee, H. Hwang, and J. K. Jeong, Appl. Phys. Lett. **98**, 103509 (2011).
[13] H. K. Noh, J. S. Park, and K. J. Chang, J. Appl. Phys. **113**, 063712 (2013).
[14] Y. K. Moon, S. Lee, W. S. Kim, B. W. Kang, C. O. Jeong, D. H. Lee, and J. W. Park, Appl. Phys. Lett. **95**, 013507 (2009).
[15] C. Kulchaisit, Y. Ishikawa, M. N. Fujii, H. Yamazaki, J. P. S. Bermundo, S. Ishikawa, T. Miyasako, H. Katsui, K. Tanaka, K. I. Hamada, M. Horita, and Y. Uraoka, J. Disp. Technol. **12**, 263 (2016).
[16] J. G. Um, M. Mativenga, P. Migliorato, and J. Jang, J. Appl. Phys. **117**, 234502 (2015).
[17] S. I. Oh, J. M. Woo, and J. H. Jang, IEEE Trans. Electron Devices **63**, 1910 (2016).
[18] J. S. Park, J. Electroceramics **28**, 74 (2012).
[19] S. Jeon, A. Benayad, S. E. Ahn, S. Park, I. Song, C. Kim, and U. I. Chung, Appl. Phys. Lett. **99**, 082104 (2011).
[20] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. **95**, 013503 (2009).
[21] A. Janotti and C. G. Van de Walle, Nat. Mater. **6**, 44 (2007).
[22] M. Mativenga, J. K. Um, D. H. Kang, R. K. Mruthyunjaya, J. H. Chang, G. N. Heiler, T. J. Tredwell, and J. Jang, IEEE Trans. Electron Devices **59**, 2501 (2012).
[23] M. D. H. Chowdhury, P. Migliorato, and J. Jang, Appl. Phys. Lett. **102** (2013).
[24] M. D. H. Chowdhury, J. G. Um, and J. Jang, Appl. Phys. Lett. **105** (2014).
[25] N. M. Lakin, T. D. Varberg, and J. M. Brown, J. Mol. Spectrosc. **183**, 34 (1997).
[26] J. Bang, S. Matsuishi, and H. Hosono, Appl. Phys. Lett. **110** (2017).