Control of Self-Heating in Thin Virtual Substrate Strained Si MOSFETs

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***Abstract*—This paper presents the first results and analysis of strained Si n-channel MOSFETs fabricated on thin SiGe virtual substrates. Significant improvements in electrical performance are demonstrated compared with Si control devices. The impact of SiGe device self-heating is compared for strained Si MOSFETs fabricated on thin and thick virtual substrates. This paper demonstrates that by using high-quality thin virtual substrates, the compromised performance enhancements commonly observed in short-gate-length MOSFETs and high-bias conditions due to self-heating in conventional thick virtual substrate devices are eradicated. The devices were fabricated with a 2.8-nm gate oxide and included NiSi to reduce the parasitic series resistance. The strained layers grown on the novel substrates comprising 20% Ge did not relax during fabrication. Good ON-state performance, OFF-state performance, and cross-wafer uniformity are demonstrated. The results show that thin virtual substrates have the potential to circumvent the major issues associated with conventional virtual substrate technology. A promising solution for realizing high-performance strained Si devices suitable for a wide range of applications is thus presented.**

***Index Terms*—MOSFETs, self-heating, silicon germanium, strained silicon, virtual substrate.**

I. Introduction

NOVEL device structures and new channel materials are required to compensate the loss in mobility encountered at advanced CMOS technology nodes due to higher channel doping and scaled gate dielectrics. Strained Si technology can provide a solution for aggressively scaled devices by enhancing the transport properties of both electrons and holes [1]. Tensile strain induces modifications to the conduction and valence energy bands, which reduces intervalley scattering and lowers carrier effective masses, leading to an increase in carrier mobility. Beneficial process-induced strain is relatively simple to implement, but the amount of strain (and, hence, mobility enhancements) that can be achieved is limited [2]–[6]. Global strain can be introduced using a "virtual substrate" of SiGe and has been shown to improve performance by more than 100% [7]–[14]. The lattice mismatch between Si and Ge results in tensile strained Si when epitaxially grown on relaxed SiGe. By varying the Ge composition in the SiGe, precise amounts of strain can be engineered into the epilayers. Compressive strain and novel multiheterojunction devices can also be realized using this approach, which increases design flexibility [15]. While difficulties associated with defect density and processing Ge (e.g., dopant diffusion, silicide formation, thermal oxidation) create challenges for the introduction of virtual substrates into mainstream production, it is anticipated that future generations of devices will need both local and global strain contributions in order to maintain Moore's law.

Performance gains of virtual substrate devices are presently compromised by self-heating due to the low thermal conductivity of SiGe [16]. This is particularly important for analog applications, which could otherwise benefit from strained Si technology [17]. Thin virtual substrates can increase device performance by reducing the effects of self-heating evident in devices fabricated on conventional thick virtual substrates. Faster epitaxial growth time and reduced material consumption for thinner layers also improve the economic viability of virtual substrate technology. However, in order to realize the potential advantages of thin virtual substrates, thermal stability and defectivity must be controlled. Conventional virtual substrates are several micrometers in thickness in order to reduce surface defectivity such as roughness arising from compositional grading and threading dislocations, which degrade electrical performance, and to maximize relaxation [18], [19]. However, advances in epitaxial growth methods over the past decade have enabled improved material quality, and recently, particular emphasis has been placed on the generation of high-quality thin virtual substrates. The intentional introduction of point defects can enhance the relaxation of virtual substrates and can be realized, for example, by incorporating a very low temperature growth stage for the SiGe. This has been achieved in thin virtual substrate material grown by both low-energy plasma-enhanced chemical vapor deposition (LEPECVD) [20] and solid-source molecular beam epitaxy (MBE) [21]–[24]. Low-energy ion implantation can also be used to create point defects within the SiGe layer and has been demonstrated using a variety of species including Si^+ [21], H^+, and He^+ [25]. With H^+ and He^+ implants, bubbles are formed below the interface, which guide the dislocation arms beneath the surface upon subsequent annealing. A technique that implants Ar^+ ions directly into the Si substrate in order to avoid defect formation within the SiGe layer, which can be close to the active device region [26],

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has also been developed. Finally, Delhougne *et al.* have shown that by incorporating a thin carbon-containing layer within the constant composition SiGe buffer layer provides sufficient nucleation sites for relaxation of thin SiGe layers [27].

Despite the wide range of methods investigated for producing thin virtual substrates, to date, there are very few reports of electrical performance from devices fabricated on thin relaxed SiGe layers. Strained Si MODFETs have been fabricated on thin virtual substrates generated by He^+ implantation [25] and low-temperature LEPECVD growth [20]. Although both growth methods resulted in improved high-frequency performance compared with devices fabricated on thick virtual substrates, high surface defectivity and incomplete virtual substrate relaxation limited device performance. Strained Si p-MOSFETs have been fabricated on thin $Si_{0.8}Ge_{0.2}$ virtual substrates and demonstrate improved performance compared with bulk Si controls, but the impact on device self-heating was not considered [28]. Thin virtual substrate strained Si n-MOSFETs have also recently been reported, but the effect of virtual substrate thickness on electrical performance was similarly not addressed [29]. Consequently, the ability of thin virtual substrate material to reduce self-heating in strained Si MOSFETs has not yet been established. While performance gains at moderate geometries may be more effectively introduced through processing, increasingly complex solutions for process-induced strained devices at very small geometries [30] may render thin virtual substrates an attractive option for advanced technology generations, i.e., in terms of both cost and process simplicity. This paper presents the first analysis of strained Si MOSFETs fabricated on thin virtual substrates. The virtual substrates are generated by the incorporation of a very low temperature growth stage in order to create a high density of point defects. This method is one of the most promising in terms of achieving highly relaxed thin SiGe virtual substrates. High performance and significant reductions in self-heating are demonstrated, thereby confirming that thin virtual substrates can extend the advantages offered by conventional virtual substrate technology by enabling greater performance gains for a wider range of applications.

II. Material Growth and Device Fabrication

The thin virtual substrate material was grown using solid-source MBE. The epitaxial layer structure is shown in Fig. 1. The first 30 nm of $Si_{0.8}Ge_{0.2}$ was grown at 160 °C in order to generate a supersaturation of point defects. In this regime, SiGe growth on Si is metastable, but the high concentration of point defects stimulates a high degree of relaxation within a small thickness in the overlying virtual substrate layers. Furthermore, the interaction of point defects with existing threading dislocations causes a reduction in the surface threading dislocation density [21]. Following the very low temperature growth stage, 50 and 120 nm of $Si_{0.8}Ge_{0.2}$ were grown at 550 °C and 575 °C, respectively, in order to induce relaxation and anneal residual point defects. A strained Si surface channel (15 nm) was finally grown at 500 °C, which was partially consumed during device fabrication. It has previously been shown that epitaxial growth at these temperatures, alloy

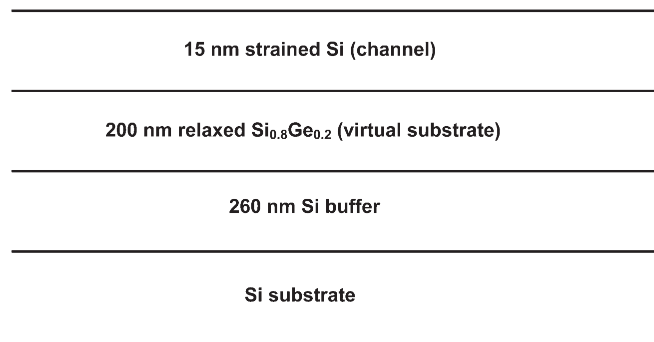

Fig. 1. Epitaxial layer structure for the strained Si devices.

compositions, and thicknesses result in full relaxation of the thin virtual substrate layers [21]. The root-mean-square (rms) surface roughness of the virtual substrate was approximately 1 nm [which was measured by atomic force microscopy (AFM) and optical surface profilometry], and no cross-hatching was observed. The improved surface morphology compared with conventional virtual substrates consisting of thick graded buffer layers is consistent with reports of thin virtual substrates grown by LEPECVD [20] and arises from relaxation being induced through point defects that coalesce and form dislocation loops near the interface. For thick graded SiGe layers, relaxation occurs via the formation of misfit dislocations from the growing surface. The stress fields associated with the misfit dislocation networks influence subsequent epitaxial growth, which leads to a cross-hatch morphology [31], [32].

The strained Si and Si control devices were processed simultaneously using a conventional fabrication scheme. Boron was used for the well and channel implants. Active areas were defined in deposited oxide, and a thermal gate oxide was grown at 700 °C. In situ phosphorus-doped polysilicon 150 nm in thickness was deposited for the gate electrode. Gate lengths ranging from 0.35 to 10 μm were defined and source/drain extensions were implanted using As. Oxide spacers were deposited, and As was used to create the source/drain diffusion regions. Implant activation was carried out at 950 °C for 30 s. NiSi was formed on the source, drain, and gate, and standard back-end processing comprising TiW and Al completed the device fabrication. A scanning electron microscope (SEM) image of a 0.35-μm device is shown in Fig. 2.

III. Results and Analysis

Strain measurements were carried out using Raman spectroscopy both before and after processing and confirmed that the fabrication process did not induce relaxation of channel macrostrain. Following device fabrication, specific devices were deprocessed down to the substrate, and Raman spectra were obtained from MOSFET channels using a 514.5-nm laser fitted to a Jobin Yvon LabRAM HR system. The laser beam spot size is reduced to less than 1 μm in diameter on the sample surface. Fig. 3 shows a spectrum from a typical strained Si device after processing. The peak due to the Si–Si vibrations in the strained Si channel is partially hidden by the large peak due to the Si–Si vibrations in the SiGe virtual substrate.

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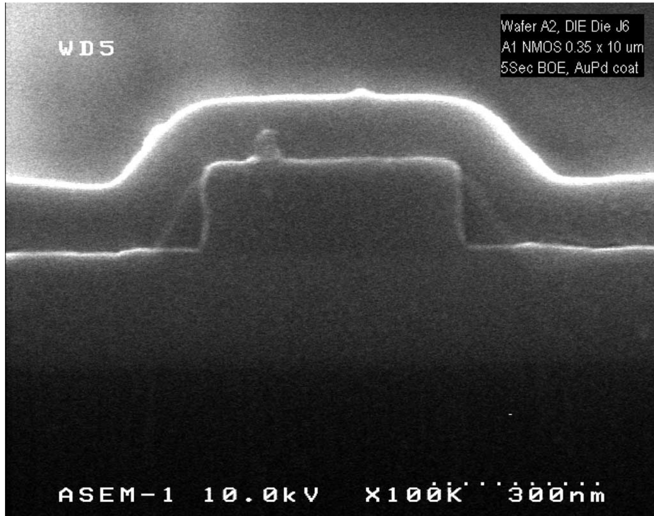

Fig. 2. SEM image of a 0.35-μm strained Si device.

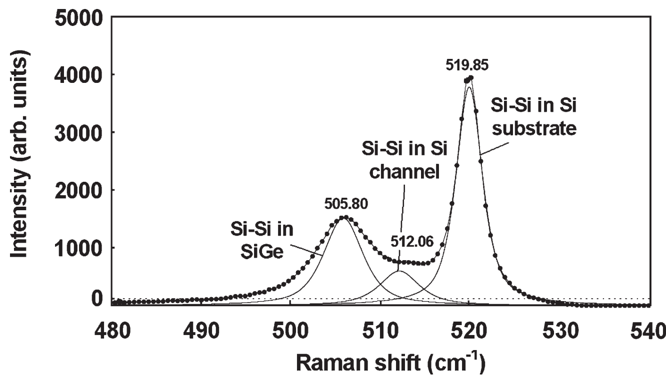

Fig. 3. Raman spectrum measured in the channel region of a strained Si device using a 514.5-nm laser. Measured values are represented by the dotted line, and solid lines represent fitted peaks. Gate layers have been removed prior to measurements.

However, it has previously been shown that peak fitting using PEAKFIT software [33] enables relatively weak signals from the Si surface channel to be accurately distinguished from the peak due to the SiGe virtual substrate [34]. Peak fitting was carried out using this technique, and the fitted spectra with their peak positions are shown in Fig. 3. Assuming full virtual substrate relaxation, which has been demonstrated on similar wafers grown using this method [21], a virtual substrate Ge composition of $Si_{0.79}Ge_{0.21}$ is determined from the SiGe peak position. This is very close to the target value of $Si_{0.80}Ge_{0.20}$. Moreover, the peak due to the Si channel is located at 512.06 cm^{-1}, which corresponds very well with the value of strain expected for a fully relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate [34]. This indicates that the high-temperature source/drain implant activation anneals and the ion implantations used for the well and channel doping did not cause degradation of channel macrostrain. Since the penetration depth for the 514.5-nm laser is approximately 570 nm in $Si_{0.8}Ge_{0.2}$ [35], a signal due to the Si substrate is also detected and is observed as a peak located on the spectra at 519.85 cm^{-1}. Strain was further assessed by Schimmel etching [36]. A micrograph of the channel region following device deprocessing and Schimmel etching is presented

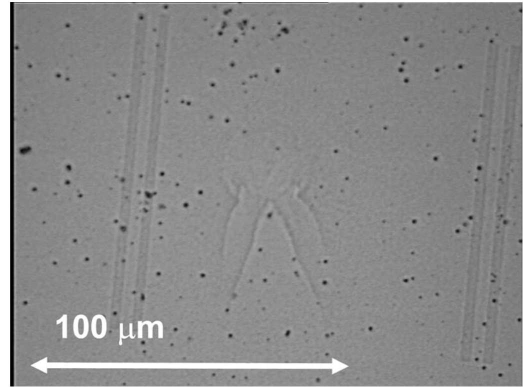

Fig. 4. Micrograph of the thin virtual substrate material underneath a gate structure following Schimmel etching. Gate layers have been removed prior to defect etching.

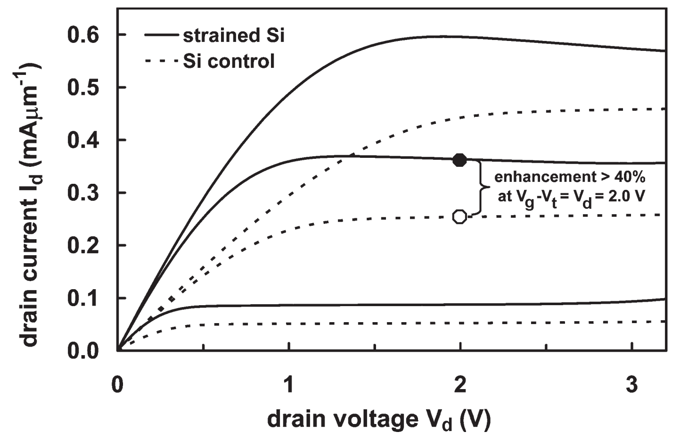

Fig. 5. Output characteristics for 0.35-μm-gate-length strained Si and Si control devices. Data were measured at gate overdrive voltages $(V_g–V_t)$ of 1.0, 2.0, and 3.0 V.

in Fig. 4. The etch pit density in the channel regions on the same die as those measured using Raman spectroscopy was found to be 9×10^5 cm^{-2}. This is comparable with that found in thick virtual substrates having the same alloy composition [37] and demonstrates that thin virtual substrates can provide both the material quality and channel robustness required for strained Si technology. The parallel lines in Fig. 4 are imprints on the substrate due to device processing.

Large increases in drain current I_d are demonstrated for the strained Si devices fabricated on thin virtual substrates compared with the bulk Si controls. Fig. 5 shows output characteristics for 0.35-μm-gate-length devices measured at gate overdrive voltages $(V_g–V_t)$ of 1.0, 2.0, and 3.0 V, where V_g is the gate voltage, and V_t is the threshold voltage. At a drain voltage $V_d = V_g - V_t = 2.0$ V, the drain current is increased by over 40% for the strained Si device compared with the Si control device. Furthermore, the near-constant drain current observed after saturation for the strained Si device demonstrates that there is only a small effect of device self-heating. This markedly contrasts with previous strained Si devices fabricated on thick virtual substrates having the same virtual substrate alloy composition and operating at the same power levels [37]. Fig. 5 therefore confirms that the detrimental effects of self-heating in strained Si MOSFETs due to the low thermal

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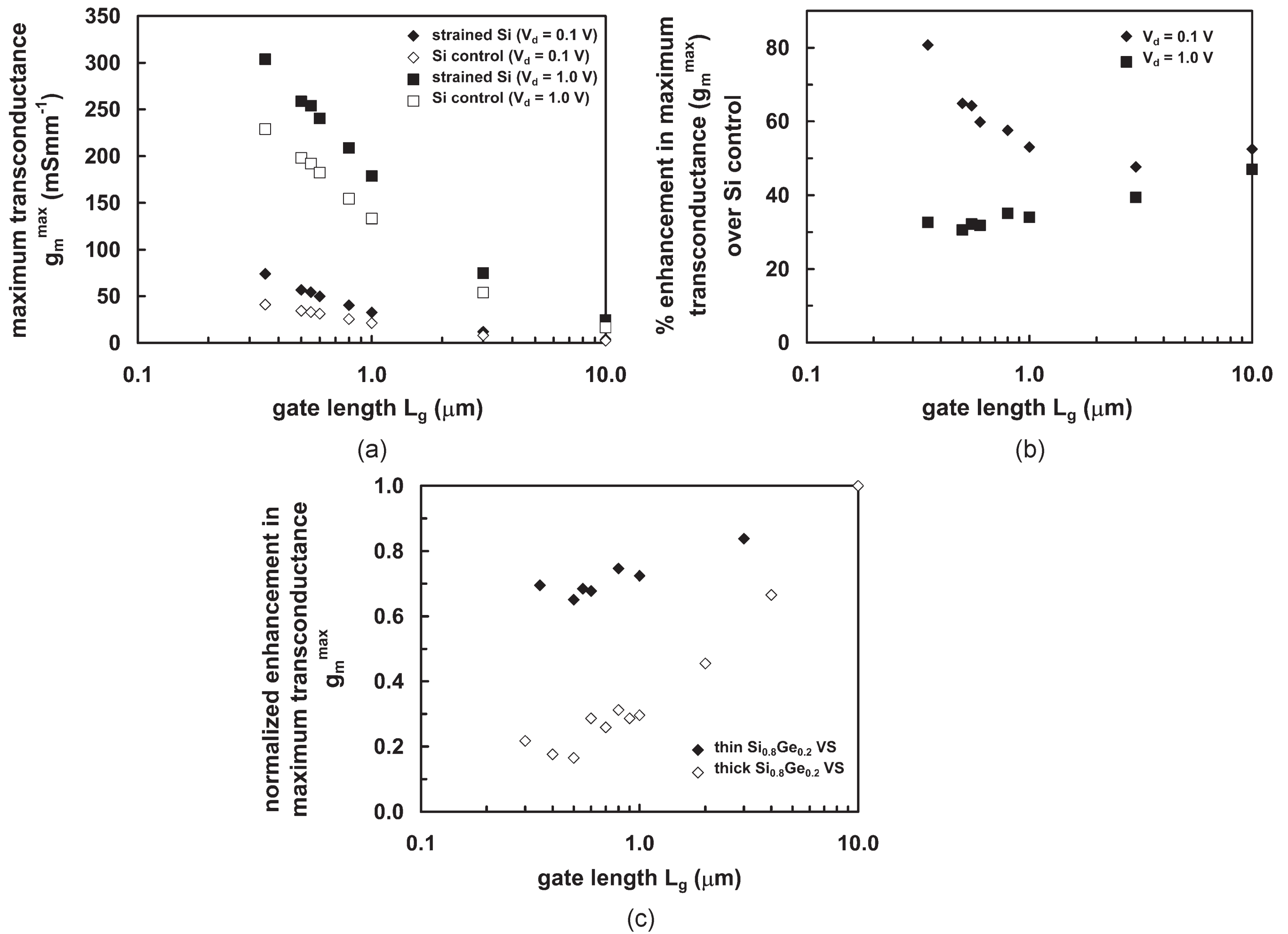

Fig. 6. (a) Variation in maximum transconductance $g_m^{\max}$ with gate length L_g for strained Si and control devices measured at drain voltages V_d of 0.1 and 1.0 V. (b) Enhancement in maximum transconductance $g_m^{\max}$ versus gate length L_g for strained Si devices compared with Si control devices measured at drain voltages V_d of 0.1 and 1.0 V. (c) Comparison of enhancements in maximum transconductance $g_m^{\max}$ for strained Si devices fabricated on thin ($\sim$ 200 nm) and thick ($\sim$ 2 μm) $\mathrm{Si}_{0.8}\mathrm{Ge}_{0.2}$ virtual substrates. Data for the thick virtual substrates were taken from [37]. Performance gains are maintained to a greater extent at short gate lengths in devices fabricated on thin virtual substrates due to reduced effects of self-heating.

conductivity of SiGe can be significantly reduced by using thin virtual substrates. Although self-heating is often believed to increase at advanced technology nodes due to higher drive currents, voltages are also scaled downward, and self-heating becomes a function of power dissipation. The 90-nm technology node uses drain voltages of 1.1 V, whereas the 0.35-μm devices in this paper operate up to drain voltages of 3.0 V. Fig. 5 shows that at a drain voltage of 2.0 V, the power dissipated is 12 mW. This is the same as the power dissipation specified for the 90-nm node based on the 2005 International Technology Roadmap for Semiconductors [38].

The gains in strained Si drain current are evident despite the increase in source/drain resistance compared with bulk Si devices. The source/drain sheet resistance (established by Van der Pauw measurements) was found to be 10 Ω/sq for the strained Si devices and 8 Ω/sq for the Si control devices. Contact resistance was also increased in the strained Si devices. For 1 μm $\times$ 1 μm contacts, the strained Si contact resistance was approximately ten times greater than on the Si control devices, which was measured using cross-bridge Kelvin structures. Since there was no difference between either the sheet resistance or the contact resistance for the gate electrode, the discrepancy between the strained Si and Si control devices in the source/drain regions is considered to be due to the presence of Ge from the virtual substrate [39]. Consequently, further optimization of the silicidation process and the contact module would enable thin virtual substrates to provide even greater performance enhancements at short channel lengths.

Significant gains in electrical performance are realized for the strained Si devices at all gate lengths fabricated, and the successful reduction in self-heating through use of thin virtual substrates is shown in Fig. 6. The maximum values of transconductance $g_m^{\max}$ at $V_d = 0.1$ V and $V_d = 1.0$ V are presented as a function of gate length L_g in Fig. 6(a). Performance enhancements for strained Si devices are obtained for all V_d and over the whole range of gate lengths. The increase in $g_m^{\max}$ compared with the Si control data is shown in Fig. 6(b). The trends in performance enhancement with L_g at both V_d are similar to those observed previously for thick virtual substrates [13]. At low V_d, the gains increase at smaller geometries, whereas

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at higher V_d, there is a slight reduction in the enhancements compared with those of larger geometry devices. There are a number of potential contributions to the observed performance loss at smaller geometries. Increased parasitic series resistance in strained Si devices compared with Si control MOSFETs will have a greater impact in short-gate-length devices, since parasitic resistance is a larger proportion of the total device resistance. Loss of channel strain may also occur at smaller gate dimensions and lower the performance enhancements. However, to date, it has not been possible to correlate channel strain with electrical performance since very few methods exist for directly measuring strain in submicrometer MOSFETs. Finally, increased power levels lead to a greater impact of poor heat dissipation in the short-channel virtual substrate devices. For thick virtual substrate devices, it has previously been shown that device self-heating is the dominating factor in the diminished performance enhancements of short-channel strained Si MOSFETs [37]. Consequently, by using thinner SiGe virtual substrates, the reduced performance gains at short channel lengths should be significantly reduced. This is clearly demonstrated in Fig. 6(c), which compares the performance enhancements at $V_d = 1.0$ V for strained Si MOSFETs fabricated on thin and thick virtual substrates. The thick virtual substrate consists of 2-μm relaxed $\mathrm{Si_{0.8}Ge_{0.2}}$ [40], whereas the thin virtual substrate used in this paper is ten times thinner (200 nm). In Fig. 6(c), the performance enhancements of the strained Si devices fabricated on the thin and thick $\mathrm{Si_{0.8}Ge_{0.2}}$ virtual substrates are presented as a function of gate length. The data are normalized against the gains in $g_m^{\max}$ achieved at long gate lengths (10 μm) in order to eliminate the effects of differing processing conditions. The gradient is significantly reduced for the thin virtual substrate data compared with the thick virtual substrate data, which indicates that the impact of self-heating is much lower in thin virtual substrate devices. For the thick virtual substrate devices, the enhancements in $g_m^{\max}$ in short-channel devices ($L_g = 0.35$ μm) are reduced to $\sim$ 20% of the enhancement observed in long-channel devices ($L_g = 10$ μm). However, for the thin virtual substrate devices, the enhancement in $g_m^{\max}$ at short channel lengths is maintained at $\sim$ 70% of $g_m^{\max}$ for long-channel devices. This represents an improvement factor of 3.5 for the thin virtual substrate devices and is in good agreement with the threefold improvement observed in the self-heating effect when the virtual substrate thickness is reduced by a similar amount in strained Si n-channel MODFETs [20]. The reduction in self-heating for thin virtual substrate strained Si MOSFETs in this paper compared with MOSFETs fabricated on thick virtual substrates was further investigated by measurements carried out using the ac conductance technique. This method uses the small-signal drain conductance at high frequency to eliminate the impact of dynamic self-heating in the channel [41]. AC measurements were carried out using a 4294A precision impedance analyzer at a frequency of 10 MHz, which enabled the thermal resistance of the devices to be evaluated. For 0.4-μm-gate-length devices, the thermal resistances of the thin and thick virtual substrates were determined to be 4.6 and 18.9 $\mathrm{K \cdot mW^{-1}}$, respectively. This represents a fourfold difference and agrees well with the 3.5-fold improvement in performance observed in thin virtual substrate short-channel devices compared with thick virtual devices [Fig. 7(c)]. The improved device performance is also in good agreement with the analytical estimate that the thermal resistance of a device on a relaxed SiGe buffer is proportional to the square root of the buffer thickness [42]. In this paper, there is a tenfold reduction in the thickness of the thin and thick virtual substrates (200 nm compared with 2 μm), which gives a predicted improvement factor of 3.3 for the self-heating effect. These results clearly demonstrate that thin virtual substrate technology goes a long way to circumvent the compromised performance enhancements commonly observed in thick virtual substrate strained Si devices [12], [13], [37], [43].

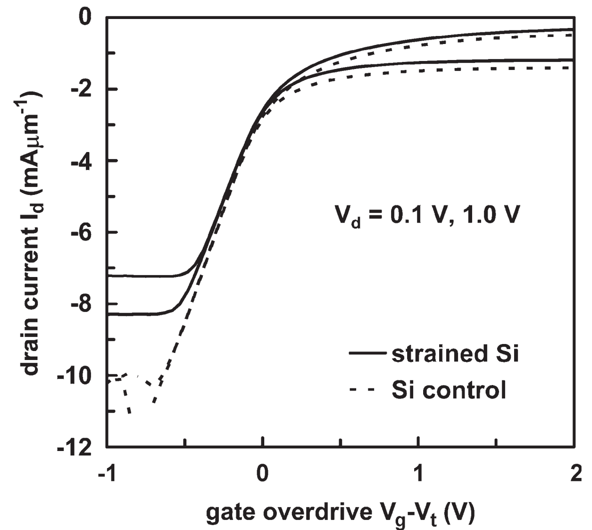

Fig. 7. Subthreshold characteristics for 0.35-μm-gate-length strained Si and Si control MOSFETs measured at drain voltages V_d of 0.1 and 1.0 V.

In addition to the large performance gains demonstrated in I_d and $g_m^{\max}$, the strained Si devices exhibit excellent subthreshold characteristics. Fig. 7 shows 0.35-μm-gate-length devices measured at $V_d = 0.1$ and 1.0 V. Drain-induced barrier lowering (DIBL) is well controlled (9 and 16 mV/V for the strained Si device and Si control device, respectively), and the subthreshold slope is found to be 90 mV/dec for the strained Si device and 80 mV/dec for the Si control. The small discrepancy in DIBL and subthreshold slope for the strained Si and bulk Si devices is likely to arise from increased diffusivity of B in both strained Si and relaxed SiGe compared with bulk Si during annealing at high temperature, as carried out during the fabrication process [44]. Both sets of devices received the same B implant conditions for the substrate doping, thus, the increased diffusivity of B in strained Si and relaxed SiGe may have led to higher channel doping in the strained Si devices.

Fig. 7 shows that the leakage floor is approximately 5 $\mathrm{nA \cdot \mu m^{-1}}$ at $V_d = 0.1$ V for the strained Si device and increases to 60 $\mathrm{nA \cdot \mu m^{-1}}$ at $V_d = 1.0$ V. For the Si control device, the leakage is almost two orders of magnitude lower at $V_d = 0.1$ V (< 0.1 $\mathrm{nA \cdot \mu m^{-1}}$), and the change in leakage as V_d is increased to 1.0 V is negligible. At low V_d, the higher values of leakage for the strained Si device is partly due to the lower bandgap of SiGe compared with Si and partly due to a finite number of threading dislocations in the virtual

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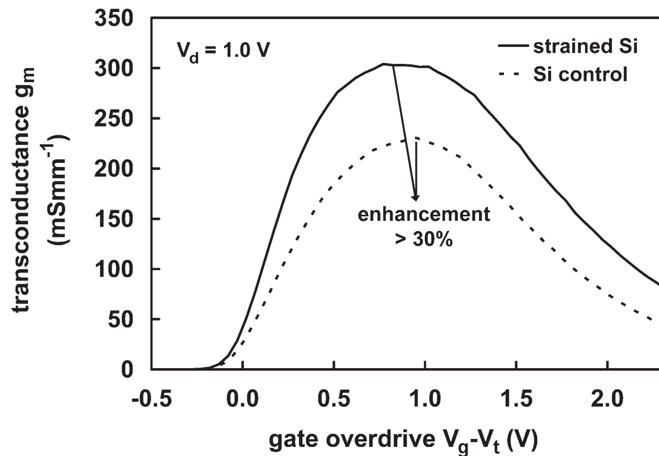

Fig. 8. Transconductance g_m versus gate overdrive $(V_g–V_t)$ characteristics for 0.35-μm-gate-length strained Si and Si control MOSFETs measured at a drain voltage V_d of 1.0 V.

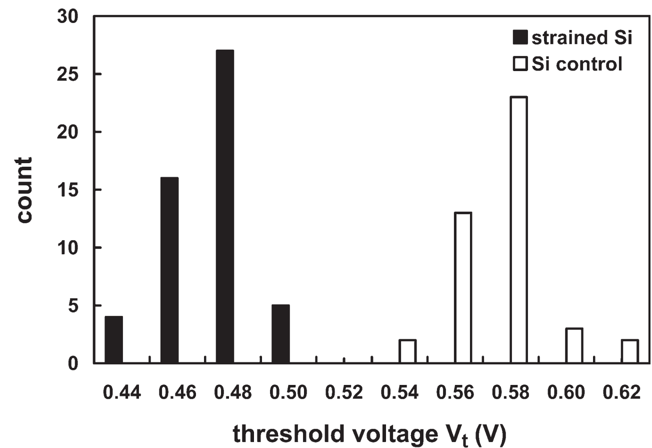

Fig. 9. Histogram showing the cross-wafer variation in threshold voltage V_t for 10-μm-gate-length strained Si and Si control MOSFETs. The spread in electrical parameters such as V_t is equivalent for both sets of devices and highlights the good uniformity of the strained Si/SiGe material.

substrate. Electrical measurements confirmed that substrate leakage was the main contributor to the OFF-state current, whereas gate oxide leakage was well controlled and less than $1 \times 10^{-7}\ \mathrm{A \cdot cm^{-2}}$ for both the strained Si and control Si devices. The greater discrepancy in the leakage between the strained Si and control devices at higher V_d is therefore likely to be a consequence of threading dislocations in the virtual substrate degrading the drain to substrate junctions. Source–drain leakage was further investigated by electrical measurements on a range of device geometries. If the measured OFF-state leakage was a result of dopant diffusion along misfit dislocations stretching between the source and the drain, as observed in [45], it would be expected that the magnitude of leakage would increase as the gate length is reduced. Source–drain leakage current was measured on all 10- and 0.35-μm-gate-length devices across the wafers. At $V_d = 0.1$ V, the median values of I_{OFF} were found to be 6.7 and 4.9 $\mathrm{pA} \cdot \mu\mathrm{m}^{-1}$ for the 10- and 0.35-μm devices, respectively. A small decrease in I_{OFF} for the Si control MOSFETs was similarly observed, reducing from 0.33 $\mathrm{pA} \cdot \mu\mathrm{m}^{-1}$ for the 10-μm devices to 0.14 $\mathrm{pA} \cdot \mu\mathrm{m}^{-1}$ for the 0.35-μm devices. Furthermore, the difference in I_{OFF} for the strained Si devices measured at $V_d = 0.1$ and 1.0 V was constant for both the 0.35- and 10-μm-gate-length MOSFETs. Therefore, source–drain leakage arising from misfit dislocations cannot be considered as a primary contributor to I_{OFF}. This agrees with the findings of Fiorenza *et al.*, who only observed an increase in I_{OFF} with reducing gate length when the strained Si layer exceeded the critical thickness. In this paper, the strained Si layer thickness (15 nm) was grown below the critical thickness for Si on relaxed $\mathrm{Si_{0.8}Ge_{0.2}}$ [15], thus, misfit dislocations arising from strain relaxation should not play a part in leakage, as observed. Fig. 8 shows the transconductance curves for the same devices measured at $V_d = 1.0$ V. Despite the higher series resistance for the strained Si MOSFETs, $g_m^{\max}$ is enhanced by more than 30% compared with the Si control device.

The excellent strained Si/SiGe material quality has also led to high wafer yield ($> 85\%$), where a fail was defined as a device exhibiting leakage above 10 $\mathrm{nA} \cdot \mu\mathrm{m}^{-1}$ at $V_d = 0.1$ V. The cross-wafer variation in performance was analyzed by measuring large MOSFET devices (10 μm gate length) on all die on the wafers. The uniformity of key electrical parameters such as $g_m^{\max}$ and V_t was found to be equivalent for the strained Si and Si control devices. A histogram showing the distribution of V_t for both wafers is shown in Fig. 9. The linear extrapolation method was used to extract V_t, and the standard deviation was found to be less than 3% of the mean value for both the strained Si and Si control devices. The good uniformity in the strained Si device characteristics is enabled by the good uniformity of the thin virtual substrate material. This was confirmed by cross-wafer measurements of material parameters such as surface roughness on a series of four wafers grown at the same time as the device wafer. The average value of surface roughness was found to be 1.2 nm, and the standard deviation of the roughness was just 0.1 nm. This is greater than the standard deviation in the electrical data and therefore confirms that surface roughness is not the dominating factor behind the distribution in device characteristics. Measurements were carried out on 260 μm $\times$ 350 μm scan areas using an optical profilometer and agreed well with the AFM data. Good cross-wafer uniformity of virtual substrate composition and strain using the same growth conditions as the device wafers used in this paper has also been confirmed [46].

Fig. 9 shows that there is a difference of approximately 90 mV in V_t for the strained Si and Si control devices. The effective oxide thickness was determined by capacitance–voltage (C–V) measurements at 1 MHz and was found to be 3 nm for both sets of devices (Fig. 10), which is in good agreement with the target physical oxide thickness of 2.8 nm. There was no appreciable difference in the gate oxide interface trap density D_{it} measured using the conductance technique [47] on MOS capacitors located on the same die as the MOSFET devices. D_{it} ranged from 7.4×10^{10} to $2.5 \times 10^{11}\ \mathrm{cm^2 \cdot eV^{-1}}$. Therefore, the reduction in threshold voltage for the strained Si devices compared with the Si control devices is considered to be primarily due to the differences in electron affinity between the strained and unstrained devices. The threshold voltage of the strained Si devices can be controlled by modification

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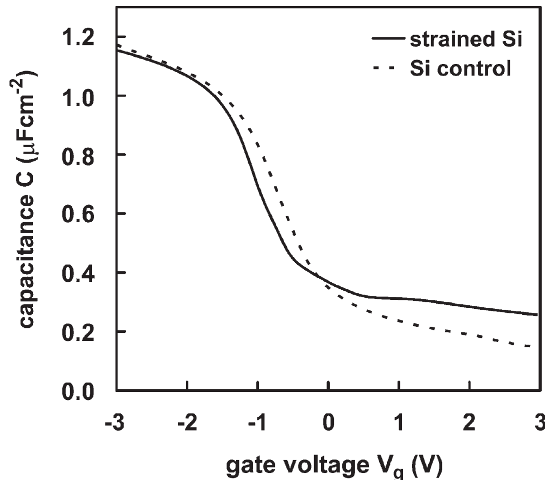

Fig. 10. C–V characteristics for strained Si and Si control MOS capacitors, demonstrating that both devices have the same effective gate oxide thickness (3 nm).

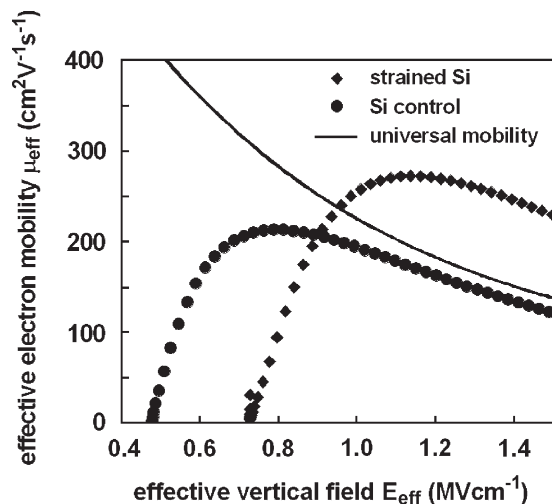

Fig. 11. Mobility-field characteristics for the strained Si and Si control devices determined by split C–V measurements.

to the channel implant dose, whereas use of gate overdrive voltage minimizes the effect of differing threshold voltages in comparisons of current–voltage (I–V) data (Figs. 5, 7, and 8).

The enhanced performance of the strained Si devices arises from the strain-induced energy splitting of the conduction band states. Split C–V was used to measure the effective electron mobility μ_{eff} as a function of the vertical effective field E_{eff}, and the results are presented in Fig. 11. The strained Si electron mobility is enhanced by almost 70% compared with the Si control devices up to vertical effective fields of 1.5 MV $\cdot$ cm^{-1}. In this regime, surface roughness scattering in addition to phonon scattering dominates electron mobility [48]. These results therefore suggest that despite the thin gate oxide, a high-quality strained Si/SiO_2 interface has been formed on the MOSFET devices. The low values of strained Si/SiGe surface roughness will contribute to the smooth strained Si/SiO_2 interface following processing [49]. The Si control data are close to the universal mobility curve for electrons [48] and further confirms successful device processing.

IV. Summary and Conclusion

Strained Si MOSFETs exhibiting significantly enhanced performance compared with their Si control counterparts have been fabricated using thin virtual substrates. A three- to fourfold reduction in the performance degradation commonly observed in conventional thick virtual substrate devices due to SiGe self-heating has been demonstrated. The power dissipation levels considered relate to the 90-nm technology generation. The thermal resistance of thin virtual substrates extracted by ac measurements was found to be four times lower than thick virtual substrates having ten times the virtual substrate thickness, which is in good agreement with analytical estimates for thermal resistance. The improved performance gains in short-gate-length MOSFETs and high-bias conditions have been achieved without compromising the virtual substrate alloy composition. Devices were fabricated using a 3-nm gate oxide and a NiSi process on a $Si_{0.8}Ge_{0.2}$ virtual substrate. Enhancements in I_d, g_m, and mobility for the strained Si devices exceed 70%, and excellent subthreshold characteristics are demonstrated. The cross-wafer uniformity in key electrical parameters is shown to be equivalent for the strained Si and Si control wafers. Good channel strain integrity, low surface roughness, and well-controlled defect density, in addition to reduced self-heating, contribute to the high performance of the strained Si MOSFETs fabricated on thin virtual substrate material.

The scalability of many local strain solutions is presently unclear, and performance gains due to process-induced stressors are relatively modest. The results have shown that providing processing issues due to the presence of Ge and material issues such as misfit dislocations can be addressed, virtual substrate technology can significantly enhance performance in a wide range of applications while avoiding the conventional restrictions due to SiGe device self-heating. Combined with processed-induced stressors, globally strained Si has the potential to play a major role in achieving maximum performance in state-of-the-art devices.

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References

[1] M. V. Fischetti and S. E. Laux, “Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys,” *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, Aug. 1996.
[2] S. Thompson *et al.*, “A 90-nm logic technology featuring strained-silicon,” *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.
[3] A. Shimizu *et al.*, “Local mechanical-stress control (LMC): A new technique for CMOS-performance enhancement,” in *IEDM Tech. Dig.*, 2001, pp. 433–436.
[4] K. Ota *et al.*, “Novel locally strained channel technique for high performance 55 nm CMOS,” in *IEDM Tech. Dig.*, 2002, pp. 27–30.
[5] V. Chan *et al.*, “High speed 45 nm gate length CMOSFETs integrated into a 90 nm bulk technology incorporating strain engineering,” in *IEDM Tech. Dig.*, 2003, pp. 77–80.
[6] C.-H. Ge *et al.*, “Process-strained Si (PSS) CMOS technology featuring 3-D strain engineering,” in *IEDM Tech. Dig.*, 2003, pp. 57–60.

Authorized licensed use limited to: Newcastle University. Downloaded on July 09,2010 at 13:31:31 UTC from IEEE Xplore. Restrictions apply.

[7] S. Dhar, H. Kosina, V. Palankovski, S. E. Ungersboeck, and S. Selberherr, "Electron mobility model for strained Si devices," *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 527–533, Apr. 2005.
[8] O. Weber *et al.*, "Fabrication and mobility characteristics of SiGe surface channel pMOSFETs with a HfO_2/TiN gate stack," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 449–456, Mar. 2006.
[9] M. Kondo *et al.*, "High performance RF power LDMOSFETs for cellular handsets formed in thick-strained-Si/relaxed-SiGe structure," in *IEDM Tech. Dig.*, 2005, pp. 365–368.
[10] O. Weber *et al.*, "Strained Si and Ge MOSFETs with high-*k*/metal gate stack for high mobility dual channel CMOS," in *IEDM Tech. Dig.*, 2005, pp. 137–140.
[11] K. Rim *et al.*, "Characteristics and device design of sub-100 nm strained Si n- and p-MOSFETs," in *VLSI Symp. Tech. Dig.*, 2002, pp. 98–99.
[12] N. Sugii, D. Hisamoto, N. Yokoyama, and S. Kimura, "Performance enhancement of strained-Si MOSFETs fabricated on a chemical–mechanical-polished SiGe substrate," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2237–2243, Dec. 2002.
[13] S. H. Olsen *et al.*, "High performance strained Si/SiGe n-channel MOSFETs fabricated using a novel CMOS architecture," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1961–1969, Sep. 2003.
[14] M. L. Lee and E. A. Fitzgerald, "Strained Si/strained Ge dual-channel heterostructures on relaxed $Si_{0.5}Ge_{0.5}$ for symmetric mobility p-type and n-type metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 80, no. 20, pp. 4202–4204, Jun. 2003.
[15] D. J. Paul, "Silicon–germanium strained layer materials in microelectronics," *Adv. Mater.*, vol. 11, no. 3, pp. 191–204, Mar. 1999.
[16] J. P. Dismukes, L. Ekstrom, E. F. Steigmeiter, I. Kudman, and D. S. Beers, "Thermal and elastic properties of heavily doped Ge–Si alloys up to 1300 K," *J. Appl. Phys.*, vol. 35, no. 10, pp. 2899–2907, 1964.
[17] K. Michelakis *et al.*, "SiGe differential pair," in *Proc. ISCAS*, 2001, pp. 679–682.
[18] E. A. Fitzgerald *et al.*, "Totally relaxed Ge_xSi_{1-x} layers with low threading dislocation densities grown on Si substrates," *Appl. Phys. Lett.*, vol. 59, no. 7, pp. 811–813, Aug. 1991.
[19] J. M. Hartmann, B. Gallas, J. Zhang, and J. J. Harris, "Gas-source molecular beam epitaxy of SiGe virtual substrates—II: Strain relaxation and surface morphology," *Semicond. Sci. Technol.*, vol. 15, no. 4, pp. 370–377, Apr. 2000.
[20] T. Hackbarth *et al.*, "Reduced self-heating in Si/SiGe field-effect transistors on thin virtual substrates prepared by low-energy plasma-enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 83, no. 26, pp. 5464–5466, 2003.
[21] E. Kasper, K. Lyutovich, M. Bauer, and M. Oehme, "New virtual substrate concept for vertical MOS transistors," *Thin Solid Films*, vol. 336, no. 1/2, pp. 319–322, Dec. 1998.
[22] M. Bauer *et al.*, "Relaxed SiGe buffers with thicknesses below 0.1 μm," *Thin Solid Films*, vol. 369, no. 1/2, pp. 152–156, Jul. 2000.
[23] K. Lyutovich *et al.*, "Thin SiGe buffers with high Ge content for n-MOSFETs," *Mater. Sci. Eng. B*, vol. 89, no. 1–3, pp. 341–345, Feb. 2002.
[24] E. Kasper and K. Lyutovich, "Strain adjustment with thin virtual substrates," *Solid State Electron.*, vol. 48, no. 8, pp. 1257–1263, Aug. 2004.
[25] T. Hackbarth *et al.*, "High frequency n-type MOSFETs on ultra-thin virtual SiGe substrates," *Solid State Electron.*, vol. 47, no. 7, pp. 1179–1182, Jul. 2003.
[26] K. Sawano *et al.*, "Fabrication of high-quality strain-relaxed thin SiGe layers on ion-implanted Si substrates," *Appl. Phys. Lett.*, vol. 85, no. 13, pp. 2514–2516, Sep. 2004.
[27] R. Delhougne, P. Meunier-Beillard, M. Caymax, R. Loo, and W. Vanderworst, "Development of a new type of SiGe thin strain relaxed buffer based on the incorporation of a carbon-containing layer," *Appl. Surf. Sci.*, vol. 224, no. 1–4, pp. 91–94, Mar. 2004.
[28] D.-L. Mei *et al.*, "Fabrication of strained Si channel PMOSFET on thin relaxed $Si_{1-x}Ge_x$ virtual substrate," *Microelectron. J.*, vol. 35, no. 12, pp. 969–971, Dec. 2004.
[29] G. Eneman *et al.*, "Fabrication of strained Si NMOS transistors on thin buffer layers with selective and non-selective epitaxial growth techniques," *Mater. Sci. Semicond. Process.*, vol. 8, no. 1–3, pp. 337–342, Feb.–Jun. 2005.
[30] A. Oishi *et al.*, "High performance CMOSFET technology for 45 nm generation and scalability of stress-induced mobility enhancement techniques," in *IEDM Tech. Dig.*, 2005, pp. 232–239.
[31] J. W. P. Hsu, E. A. Fitzgerald, Y. H. Xie, P. J. Silverman, and M. J. Cardillo, "Surface morphology of related Ge_xSi_{1-x} films," *Appl. Phys. Lett.*, vol. 61, no. 11, pp. 1293–1295, Sep. 1992.
[32] S. Y. Shiryaev, F. Jensen, and J. W. Petersen, "On the nature of cross-hatch patterns on compositionally graded $Si_{1-x}Ge_x$ alloy layers," *Appl. Phys. Lett.*, vol. 64, no. 24, pp. 3305–3307, Jun. 1994.
[33] PeakFit Software, Aspire Software International. [Online]. Available: www.aspiresoftwareintl.com
[34] P. Dobrosz, S. J. Bull, S. H. Olsen, and A. G. O'Neill, "The use of Raman spectroscopy to identify strain and strain relaxation in strained Si/SiGe structures," *Surf. Coatings Technol.*, vol. 200, no. 5/6, pp. 1755–1760, Nov. 2005.
[35] K. Lyutovich, J. Werner, M. Oehme, E. Kasper, and T. Perova, "Characterisation of virtual substrates with ultra-thin $Si_{0.6}Ge_{0.4}$ strain relaxed buffers," *Mater. Sci. Semicond. Process.*, vol. 8, no. 1–3, pp. 149–153, Feb.–Jun. 2005.
[36] D. G. Schimmel, "Defect etch for (100) silicon evaluation," *J. Electrochem. Soc.*, vol. 126, no. 3, pp. 479–483, Mar. 1979.
[37] S. H. Olsen *et al.*, "Study of strain relaxation in Si/SiGe metal–oxide–semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 97, no. 11, pp. 114504-1–114504-9, 2005.
[38] International Technology Roadmap for Semiconductors. (2005). [Online]. Available: www.itrs.net
[39] J. Seger *et al.*, "Influence of a Si layer intercalated between $Si_{0.75}Ge_{0.25}$ and Ni on the behavior of the resulting $NiSi_{1-u}Ge_u$ film," *J. Appl. Phys.*, vol. 96, no. 12, pp. 7179–7182, Dec. 2004.
[40] S. H. Olsen *et al.*, "Optimization of alloy composition for high performance strained Si/SiGe n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1156–1162, Jul. 2004.
[41] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, J. T. Bunyan, and M. J. Uren, "Self-heating effects in SOI MOSFET's and their measurement by small signal conductance techniques," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996.
[42] K. A. Jenkins and K. Rim, "Measurement of the effect of self-heating in strained-silicon MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 360–362, Jun. 2002.
[43] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Fabrication and analysis of deep submicron strained-Si n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1406–1415, Jul. 2000.
[44] N. R. Zangenberg, J. Fage-Pederson, J. L. Hansen, and A. N. Larsen, "Boron and phosphorus diffusion in strained and relaxed Si and SiGe," *J. Appl. Phys.*, vol. 94, no. 6, pp. 3883–3890, Sep. 2003.
[45] J. G. Fiorenza *et al.*, "Film thickness constraints for manufacturable strained Si CMOS," *Semicond. Sci. Technol.*, vol. 19, no. 1, pp. L4–L8, Jan. 2004.
[46] T. Perova *et al.*, "Micro-Raman investigations of the degree of relaxation in thin SiGe buffer layers with high Ge content," *J. Mater. Sci., Mater. Electron.*, vol. 14, no. 5–7, pp. 441–444, May 2003.
[47] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.
[48] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's—Part I: Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.
[49] S. H. Olsen *et al.*, "Impact of virtual substrate quality on performance enhancements in strained Si/SiGe heterojunction n-channel MOSFETs," *Solid State Electron.*, vol. 47, no. 8, pp. 1289–1295, Aug. 2003.

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