Control of Three-Phase, Four-Wire PWM Rectifier

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***Abstract*—This paper presents the analysis, design, and control of a four-wire rectifier system using split-capacitor topology. The proposed controller does not require any complex transformation or input voltage sensing. A detailed analysis of the distortions in the line and the neutral currents is presented. It is shown that the single-carrier-based, conventional sine-triangle PWM (CSPWM) scheme results in a peak-to-peak neutral current ripple, which is greater than the peak-to-peak ripple of any of the line currents. Also, for the same operating condition, the distortions in the line and the neutral currents increase considerably, when a three-limb boost inductor is used instead of three single-phase inductors. A three-carrier-based SPWM scheme is proposed in this paper. Compared to CSPWM, the proposed scheme significantly reduces the neutral current ripple when three single-phase inductors are used, and reduces both line and neutral current ripples when a three-limb inductor is used. The control scheme is verified through Matlab simulation. It is implemented on an field-programmable gate-array (FPGA)-based digital controller and tested on a prototype. Simulation and experimental results are presented.**

***Index Terms*—AC-DC power conversion, boost rectifier, current control, digital control, four-wire converter, harmonic analysis, harmonic distortion, neutral current, sine-triangle PWM.**

I. Introduction

In an electrical power distribution system, electrical power is typically distributed through three-phase, four-wire networks. Because of the ever-increasing computer loads, the loads supplied by the utility are increasingly of single-phase and nonlinear nature. While critical loads such as computers require well-regulated and sinusoidal voltages to be applied, these draw distorted currents from the mains at a poor power factor. Consequently, the line currents in the distribution system contain considerable lower order harmonics, the neutral wire carries excessive current, and the system operates at low input power factor. These cause considerable overheating in the neutral wire and in the distribution transformer supplying the load [1]–[3].

The computer loads could be fed from the mains through a three-phase ac–dc–ac converter [4]–[7], drawing sinusoidal currents from the mains at a high power factor and maintaining regulated and sinusoidal voltages at the output.

The above three-phase line conditioner comprises two back-to-back connected three-phase converters. The conditioner must have a four-wire output to feed several single-phase loads connected at its output. The output neutral must be connected to the mains neutral to facilitate earth fault protection for the loads and to stabilize the potential of the output neutral with respect to the potential of the source neutral [6]–[8]. The latter is absolutely essential as the load enclosures are grounded at the source neutral [8].

Both the front-end converter and the inverter could be a three-leg converter. The source and the load neutrals could be connected to the star-point of the secondary windings of an isolation transformer, whose primary is fed from the inverter [4].

Alternatively, to avoid the requirement of an isolation transformer, three-leg converters with split dc bus capacitors could be considered [5], [6]. The mains and the load neutrals could be connected to the midpoint of the dc bus. Another option is to have an additional leg in one of the two converters and to connect the two neutrals to the midpoint of this additional leg [7]. The relative merits and demerits of the two topologies have been discussed in [9], [10]. This paper deals with the analysis, design, and control of a three-leg converter with split dc bus [11], [12], which can be used as a four-wire front-end converter in three-phase transformerless line conditioner and UPS applications [5], [6].

A number of control techniques have been reported for three-phase ac–dc converters [6], [10]–[19]. Most of them require complex transformations, PLL [20], and a number of voltage and current sensors. As a result, the associated control scheme becomes complex and its implementation requires large computational power.

Addressing the above issues, the indirect current control scheme has been reported for three-wire rectifier [21] and single-phase, half-bridge rectifier [22], which do not require input voltage sensing. This paper extends the above concept to four-wire PWM rectifier with the split-capacitor topology [11]. Various issues such as balancing the two halves of the dc bus and maintaining low neutral current are addressed.

The control schemes presented in [5] and [6] use a conventional sine-triangle PWM (CSPWM) scheme to generate the gating pulses for the converter switches. The three sinusoidal voltage references are compared with a common high-frequency triangular carrier. In this paper, it is shown that the above PWM scheme results in a peak-to-peak neutral current ripple greater than the peak-to-peak ripple in the line currents. A three-carrier-based SPWM scheme is proposed, which considerably reduces the rms ripple in the neutral current compared to the CSPWM scheme.

In three-phase application, a three-limb inductor is more widely used than three single-phase inductors due to cost, size and weight considerations [23], [24]. A recent publication [24] shows that the zero-sequence circulating current characteristics of parallel three-phase inverters change drastically, when a three-limb inductor replaces three single-phase inductors. In the

Manuscript received September 29, 2006; revised March 22, 2007. Recommended for publication by Associate Editor S. Choi.

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Digital Object Identifier 10.1109/TPEL.2007.911783

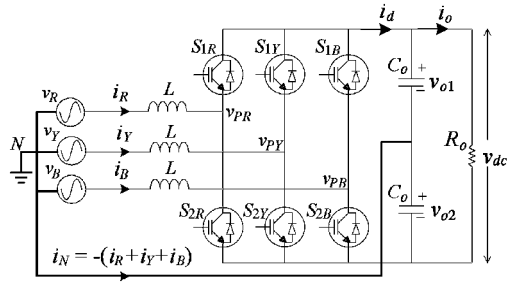

Fig. 1. Three-phase, four-wire PWM rectifier.

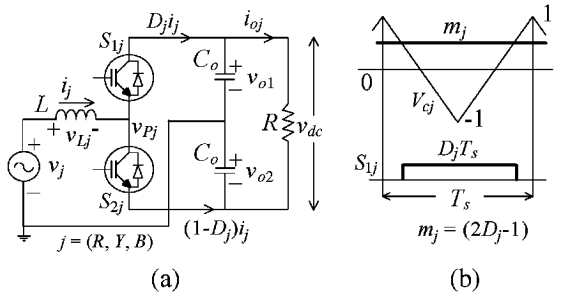

Fig. 2. (a) Single-phase half-bridge rectifier and (b) sine-triangle modulation scheme.

present work, it is shown that the switching-frequency ripples in the line and neutral currents of a four-wire converter, with the CSPWM scheme, increase considerably with the above change. It is also shown that, in addition to reducing the neutral current distortion, the proposed SPWM scheme effectively reduces the line current distortion when a three-limb boost inductor is used.

The proposed control scheme and the SPWM scheme are simulated in Matlab/Simulink. These are implemented on an field-programmable gate-array (FPGA)-based digital controller [25] and validated experimentally on a laboratory scale prototype. Simulation and experimental results are presented.

II. Analysis and Control

This section presents the proposed control scheme for the four-wire rectifier. The analysis of the four-wire rectifier with the proposed method of control is also presented.

A. Proposed Control Scheme

A four-wire PWM rectifier is shown in Fig. 1. For the purpose of analysis, it can be regarded as three independent single-phase half-bridge rectifiers [22], sharing a common dc bus. Fig. 2(a) shows the jth phase half-bridge rectifier.

The four-wire rectifier is controlled such a way that its jth phase averaged input current I_j is proportional to the jth phase input voltage v_j as shown in (1), where $j = R, Y, B$, and R_e is the emulated resistance of the converter [22]. Consequently, the rectifier draws balanced and sinusoidal currents from the supply mains, when the input voltages are balanced and sinusoidal

$$I_j = v_j/R_e. \tag{1}$$

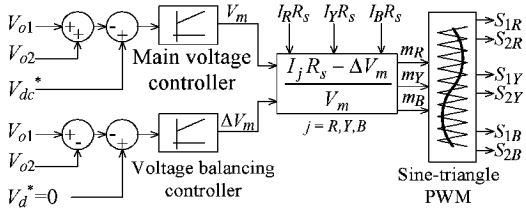

Fig. 3. Block diagram of the proposed control scheme.

In each switching cycle T_s, the switches S_{1j} and S_{2j} are operated with complementary gating pulses of duty ratios D_j and $(1 - D_j)$, respectively. The switching-cycle averaged pole voltage V_{Pj} is as shown in (2), where the averaged voltage drops across the inductors L are neglected and $V_d = V_{o1} - V_{o2}$. Equations (1) and (2) yield (3), where R_s is the current sensing gain [22]

$$V_{Pj} = V_{\rm dc}(2D_j - 1)/2 + V_d/2 \approx v_j \tag{2}$$

$$I_j R_s = \frac{V_{\rm dc} R_s}{2R_e}(2D_j - 1) + \frac{V_d R_s}{2R_e}. \tag{3}$$

A voltage controller is used to control the output voltage $V_{\rm dc}$ and another to maintain balance between V_{o1} and V_{o2} (see Fig. 3). The two controller outputs are defined in (4) and (5), respectively [22]. Equations (3)–(5) yield (6)

$$V_m = V_{\rm dc} R_s/(2R_e) \tag{4}$$

$$\Delta V_m = V_d R_s/(2R_e) \tag{5}$$

$$D_j = \frac{1}{2}\left(1 + \frac{I_j R_s - \Delta V_m}{V_m}\right). \tag{6}$$

A sine-triangle PWM scheme may be used to generate the gating pulses for the switch S_{1j} as shown in Fig. 2(b), where V_{cj} is the$j$th phase triangular carrier and m_j is the jth phase pole voltage reference as shown in (7). Using (2), (6), and (7), the voltage V_{Pj} is expressed as shown in (8)

$$m_j = 2D_j - 1 = \frac{I_j R_s - \Delta V_m}{V_m} \tag{7}$$

$$V_{Pj} = m_j\left(\frac{V_{\rm dc}}{2}\right) + \frac{V_d}{2} = \left(\frac{I_j R_s - \Delta V_m}{V_m}\right)\frac{V_{\rm dc}}{2} + \frac{V_d}{2}. \tag{8}$$

The block diagram of the proposed control scheme is shown in Fig. 3. It should be noted that due to neutral connection, the use of conventional space vector PWM for better utilization of the dc bus must be avoided [11].

Since the proposed controller does not use any input voltage sensor/estimator, PLL, current controller and complex transformation, it is much simpler than the conventional controllers presented in [6] and [13]–[18]. Consequently, its implementation would require less computational power than the above schemes.

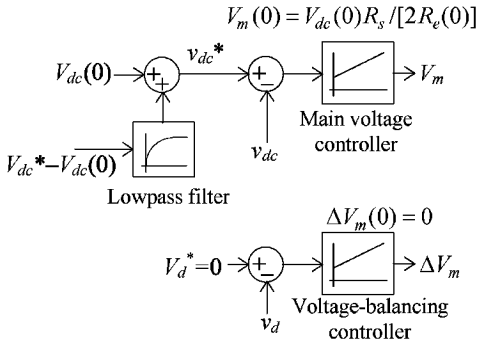

Fig. 4. Proposed soft startup algorithm.

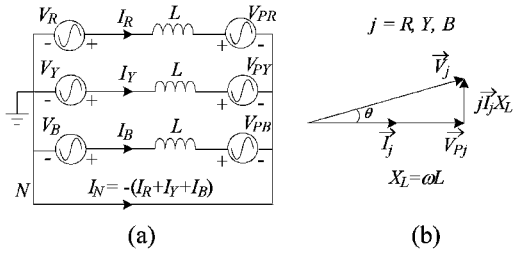

Fig. 5. (a) Averaged model of the input side of the rectifier and (b) its phasor representation.

B. Soft Startup Scheme

A boost rectifier draws abnormal line currents from the supply mains during startup, when its dc bus is uncharged and the initial average pole voltage is substantially different from the mains voltage. In order to prevent this, the dc bus is precharged up to a voltage $V_{\rm dc}(0)$ (usually the peak line voltage) and the initial average pole voltage is decided based on the measured input voltage before the control pulses to the devices are released.

Unlike the conventional controller [6], the input voltage is not measured in the proposed control scheme. Let us assume that the initial conditions for $V_{\rm dc}$, V_d, V_m, and ΔV_m at the instant of releasing the gating pulses are $V_{\rm dc}(0)$, zero, $V_m(0)$, and zero, respectively. With this, the jth phase input side of the four-wire rectifier may be represented by (9) for the first few switching cycles, where $R_e(0)$ is the initial emulated resistance as shown in (10) [see (8)]

$$L\frac{dI_j}{dt} + R_e(0)I_j = v_j \tag{9}$$

$$R_e(0) = \frac{V_{\rm dc}(0)R_{\rm s}}{2V_m(0)}. \tag{10}$$

It can be seen from (9) that irrespective of the power rating of the converter, the starting current can be limited by choosing a high-valued $R_e(0)$. Since the initial condition for V_m cannot be set at zero [see (7)], it must be selected to be small to keep $R_e(0)$ high.

Further, the charging rate of the dc bus can be controlled to charge the dc bus capacitor slowly from $V_{\rm dc}(0)$ to $V_{\rm dc}^*$ over a period of few seconds after releasing the gating pulses. This can be achieved by varying the reference voltage $v_{\rm dc}^*$ gradually from $V_{\rm dc}(0)$ to $V_{\rm dc}^*$ using a lowpass filter as shown in Fig. 4. The desired initial conditions for V_m and ΔV_m are shown in Fig. 4. Further details are given in Section VI, where an experimental verification of the soft startup scheme is presented.

C. Averaged Input Characteristics

Fig. 5(a) shows the averaged input side model of the rectifier. At steady state, both ΔV_m and V_d corresponding to the jth phase are close to zero, and V_m is a constant [see Section II-D]. As a result, the pole voltage V_{Pj} is in phase with its respective line current I_j as shown in Fig. 5(b). If the average voltage drop across L is considered, unlike in (2), then the source voltage v_j is as shown in Fig. 5(b).

The corresponding input power factor is given in (11), where V_R and V_{P1} are the rms values of v_j and V_{Pj}, respectively, and P_o is the output power. The power factor is load dependent but close to unity as seen from

$$\cos\theta = \frac{V_{P1}}{V_R} = \cos\left(\frac{1}{2}\sin^{-1}\left(\frac{2P_oX_L}{3V_R^2}\right)\right). \tag{11}$$

D. DC Bus Voltage-Imbalance

The dc side of the rectifier shown in Fig. 2(a) may be represented by (12) and (13), where R_c is the equivalent shunt resistance of the capacitors C_o. Equations (12) and (13) yield (14), where $\tau = R_CC_o$ and $v_d = v_{o1} - v_{o2}$

$$C_o\dot{v}_{o1} = D_jI_j - \frac{v_{o1}}{R_c} - \frac{v_{o1}+v_{o2}}{R} \tag{12}$$

$$C_o\dot{v}_{o2} = -(1-D_j)I_j - \frac{v_{o2}}{R_c} - \frac{v_{o1}+v_{o2}}{R} \tag{13}$$

$$\dot{v_d} + \frac{1}{\tau}v_d = \frac{I_j}{C_o}. \tag{14}$$

The actual averaged input current might contain a small dc offset $I_{o1(\rm ss)}$ at steady state as shown in (15) due to various asymmetries in the system as pointed out in [26]–[28]

$$I_j = I_m\sin\omega t - I_{o1(\rm ss)}. \tag{15}$$

The effect of the above offset current on the output voltage imbalance is shown in (16), where $V_d(0)$ is the initial voltage imbalance at $t = 0$, $\phi = \tan^{-1}(\omega\tau)$ and $\omega\tau \gg 1$ [27]. At steady state, the first term in the RHS of (16) does not decay, when R_c is neglected (i.e., $R_c = \infty$) [27]. However, it decays to zero, when R_c is considered to be finite. The second term in the RHS of (16) causes a sinusoidal ripple in v_d, while the last term causes a steady-state dc voltage imbalance $V_{d(\rm dc,ss)} = -I_{o1(\rm ss)}R_{\rm c}$

$$v_d(t) = \left[V_d(0) + \frac{I_m}{\omega C_o}\right]e^{\frac{-t}{\tau}} + \frac{I_m}{\omega C_o}\sin(\omega t - \phi) - I_{o1(\rm ss)}R_c\left[1 - e^{\frac{-t}{\tau}}\right]. \tag{16}$$

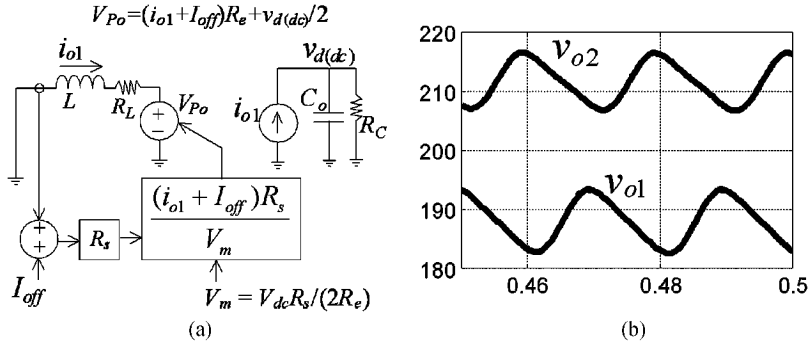

Fig. 6. (a) Dc equivalent model of the R-phase of the rectifier system and (b) simulated dc bus voltage imbalance.

TABLE I
PARAMETERS AND COMPONENTS OF THE SYSTEM

P_o	1600W	C_o	2200μF
V_R	110V	R_s	1/10Ω
V_{o1}, V_{o2}	200V	f_{sw}	10kHz
f	50Hz	R_c	10000Ω
Single-phase inductor	$L_d = L_c$ = 8.6mH	Three-limb inductor	L_d = 8.2mH L_c = 0.132 L_d

The steady offset current $I_{o1(\mathrm{ss})}$ may be due to error in current measurement among the possible causes [26]–[28]. A small offset I_{off} due to the current sensor causes a corresponding offset in V_{Pj} as per (8). The effect of I_{off} on voltage imbalance can be studied using the dc equivalent model of the R-phase of the rectifier (without any voltage balancing mechanism) shown in Fig. 6(a). Here V_{Po} is the averaged pole voltage due to offset $(i_{o1} + I_{\mathrm{off}})$ as shown in Fig. 6(a). Further, $v_{d(\mathrm{dc})}$ is the line-cycle average of v_d and R_L is the resistance of L. The above system may be represented by (17). The steady state values of i_{o1} and $v_{d(dc)}$ are shown in (18) and (19), respectively, where $R_c \gg R_e$ and $R_e \gg R_L$

$$\begin{bmatrix} \dot{i}_{o1} \\ \dot{v}_{d(\mathrm{dc})} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+R_c)}{L} & \frac{-1}{2L} \\ \frac{1}{C_o} & \frac{-1}{R_cC_o} \end{bmatrix} \begin{bmatrix} i_{o1} \\ v_{d(\mathrm{dc})} \end{bmatrix} + \begin{bmatrix} \frac{-R_e}{L} \\ 0 \end{bmatrix} I_{\mathrm{off}} \quad (17)$$

$$I_{o1(\mathrm{ss})} \approx -(2R_e/R_c)I_{\mathrm{off}} \quad (18)$$

$$V_{d(\mathrm{dc,ss})} \approx -(2R_e)I_{\mathrm{off}}. \quad (19)$$

The above analysis is also verified through simulation. The R-phase of the rectifier system, without closing the voltage-balancing loop, is simulated in Matlab with the following parameters: $P_o = 500$ W, $R_c = 10$ kΩ, $I_{\mathrm{off}} = 0.5$ A, $L = 8.6$ mH, $R_L = 0.5$ Ω and $V_{\mathrm{dc}}^* = 400$ V (other parameters are shown in Table I). The corresponding emulated resistance R_e is 24 Ω. Fig. 6(b) shows the steady-state output voltage waveforms, where the dc voltage imbalance $V_{d(\mathrm{dc,ss})}$ is found to be −24 V. This may also be obtained using (19).

In the proposed scheme, the dc bus voltage imbalance is corrected by adding a dc component ΔV_m in the averaged pole voltages V_{Pj} [see (8)]. This circulates suitable dc currents through the lines, and hence through the neutral, to compensate for the voltage imbalance due to various system asymmetries. The steady-state value of $\Delta V_m \approx I_{o1(\mathrm{ss})}R_s$ is close to zero.

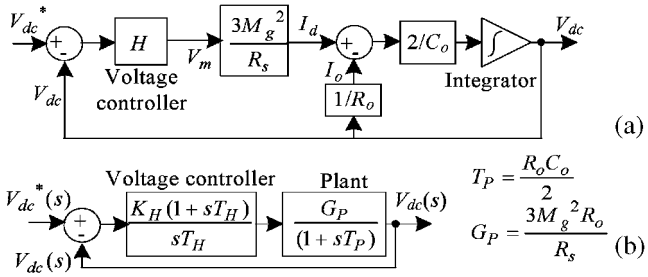

Fig. 7. Main voltage loop: (a) averaged model and (b) frequency domain model.

E. Voltage Loops

Using (4) and the input-output power balance, the averaged dc bus current I_d corresponding to a given V_m is obtained as shown in (20), where $M_g = \sqrt{2}V_R/V_{\mathrm{dc}}$

$$I_d = \left(\frac{3M_g^2}{R_s}\right) V_m. \quad (20)$$

Using (20), and Figs. 1 and 3, the averaged and the frequency domain models of the main voltage loop, which controls V_{dc}, are derived. These are shown in Fig. 7(a) and (b), respectively. Fig. 6(a) may be used to obtain the averaged voltage-balancing loop and its frequency domain model shown in Fig. 8(a) and (b), respectively. The above models are useful in selection of controller parameters for the voltage loops.

III. PWM WITH PHASE-SHIFTED CARRIERS

The rms ripple in the neutral current must be maintained low to reduce EMI and overall system losses [1]–[3]. The instan-

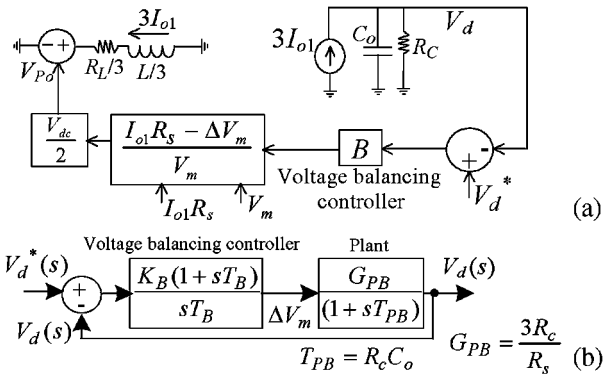

Fig. 8. Voltage-balancing loop: (a) averaged model and (b) frequency domain model.

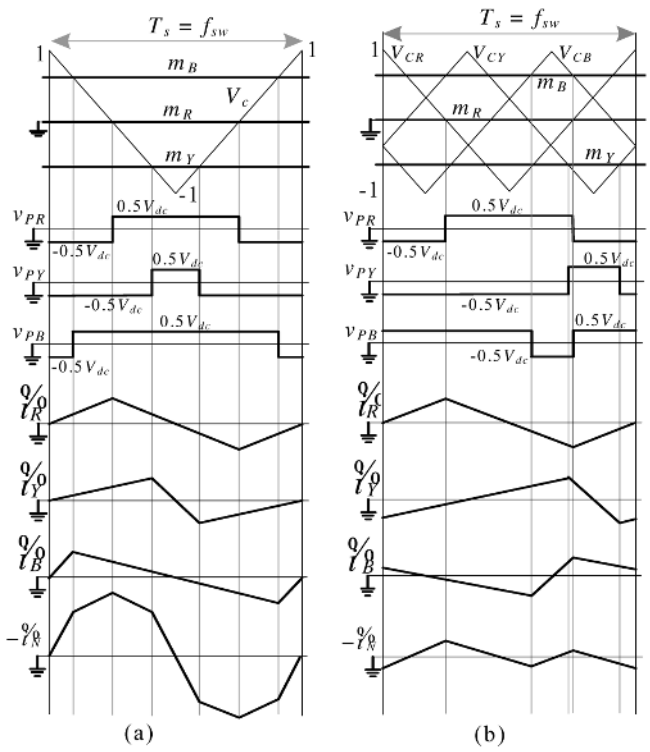

Fig. 9. (a) Conventional sine-triangle PWM scheme and (b) proposed sine-triangle PWM scheme.

taneous neutral current i_N is as shown in Fig. 1. Though the averaged neutral current in a balanced system is zero, the instantaneous neutral current contains switching-frequency ripple as follows:

$$i_N = \widetilde{i}_N = -(\widetilde{i}_R + \widetilde{i}_Y + \widetilde{i}_B). \tag{21}$$

Fig. 9(a) shows the CSPWM scheme, where the pole voltage references m_R, m_Y and m_B are compared with a common triangular carrier V_c to generate the gating pulses for the converter switches [6]. The ripples in the three line currents over a switching cycle T_s are as shown in Fig. 9(a). The current ripples in the three phases are of the same sign in a given half carrier cycle. Hence, the three get added up, resulting in a high neutral current ripple as seen from Fig. 9(a).

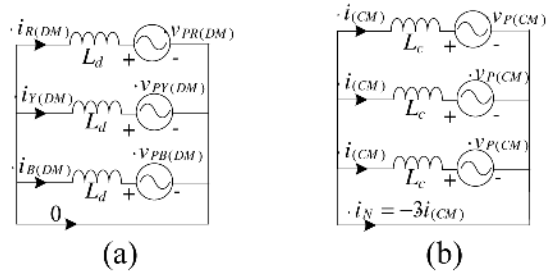

Fig. 10. (a) Differential mode ripple equivalent circuit and (b) common mode ripple equivalent circuit.

To reduce the neutral current ripple, it must be ensured that not all three line current ripples are of the same sign at a given instant. This is easily achieved by using three carriers, shifted in phase by 120° at the carrier frequency, as shown in Fig. 9(b). Compared to Fig. 9(a), there is significant reduction in the neutral current ripple as can be seen in Fig. 9(b). The effect of using phase-shifted carriers on the individual line current ripple is negligible.

It should be noted that in three-phase application, the study of single-carrier PWM versus phase-shifted, three-carrier PWM has been reported by numerous researchers [29], [30]. Since the main focus has been on minimizing the line current distortion in three-wire applications in these works, the single-carrier PWM has been found to be better than three-carrier PWM. However, in case of four-wire application, the three-carrier PWM is seen to be more effective than the single-carrier PWM in terms of neutral current distortion as seen qualitatively from Fig. 9.

Further analysis could be done considering the ripple in the instantaneous pole voltage v_{Pj}, which causes the ripples in the line and neutral currents. The voltage v_{Pj} is as shown in (22), where the switching function S_{1j} equals one, if the top device of jth phase is on or equals zero, if the bottom device is on. Also, in (22), $\widetilde{v}_{Pj}$ is the ripple in the pole voltage v_{Pj}, respectively

$$v_{Pj} = (2S_{1j} - 1)V_{\rm dc}/2 = V_{Pj} + \widetilde{v}_{Pj}. \tag{22}$$

Similar to the line current ripples, the instantaneous sum of the ripples of the three pole voltages is nonzero. For the purpose of analysis, the jth phase ripple quantities $\widetilde{v}_{Pj}$ and $\widetilde{i}_j$ can be divided into a common mode and a differential mode components, $[\widetilde{v}_{P(\rm CM)}, \widetilde{v}_{Pj(\rm DM)}]$ and $[\widetilde{i}_{(\rm CM)}, \widetilde{i}_{j(\rm DM)}]$ as shown in (23) and (24), respectively [31]

$$\begin{aligned} \widetilde{v}_{P(\rm CM)} &= (\widetilde{v}_{PR} + \widetilde{v}_{PY} + \widetilde{v}_{PB})/3 \\ \widetilde{v}_{Pj(\rm DM)} &= \widetilde{v}_{Pj} - \widetilde{v}_{P(\rm CM)} \end{aligned} \tag{23}$$

$$\begin{aligned} \widetilde{i}_{(\rm CM)} &= (\widetilde{i}_R + \widetilde{i}_Y + \widetilde{i}_B)/3 \\ \widetilde{i}_{j(\rm DM)} &= \widetilde{i}_j - \widetilde{i}_{(\rm CM)}. \end{aligned} \tag{24}$$

The ripples $\widetilde{v}_{Pj(\rm DM)}$ and $\widetilde{v}_{P(\rm CM)}$ cause the ripple currents $\widetilde{i}_{j(\rm DM)}$ and $\widetilde{i}_{(\rm CM)}$ as shown in Fig. 10(a) and (b), respectively, where L_d and L_c are the differential mode and the common mode inductances offered by the inductors L (see Fig. 1) to

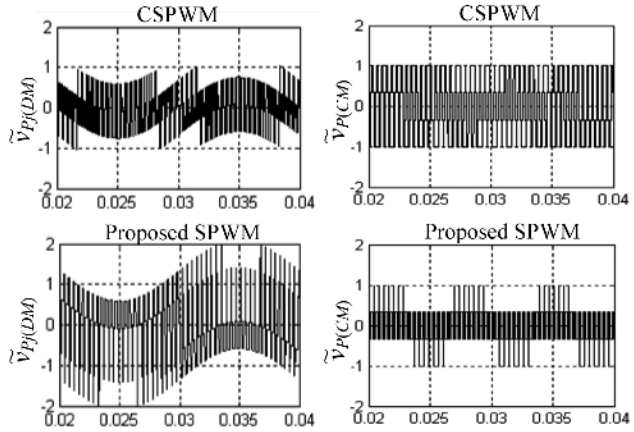

Fig. 11. Simulated waveforms of differential mode and common mode ripple voltages for $M = 0.75$ and $f_{sw} = 2.5$ kHz.

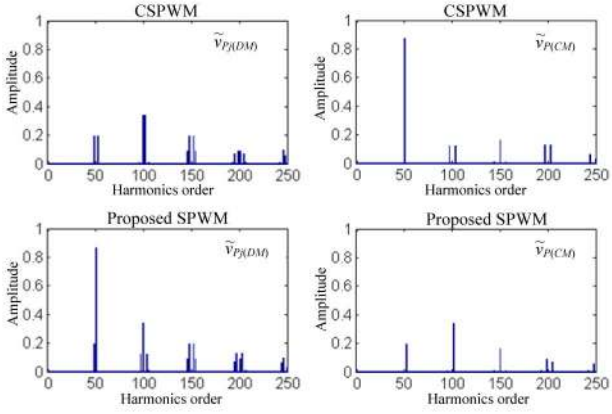

Fig. 12. Simulated spectra of differential mode and common mode ripple voltages for $M = 0.75$ and $f_{sw} = 2.5$ kHz.

$\widetilde{i}_{j(\mathrm{DM})}$ and $\widetilde{i}_{(\mathrm{CM})}$, respectively. The ripple $\widetilde{i}_{(\mathrm{CM})}$ determines the neutral current as shown in

$$i_N = -3\widetilde{i}_{(\mathrm{CM})}. \tag{25}$$

The ripple voltages $\widetilde{v}_{Pj(\mathrm{DM})}$ and $\widetilde{v}_{P(\mathrm{CM})}$ depend on the carrier frequency f_{sw}, peak-to-peak carrier, V_{dc} and m_j. A three-phase, two-level voltage source inverter using both CSPWM and the proposed SPWM schemes is simulated in Matlab. The parameters are as follows: $V_{\mathrm{dc}} = 2$ p.u., peak-to-peak carrier $= V_{\mathrm{dc}}/2$ p.u., $f = 50$ Hz, $m_j = M\sin(\omega t - \phi_j)$p.u., $\phi_R = 0°$, $\phi_Y = 120°$, $\phi_B = 240°$ and $V_{P1} = M/\sqrt{2}$. Fig. 11 shows the waveforms of $\widetilde{v}_{Pj(\mathrm{DM})}$ and $\widetilde{v}_{P(\mathrm{CM})}$ over a line cycle for $M = 0.75$ and $f_{sw} = 2.5$ kHz. The corresponding harmonic spectra are shown in Fig. 12. As seen from the left column of Fig. 12, the dominant differential mode component due to the proposed SPWM is much higher than the corresponding component due to CSPWM. On the other hand, as seen from the right column of the figure, the dominant common mode component due to CSPWM is much higher than the corresponding component due to the proposed SPWM. Thus, the proposed SPWM leads to higher differential mode distortion, but lower common mode distortion, compared to CSPWM. Further, it is seen from Fig. 12 that both $\widetilde{v}_{Pj(\mathrm{DM})}$ and $\widetilde{v}_{P(\mathrm{CM})}$ have components around f_{sw} and its multiples. However, the two do not contain harmonics of the same order. The ripple currents $\widetilde{i}_{j(\mathrm{DM})}$ and $\widetilde{i}_{(\mathrm{CM})}$ have components at the same frequencies as those of $\widetilde{v}_{Pj(\mathrm{DM})}$ and $\widetilde{v}_{P(\mathrm{CM})}$, respectively.

The input current total harmonic distortion factor (THD) I_{THD} is as shown in (26), where $I_{\mathrm{THD(DM)}}$ and $I_{\mathrm{THD(CM)}}$ are the THD components contributed by $\widetilde{i}_{j(\mathrm{DM})}$ and $\widetilde{i}_{(\mathrm{CM})}$, respectively, as shown in (27). Further, in (27), I_{R1} is the rms value of the fundamental component of the line currents, $\widetilde{I}_{j(\mathrm{DM})k}$, $\widetilde{I}_{(\mathrm{CM})k}$, $\widetilde{V}_{Pj(\mathrm{DM})k}$ and $\widetilde{V}_{P(\mathrm{CM})k}$ are the rms values of the kth harmonic components of $\widetilde{i}_{j(\mathrm{DM})}$, $\widetilde{i}_{(\mathrm{CM})}$, $\widetilde{v}_{Pj(\mathrm{DM})}$ and $\widetilde{v}_{P(\mathrm{CM})}$, respectively, $X_d = \omega L_d$, $X_c = \omega L_c$, $\omega = 2\pi f$ rad/s, and $V_{\mathrm{WTHD(DM)}}$, and $V_{\mathrm{WTHD(CM)}}$ are the weighted THD (WTHD) components of v_{Pj} as shown in (28). The rms neutral current I_N may be normalized with respect to I_{R1} as shown in (29)

$$I_{\mathrm{THD}} = \sqrt{I^2_{\mathrm{THD(DM)}} + I^2_{\mathrm{THD(CM)}}} \tag{26}$$

$$\begin{aligned} I_{\mathrm{THD(DM)}} &= \sqrt{\sum_{k=2}^{\infty}\left(\frac{\widetilde{I}_{j(\mathrm{DM})k}}{I_{R1}}\right)^2} \\ &= \left(\frac{V_{P1}}{X_d I_{R1}}\right) V_{\mathrm{WTHD(DM)}} \\ I_{\mathrm{THD(CM)}} &= \sqrt{\sum_{k=2}^{\infty}\left(\frac{\widetilde{I}_{(\mathrm{CM})k}}{I_{R1}}\right)^2} \\ &= \left(\frac{V_{P1}}{X_c I_{R1}}\right) V_{\mathrm{WTHD(CM)}} \end{aligned} \tag{27}$$

$$\begin{aligned} V_{\mathrm{WTHD(DM)}} &= \sqrt{\sum_{k=2}^{\infty}\left(\frac{\widetilde{V}_{Pj(\mathrm{DM})k}}{kV_{P1}}\right)^2} \\ V_{\mathrm{WTHD(CM)}} &= \sqrt{\sum_{k=2}^{\infty}\left(\frac{\widetilde{V}_{P(\mathrm{CM})k}}{kV_{P1}}\right)^2} \end{aligned} \tag{28}$$

$$I_N/I_{R1} = 3I_{\mathrm{THD(CM)}}. \tag{29}$$

Equations (26)–(29) show that for a particular set of I_{R1}, V_{P1}, X_d and X_c, the line and neutral current distortions can be estimated from the weighted THD's $V_{\mathrm{WTHD(DM)}}$ and $V_{\mathrm{WTHD(CM)}}$. Fig. 13 shows the $V_{\mathrm{WTHD(DM)}}$ and $V_{\mathrm{WTHD(CM)}}$ as obtained through simulation for different values of M and f_{sw}. Compared to CSPWM, the proposed SPWM increases the differential mode voltage distortion, while decreasing the common mode voltage distortion. The overall WTHD of the pole voltages, however, remains practically the same.

Let us consider an example, where $V_{P1} \approx V_R$ [see Fig. 5(b)], $L_d = L_c = 8.6$ mH and the other parameters are as shown in Table I. The estimated line and neutral current distortions are tabulated in Table II. It can be seen that the differential mode current distortion is higher under proposed SPWM scheme, while the common mode current distortion is higher in CSPWM

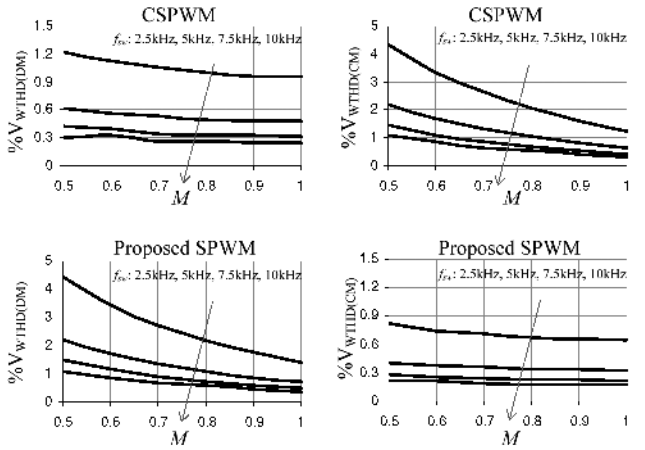

Fig. 13. The weighted THD's $V_{\mathrm{WTHD(DM)}}$ and $V_{\mathrm{WTHD(CM)}}$ under CSPWM and proposed PWM schemes.

TABLE II
ESTIMATED LINE AND NEUTRAL CURRENT DISTORTIONS

	$L_d = L_c = 8.6$mH		$L_d = 8.2$mH and $L_c = 0.132L_d$	
	CSPWM	Proposed SPWM	CSPWM	Proposed SPWM
$I\_THD_{(DM)}$	2.2%	4.56%	2.3%	4.76%
$I\_THD_{(CM)}$	4.24%	1.4%	33.6%	11%
I_THD	4.77%	4.77%	33.76%	11.9%
I_N/I_{R1}	12.7%	4.2%	101%	33%

scheme. Since, the overall line current distortions under both the SPWM schemes are practically the same, the increased differential mode current distortion should not be seen as a drawback of the proposed SPWM scheme. On the other hand, the decreased common mode current ripple associated with the proposed SPWM scheme considerably reduces the neutral current distortion as seen from Table II.

It should be noted that both the common mode ripple $\widetilde{i}_{(\mathrm{CM})}$ and the distortion factor $I_{\mathrm{THD(CM)}}$ are zero, when the midpoint of the dc bus is disconnected from the supply neutral (see Fig. 1). This is similar to the case of a three-wire PWM rectifier [21]. As the differential mode distortion factor $I_{\mathrm{THD(DM)}}$ alone decides the line current THD, it is not preferred to use the proposed SPWM scheme in such application.

IV. INDUCTORS FOR THREE-PHASE APPLICATION

The boost inductors L can be either three single-phase inductors or a three-limb inductor as shown in Fig. 14(a) and (b), respectively. However, a three-limb inductor is more widely used due to economic considerations as discussed in section I and in [23], [24].

Unlike single-phase inductors, a three-limb inductor does not have independent magnetic circuits for the three-phase fluxes. Compared to differential mode fluxes, the magnetic core of such an inductor offers high reluctance to the common mode fluxes. Therefore, compared to differential mode currents, the above inductor offers very low-valued inductance to the common mode currents [24]. The decreased common mode

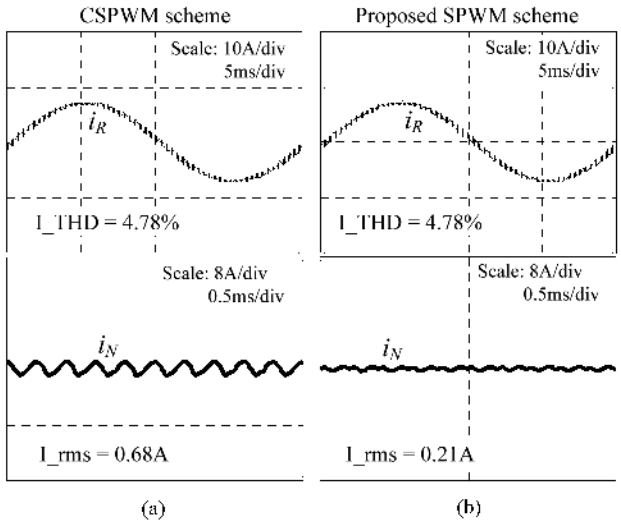

Fig. 14. (a) Single-phase inductor and (b) three-limb inductor.

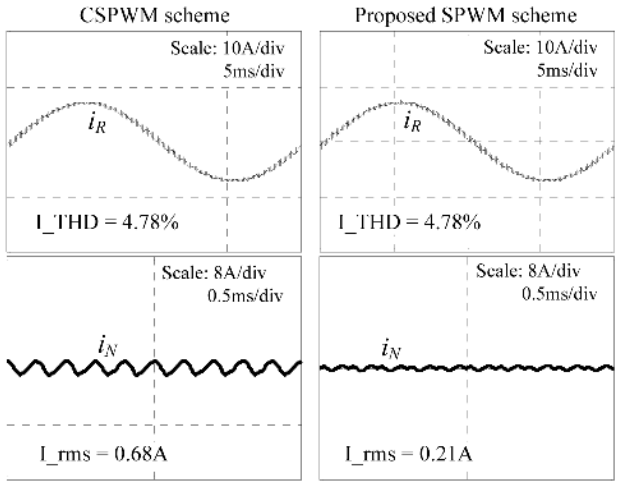

Fig. 15. Simulated line and neutral current waveforms using three single-phase boost inductors (each of 8.6 mH).

inductance has an effect of increasing the common mode ripple in line current and the neutral current. The differential mode line current ripple, however, remains same as that of using three equivalent single-phase inductors. Since, the proposed SPWM scheme considerably reduces the common mode voltage ripple (see Figs. 11 to 13), the ripples in the line and neutral currents are expected to be less under proposed SPWM scheme than under CSPWM scheme.

In order to verify the above predictions, a practical three-limb inductor is considered. The ratio of L_c to L_d for this inductor is experimentally found to be 0.132. The parameters are as shown in Table I. Using (26), (27), and (29) and Fig. 13, the estimated line and neutral current distortions under both the CSPWM and the proposed SPWM schemes are tabulated in Table II (for $L_d = 8.2$ mH and $L_c = 0.132L_d$). These may be compared with the corresponding results as obtained using three single-phase inductors (for $L_d = L_c = 8.6$ mH).

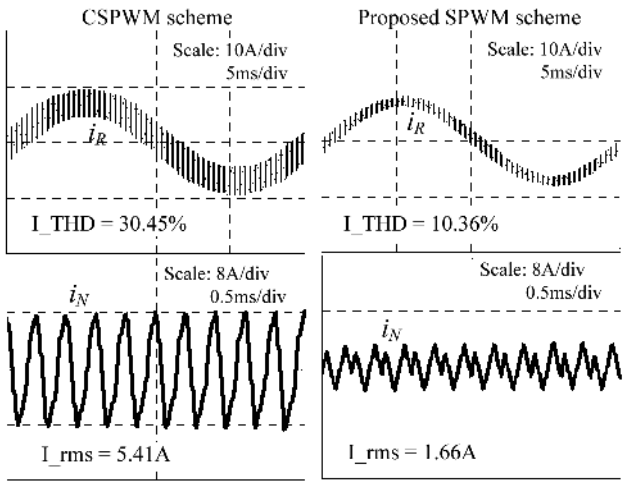

Fig. 16. Simulated line and neutral current waveforms using a three-limb boost inductor ($L_d = 8.2$ mH and $L_c = 0.132\,L_d$).

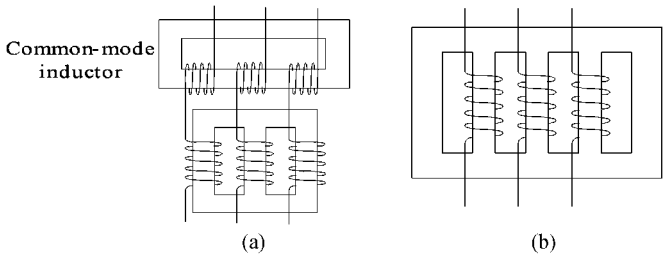

Fig. 17. (a) A three-limb inductor connected in series with a common mode inductor and (b) a five-limb inductor.

V. Simulation Results

The four-wire rectifier system (Figs. 1 and 3) using both the CSPWM and the proposed SPWM schemes is simulated in Matlab/Simulink. The parameters used are as shown in Table I. The inductor model used in the simulation is as shown in (30), where v_{Lj} is the voltage across the jth phase inductor [see Fig. 2(a)], $x = L_c/L_d$, and $i_{j(\mathrm{DM})}$ and $i_{(\mathrm{CM})}$ are the instantaneous differential mode and common mode components of the line current i_j. The simulation results are shown in Figs. 15 and 16. These results agree well with the estimated results presented in Table II

$$\begin{aligned} v_{Lj} &= L_d \frac{di_{j(\mathrm{DM})}}{dt} + xL_d \frac{di_{(\mathrm{CM})}}{dt} + R_L i_j \\ &= L_d \frac{di_j}{dt} - (1-x)L_d \frac{di_{(\mathrm{CM})}}{dt} + R_L i_j. \end{aligned} \tag{30}$$

In order to reduce the common mode ripple current, a common mode inductor can be used in series with a three-limb inductor as shown in Fig. 17(a). Another choice is to use a five-limb inductor as shown in Fig. 17(b), which is a combination of a common mode inductor and a three-limb inductor in a single frame.

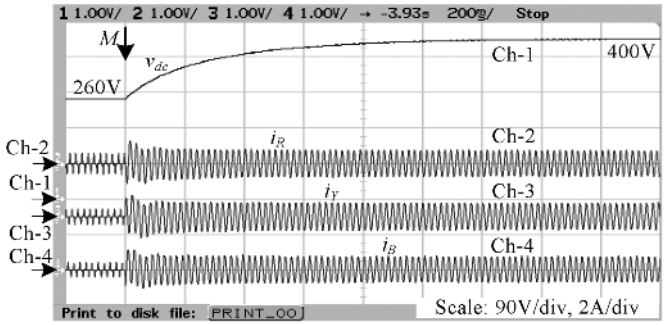

Fig. 18. Measured startup transients.

VI. Experimental Verification

This section presents the experimental setup and the various experimental results.

A. Experimental Prototype

The power circuit of the four-wire rectifier prototype is shown in Fig. 1. The parameters are shown in Table I. The proposed control scheme (Fig. 3) is implemented on an Altera EP1C12Q240C8 FPGA platform [25]. The total number of logic elements used is 2860.

In order to have a one-to-one comparison of the number of logic elements consumed, the synchronous reference frame control scheme discussed in [6] is implemented. This control scheme is found to consume 8496 logic elements. The requirement of additional 5636 logic elements may be attributed to the additional functional blocks, namely the PI current controllers, three-phase to dq transformation, dq to three-phase transformation and unit vector generation, which are not required in the proposed control scheme.

The main voltage loop and the voltage-balancing loop (Figs. 7 and 8) are designed for a closed loop bandwidth of 40 Hz and a phase margin of 65°. In each switching cycle T_s, the measured line currents i_R, i_Y, and i_B are sampled at the peaks of their respective carriers V_{CR}, V_{CY} and V_{CB} [see Fig. 9(b)]. This sampling strategy helps avoid sampling the switching noises and obtain samples closer to the averaged currents I_R, I_Y, and I_B [32]. The output voltages v_{o1} and v_{o2} are sampled at the peak of the carrier V_{CR}.

B. Steady State and Dynamic Performances

During these tests, three single-phase boost inductors (see Table I) are used. To start the converter, the dc bus is precharged up to $V_{\mathrm{dc}}(0) = 260$ V before the control pulses to the devices are released. The lowpass filter (Fig. 4) time constant is set at 400 ms. The initial condition for ΔV_m is set at zero, while the same for V_m is set corresponding to an initial emulated resistance $R_e(0)$ of 200 Ω. An 800 Ω load-resistor is connected across the dc bus. The measured starting transient is shown in Fig. 18, where the gating pulses are applied at an instant M. It can be seen that the proposed soft-start algorithm helps the output voltage build gradually, keeping the starting current low.

The measured input voltage, input current and neutral current at output powers of 1600 and 800 W are shown in Fig. 19. The

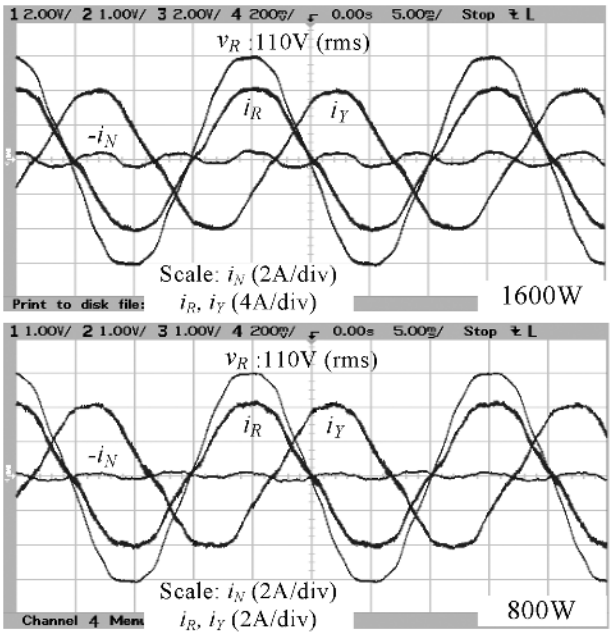

Fig. 19. Steady state input voltage, input current and neutral current waveforms for the output powers at 1600 and 800 W.

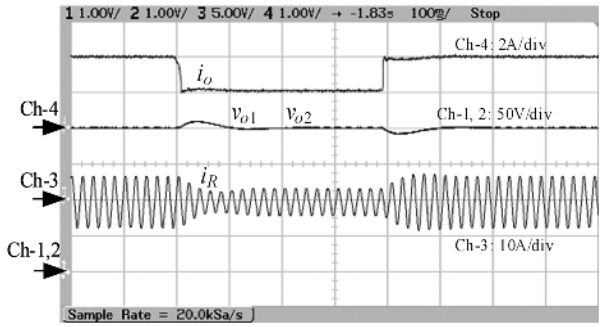

Fig. 20. Dynamic response of the four-wire rectifier system.

corresponding input current THD's are 4.3% and 4.6%, respectively, which satisfy the harmonic standard [33]. In both cases, the input power factor is close to unity and the neutral current is low.

It should be noted that during the above tests, the input phase voltages contain significant lower order harmonic distortion (see Fig. 19). Since the proposed control scheme forces the input currents to replicate their respective input voltages (1), similar lower order harmonic distortions are seen in the line currents. The triplen harmonic components of the input phase voltages result in corresponding neutral currents as seen in Fig. 19.

Fig. 20 shows the dynamic response of the rectifier system, when the output power is suddenly changed between 1600 and 800 W. The dynamic response can be further improved by using load current feedforward [34]. Fig. 20 also shows that the proposed controller maintains balance between the voltages of the two halves of the dc bus successfully during steady state as well as during transients.

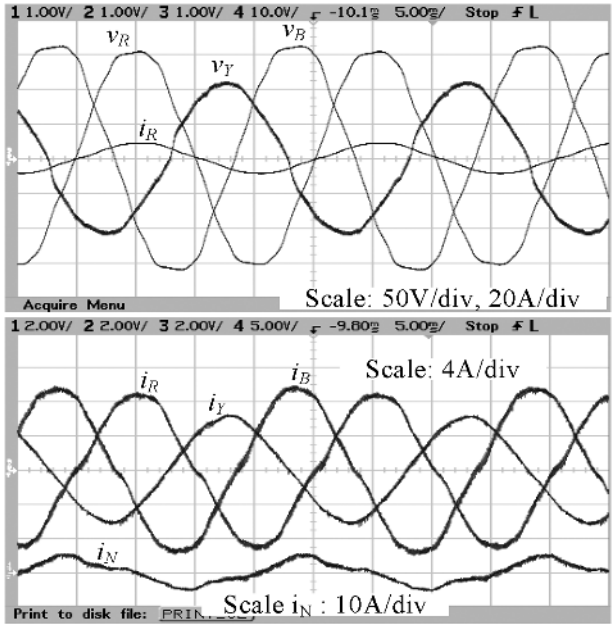

Fig. 21. Steady state sampled input voltage, input current and neutral current waveforms under unbalanced input voltage condition.

C. Effect of Input Voltage Unbalances

The control scheme presented in this paper is derived based on the assumption that the input phase voltages are balanced. In order to check its performance against input voltage unbalances, an unbalance is created by supplying the Y-phase of the rectifier through an additional series impedance of $(5+\mathrm{j}6.3)\Omega$. The corresponding experimental results for an output power of 1600 W are shown in Fig. 21. It can be seen that due to resistance emulation action [see (1)], the phase currents are roughly proportional to their respective input phase voltages. The unbalanced line currents return to the source through the neutral as shown.

D. The Line and Neutral Current Distortions

The rectifier system is tested at 1600 W output power using both CSPWM and proposed SPWM schemes. In each case, both single-phase inductors and three-limb inductor are considered (see Table I). The various experimental results are shown in Figs. 22 and 23. The measured input current THD's and the rms values of the neutral current are shown in Figs. 22 and 23.

The above experimental results agree well with the corresponding simulation results shown in Figs. 15 and 16. It can be seen that the measured line and neutral current distortions are better than the corresponding distortions as obtained through simulation. This can be attributed to the source inductances adding up to the boost inductances in the experimental setup, while the source inductances have been neglected in the simulation.

VII. Conclusion

A control method is presented for a three-phase, four-wire PWM rectifier. The necessary control operations are performed by processing the measured three line currents and two output voltages measured without using input voltage information

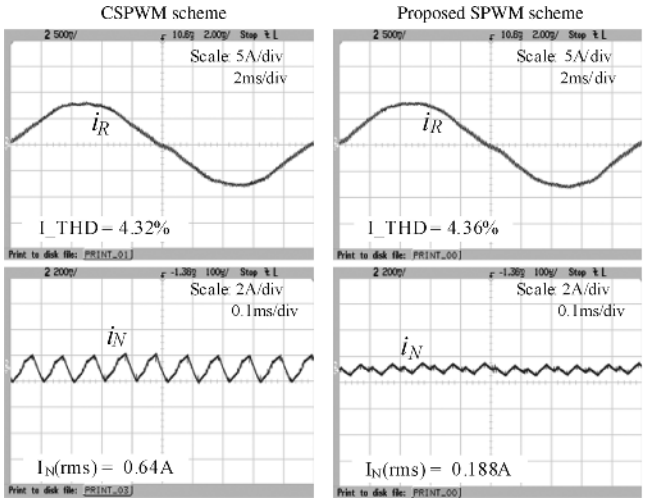

Fig. 22. Experimental line and neutral current waveforms using three single-phase boost inductors (each of 86 mH).

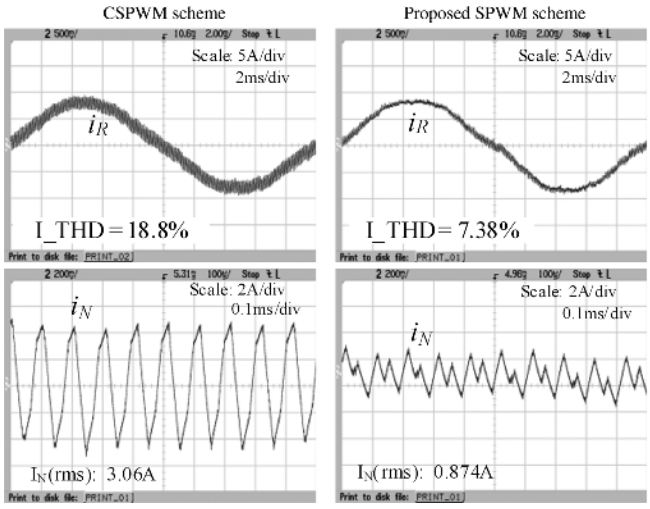

Fig. 23. Experimental line and neutral current waveforms using a three-limb boost inductor ($L_d = 8.2$ mH and $L_c = 0.132L_d$).

and/or any complex transformation. Two voltage controllers are used to hold the output voltage at the reference and to maintain balance between the two halves of the dc bus, respectively. A soft-startup algorithm is presented to start the converter smoothly without causing any appreciable transients. The analysis of the averaged input characteristics, dc bus voltage-imbalance, the main voltage loop and the voltage balancing loop is presented.

A three-carrier-based sine-triangle PWM (SPWM) scheme is proposed for the four-wire PWM rectifier, which considerably reduces the rms ripple in the neutral current compared to the conventional SPWM scheme, when three single-phase inductors are used as the boost inductors. Further, compared to CSPWM scheme, the proposed PWM scheme considerably reduces both the line and the neutral current distortions, when a three-limb inductor is used as the boost inductors. A complete analysis of the line and neutral current distortions is presented.

Finally, the proposed control and the PWM scheme are simulated in Matlab. These are implemented on an FPGA based digital platform and validated experimentally on a laboratory scale prototype. The simulation and experimental results are presented.

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