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Control of Three-Phase Solid-State Transformer with Phase-Separated Configuration for Minimized Energy Storage Capacitors

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***Abstract*—This paper presents the control structure of a solid-state transformer for three-phase AC/AC, to reduce the required size of capacitors. The structure consists of an AC/DC converter based on cascaded H-bridge converters, isolated DC/DC converters, and a DC/AC inverter. The phase separated configuration requires a high capacitance for the smoothing capacitors owing to the instantaneous power oscillation at the double-line frequency. This paper reviews control methods of the DC/DC converter to achieve synchronous instantaneous power with the AC/DC converter, and thereby cancel the double-line frequency component applied to the capacitors between the AC/DC and DC/DC converters. This study also proposes incorporating a control method to cancel the oscillating instantaneous power caused by an unbalanced load current. The overall control was demonstrated using a 6-kVA laboratory prototype. The required minimum capacitance, which is decided by the switching frequency, is discussed, and the demonstration of a design case study on a 300-kVA system is described. The likely increase in loss in the isolated DC/DC converter owing to the power oscillation controls was evaluated with a 10-kW loss evaluation-model of a DC/DC converter.**

***Index Terms*—Solid-state transformer, power quality, smoothing capacitor.**

I. Introduction

THE concept of solid-state transformer (SST) or power-electronics transformer (PET) has received considerable attention with regard to traction and smart grid applications [1], [2], [3]. The concept of SST includes not only AC/AC conversion but also AC/DC, and DC/DC conversions with galvanic isolation and voltage adaptation. The SSTs for the AC/DC is considered to be advantageous because of the reduced number of conversion stages; however, there are still a lot of studies and projects related to the SSTs for the AC/AC, which can be considered as the replacement of line-frequency transformers (LFT) [4], [5], [6], [7]. For the AC/AC, the size and weight reductions are strongly demanded. It typically consists of a converter directly connected to a medium voltage AC line, high- or medium-frequency transformers for isolation and voltage adaptation, and a low voltage DC/AC converter. The main purpose of this concept is to achieve a high-power density compared to LFT and to incorporate certain controllability and functionalities such as energy storage and power quality improvements.

The primary side voltage is generally high compared to the voltage ratings of commercially available semi-conductor devices. Therefore, multi-level topologies, particularly cascaded H-bridge (CHB) converters, are potential candidates for the primary side AC/DC converter, rather than single-level topologies that use high voltage semiconductor devices [8]. Numerous laboratory prototypes with CHB-based configurations for medium voltage grid applications have been reported recently [9], and their controls have been studied effectively, particularly for voltage and power balancing among cascaded cells [10], [11], [12], [13]. In addition, improving reliability has also been studied. Introducing an intentional unbalance to improve reliability, and the usage of redundant cells have also been proposed and discussed [14], [15], [16].

The CHB-based topologies utilize single-phase converters; therefore, the capacitors between the single-phase AC/DC and DC/DC converters exhibit strong instantaneous power fluctuations with frequencies two times that of the line frequency. This results in a considerable increase in the size of the capacitor, which can nullify the size advantage of the multi-level concept. Film capacitors are preferred for power system applications because of the requirement of high reliability. However, the increase in size becomes a drawback when they are applied to phase separated configurations.

Active power decoupling techniques have been proposed for single-phase power oscillation and have been widely studied for single-phase rectifiers and grid-connecting inverters [17], [18], [19], [20]. These techniques can reduce the capacitance requirement of energy storage capacitors by oscillating the voltage; however, additional semiconductor switches and inductors are required. For CHB-based STATCOMs, a method was proposed to reduce the required size of capacitors without modifying the circuit topology [21], [22], [23]. Moreover, size reduction in the case of using film capacitors was discussed [24]. However, this method can be applied only to the STATCOMs dedicated for reactive power generation.

For two-stage cascaded converters, regulation of the DC/DC converter to handle the oscillating power has been proposed to prevent power fluctuations from affecting the intermediate smoothing capacitor [25], [26]. These converters consist of a single-phase AC/DC converter and a DC/DC converter

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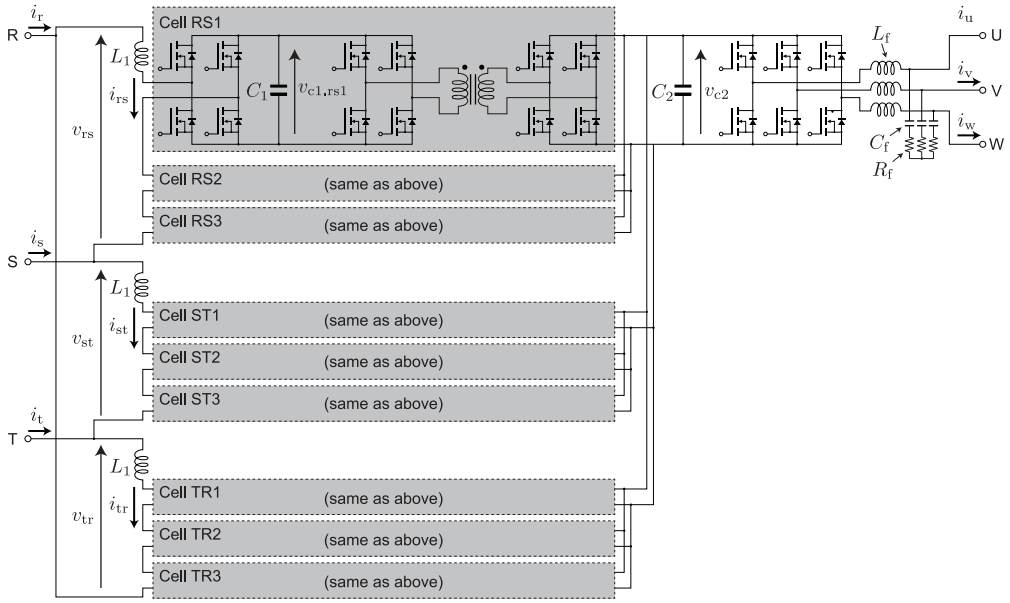

Fig. 1. Configuration of SST for three-phase input and output. In this example, the number of cascades is three.

and are used in on-board battery chargers. This concept can reduce the capacitance of the intermediate capacitor without additional components. Several works have also proposed to apply this concept to SSTs with the above-mentioned configurations. Fundamentally, this can be achieved by a simple feedback control of the capacitor voltage. In addition, a few implementations have been proposed to improve its control performance. An effective method is to feed-forward the specified instantaneous power at the AC/DC stage to the power reference supplied to the DC/DC converter [27]. Application of a resonant controller to the feedback controller has also been proposed [28]. This can improve the control performance for periodic signals. By applying the oscillating power concept to SSTs with three-phase input, the oscillating power flowing into the common DC bus can be cancelled [29].

The authors have proposed a control method for an entire system of SSTs having three-phase input and output [30]. In addition to providing oscillating power control (OPC) to the DC/DC converter, the oscillating power flows inside the system are regulated, and unbalanced primary side currents are permitted for possible unbalanced secondary side currents, similar to that in conventional LFTs. These enable the reduction of the capacitance requirement of all the energy storage capacitors. This strategy forgoes power quality improvement to a certain degree while prioritizing power density improvement.

This study reviewed the proposed control methods for both the CHB side capacitors and the common DC bus capacitor through experimental demonstrations with a 6-kVA laboratory prototype. The prototype employed a dual active bridge (DAB) converter for the isolation. This paper discusses the minimum possible capacitance using the proposed methods and describes the demonstration of the operation with the calculated minimum capacitance in the laboratory prototype. In addition, it discusses the likely increase in the loss in high-frequency transformers and semi-conductor devices caused by the oscillating power conversion at two times the line frequency, with the aid of certain experimental results obtained from a 10-kW practical scale single cell setup. An estimation method of the loss increase by the oscillating instantaneous power is presented.

II. Proposed Control Method

A. Discussed Configuration of SST

Fig. 1 shows the schematic diagram of an SST with three-phase input and three-phase output. The primary side is generally connected to a high or medium voltage system. Therefore, it consists of several series-connected single-phase AC/DC converters. The dc terminals of the AC/DC converters are connected to DAB converters (which provide galvanic isolation and voltage adaptation) via the smoothing capacitor C_1. The secondary sides of all the DAB converters are connected in parallel and supplies power to a three-phase DC/AC inverter via another smoothing capacitor C_2.

B. Capacitance Reduction of CHB Capacitors

Single phase AC/DC conversion generates an oscillating instantaneous power, which flows into the capacitor C_1 as

$$p_{\mathrm{acdc}} = V_{\mathrm{conv1}} I_1 \cos\phi - V_{\mathrm{conv1}} I_1 \cos(2\omega t - \phi), \quad (1)$$

where V_{conv1} and I_1 are the rms values of the converter voltage and current, respectively; ϕ is the power factor angle; and ωt is the line phase angle. It consists of a constant part and a double-line frequency component. With a basic control, its average power is drawn by the following DAB converter; the remaining oscillating component causes a capacitor voltage ripple. The capacitor voltage can be expressed as

$$v_{\mathrm{c1}} = \sqrt{{V_{\mathrm{dc.center}}}^2 - \frac{V_{\mathrm{conv1}} I_1}{\omega C_1} \sin(2\omega t - \phi)}, \quad (2)$$

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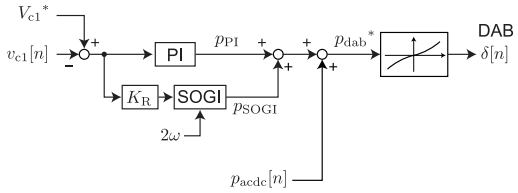

Fig. 2. Block diagram of proposed control for v_{c1}. It mainly consists of feed-forwarding power inflow from the AC side, p_{acdc}, to the dual active bridge (DAB) control, and a feedback control with a resonant controller. The latter is implemented using a SOGI.

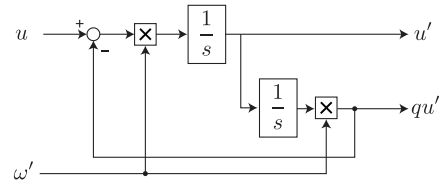

Fig. 3. Block diagram of second order generalized integrator (SOGI).

where $V_{dc.center}$ is the capacitor voltage at the zero current instant. To ensure an acceptably low voltage ripple, a high capacitance is selected for C_1 in the conventional design.

Fig. 2 shows the block diagram of the proposed control scheme. By regulating the DAB converter to convert the same instantaneous power with the AC/DC converter synchronously, the double-line frequency component applied to C_1 can be eliminated and a low capacitance can be selected. This can be achieved by a simple capacitor voltage feedback control. However, feed-forwarding the specified AC/DC instantaneous power, p_{acdc}, to the feedback controller output can improve its control performance. Here, p_{acdc} can be calculated from the measured ac current and voltage reference supplied to the corresponding AC/DC converter.

The resulting controller output, ${p_{dab}}^*$, is a power set-point, and therefore, should be converted to a reference variable, which can directly operate the DAB. Several control strategies for phase shifting have been proposed [31]. In this study, a single-phase-shift (SPS) control was selected for simplicity. For the SPS regulated DAB, the phase angle difference, δ, can be expressed as

$$\delta = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8{p_{dab}}^* f_{sw.dab} L_{dab}}{{V_{dab.1}}^2}}\right), \tag{3}$$

where $f_{sw.dab}$ is the switching frequency of the DAB, L_{dab} is the primary-side referred equivalent series inductance of the transformer, and $V_{dab.1}$ is the primary-side dc voltage of the DAB. This arises from the established fundamental operation characteristics of the DAB converter with balanced dc voltages, without considering the lossless snubber capacitors and dead time [32]. This calculation can be implemented as a look-up-table.

The feedback control is still required to maintain v_{c1} against likely errors in the calculation of p_{acdc} and the operation characteristics of the DAB. The feedback can be provided by using a simple proportional-integral controller. The error is likely to be periodic and mainly in the double-line frequency. Therefore, a resonant controller tuned at the double-line frequency is added to improve the ripple cancellation performance without increasing the proportional control gain. For this purpose, a second order generalized integrator (SOGI) [33] shown in Fig. 3 can be used. Its transfer function is expressed as

$$\frac{u'}{u} = \frac{s}{s^2 + {\omega'}^2}, \tag{4}$$

where ω' is the specified tuning frequency. The output signal, u', is the band-passed signal for the input signal, u, and qu' is the in-quadrature signal of u'. In this case, u' is used to detect the remaining oscillating component in v_{c1}. The SOGI functions as a frequency adaptive filter, and only the double-line frequency component in the error capacitor voltage is selectively regulated. Other higher order components can also be regulated by cascading SOGIs tuned at each frequency in parallel.

C. Capacitance Reduction for Unbalanced Load

By applying the above discussed controls, the single-phase AC/DC converter and DAB converter are synchronously controlled. Their combination can be considered as a direct converter such as a matrix converter. The capacitance of the CHB capacitors, C_1, can be reduced. However, a new power oscillation will be introduced on the secondary side of the DAB converter. The power oscillations from different phases will cancel each other if the power from the primary side is balanced. However, a large capacitance for C_2 is still required for the likely unbalance load connected to the secondary side of the SST.

With regard to the unbalanced power outflow to the secondary side, regulating the power inflows using sets of DAB and AC/DC converters can remove the double-line frequency power oscillation applied to C_2. Fig. 4 shows the block diagram of the proposed control required to achieve this. The control assumes that the DC/AC converter is operated with open-loop or voltage control. Hence, the load currents, i_u, i_v, and i_w, are determined by the load side. The capacitor voltage, v_{c2}, is regulated by the source side, i.e., the primary side currents, i_{rs}, i_{st}, and i_{tr}, in this case.

In the proposed control structure, a feed-forward control is introduced in addition to a simple PI feedback control, similar to that used for controlling v_{c1}. From the measured load currents, i_u, i_v, and i_w, and the reference phase voltages specified for the pulse width modulation (PWM), v_u^*, v_v^*, and v_w^*, the instantaneous power variables can be calculated as

$$p_2 = v_{2\alpha}^* i_{2\alpha} + v_{2\beta}^* i_{2\beta}, \tag{5}$$

$$q_2 = v_{2\alpha}^* i_{2\beta} - v_{2\beta}^* i_{2\alpha}, \tag{6}$$

where $v_{2\alpha}^*$ and $v_{2\beta}^*$ are obtained from v_u^*, v_v^*, and v_w^*, and $i_{2\alpha}$ and $i_{2\beta}$ are obtained from i_u, i_v, and i_w, using Clarke

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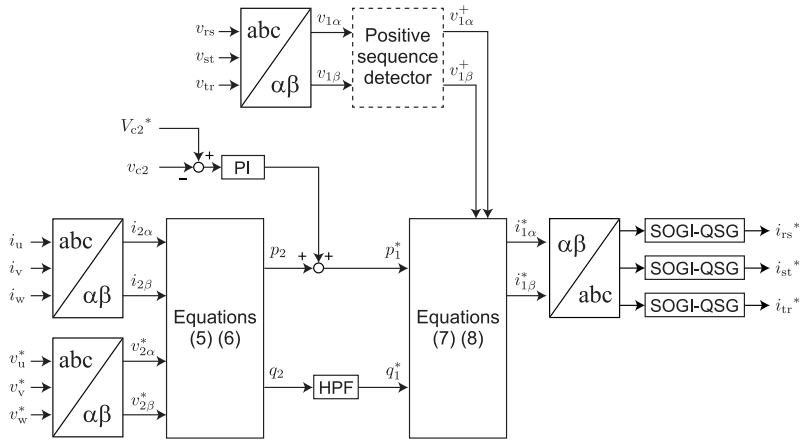

Fig. 4. Block diagram of proposed control for v_{c2}. It consists of feed-forwarding instantaneous power variables at the secondary side to the primary side current controller, and a simple PI feedback control.

transformation. These power variables can be transformed into the primary side current set-points, $i^*_{1\alpha}$ and $i^*_{1\beta}$, as

$$i^*_{1\alpha} = \frac{p^*_1 v_{1\alpha} - q^*_1 v_{1\beta}}{{v_{1\alpha}}^2 + {v_{1\beta}}^2}, \quad (7)$$

$$i^*_{1\beta} = \frac{p^*_1 v_{1\beta} + q^*_1 v_{1\alpha}}{{v_{1\alpha}}^2 + {v_{1\beta}}^2}, \quad (8)$$

where p^*_1 and q^*_1 are the reference instantaneous power variables; $v_{1\alpha}$ and $v_{1\beta}$ are obtained by the Clarke transformation of the primary side voltages, $v_{\rm rs}$, $v_{\rm st}$, and $v_{\rm tr}$ [34]. Then, the current set-points are obtained by inverse Clarke transformation. It should be noted that only $p^*_1 = p_2$ is essential for reducing the power oscillation applied to C_2. However, $q^*_1 = q_2$ can also be applied for calculating the instantaneous primary side current.

Using the above method, the input power can be synchronized with the power outflow to the load. However, a feedback control is still required to maintain the capacitor voltage, v_{c2}, at the specified reference voltage, V^*_{c2}. This is because it can be affected by the loss generated in the converters and by the likely errors in power estimation. A simple proportional-integral (PI) controller can be used for this purpose; its output is added to p_2 and supplied to the primary side control as p^*_1. The PI controller is required only for the loss and error compensation; therefore, a very high-speed response is not required.

Meanwhile, q_2 can be supplied to the primary side control as q^*_1 without modification. However, it is likely to contain an offset corresponding to the balanced reactive power component. The removal of the offset component results in power factor improvement on the primary side and loss reduction in the AC/DC and DAB converters owing to the reduced current. A simple high-pass filter can be used for this purpose because a very high-speed response is not required for the offset rejection.

The likely unbalance of the primary side voltage causes distorted primary current references if the unbalanced voltage is directly supplied as $v_{1\alpha}$ and $v_{1\beta}$ in (7) and (8). To prevent the distortion, positive sequence detectors (e.g., the so-called Dual SOGI [33]) can be used. By providing only a positive sequence voltage to the equations, pure sinusoidal primary current references can be obtained for sinusoidal secondary currents. However, this strategy can introduce a difference in the instantaneous power between the primary and secondary sides, and result in a voltage ripple in C_2. To effectively achieve both oscillating power cancellation and pure sinusoidal primary currents simultaneously, the load side voltages can be regulated to be unbalanced as the conventional LFTs do. This strategy can be required for short-time abnormal conditions, although the impact of the source voltage unbalance in normal situations can be considered to be negligible. This paper does not discuss this strategy further.

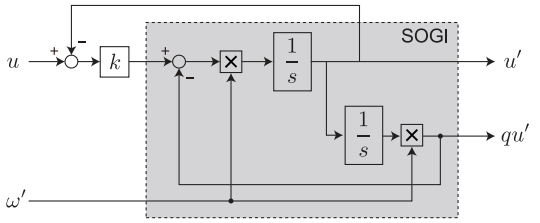

Fig. 5. Block diagram of SOGI configured as a quadrature signal generator (SOGI-QSG).

Harmonic components in the load currents result in corresponding harmonic components in the primary current references. This paper proposes the application of a SOGI configured as a quadrature signal generator (SOGI-QSG) [33] to remove the harmonic components. The configuration of the SOGI-QSG is shown in Fig. 5. It functions as a notch-filter with the specified angular frequency, ω'; therefore, it can generate the fundamental component of the distorted current reference by tuning it at the fundamental frequency. The harmonic rejection can cause a difference between the input and output instantaneous powers; this results in oscillations of v_{c2} with frequencies two times that of the harmonic frequencies. However, the amplitude of oscillation is relatively low as compared to that with two times the fundamental frequency.

Compared with the OPC of the DAB for C_1 reduction, the

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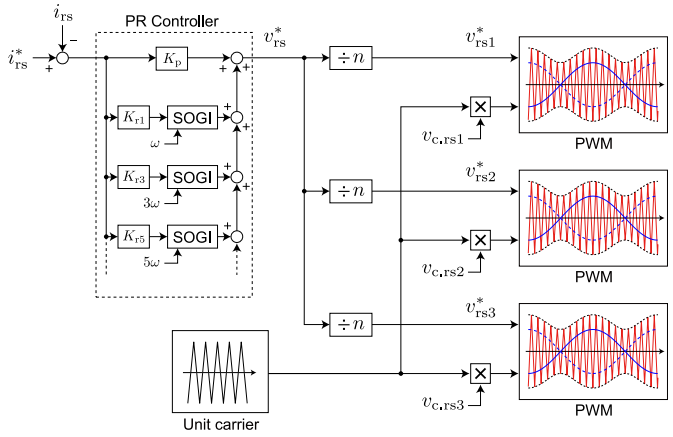

Fig. 6. Block diagram of current control and modulation of CHB-AC/DC converter for each phase. In this case, the R-S phase of the Δ connected configuration is shown.

proposed control for C_2 reduction has certain drawbacks and limitations. Apparently, the frequency of the secondary side must be equal to that of the primary side. In principle, a certain amount of energy storage is required for compensating the unbalanced power and harmonics. The design strategy for the capacitance depends on the power quality improvements required for the application.

The proposed OPC for C_2 exhibits another drawback, that is circulating current between phases. The fundamental concept of the proposed OPC causes unequal instantaneous power flows among phases. In addition to that, when the load current is strongly unbalanced, the instantaneous power flowing through certain phases can be negative. These can be considered as circulating current between phases; they result in the increase in loss compared to that with the conventional control.

D. Current Control

The primary side current can be regulated by any method that can be applied to CHB-based AC/DC converters. This paper proposes to regulate the current in each phase separately and to address the sinusoidal current references, $i^*_{\rm rs}$, $i^*_{\rm st}$, and $i^*_{\rm tr}$, on a stationary reference frame. Fig. 6 shows the control structure for a phase. A proportional-resonant (PR) controller is used for single-phase current regulation [35], [36]. As shown in Fig. 6, the output signal from the PR controller is the voltage reference, which is divided by the number of cascades and supplied to the PWM modulation blocks. By using several SOGIs tuned at high order harmonic frequencies, the harmonic current can be regulated. This feature is attractive, particularly in the cases in which inductors with low inductance are used, where it is necessary to reduce harmonics in currents during grid voltage distortions.

Although the proposed control achieves almost flat capacitor voltages, a carrier-based PWM scaled by the capacitor voltage is applied to achieve adequate effective linearity for the current regulation. This is also effective for high voltage ripple conditions during experiments for cases without the proposed control (described subsequently). DC-voltage balancing controls are not required, because the individual $v_{\rm c1}$ is regulated by the corresponding DAB.

TABLE I
SPECIFICATIONS OF CONSIDERED SST

System	Output capacity	S	300 kVA
	Input voltage	V_1	6.6 kV
	Line frequency	$f_{\rm line}$	50 Hz
AC/DC	Number of cascades	n	12
	Configuration		Δ
	Grid connecting inductance	L_1	69.3 mH (5%)
	Nominal line-to-line current	$I_{\rm ac1}$	15.2 A
	Nominal cell output voltage	$V_{\rm conv1}$	578 V
	DC voltage	$V_{\rm c1}$	858 V
	Smoothing capacitor	C_1	(to be discussed)
	Carrier frequency	$f_{\rm sw.acdc}$	(to be discussed)
DC/AC	Nominal phase current	$I_{\rm ac2}$	433 A
	Nominal line-to-line voltage	$V_{\rm ac2}$	400 V
	DC voltage	$V_{\rm c2}$	720 V
	Smoothing capacitor	C_2	(to be discussed)
	Carrier frequency	$f_{\rm sw.dcac}$	(to be discussed)

III. Design Case Study

A. Minimum Required Capacitance

By applying the proposed control to reduce C_1, the double-line frequency component in $v_{\rm c1}$ can be cancelled. However, the ripple components caused by switching cannot be cancelled. In this section, the minimum required capacitance is assumed to be decided by the acceptable ripple voltage caused by the switching.

The peak-to-peak of the voltage ripple under uni-polar switching of a full-bridge inverter, $\Delta v_{\rm c1}$, can be expressed as

$$\Delta v_{\rm c1} = \frac{d\left(\sqrt{2}I_{\rm ac}|\sin\omega t| - i_{\rm dab}\right)}{2C_1 f_{\rm sw.acdc}}, \tag{9}$$

where $I_{\rm ac}$ is the rms value of the ac current of the inverter. This current is assumed to be pure sinusoidal and constant during one half of the switching cycle. d is the duty ratio of the voltage output in a half switching cycle and can be expressed as $d = \sqrt{2}V_{\rm conv}|\sin\omega t|/V_{\rm c1}$, where $V_{\rm conv}$ is the rms value of the reference voltage. $i_{\rm dab}$ is the current drawn by the DAB converter and can be expressed as $i_{\rm dab} = 2V_{\rm conv}I_{\rm ac}\sin^2\omega t/V_{\rm c1}$ for the case with the proposed control. The switching frequency of the DAB converter is generally substantially higher than that of the AC/DC converter; therefore, the current drawn by the DAB is assumed to not generate voltage ripple in C_1 and be smooth.

$\Delta v_{\rm c1}$ varies in a line cycle; however, it achieves its peak when $d = 2/3$ under the step-up ratio, α, which is lower than $3/2$. Here, α is defined as $\alpha = V_{\rm c1}/\sqrt{2}V_{\rm conv}$. The maximum $\Delta v_{\rm c1}$ in a line cycle is expressed as

$$\Delta v_{\rm c1.max} = \frac{2\sqrt{2}I_{\rm ac}\alpha}{27C_1 f_{\rm sw.acdc}}. \tag{10}$$

B. Required Capacitance for a 300-kVA SST

The case presented in Table I is considered as a practical real-scale SST for power system applications. Fig. 7 shows the value of C_1 required to achieve 5% voltage ripple in the

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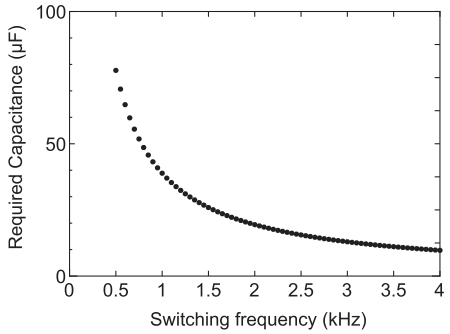

Fig. 7. Capacitance C_1 required to achieve 5% voltage ripple with the proposed control for the considered 300-kVA SST as a function of the switching frequency, $f_{\mathrm{sw.acdc}}$.

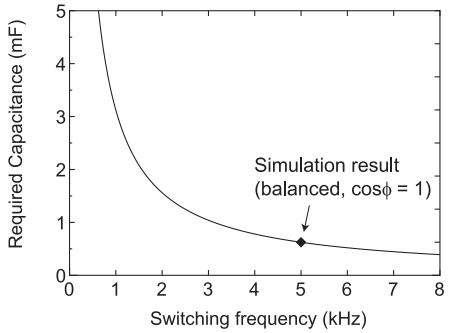

Fig. 8. Capacitance C_2 required to achieve 5% voltage ripple with the proposed control albeit without harmonic compensation capability for the considered 300-kVA SST as a function of the switching frequency, $f_{\mathrm{sw.dcac}}$.

SST; it is obtained from equation 10. The capacitance required for C_1 depends on the switching frequency, $f_{\mathrm{sw.acdc}}$. The switching frequency for CHB-based converters can be comparatively low when a carrier phase shift concept is applied; however, a remarkable capacitance reduction to 77.7 μF can be achieved even for a sufficiently low switching frequency of 500 Hz. Meanwhile, the capacitance required to achieve 5% voltage ripple with the average power in a line cycle, which is constantly drawn by the DAB converter, is calculated as 748 μF from equation 2.

To discuss the minimum required C_2, it is assumed that the voltage ripple in C_2 is caused only by the DC/AC converter and not the DABs. By applying the proposed control albeit without the harmonic compensation, the ripple is determined only by the switching. However, the operation of the DC/AC converter has numerous possibilities (e.g., power factor, unbalance). Therefore, the theoretical calculation of the voltage ripple for C_2 is complex.

This study used a time-domain circuit simulation result for reference. The balanced rated load with unity power factor was tested in the simulation, and the instantaneous capacitor current was obtained. The capacitor voltage can be obtained by integrating the capacitor current. The required capacitance to achieve 5% voltage ripple for 5 kHz ($= f_{\mathrm{sw.dcac(ref)}}$) was 634 μF ($= C_{2(\mathrm{ref})}$). The required capacitance for a general frequency, $f_{\mathrm{sw.dcac}}$, can be calculated as

$$C_2 = C_{2(\mathrm{ref})} \cdot \frac{f_{\mathrm{sw.dcac(ref)}}}{f_{\mathrm{sw.dcac}}}. \tag{11}$$

The results are plotted in Fig. 8.

Meanwhile, the capacitance required to achieve 5% voltage ripple for an unbalanced load without the proposed control was calculated by equation 2. The C_2 required for a single-phase load connected between two lines with nominal current is 21 mF.

It should be noted that the maximum permissible current of the capacitors tends to be low for capacitors with low capacitance. However, it is likely that a considerable decrease in the capacitance is achieved when film capacitors are used, owing to their high allowable ripple current.

C. Capacitor Volume Estimation

In general, the volume of capacitors is considered to be linear to the stored energy for identical capacitor technology. A concept of meta-parameterization has been proposed to estimate the capacitor volume [24]. If an identical capacitor technology is applied for different capacitance values and rated peak voltages, the overall capacitor volume can be predicted by

$$Vol_{\mathrm{C}} = K_{\mathrm{V0}} \cdot C^{K_{\mathrm{V1}}} \cdot {V_{\mathrm{CN}}}^{K_{\mathrm{V2}}}, \tag{12}$$

where C is the rated capacitance; V_{CN} is the rated operating peak voltage; and K_{V0}, K_{V1}, and K_{V2} are proportionality regression coefficients determined by extracting data from the reference capacitor technology.

Table II lists the capacitor parameters for a design for the case of Table I, and the resulting volumes. The switching frequencies are set at 500 Hz and 5 kHz for the AC/DC and DC/AC, respectively. A set of meta-parameters of MKP-B2562 (TDK) reported in [24] is used: $K_{\mathrm{V0}} = 8.5362$ (cm^3), $K_{\mathrm{V1}} = 0.8204$, $K_{\mathrm{V2}} = 1.5797$. As a safety factor, $\hat{V}_{\mathrm{c1}} \times 1.1$ and $\hat{V}_{\mathrm{c2}} \times 1.1$ are specified as V_{CN}.

The estimation specifies that a drastic volume reduction can be achieved in both C_1 and C_2. It should be noted that the meta-parameters were extracted from the capacitors whose capacitances were between 40 μF and 1,500 μF; the capacitance of C_2 with the conventional control is out of this range. However, it can be considered that the volume will be higher than the estimated value if the capacitor is composed of multiple low-capacitance capacitors.

IV. Control Demonstration

A. Small-Scale Setup

To verify the proposed control structures, a small-scale model was fabricated and experiments were conducted using this model. Fig. 9(a) shows the overview, and Table III lists the main specifications of the small-scale model. It should be noted that this small-scale model was mainly designed for control verification. Although the primary side voltage is 200 V, the primary side AC/DC converter consists of three series-connected single-phase AC/DC converters for each phase. The dc-link voltage is significantly lower than the

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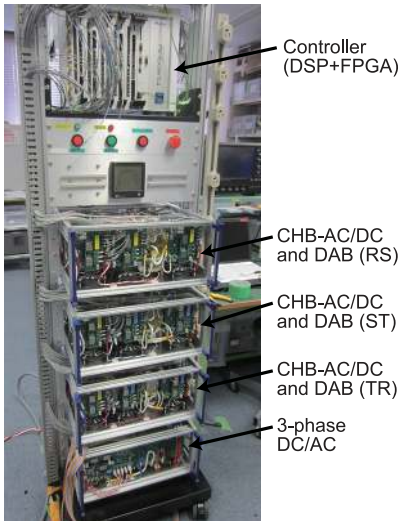
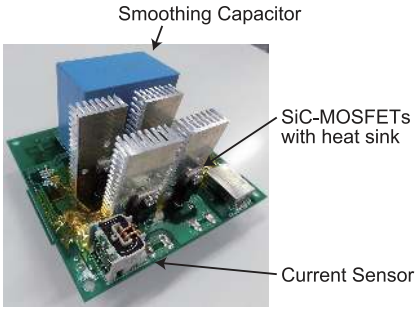
TABLE II
CAPACITOR VOLUME ESTIMATION

			(Proposed)	(Conventional)
AC/DC	Selected carrier frequency	$f_{\mathrm{sw.acdc}}$	500 Hz	(any)
	Peak voltage	$\hat{V}_{\mathrm{c1}}$	879 V ($V_{\mathrm{c1}} \times 1.025$)	
	Required capacitance	C_1	77.7 μF	748 μF
	Number of capacitors	N_{C1}	36	
	Estimated volume	Vol_{C1}	6.79 dm^3	43.54 dm^3
DC/AC	Selected carrier frequency	$f_{\mathrm{sw.dcac}}$	5 kHz	(any)
	Peak voltage	$\hat{V}_{\mathrm{c2}}$	738 V ($V_{\mathrm{c2}} \times 1.025$)	
	Required capacitance	C_2	624 μF	21 mF
	Number of capacitors	N_{C2}	1	
	Dimensional volume	Vol_{C2}	0.79 dm^3	14.15 dm^3
Total	Estimated volume	Vol_{C}	7.58 dm^3	57.69 dm^3



(a)



(b)

Fig. 9. Overview of (a)fabricated 6-kVA demonstrator with a controller, and (b)single converter cell for AC/DC.

TABLE III
SPECIFICATIONS OF 6-KVA DEMONSTRATOR

System	Output capacity	S	6 kVA
	Input voltage	V_1	200 V
	Output voltage	V_2	200 V
	Line frequency	f_{line}	50 Hz
AC/DC	Number of cascades	n	3
	Configuration		Δ
	Grid connecting inductance	L_1	1.91 mH
	Smoothing capacitor	C_1	100 μF
	DC voltage set-point	$V_{\mathrm{c1}}{}^*$	120 V
	Carrier frequency	$f_{\mathrm{sw.acdc}}$	4 kHz
DAB	Nominal primary voltage	$V_{\mathrm{dab.1}}$	120 V
	Nominal secondary voltage	$V_{\mathrm{dab.2}}$	360 V
	Winding ratio of transformer	N_2/N_1	3
	Equivalent series inductance*	L_{dab}	5 μH
	Switching frequency	$f_{\mathrm{sw.dab}}$	100 kHz
DC/AC	Phase		3
	Filter inductor	L_{f}	0.55 mH
	Filter capacitor	C_{f}	10 μF
	Filter damping resistor	R_{f}	5 Ω
	Smoothing capacitor	C_2	300 μF
	DC voltage set-point	$V_{\mathrm{c2}}{}^*$	360 V
	Carrier frequency	$f_{\mathrm{sw.dcac}}$	24 kHz

* Primary side referred

voltage rating of the semiconductor devices. Hence, the loss is not optimized.

Fig. 9(b) shows an overview of the cell converter for AC/DC. It consists of semiconductor switches and a smoothing capacitor. The identical design concept was applied to the primary and secondary bridge converters for DC/DC. However, those do not have such a large smoothing capacitor. SiC-MOSFETs (SCT2120AF, Rohm) were used for all the converter cells. A film capacitor (B32778G4107K, TDK) was used as the smoothing capacitor. The semiconductor switches and smoothing capacitor have excessively high voltage ratings (650 V and 450 V, respectively) because appropriate components for such a low dc-link voltage of the small-scale control demonstrator were not available.

All the control structures discussed in Section II were implemented on a DSP and FPGA based controller. The carriers for the three cascaded AC/DC converters were shifted by 60°, and unipolar switching was applied in each AC/DC converter. Both the edges of all the three carriers invoked an interrupt; therefore, the main control cycle was 41.7 μs, except for updating the reference voltage and A/D conversion, which were invoked at both the edges of the corresponding carrier. The SOGI was implemented on the DSP with this control cycle, and the discrete-time implementation demonstrated in [37] was applied.

B. Operation with Reduced CHB Capacitors

The proposed control for v_{c1}, which is shown in Fig. 2, was experimentally tested with a single-cell test setup. The parameters of the setup are identical to those listed in Table III; however, the capacitance C_1 was changed to test the performance of the control. According to equation 2, when

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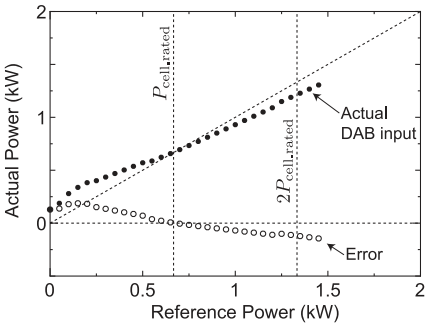

Fig. 10. Measured power input to DAB converter as a function of the specified power reference, $p_{\text{dab}}{}^{*}$, and the error between them.

conventional control is applied, C_1 should be approximately 1600 μF to maintain the voltage ripple within 10% at the rated current. Meanwhile, according to equation 10, the capacitance required to achieve 10% ripple with the proposed control is 26.4 μF; therefore, 20 μF in addition to the 1.5 μF of the on-board capacitor was selected for the test. The inductance of the grid-connecting inductor was also changed to 5.73 mH in order to maintain the current ripple low during single-cell operation.

Firstly, the power characteristics of the DAB converter were measured. Fig. 10 shows the measured input power to the DAB converter as a function of $p_{\text{dab}}{}^{*}$, which is supplied to the calculation for δ, which is expressed in equation 3. An almost linear error was observed between the reference power and actual power; it can generate a double-line frequency error with an offset in the power oscillating operation when only feed-forward control is applied. Therefore, the resonant controller is likely to be effective and to provide the double-line frequency error component.

Fig. 11(a) shows the waveforms, including that of v_{c1}, with the conventional control. The conventional control was achieved by disabling the feed-forward part and resonant controller. With the conventional control, operation was not feasible with the selected 21.5 μF capacitors; therefore, an additional 1,600 μF capacitor was connected. However, oscillation continued to occur in v_{c1}. Fig. 11(b) shows the waveforms with the proposed control. An almost flat v_{c1} was observed with the selected capacitor of 21.5 μF. The calculated power from the AC/DC stage, p_{acdc}, provided a major part of the reference power supplied to the DAB; however, the resonant controller also provided certain values corresponding to the errors.

Fig. 12 shows the amplitudes of the harmonic components in v_{c1} with different control settings. Without the resonant controller, there were significant second and fourth order components. By applying the resonant controller tuned at 100 Hz, the second-order component was completely removed. The waveforms with this setting are shown in Fig. 11(b). The fourth-order component was also present and could be removed by applying an additional resonant controller tuned at 200 Hz.

C. Operation with Reduced Secondary Side Capacitor

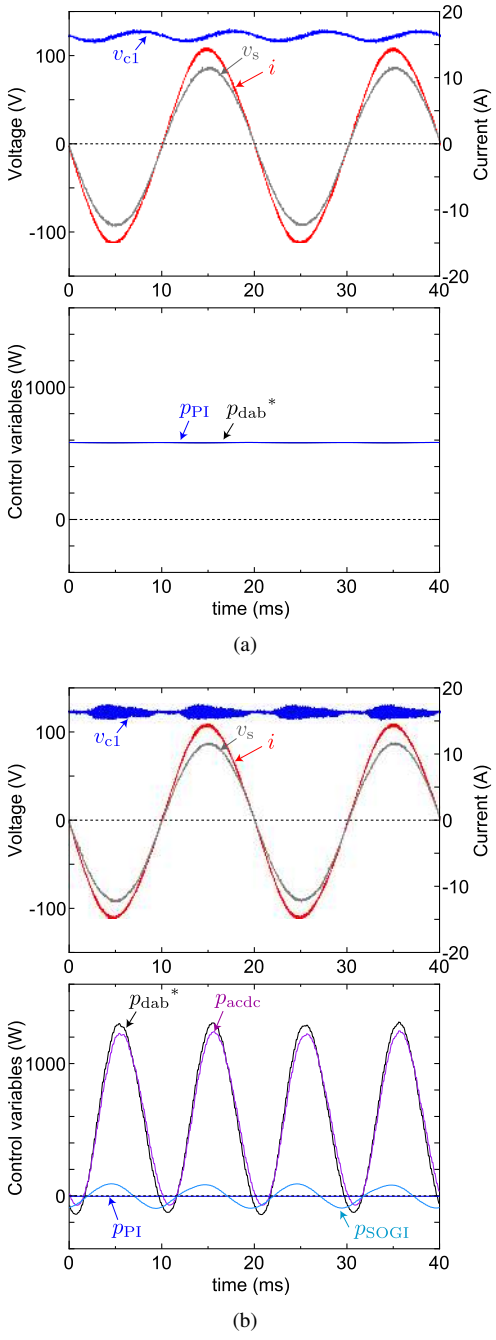

Fig. 11. Experimental waveforms and control variables in DSP with I_{rs} = 10 A: (a) with conventional control and C_1 = 1600 μF, (b) with the proposed control, including feed-forward control and resonant controller tuned at 100 Hz and C_1 = 21.5 μF.

1) Balanced Resistive Load Operation: The overall operation with different load conditions, including unbalance and nonlinear loads, with a reduced capacitance for C_2 was tested using the entire setup. In this setup, the value of C_2 was 300 μF, which is sufficiently low compared to the capacitance required for maintaining the voltage ripple within 10% with the conventional control when full unbalance load is applied. According to equation 2, the voltage ripple with this capacitance for a highly unbalanced load; for example, the single-phase load connected to two lines with rated current,

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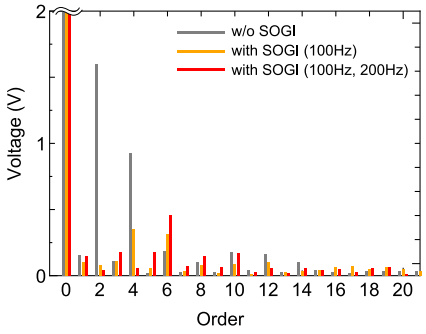

Fig. 12. Amplitudes of harmonic components in the capacitor voltage v_{c1} with the proposed control and settings.

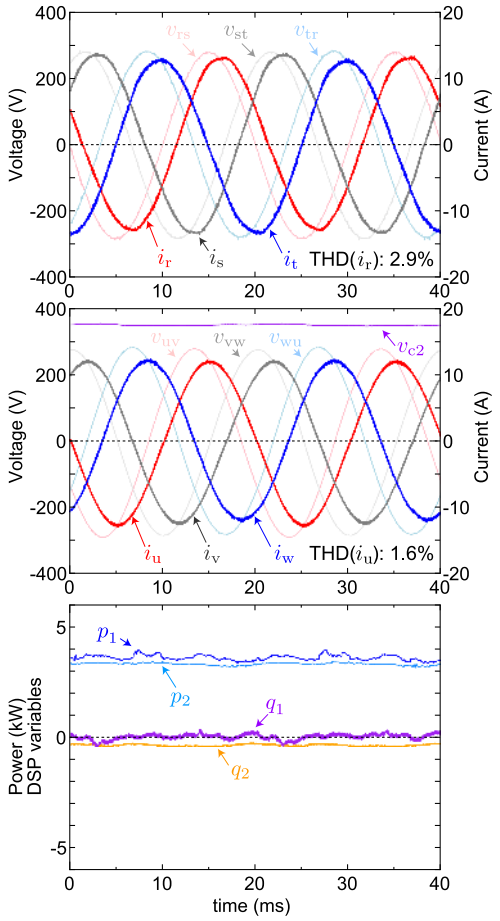

Fig. 13. Experimental waveforms for balanced resistive load. The primary side line currents, i_r, i_s, and i_t, secondary side line currents, i_u, i_v, and i_w, and capacitor voltage, v_{c2}, with the proposed control are shown. The variables used in the DSP, namely. p_2, q_2, p_1, and q_1 are also shown.

will be approximately 30%.

As a reference, a balanced resistive load was applied. The obtained waveforms are shown in Fig. 13. The line current waveforms were delayed by 30° from the line-to-line voltages; this indicates that an almost unity power factor was observed on both the sides. The waveforms of p_2 and q_2 (calculated based on the measured secondary currents i_u, i_v, and i_w and the reference voltages supplied to the DC/AC converter) and those of p_1 and q_1 (calculated based on the measured primary

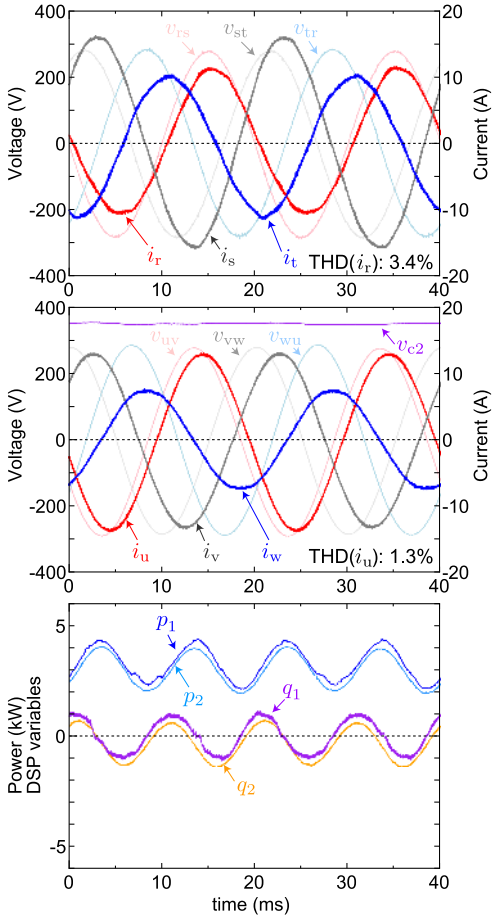

Fig. 14. Experimental waveforms for unbalanced resistive load with the proposed control.

line-to-line currents i_{rs}, i_{st}, and i_{tr}, and the voltages, v_{rs}, v_{st}, and v_{tr}) are also shown. These were almost constant because the load was balanced. The losses generated in the converters caused a marginal difference between p_2 and p_1; the PI control provided this difference to maintain v_{c2} at the reference value.

2) Unbalanced Resistive Load Operation: An unbalanced resistive load was tested with and without the proposed control. Fig. 14 shows the measured waveforms and the corresponding DSP variables with the proposed control. Owing to the unbalanced load, p_2 and q_2 oscillated at two times the line frequency. With the proposed control, the primary side currents were regulated to be unbalanced corresponding to the unbalanced load currents. The values of p_1 and q_1 were almost identical to those of p_2 and q_2, respectively. Moreover, there was no significant oscillation in v_{c2} because synchronous power oscillation between the secondary and primary sides was achieved. Fig. 14 clearly demonstrates the operation of the proposed OPC.

As a reference, a conventional control achieved by disabling the feed-forward part in the block diagram shown in Fig. 4 was tested. Fig. 15 shows the measured waveforms and DSP variables. As is evident from the waveforms, the primary side currents were almost balanced, unlike that in the case with the proposed control. This is because the PI control could

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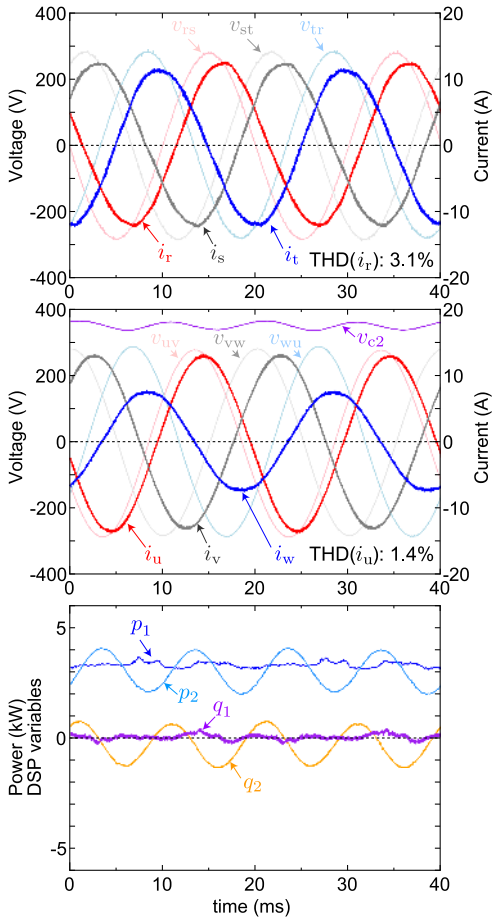

Fig. 15. Experimental waveforms for unbalanced resistive load with the conventional control.

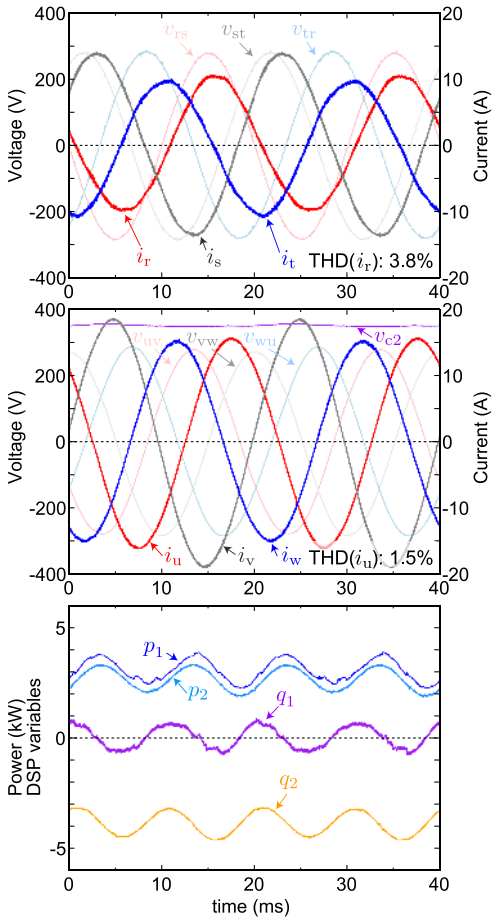

Fig. 16. Experimental waveforms for unbalanced inductive load with the proposed control.

not follow to compensate for the oscillating capacitor voltage. However, v_{c2} exhibited significant oscillation with the double-line frequency owing to the difference between p_1 and p_2.

3) Inductive Load Operation: An unbalanced inductive load achieved by a set of inductors and resistors was tested. Fig. 16 shows the waveforms and control variables in the DSP. The synchronous power control between p_1 and p_2 was verified. The variable q_2 contained a negative offset corresponding to the balanced reactive power component; however, the offset component was successfully removed, and as expected, only the double-line frequency component remained in q_1. Owing to the offset rejection, the primary side currents were lower than the secondary side currents.

4) Non-linear Load Operation: A three-phase diode rectifier with a large smoothing capacitor and series inductors on the ac-side was tested as a non-linear load. Fig. 17 shows the waveforms and control variables with the proposed harmonic current compensation using the SOGI-QSG. Highly distorted current waveforms were observed at the secondary side, and the sextuple line frequency component was observed in p_2. Meanwhile, the primary side currents were not distorted with the proposed method. The resulting p_1 was almost flat. The difference between p_1 and p_2 generated an oscillation of v_{c2} at the sextuple line frequency; however, its amplitude was comparatively low.

As a reference, the operation without the harmonic current compensation was tested. The measured waveforms are shown in Fig. 18. In contrast to the result with the proposed harmonic current compensation, the primary side currents were highly distorted, and the resulting p_1 followed p_2 adequately. This strategy appears to achieve a significantly lower ripple in v_{c2} than that obtained by enabling the harmonic current compensation control. However, the impact of the harmonic currents on the voltage ripples was comparatively lower than that of the fundamental unbalance. Therefore, it can be considered that the advantage of the improved current waveforms by the proposed control overcomes the disadvantage of the ripple increase in v_{c2}.

5) Load Step Change: A step load change was tested with a balanced resistive load. Fig. 19 shows the measured waveforms around the step change. Certain cell capacitor voltages, $v_{c1.rs3}$, $v_{c1.st3}$, and $v_{c1.tr3}$, and the secondary capacitor voltage, v_{c2}, were measured. There was no significant voltage drop in the cell capacitors; however, a marginal voltage drop was observed in the secondary capacitor voltage after the step load increase. A gradual response of the feedback compensation for the increased loss is likely to be the cause, although the synchronous power control follows the output power rapidly.

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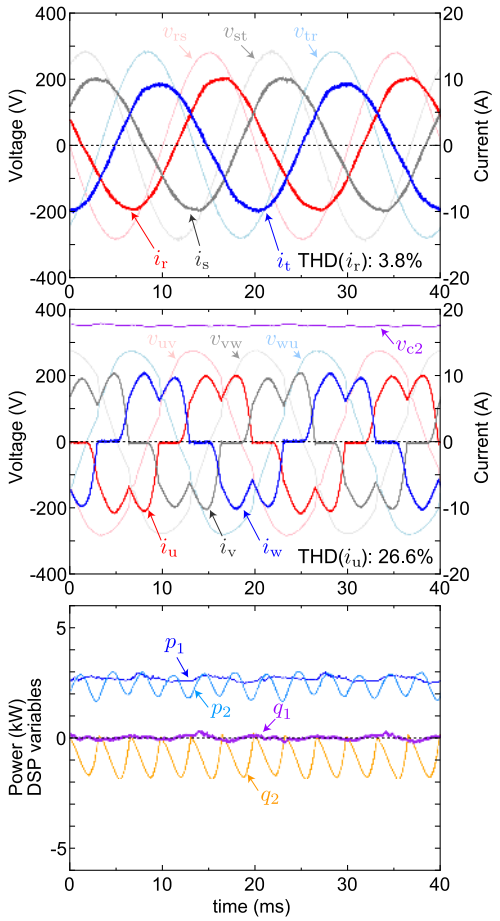

Fig. 17. Experimental waveforms for non-linear load with the proposed harmonic current compensation.

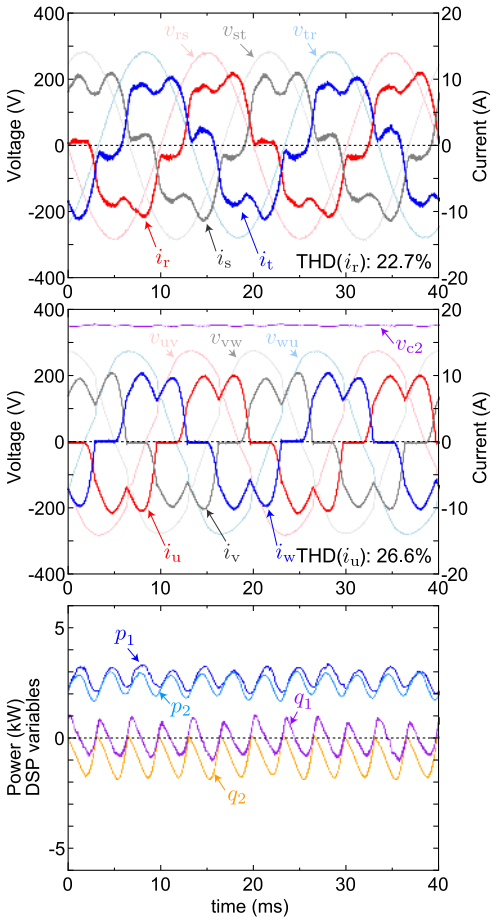

Fig. 18. Experimental waveforms for non-linear load without the proposed harmonic current compensation.

However, the loss can be comparatively low to the conversion power in the practical scale system and will not be a critical problem.

6) Operation in Unbalanced Voltage: As a severe operating condition, a grid voltage unbalance was tested with the balanced resistive load. The primary side voltage was supplied by Y-connected three AC power supplies and the voltage of a certain phase was set at 70% of that for the others. Their line-to-line voltages, $v_{\rm rs}$, $v_{\rm st}$, and $v_{\rm tr}$, were supplied to the system. The positive sequence detector for the primary side voltage was enabled for the experiments. With this setting, the resulting ratio of the negative sequence component to the positive sequence component in the line-to-line voltages was 11.1%.

Fig. 20 shows the measured waveforms and control variables. It was confirmed that almost pure sinusoidal currents were observed even with the strongly unbalanced grid voltage. However, the instantaneous power on the primary-side, p_1, was oscillating at the double-line frequency. As a result, a marginal voltage ripple was observed in C_2. The result indicates that a certain degree of the increase in the capacitance is required to ensure the operation with a strong unbalanced grid voltage.

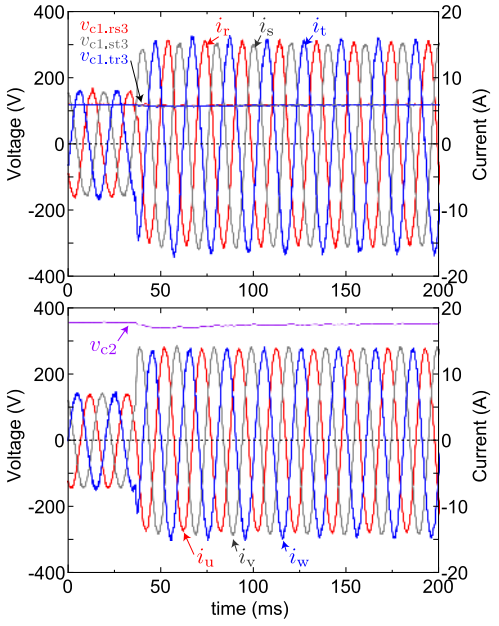

Fig. 19. Experimental waveforms for step change response. A balanced resistive load was applied in step, in addition to an additional balanced resistive load.

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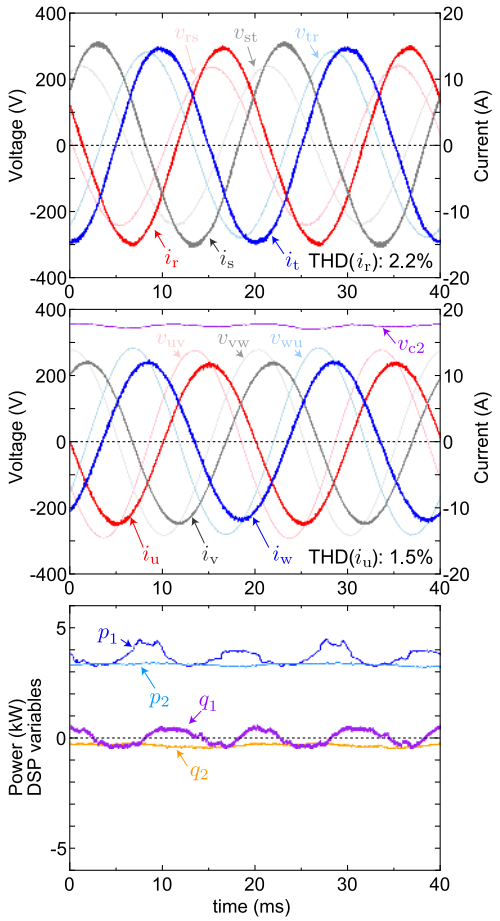

Fig. 20. Experimental waveforms for balanced resistive load with unbalanced primary side voltage. The positive sequence detector was enabled for the operation.

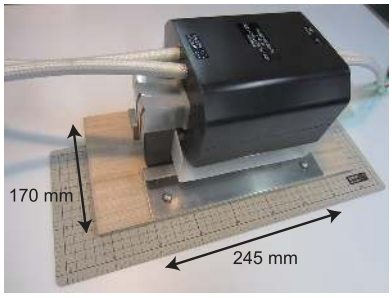

Fig. 21. Overview of fabricated 15-kVA transformer for loss evaluation.

V. DAB Converter Loss Comparison and Evaluation

The proposed control can reduce the required size of capacitors; however, the oscillating power flowing inside the system can cause increased stress on the components. In the SST configuration discussed in this paper, the DAB converter is the most critical part for system efficiency. This paper discusses the likely increase in loss in the DAB converter when the proposed OPC is applied to reduce C_1.

For the discussion, a 10-kW class DAB converter designed as the model of a practical-scale single cell for the 300-kVA SST discussed in Section III was fabricated. The specifications of the DAB converter and its components are listed in Table IV. Fig. 21 shows a high-frequency transformer used for the DAB. The windings are Urethane molded and have adequate insulation for application in the SST.

Fig. 22 shows the statically measured losses and efficiencies of the fabricated DAB converter. The loss characteristics agree well with the expected ones. There is a comparatively high offset loss owing to the transformer core loss and switching losses; moreover, the light-load losses are marginally high owing to the shorting of the device output capacitance. $P_{\mathrm{cell.rated}}$ is the preliminary power rating of the DAB converter, which is assumed to be 10 kW. With the proposed OPC, the average

TABLE IV
Specifications of DAB Converter for Loss Evaluation

Transformer	Nominal capacity	15.4 kVA
	Primary side winding	855 V, 20 kHz (Square wave)
	Secondary side winding	855 V, 18 A
	Equivalent series inductance (measured)	61 μH
	Insulation between windings	AC 22 kV (1 min.)
Semiconductor	Type	C2M0045170D
	Voltage rating	1700 V
	Current Rating	72 A
	On-state resistance	45 mΩ
Operation	Primary side dc voltage	855 V
	Secondary side dc voltage	855 V
	Frequency	20 kHz
	Dead-time	0.5 μs

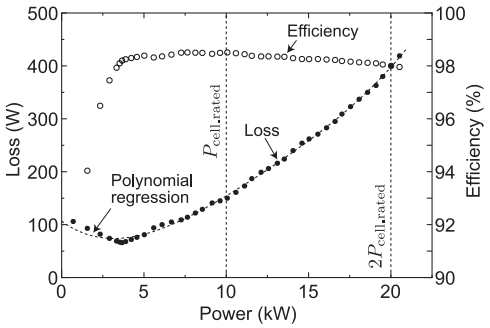

Fig. 22. Power losses and efficiencies of DAB converter with constant power references. The polynomial regression for the losses is also shown (dotted line).

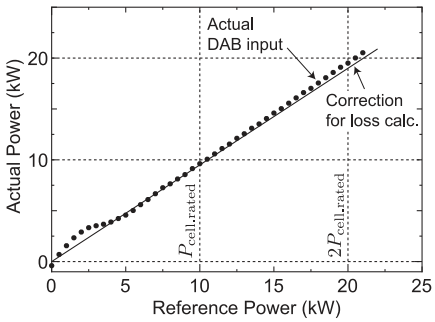

Fig. 23. Measured power input to DAB converter as a function of the supplied power reference. The correction factor for the loss calculation is also shown (solid line).

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conversion power does not change; however, the instantaneous power attains two times the power rating. Therefore, the loss was measured within the range of $2P_{\mathrm{cell.rated}}$. Fig. 23 shows the relationship between the reference power and actual input power. The reference power was converted into the phase angle difference by equation 3. The resulting input power was almost identical to the reference power.

The power loss, P_{loss}, can be expressed as a function of the conversion power, P_{dab}, as follows:

$$P_{\mathrm{loss}}\left(P_{\mathrm{dab}}\right)=\sum_{i=0}^{n} a_i \cdot {P_{\mathrm{dab}}}^{i}, \tag{13}$$

where n is the polynomial order. The coefficients, a_i, can be obtained by curve fitting; the fitted curve with a polynomial order of four is shown in Fig. 22. The power loss with the conventional control is expected to be equal to the statically measured loss.

The average loss with the proposed OPC, $P_{\mathrm{loss.OPC}}$, can be calculated for a specified conversion power, P_{dab}, by averaging the instantaneous power loss in a half line period, $T/2$, as

$$P_{\mathrm{loss.OPC}}=\frac{2}{T}\int_{0}^{T/2} P_{\mathrm{loss}}\left(p_{\mathrm{dab.OPC}}\right)dt, \tag{14}$$

where $p_{\mathrm{dab.OPC}}$ is the instantaneous conversion power expressed as

$$p_{\mathrm{dab.OPC}}=P_{\mathrm{dab}}\left(1-\cos 2\omega t\right). \tag{15}$$

From equations 13 to 15, $P_{\mathrm{loss.OPC}}$ can be expressed by

$$P_{\mathrm{loss.OPC}}\left(P_{\mathrm{dab}}\right)=\sum_{i=0}^{n} a_i \cdot {P_{\mathrm{dab}}}^{i} \cdot \frac{2}{T}\int_{0}^{T/2}\left(1-\cos 2\omega t\right)^{i} dt. \tag{16}$$

From equations 16 and 13, it can be determined that the proposed OPC has identical polynomial loss coefficients as those of the conventional control for $i=0$ and 1 (offset and linear components), albeit higher coefficients for $i>1$.

Fig. 24 shows the reference power and the calculated instantaneous power loss based on the loss characteristics shown in Fig. 22 in a half line period, for the conventional and proposed controls, and for two average conversion power cases. It is apparent that the power loss with the conventional control is constant in a line period because the reference power remains constant; however, the power loss with the proposed control changes as the reference power changes. The average of $p_{\mathrm{loss.OPC}}$ becomes $P_{\mathrm{loss.OPC}}$, and $P_{\mathrm{loss.OPC}}$ can be higher than the loss with the constant reference power, P_{loss}, in most cases.

Fig. 25 shows the experimentally measured losses when the DAB converter is operated with the oscillating power reference, which simulates the proposed OPC. The sinusoidal reference power

$${p_{\mathrm{dab}}}^{*}={P_{\mathrm{dab}}}^{*}\left(1-\cos 2\omega t\right), \tag{17}$$

was provided, where ${P_{\mathrm{dab}}}^{*}$ is the average reference power. In high-load operations, the losses were high with the proposed control than those with the conventional control. The increase in loss with the OPC at the rated power was 17%. This is

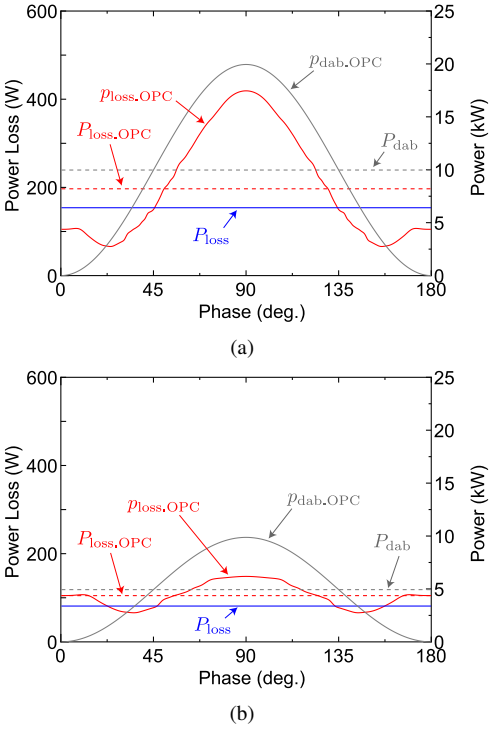

Fig. 24. Instantaneous power loss with the proposed OPC, $p_{\mathrm{loss.OPC}}$, in a half line cycle, its average, $P_{\mathrm{loss.OPC}}$, and loss with conventional control, P_{loss}, with (a) Rated power (9.97 kW) operation, and (b) 4.94 kW operation. The reference power for the OPC, $p_{\mathrm{dab.OPC}}$, and its average (and therefore the reference power for the conventional control), P_{dab}, are also shown.

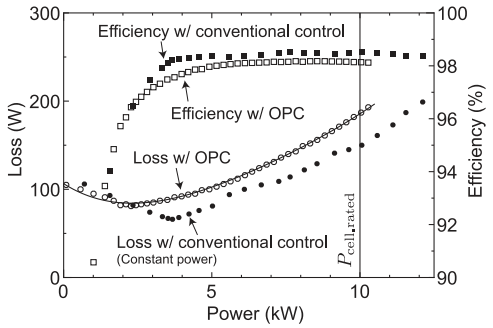

Fig. 25. Power losses and efficiencies of DAB converter with conventional control and proposed control, OPC. The loss estimation based on the static loss characteristics according to equation 16 is also shown (solid line).

because the static loss of the DAB converter in the high-load operating range increases as a function of the conversion power with an exponent higher than unity; therefore, the average loss with power oscillation is higher than that without power oscillation. However, it can be considered that the amount of increase was not severe in this case. The major loss component of the DAB converter was the offset loss, which did not increase with the proposed control.

The loss calculated according to equation 16 is also shown in the same figure. The actual average conversion power, P_{dab}, is not equal to ${P_{\mathrm{dab}}}^{*}$, as shown in Fig. 23. Therefore, a linear correction shown in Fig. 23 is applied to illustrate the calculated loss curve with the experimental results. The

tendency of the measured losses with the proposed OPC was consistent with the calculation; however, a marginal difference was observed; this could have been owing to the accumulative error in the polynomial approximation used in the calculation.

From the results, it was verified that the loss increase by the shorting of the device output capacitance in the light-load range impacted the loss increase with the OPC for all the power range. This is consistent because the light-load condition is always used with the OPC. A technique to prevent the application of the light-load operation is to modulate a high-power operation and suspension period; this is the so-called burst mode [38], [39]. It can be an effective method for improving the performance.

The transformer was not designed for handling $2P_{\mathrm{cell.rated}}$; however, it is considered that the instantaneous power of $2P_{\mathrm{cell.rated}}$ can be handled without major modification because the maximum flux density does not change by the proposed control. However, with the proposed control, the power oscillation increases the rms values of the winding currents by approximately 22% compared to those with the conventional control. This is a reason for the increase in loss discussed in this section. The winding losses are proportional to the square of the current in rms. Therefore, if similar transformer thermal profiles are required in both the control approaches, a certain increase in the transformer volume is likely with the oscillating control approach owing to the increase in winding loss compared to the conventional control approach; however, the transformer volume need not be increased to two times. Furthermore, the control approach could be considered in the transformer design in order to optimize the volume-loss trade-off and obtain comparable designs for both the control approaches.

VI. Conclusion

The phase-separated power conversion of the CHB configuration results in strong double-line frequency power oscillations in the smoothing capacitors. Therefore, a considerably high capacitance is required to maintain the voltage ripples within an acceptable range. This paper reviews the control methods of CHB-based SSTs for preventing the single-phase power oscillations applied to CHB capacitors; moreover, it proposes the addition of an unbalance power control technique for three-phase input and output systems. The feasibility of these methods was verified through experiments with a 6-kVA laboratory prototype.

The low-frequency components in the capacitor voltages can be removed by the controls; therefore, the switching ripple is the key factor that decides the extent of downsizing that can be achieved for the capacitors. In CHB-based AC/DC converters, the switching frequency of each cell converter can be lowered by applying a carrier phase shift; however, remarkable capacitance reduction is likely even for a sufficiently low switching frequency. There is a trade-off between capacitance reduction and switching loss reduction. The recent progress of semiconductor technologies is likely to shift this trade-off to a lower capacitance with a higher switching frequency. Meanwhile, a certain amount of energy storage in the common dc-bus capacitor is required to achieve power quality improvement capabilities. This paper concludes that unbalance compensation for the load current essentially requires certain energy storage. However, harmonics rejection can be achieved with considerably lower capacitance. The unbalance compensation for the source voltage also requires certain energy storage. However, the increase in capacitance required for the voltage unbalance observed in normal operations is low. Meanwhile, a special control for short-time abnormal conditions can be required.

Another trade-off exists between capacitor downsizing and transformer loss. This paper discusses the likely increase in loss owing to the oscillating power and concluded that the increase in loss is not severe, owing to the typical loss characteristics of a DAB converter. From the case study discussed in this paper, the capacitance for the CHB side can be one-tenth of that without the OPC even with a sufficiently low switching frequency; the total volume can be estimated to be approximately 13%. Meanwhile, the loss evaluation of the DAB converter with the practical scale model indicated that the increase in loss with the OPC was 17% in this case. The size of the transformer depends on the frequency, insulation level [40], losses and thermal profiles and can be optimized [41], [42]. In addition, the design of the transformer can be optimized for the oscillating power, and the overall system evaluation should be discussed. However, the impact of capacitor size reduction is likely to be significantly higher than that of transformer size increase, which can be caused by the increase in loss.

References

[1] S. Xu, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, No. 3, pp. 186–198, 2013.

[2] J. W. Kolar, and G. Ortiz, "Solid-state-transformers: key components of future traction and smart grid systems", *Proceedings of the International Power Electronics Conference – ECCE Asia (IPEC 2014)*, Hiroshima, Japan, May 18–21 (2014)

[3] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today ' s and future distribution grids," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.

[4] L. Ferreira Costa, G. De Carne, G. Buticchi and M. Liserre, "The smart transformer: a solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electronics Magazine*, vol. 4, no. 2, pp. 56–67, June 2017.

[5] H. Chen and D. Divan, "Design of a 10-kVA soft-switching solid-state transformer (S4T)," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5724–5738, July 2018.

[6] H. Chen, A. Prasai and D. Divan, "Dyna-C: a minimal topology for bidirectional solid-state transformers," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 995–1005, Feb. 2017.

[7] T. Guillod, F. Krismer and J. W. Kolar, "Protection of MV converters in the grid: the case of MV/LV solid-state transformers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 393–408, March 2017.

[8] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage multilevel converters," *2013 IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Denver, CO, pp. 359–366, 2013.

[9] X. She, X. Yu, F. Wang and A. Q. Huang, "Design and demonstration of a 3.6 kV–120 V/10 kVA solid-state transformer for smart grid application", *2014 IEEE Applied Power Electronics Conference and Exposition (APEC 2014)*, Fort Worth, TX, pp. 3429–3436, 2014.

[10] J. Shi, W. Gou, H. Yuan, T. Zhao and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer", *IEEE Transactions on Power Electronics*, vol. 26, No. 4, pp. 1154–1166, 2011.

[11] T. Zhao, G. Wang, S. Bhattachaya, A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer", *IEEE Transaction on Power Electronics*, vol. 28, No. 4, pp. 1523–1532, 2013.

[12] Z. Zhang, H. Zhao, S. Fu, J. Shi and X. He, "Voltage and power balance control strategy for three-phase modular cascaded solid stated transformer", *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, pp. 1475–1480, 2016.

[13] X. Wang, J. Liu, S. Ouyang, T. Xu, F. Meng and S. Song, "Control and experiment of an H-bridge-based three-phase three-stage modular power electronic transformer," *in IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2002–2011, March 2016.

[14] M. Liserre, M. Andresen, L. Costa, G. Buticchi, "Power routing in modular smart transformers: active thermal control through uneven loading of cells", *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, 2016.

[15] Y. Ko, M. Andresen, G. Buticchi and M. Liserre, "Power routing for cascaded H-bridge converters", *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9435–9446, 2017.

[16] J. Tian, C. Mao, D. Wang, S. Nie and Y. Yang, "A short-time transition and cost saving redundancy scheme for medium-voltage three-phase cascaded H-bridge electronic power transformer," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9242–9252, Nov. 2018.

[17] T. Shimizu, Y. Jin and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Transactions on Industry Applications*, vol. 36, no. 5, pp. 1419–1429, Sep/Oct 2000.

[18] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos and D. Boroyevich, "Study of energy storage capacitor reduction for single phase PWM rectifier," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, pp. 1177–1183, 2009.

[19] H. Li, K. Zhang, H. Zhao, S. Fan and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1308–1319, March 2013.

[20] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1855–1865, April 2015.

[21] T. Isobe, D. Shiojima, K. Kato, Y. R. R. Hernandez, and R. Shimada, "Full-bridge reactive power compensator with minimized-equipped capacitor and its application to static Var compensator," *IEEE Trans. on Power Electron.*, vol. 31, No. 1, pp. 224–234, 2016.

[22] T. Isobe, L. Zhang, R. Iijima, H. Tadano, Y. Kawanami, K. Terazono, "Experimental verification of capacitance reduction in MMC-Based STATCOM", *in proceeding of 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, United States, 18–22 September, 2016.

[23] T. Isobe, L. Zhang, H. Tadano, J. A. Suul, M. Molinas "Control of DC-capacitor peak voltage in reduced capacitance single-phase STATCOM," *in Proceedings of the Seventeenth IEEE Workshop on Modeling and Control for Power Electronics*, COMPEL 2016, Trondheim, Norway, 27–30, June 2016.

[24] T. Isobe, R. A. Barrera-Cardenas, and H. Tadano, "Capacitor size reduction of MMC-based STATCOM for medium voltage power distribution network," *EPE2016 ECCE Europe*, Karlsluhe, Germany, 5–9 September, 2016.

[25] K. M. Yoo, K. D. Kim and J. Y. Lee, "Single- and three-phase PHEV onboard battery charger using small link capacitor," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 3136–3144, 2013.

[26] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli and D. Diaz, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.

[27] T. Zhao, X. She, S. Bhattacharya, G. Wang, F. Wang, A. Huang, "Power synchronization control for capacitor minimization in Solid State Transformers (SST)", *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 17–22 September, 2011.

[28] H. Qin and J. W. Kimball, "Closed-loop control of DCDC dual-active-bridge converters driving single-phase inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 1006–1017, 2014.

[29] B. Zhang, X. Yang, L. Qiao, L. Huang, X. Ma, P. Xu, X. Hao, "Voltage control and fluctuation suppression of the three-phase SST with DC bus in dual rotating reference frames", *IEEE International Power Electronics and Motion Control Conference (IPEMC)*, Hefei, China, 2016, pp. 1084–1087.

[30] T. Isobe, Z. He, Y. Zou and H. Tadano, "Control of solid-state-transformer for minimized energy storage capacitors", *Energy Conversion Congress and Exposition (ECCE), 2017 IEEE*, Cincinnati, OH, 1–5 October, 2017.

[31] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DCDC converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[32] M. H. Kheraluwala, R. W, Gascoigne, D. M, Divan, E. Bauman, "Performance characterization of a high-power dual active bridge DC/DC converter", *IEEE Transactions on Industry Applications*, vol. 28, No. 6, pp. 1294-1301, Nov./Dec. (1992).

[33] P. Rodrguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," *in Proceedings of the 37th Annual IEEE Power Electronics Specialists Conference, PESC'06*, Jeju, Korea, 18-22 June 2006.

[34] H. Akagi, Y. Kanazawa and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Transactions on Industry Applications*, vol. IA-20, no. 3, pp. 625–630, May 1984.

[35] R. Teodorescu, F. Blaabjerg, M. Liserre, P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *in IET Proceedings - Electric Power Applications*, vol. 153, No. 5, pp. 750–762, September 2006.

[36] X. Yuan, W. Merk, H. Stemmler, J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *in IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp 523–532, March/April 2002.

[37] F. J. Rodriguez, E. Bueno, M. Aredes, L. G. B. Rolim, F. A. S. Neves and M. C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," *in Proceedings of the 34th Annual Conference of the IEEE Industrial Electronics Society, IECON2008,* Orlando, FL, pp. 176–181, 2008.

[38] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 790–804, Feb. 2015.

[39] G. G. Oggier and M. Ordonez, "High-efficiency DAB converter using switching sequences and burst mode," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2069–2082, March 2016.

[40] Q. Chen, R. Raju, D. Dong and M. Agamy, "High frequency transformer insulation in medium voltage SiC enabled air-cooled solid-state transformers," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, pp. 2436–2443, 2018.

[41] R. Barrera-Cardenas, T. Isobe, K. Terazono, and H. Tadano, "Design and experimental verification of a DAB medium frequency transformer for a 6.6kV/200V solid state transformer," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, pp. 3431–3438, 2018.

[42] M. Leibl, G. Ortiz and J. W. Kolar, "Design and experimental analysis of a medium-frequency transformer for solid-state transformer applications," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 110–123, March 2017.

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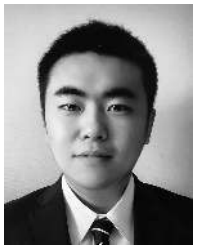

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