

# Control of UPQC Based on Steady State Linear Kalman Filter for Compensation of Power Quality Problems\*

*Sayed Javed Alam and Sabha Raj Arya\**

(Department of Electrical Engineering, Sardar Vallabhai National Institute of Technology,  
Suart 395007, India)

**Abstract:** A frequency lock loop (FLL) based steady state linear Kalman filter (SSLKF) for unified power quality conditioner (UPQC) control in three-phase systems is introduced. The SSLKF provides a highly accurate and fast estimation of grid frequency and the fundamental components (FCs) of the input signals. The Kalman filter is designed using an optimized filtering technique and intrinsic adaptive bandwidth architecture, and is easily integrated into a multiple model system. Therefore, the Kalman state estimator is fast and simple. The fundamental positive sequence components (FPSCs) of the grid voltages in a UPQC system are estimated via these SSLKF-FLL based filters. The estimation of reference signals for a UPQC controller is based on these FPSCs. Therefore, both active filters of a UPQC can perform one and more functions towards improving power quality in a distribution network. In addition to the SSLKF-FLL based algorithm, a bat optimization algorithm (based on the echolocation phenomenon of bats) is implemented to estimate the value of the proportional integral (PI) controller gains. The bat algorithm has a tendency to automatically zoom into a region where a promising alternative solution occurs, preventing the solution from becoming trapped in a local minima. The complete three-phase UPQC is simulated in the Matlab/Simulink platform and the hardware is tested under various power quality problems.

**Keywords:** Damping factor, echo-location, FPSC, harmonics, ITSE, SSLKF-FLL, power quality

## 1 Introduction

The fast development of nonlinear loads in electrical systems is resulting in a deterioration of both the voltage and current power quality (PQ) at the point of common coupling (PCC)<sup>[1]</sup>. The nonlinear loads are mostly based on power electronics devices<sup>[2]</sup>. Similarly, the growth of digital electronics and microprocessor-based control has increased the number of critical loads that require ideal sinusoidal input signals to function appropriately<sup>[3]</sup>. Disruptions to the grid voltage affect the critical industrial load, resulting in frequent tripping<sup>[4]</sup>. Power electronics based flexible AC transmission system (FACTS) devices are attractive tools for enhancing the reliability and control of reactive power in transmission systems<sup>[5]</sup>. These devices offer greater system flexibility and respond quickly to

any disturbances<sup>[6]</sup>. The unified power flow controller (UPFC) is chosen for regulation of bus voltage and control of power flow in a transmission system via a common DC link<sup>[7]</sup>. Similar FACTS devices is configured, such as shunt, series, and hybrid, for improving the PQ in distribution power system<sup>[8]</sup>. In these systems, a unified power quality controller (UPQC) is a hybrid device configured similarly to a UPFC, which combines the functionality of shunt and series active power filters (APF)<sup>[9]</sup>. The shunt APF compensates for current based disturbances, while the series APF suppresses voltage based PQ problems. Simultaneously, the UPQC mitigates reactive current components of the load and improves the power factors of the system<sup>[10]</sup>. Therefore, the UPQC is acknowledged as one of the most powerful devices for mitigating PQ problems.

A comprehensive review of UPQC control structures are discussed in Refs. [10-11]. Most methods used to regulate UPQC control are based on time domains as they involve easy calculations and fewer memory space requirements<sup>[12]</sup>. The majority of techniques frequently used in UPQC include instantaneous

Manuscript received October 13, 2019; revised February 9, 2020; accepted May 11, 2020. Date of publication June 30, 2020; date of current version June 12, 2020.

\* Corresponding Author, Email: sabharaj79@gmail.com

\* Supported by the Science and Engineering Research Board-New Delhi Project-Extra Mural Research Funding Scheme(SB/S3/EECE/030/2016).

Digital Object Identifier: 10.23919/CJEE.2020.000011

reactive power theory (IRPT)<sup>[13]</sup>, synchronous reference frame theory (SRF)<sup>[14]</sup>, the unit vector template method<sup>[15]</sup>, and instantaneous symmetrical components theory (ISCT)<sup>[16]</sup>. Among these, the SRF method is the simplest owing to its simple structure and low computation cost. However, the SRF algorithm still uses low pass filter (LPF) dependency on numerical filter, which creates delay in the signal<sup>[17]</sup>. The retrieval of fundamental components of the grid voltage is a vital requirement for injecting a balanced positive sequence current under asymmetric voltage or harmonic distortion conditions<sup>[18]</sup>. In Ref. [19], the use of conventional second order generalized integrator frequency lock loop (SOGI-FLL) filters for extracting fundamental components (FCs) is suggested, they provide high accuracy when the grid voltage is smooth. However, the synchronization error is unacceptable under distorted grid conditions due to the limited attenuation capacity of the second order generalized integrator (SOGI) filters<sup>[20]</sup>, these are highly vulnerable to the presence of lower order harmonics and DC offset in the system<sup>[21]</sup>. Some modifications, on the basis of conventional PLL structures, are suggested in the literature resulting in advanced SOGI-PLLs, their performance is further improved by employing Kalman filter techniques<sup>[22]</sup>. Similarly, a steady state linear Kalman filter (SSLKF) based frequency lock loop (FLL) is been proposed for extracting FCs under distorted conditions, which is superior to conventional SOGI filters<sup>[23]</sup>. This includes a linear Kalman filter (LKF) for extracting the in-phase FC signal and its quadrature and a frequency estimation of the input signals. The SSLKF-FLL significantly improves DC offset filtering and has a lower computational cost and faster dynamic response, compared to the standard SOGI-FLL. This characteristic plays a major role in the design of the aforementioned classical control algorithm to better mitigate PQ issues for a UPQC system.

In combination with the SSLKF control algorithm, PQ issues are continuously and effectively mitigated when the UPQC DC link voltage is maintained at the desired magnitude, usually via control schemes and, specifically, a proportional integral (PI) controller. The PI controller gains, filtering parameters, and other gains of the UPQC are calculated using a linearized

mathematical model of the system. However, such design parameter values might not provide satisfactory results under dynamic working conditions or when the system is a highly nonlinear complex structure. To overcome this, the application of genetic algorithms is proposed by researchers for the optimal choice, location, and sizing of FACTS devices in deregulated power systems<sup>[24]</sup>. In Ref. [25], a nature-inspired bat algorithm (BA), based on the echolocation phenomenon used by bats, is implemented in a static VAR compensator (SVC) for power system stability enhancement. Similarly, the BA in Ref. [26] is adopted for tuning the PID-controller design variables in a biological wastewater treatment plant. The BA can automatically zoom into a region where a promising alternative solution has been found, using echolocation and frequency tuning techniques to solve problems<sup>[27]</sup>. The control parameters used in the BA can be varied throughout the iterative process, it provides a way to automatically transition from exploration and exploitation as the optimal solution approaches<sup>[28]</sup>. The BA has several further advantages, such as speed, accuracy, flexibility, and ease of execution. It can efficiently resolve a broad variety of issues and highly nonlinear problems<sup>[29]</sup>. This advantage of the BA is useful for calculating PI controller gains to achieve better performance of a UPQC with highly nonlinear loads.

In this paper, a SSLKF control based FLL algorithm is developed for a three-phase UPQC. The SSLKF is placed in front of the FLL in order to obtain sinusoidal waveforms that match the input signal as closely as possible, even when the voltage is highly distorted. This ensures fast and low distortion operation of the FLL and hence of the UPQC system. The computational burden is relatively modest, as the Kalman filter is fully linear. The fundamental components of the current, voltage, and angle can be obtained from the initial state via the Kalman filter. Consequently, this method is fast and simple. Two sets of SSLKF-FLLs are used for the extraction of the fundamental positive sequence components (FPSCs) from the common coupling point bus, these further help to build reference signals for both APFs. The reference currents generated from the Kalman filter based control for the shunt compensator are sinusoidal and balanced. Similarly, the series APF is used to maintain the

sinusoidal load voltage at a required magnitude. In addition to a SSLKF-FLL based control algorithm, the BA is implemented to calculate the gain of the PI-controller, improving the system response. The performance analysis of the UPQC is validated under commonly encountered dynamic conditions, such as voltage, sag/swell, load unbalancing, and distortion in the three-phase supply system.

## 2 UPQC configuration and design

The complete power circuit diagram is shown in

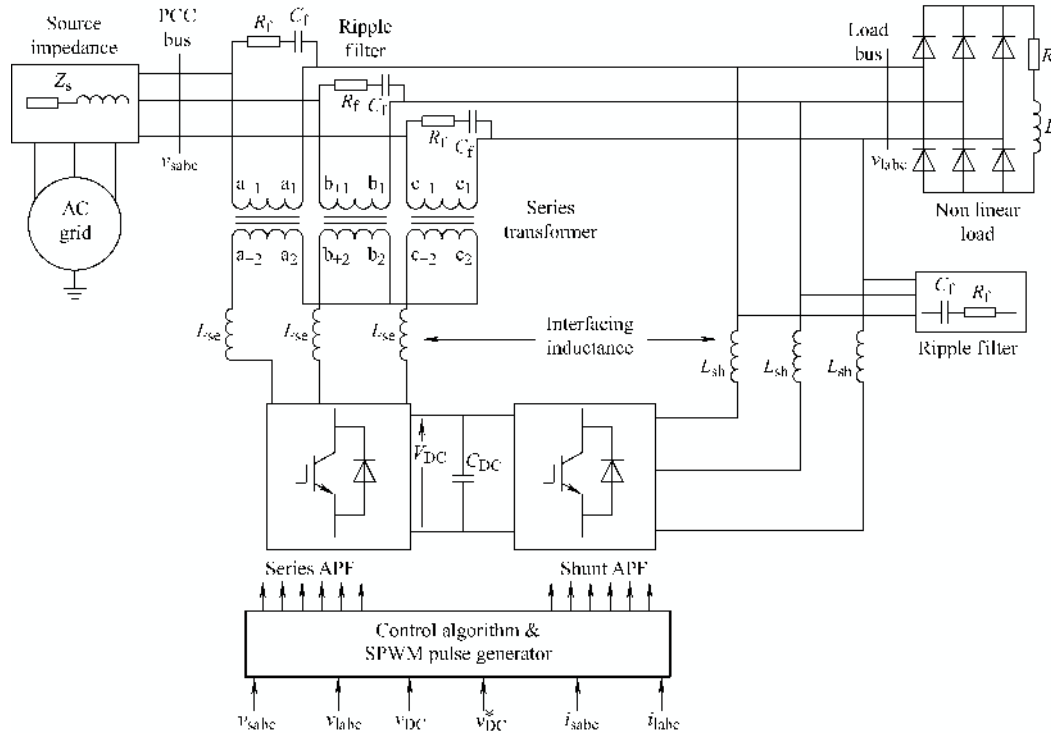


Fig. 1 Configuration of UPQC

Similarly, the shunt compensator must compensate for current-related PQ problems on the load side via the shunt APF. Each APF consists of six insulated gate bipolar transistor (IGBT) switches. The series and shunt APFs interface with the grid via the interfacing inductors  $L_{se}$  and  $L_{sh}$ , respectively. The series injection transformer is employed to insert the necessary compensating voltages produced by the series APF, providing the desired sinusoidal voltages to sensitive loads. The supply side impedance of the grid is taken as  $Z_s$ . The ripple filters ( $R_f$ ,  $C_f$ ) are designed to evade the harmonics generated when both APFs are switched.

The UPQC system design process begins from the consideration of system parameters, such as nominal voltage, frequency, load power rating, etc. The shunt

Fig. 1. The main components of the UPQC system are shunt compensator (shunt APF), series compensator (series APF), attached alongside a DC capacitor ( $C_{DC}$ ), series and shunt interfacing inductors ( $L_{se}$ ,  $L_{sh}$ ) and ripple filters ( $R_f$ ,  $C_f$ ). The DC bus voltage is controlled via the proposed SSLKF-FLL algorithm, with proportional integral (PI) control and sinusoidal pulse width modulation (SPWM) switching techniques. As a series compensator, voltage-related PQ problems on the source side must be compensated for using the series APF.

compensator is configured to mitigate current harmonics and full-load reactive power. In sequence to incorporate the required series compensator design, e.g., turns ratio ( $N$ ), injection DVR transformer, DC bus capacitor ( $C_{DC}$ ), and series interfacing inductor ( $L_{se}$ ). The other specifically designed components are the shunt interfacing inductors ( $L_{sh}$ ) and ripple filters ( $R_f$ ,  $C_f$ ). The design of the UPQC system is given below.

### 2.1 DC link voltage ( $V_{DC}$ )

The magnitude of the DC-link voltage is calculated based on modulation index ( $m$ ) and grid line voltage ( $V_L$ ) and expressed as <sup>[2,18]</sup>

$$V_{DC} = \frac{2\sqrt{2}V_L}{\sqrt{3}m} \quad (1)$$

## 2.2 DC bus capacitor ( $C_{DC}$ )

The DC capacitor bus value builds upon the instantaneous energy of the shunt compensator during the transients. The factors that should be considered during transient operation are the overloading factor ( $a$ ), phase voltage ( $V_{ph}$ ), shunt APF phase current ( $I_{sh}$ ), variation in energy dynamics ( $k$ ), and  $t$  is the time through which the DC link voltage is to be recovered. According to the conservation of energy principle, the  $C_{DC}$  is formulated as

$$C_{DC} = \frac{3kaV_{ph}I_{sh}t}{0.5(V_{DC}^2 - V_{DC1}^2)} \quad (2)$$

where  $V_{DC}$  is the nominal DC voltage equal to the reference level DC quantity and  $V_{DC1}$  is the minimum DC voltage value.

## 2.3 Shunt interfacing inductor ( $L_{sh}$ )

This relies on the current ripple ( $I_{cr,pp}$ ), switching frequency ( $f_{sw}$ ), overloading factor ( $a$ ), modulation index ( $m$ ), DC link voltage ( $V_{DC}$ ), and is selected as

$$L_{sh} = \frac{\sqrt{3}mV_{DC}}{12af_{sw}I_{cr,pp}} \quad (3)$$

## 2.4 Series injection transformer

This is a single unit three-phase transformer in which series APF side winding are joined together in a star arrangement and line side windings of the transformer are attached to each line in series, as demonstrated in Fig. 1. Let 'x' be the maximum p.u. swell/sag calculated when the reference load voltage ( $V_L$ ) is taken with supply voltage ( $V_s$ ). The series transformer ( $S_{SE}$ ) rating is based on the injected voltage ( $V_{inj}$ ), DC bus voltage of the APF ( $V_{APF}$ ), current carried during sag ( $I_{se,sag}$ ), and turns ratio ( $N$ ) and formulated as

$$\begin{cases} x = \frac{V_s}{V_L} & N = \frac{V_{APF}}{V_{inj}} & S_{SE} = 3V_{inj}I_{se,sag} \\ I_{se,sag} = \frac{P_L}{3V_{ph}(1-x)} \end{cases} \quad (4)$$

## 2.5 Series interfacing inductor ( $L_{se}$ )

It is calculated using the ripple current at swell condition ( $I_{cr,swell}$ ), turns ratio ( $N$ ), overloading factor

( $a$ ), modulation index ( $m$ ), and switching frequency ( $f_{sw}$ ) and the DC link voltage can be given as

$$\begin{cases} L_{se} = \frac{\sqrt{3}mV_{DC}N}{12af_{sw}I_{cr,swell}} \\ I_{se,swell} = \frac{P_L}{3V_{ph}(1+x)} \end{cases} \quad (5)$$

## 2.6 Ripple filters ( $R_f, C_f$ )

A first order high-pass filter designed and calibrated for filtering out the higher frequency noise at half of the switching frequency. The time constant for a ripple filter should be very small compared to the fundamental time period ( $T$ ),  $R_f \times C_f \ll T/10$ , where  $R_f$  and  $C_f$  are the filter resistance and capacitance, respectively.

## 3 Control strategy

The complete control strategy for generalized UPQC is illustrated in Fig. 2. Here, the reference signal generation for both APFs is broadly illustrated using SSLKF-FLL. Fig. 2 depicts the block diagram of a SSLKF based FLL filter. The SSLKF-FLL is used to extract the FCs from the PCC voltage. Subsequently, these signals are used to generate reference signals for both the shunt and series compensators. Finally, the BA optimization technique is helpful in tuning the PI controller gains, rather than tuning the gains via a trial and error (manual) method. This section includes each aspect of the control strategy, including the BA for PI gains tuning.

### 3.1 Fundamental component extraction using SSLKF-FLL

Fig. 2 shows the block diagram of a SSLKF based FLL filter. It is inherently a discrete time domain algorithm that involves a LKF to extract the in-phase FCs and quadrature of the input signal. Simultaneously, the FLL circuit is used to estimate the frequency of the system. The Kalman filter is used to extract unknown variables from the noisy and linearly related states of the linear dynamic system. The primary distinction between the SSLKF-FLL and conventional SOGI is that some computationally demanding recursive equations are used to update the Kalman gains. The grid frequency,  $\omega$ , estimation

depends only upon the gains,  $\lambda$ . Therefore, as the steady-state grid frequency shows a slight variation across the nominal frequency, it can be analyzed that the steady-state values of  $\lambda$  has minor modifications to their nominal frequency. The SSLKF-FLL provides a significant improvement to DC offset filtering, with less computational burden and a faster dynamic response<sup>[23]</sup> compared to standard SOGI-FLL.

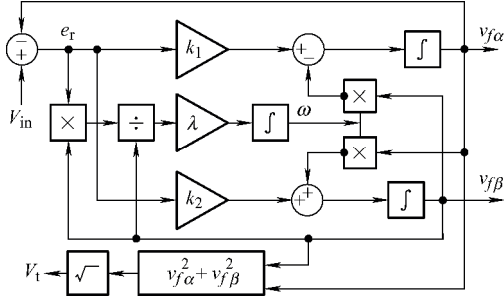


Fig. 2 Proposed steady state linear Kalman filter based frequency lock loop structure

Let  $\omega$  in Fig. 2 be constant. Therefore, the transfer functions relating the output signals,  $v_{f\alpha}$  and  $v_{f\beta}$ , to the input signal,  $V_{in}$ , can be obtained as

$$TF_{\alpha} = \frac{v_{f\alpha}}{V_{in}} = \frac{sk_1 - k_2\omega}{s^2 + sk_1 + \omega(\omega - k_1)} \quad (6)$$

$$TF_{\beta} = \frac{v_{f\beta}}{V_{in}} = \frac{sk_2 + k_1\omega}{s^2 + sk_1 + \omega(\omega - k_2)} \quad (7)$$

Based on the SOGI-FLL tuning conditions,  $\omega = \omega_n = 100\pi$  rad/s is selected for the computation of the gain parameters of SSLKF-FLL. By defining  $k_1 = k\omega$ ,  $k_2 = 2\omega_n - \sqrt{4\omega_n^2 + (k_1)^2}$ ,  $\lambda$ -Kalman gain, nominal frequency and damping factor ( $\zeta = 1/\sqrt{2}$ ) according to the preferred dynamic behavior, the SSLKF-FLL controls are chosen as  $k_1 = 100\sqrt{2}\pi$ ,  $k_2 = -141.2$ , and  $\lambda = -1000$ .

For different combinations of damping factor and Kalman parameters ( $k_1, k_2$ ), bode plots of the in-phase signal ( $v_{f\alpha}$ ) of the SSLKF with respect to supply signal ( $V_{in}$ ) are shown in Fig. 3. Similarly, the bode plot of the quadrature ( $v_{f\beta}$ ) components can be plotted with the help of Eq. (7). Here,  $\omega = \omega_n = 100\pi$  rad/s is selected. Note that the phase structure of the SSLKF, shown in Fig. 3, behaves as a band pass filter for a damping factor  $\zeta = 1/\sqrt{2}$ , which is more stable than the other damping factors. However, the quadrature components of the SSLKF behave like a low pass filter.

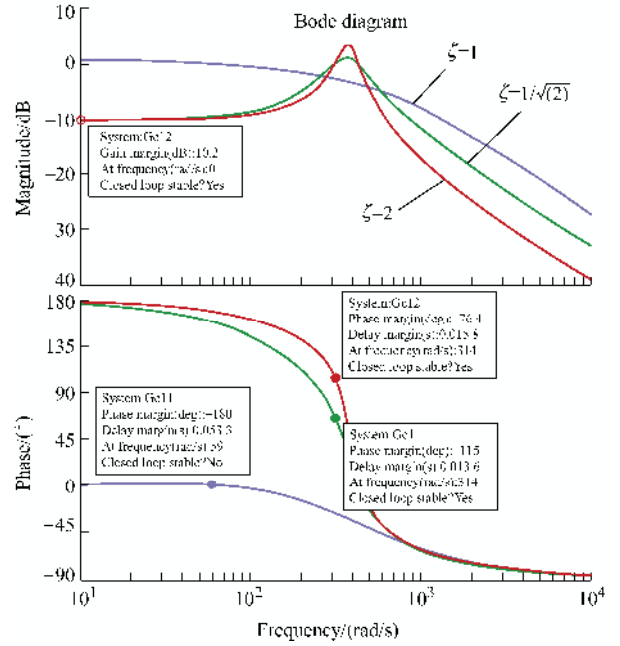


Fig. 3 Bode plots of the SSLKF-FLL for in-phase component ( $v_{f\alpha}$ ) with respect to input signal ( $V_{in}$ )

From Fig. 3, it can be concluded that the SSLKF-FLL yields a relatively greater DC offset and better harmonic rejection capability. These features can be attributed to the second control gain (the  $\beta$ -axis gain) of the SSLKF-FLL. Therefore, it has a slightly greater and more damped dynamic response than the SOGI-FLL.

### 3.2 Reference signal generation using SSLKF-FLL for UPQC

The development of the reference signal for UPQC relies on the fundamental positive sequence components (FPSCs) of the PCC signals. The separation of the FPSCs is a key task for the generation of reference signals in UPQC control. In this paper, the FPSCs are estimated using the SSLKF-FLL, with a positive sequence transformation matrix,  $T^+$ , illustrated in Eqs. (8)-(9). As can be observed from Fig. 2, the SSLKF-FLL provides fundamental in-phase ( $v_{f\alpha}$ ) and quadrature ( $v_{f\beta}$ ) version components of the input signal ( $V_{in}$ ).

To extract the FPSCs from the input voltages ( $v_{sabc}$ ), a Kalman filter is employed, shown in Fig. 4. The three-phase voltages ( $v_{sa}$ ,  $v_{sb}$ , and  $v_{sc}$ ) are transformed to two-phase voltages ( $\alpha$ - $\beta$  frame) using Clark's transformation matrix. The  $\alpha$  components,  $v_{\alpha}$ , and  $\beta$  components,  $v_{\beta}$ , of the voltages are filtered using SSLKF-FLL filters to estimate the fundamental ( $v_{f\alpha}, v_{f\beta}$ ) and quadrature components ( $qv_{f\alpha}, qv_{f\beta}$ ). The relationship between the FPSCs and FCs is illustrated as

$$v_{f\alpha}^+ = \frac{1}{2}(v_{f\alpha} - qv_{f\beta}) \quad (8)$$

$$v_{f\beta}^+ = \frac{1}{2}(v_{f\beta} + qv_{f\alpha}) \quad (9)$$

The fundamental positive sequence voltages in the  $\alpha$ - $\beta$  frame ( $v_{f\alpha}^+, v_{f\beta}^+$ ) are transformed again using the inverse of Clark's transformation matrix to extract the FPSCs of the PCC voltages in a stationary frame ( $v_{sa}^+, v_{sb}^+, v_{sc}^+$ ), thus obtaining reference signals for both power filters. The control method for generation of the reference signals for the shunt APF are governed in such a way that the currents carried from the PCC are balanced positive sequences under all PQ conditions and irrespective of load, as shown in Fig. 4. The average load power can be obtained by processing the dot product of the load voltages ( $v_{labc}$ ) and load currents ( $i_{labc}$ ). The DC link voltage is managed at its appropriate reference value via the PI controller gains. The input to the PI controller is an error ( $V_{de}$ ), generated from the reference DC link voltage ( $v_{DC}^*$ ) and actual sensed  $V_{DC}$  voltage. The outcome of this PI controller is a power loss component ( $P_{loss}$ ) for both APFs, which can be expressed at the  $t^{\text{th}}$  sample time as

$$P_{loss}(t) = P_{loss}(t-1) + K_p \{V_{de}(t) - V_{de}(t-1)\} + K_i V_{de}(t) \quad (10)$$

where power,  $P_{loss}(t)$  is projected as active power of the supply current at instant  $t$ .  $K_p$  and  $K_i$  are the PI controller constants.

The  $P_{loss}$  not only contains all the switching losses but also the ohmic losses of the compensators. It is a necessary element for controlling the DC link voltage over PQ disruptions in order for the shunt compensator to regulate the DC link voltage to its required level. Accordingly, the reference power ( $P_{ref}$ ) to be drawn from the grid is obtained as,  $P_{ref} = P_{lavg} + P_{loss}$ . The balanced positive sequence reference grid input current ( $i_{sabc}^+$ ) is then calculated as

$$i_{sabc}^+ = \frac{v_{sabc}^+}{(v_{s\alpha}^+)^2 + (v_{s\beta}^+)^2} P_{ref} \quad (11)$$

These fundamental positive reference currents ( $i_{sabc}^+$ ), obtained from Eq. (11), act as reference supply currents ( $i_{labc}^*$ ). They are then with the sensed actual currents ( $i_{sabc}$ ) via a SPWM controller to generate the gating pulses required for the shunt APF, as shown in Fig. 4.

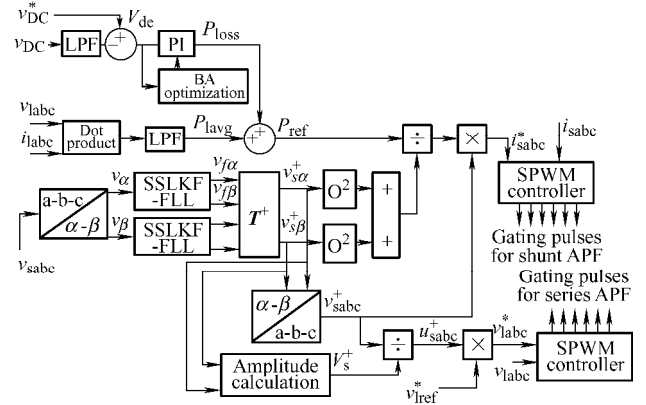


Fig. 4 Reference signal generation through SSLKF-FLL for UPQC compensator

The main function of the series APF is to protect critical loads from PCC voltage disturbances. Fig. 4 also illustrates the reference load voltage generation for the series connected compensator. The magnitude of the FPSC from the PCC voltage is determined as

$$V_s^+ = \sqrt{(v_{s\alpha}^+)^2 + (v_{s\beta}^+)^2} \quad (12)$$

This amplitude is used in calculation of unit templates from FPSC. It is given as

$$u_{sabc}^+ = \frac{v_{sabc}^+}{V_s^+} \quad (13)$$

The load reference voltage ( $v_{labc}^*$ ) is determined by multiplying the peak reference voltage ( $v_{lref}^*$ ) with the unit templates ( $u_{sabc}^+$ ). These reference load voltages ( $v_{labc}^*$ ) are compared to the actual sensed load voltages ( $v_{labc}$ ) to generate the gating pulses. These SPWM based gate signals are required for the series APF. This can be clearly observed in Fig. 4.

### 3.3 PI-controller gains evaluation from bat algorithm technique

This section investigates the BA for PI parameters in the UPQC control scheme, such that the UPQC can produce better outcomes with respect to error regulation, strengthening the UPQC performance. The BA is based on micro bats echo-location characteristics. This uses a frequency tuning technique to increase the diversity of potential solutions within the population pool, while concurrent automated zooming aims to balance exploration and exploitation during the search cycle. BA optimization is a stochastic algorithm, in which diverse results are achieved each time, although the same initial point is

considered for further evaluation. The BA optimization is therefore repeated 20 times to provide reasonable observations for further analysis. This is to achieve optimal PI-Controller gain results, based on when the stopping criteria is met, i.e., in this study, reaching the maximum number of iterations ( $t$ ). The result was chosen on the basis of the integral time square error (ITSE) as the cost function or objective function. This selection is due to characteristics of this function, which improves dynamic response with satisfactory settling time. ITSE can be expressed as

$$\text{ITSE} = \int_0^t e(t)^2 dt \quad (14)$$

where  $e(t) = y(t) - r(t)$  is the error in Eq. (14) and  $y(t)$  and  $r(t)$  are the output and required output of the system. Thus, a smaller error results in a smaller burden on the PI-controller gains of Eq. (10) in the UPQC system. The optimal tuned PI-controller gains values are selected when value of objective function (ITSE value) is smallest. Thus, the UPQC system performs better when the cost function ITSE value is lowest.

The BA's approximate rules can be classified into three categories<sup>[28-29]</sup>. First, each bat use echo-location to sense distance and in some unknown manner they also understand the distinction between food/prey and the surrounding obstacles. Second, bats fly arbitrarily, with variable frequency ( $f$ ), variable wavelength ( $\lambda$ ), and loudness ( $A_0$ ), investigating for prey by automatic adjusting the frequency of their emitted pulses. Finally, although the loudness may differ in various ways, it is expected to vary within the range  $A_0$  to minimum constant value  $A_{\min}$ . Fig. 5 shows the BA flowchart.

The BA techniques are specified as following.

(1) Initialize the randomly generated micro bats and initial population size of bats in an  $N$ -dimensional search space.

(2) Estimate the objective function for each random number of bats. The internal parameters are also initialized including pulse frequency, pulse rate, and loudness.

(3) Generate the initial bats position and velocity.

(4) If a random number between 0 and 1 is bigger than the pulse rate (i.e.,  $\text{random} > \text{pulse rate}$ ), choose the best solution from the bats groups.

(5) If a random number is greater than loudness

(i.e.,  $\text{random} > \text{loudness}$ ) and  $f_{\text{new}} \leq f_{\min}$ , acknowledge this as a new solution.

(6) Keep this location and increase the pulse rate and loudness. Determine the optimum and rank the bats accordingly.

(7) Return to Step (3) and repeat all steps until the criteria for stopping is met.

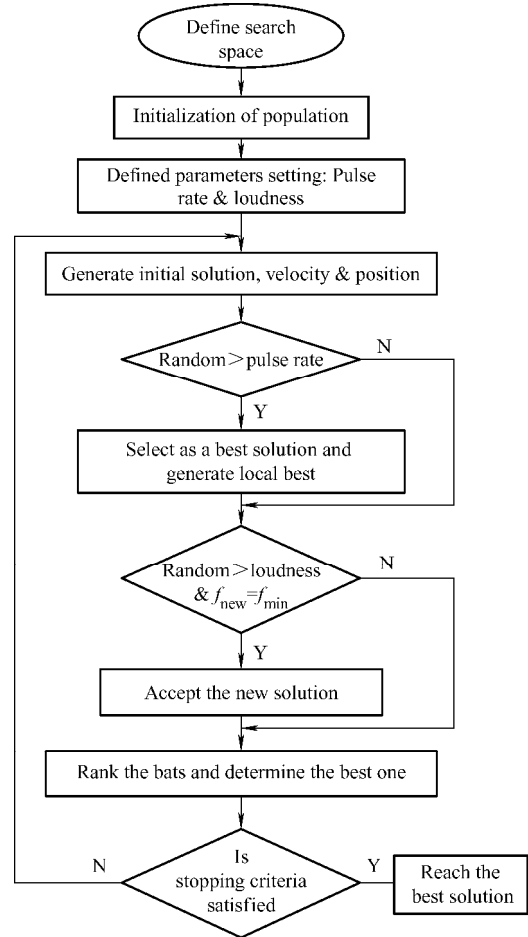


Fig. 5 Flowchart of bat algorithm for PI gains

Each bat is connected in a  $d$ -dimensional search of the solution space, with velocity ( $v_i^t$ ) and location ( $x_i^t$ ) at the  $t^{\text{th}}$  iteration. There is a current best solution ( $x_*$ ) among all the bats. Each bat is moved according to the following equations to yield a new solution for the next iteration.

$$f_i = f_{\min} + (f_{\max} - f_{\min})\beta \quad (15)$$

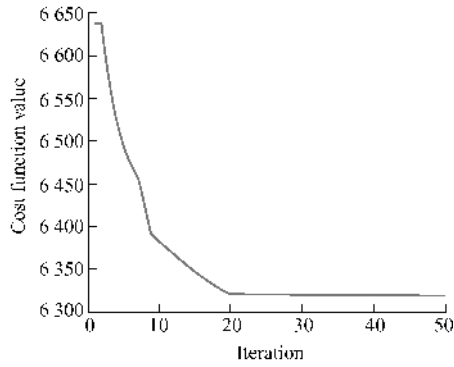
$$v_i = v_i^{t-1} + (x_i^{t-1} - x_*)f_i \quad (16)$$

$$x_i = x_i^{t-1} + v_i^t \quad (17)$$

where  $\beta \in [0, 1]$  is a random vector derived from an even distribution;  $x_i^t$  is the present global best location (solution) found after computing each bat to the entire solution. The present best solution is obtained by

$$x_{\text{new}} = x_{\text{old}} + \partial A^t \quad (18)$$

where  $A^t$  is the average loudness of all the best components in the current iteration process; the constant  $\partial \in [-1,1]$  is a random number. By executing these steps, the optimum PI gains ( $K_p$  and  $K_i$ ) are predicted using the optimal cost function  $f(x)$  of 6 318.74, as shown in Fig. 6. Using these acquired PI values, the UPQC has a better dynamic response when compared with manually tuned values. This method improves UPQC's output, improving the PQ.



(a) Cost function with respect to iteration

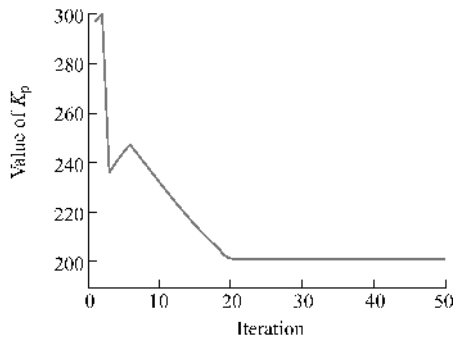
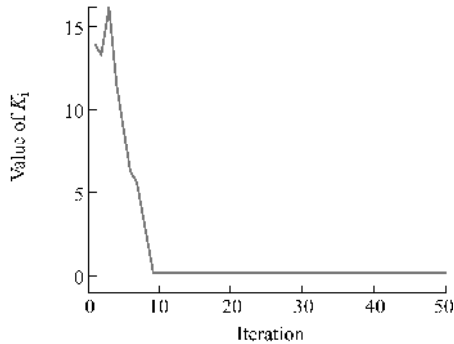

 (b)  $K_p$  with respect to iteration

 (c)  $K_i$  with respect to iteration

Fig. 6 Plot of 3 scenarios

Here, the BA uses 20 agents and 2 design variables ( $K_p$  and  $K_i$ ) for 50 iterations. Fig. 6a depicts the adjustment of the objective function values in comparison to iterations reached after the 20 iterations at 6 318.74. Fig. 6b and Fig. 6c demonstrates the  $K_p$

and  $K_i$  PI gains plots for a DC link voltage, which settled at 200.15 and 1.0, respectively. These acquired PI values improve the performance of the UPQC's output, improving the PQ. In order to check the acknowledgment and reliability of the PI controller with the BA technique, the DC bus voltage with the previously mentioned PQ disturbances is examined. It is determined that the BA techniques result in a more stable and rapid DC-bus voltage, compared to trial and error tuning techniques. The optimized value of  $K_p$  and  $K_i$ , retrieved via the BA, will assist in UPQC control. The results of which are explained in the following section.

## 4 Simulation results

The performance evaluation of the proposed SSLKF based FLL control algorithm is carried out on the UPQC system. The model is analyzed using the Matlab/Simulink software platform, with a fixed sampling time of 10  $\mu$ s and a discrete domain through 5 ode solvers. The PI controller parameter values obtained via the BA are also employed to estimate the performance of the UPQC. Throughout this section, the results for system disturbances, such as voltage sag, swell, harmonics, and unbalanced loading conditions are reported to demonstrate the successful operation of the SSLKF-FLL controller with a nonlinear load on the UPQC system. Tab. 1 contains system parameters and detailed design values of three wire UPQC for performance analysis.

**Tab. 1 Parameters used for simulation work**

Parameter	Value
PCC source voltage $V_s$	415 V, 50 Hz
Non-linear load: 3- $\phi$ bridge rectifier	$R = 20 \Omega$ , $L = 200$ mH
DC-link voltage $V_{DC}$	700 V
Injecting DVR transformer	120/120 V, 4 kVA
Source impedance $Z_s$	$R = 0.060 \Omega$ , $L = 1.5$ mH
Interfacing inductance at shunt side $L_{sh}$ /mH	3
Interfacing inductance at series side $L_{se}$ /mH	1.5
RC filter	$R_f = 5 \Omega$ , $C_f = 20 \mu$ F
PI-controller gains	$K_p = 200.15$ , $K_i = 1.0$
Selected cutoff frequency of LPF/Hz	10
Switching frequency of both APFs/kHz	10
Sampling time $T_s/\mu$ s	10
SSLKF-FLL internal gains	$k_1 = 100\sqrt{2}\pi$ $k_2 = -141.2$ $\lambda = -1.000$



#### 4.1 Dynamic behavior SSLKF-FLL based control and shunt converter used in UPQC

The dynamic behavior of the UPQC under unbalanced loading and current distortions is presented in Fig. 7. Load unbalancing is obtained in phase ‘c’, when it is injected at time 0.5 s and before that it is in two phases connection to line appearing in the unbalanced load situations. Due to phase removal the balanced supply currents ( $i_s$ ) have been observed during load current ( $i_l$ ) unbalancing. The compensating current ( $i_{coma}$ ,  $i_{comb}$ , and  $i_{comc}$ ) of the shunt APF, as shown in Fig. 7, indicates the well-organized reactive power compensation for the supply current. The self supporting DC bus voltage ( $V_{DC}$ ) summary is also shown here, which is within the 3% tolerance limit. The  $V_{DC}$  is accommodating of its 700 V level from fluctuations of 16 V. There is an imperceptible shift of one cycle in the waveforms due to the use of lower order filters in the DC link voltage and active average power ( $P_{lavg}$ ) calculation. It is necessary for the UPQC controller to estimate reference power ( $P_{ref}$ ) calculations. The load voltage ( $v_l$ ) profile is sustained at its desired level irrespective of load unbalancing conditions. The FPSCs of the supply voltage in the  $\alpha$ - $\beta$  frame signals ( $v_{s\alpha}^+$ ,  $v_{s\beta}^+$ ) are used to estimated balanced reference positive sequence currents under all PQ conditions.

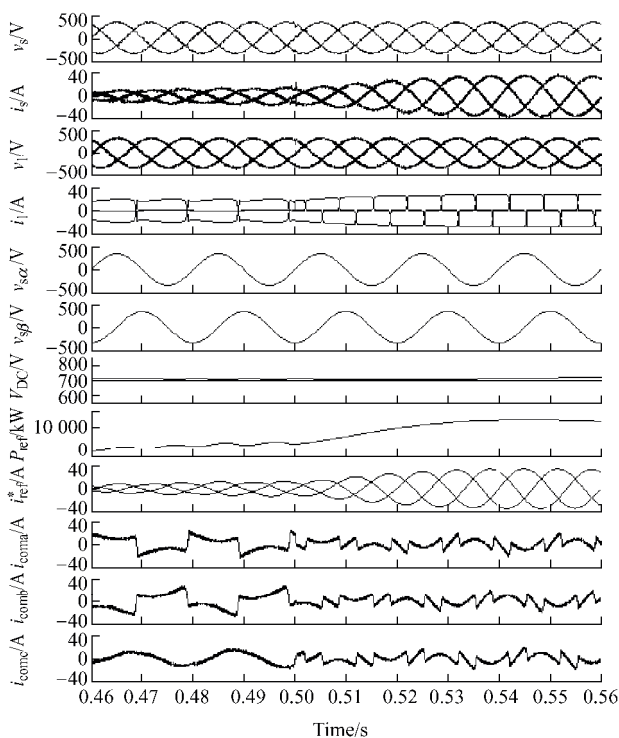


Fig. 7 Dynamic behavior of control algorithm and shunt converter used in UPQC

The waveforms show that the three-phase supply current ( $i_s$ ) almost follows the reference supply currents ( $i_{sref}^*$ ) under dynamics disruption due to the shunt APF injected current. It is also of note that supply voltage ( $v_s$ ), load voltage ( $v_l$ ), and supply current ( $i_s$ ) are in phase with each other. Thus, it is concluded that the shunt compensator of UPQC functions as power factor correction during load dynamics. From the results, the load in “phase c” is connected from 0.5 s and the variation in compensating currents ( $i_{coma}$ ,  $i_{comb}$ , and  $i_{comc}$ ) of all phases are shown. At this time, it is observed that the shunt APF provides the necessary compensating currents with desired magnitude in all three phases, before and after the unbalanced load conditions, to maintain the sinusoidal supply current.

#### 4.2 Steady-state and dynamic response of UPQC with SSLKF-FLL

The steady-state and dynamic response of UPQC with SSLKF-FLL control is shown in Fig. 8. The waveforms seen in this figures are the three-phase supply voltages ( $v_s$ ), supply currents ( $i_s$ ), load voltage ( $v_l$ ), load currents ( $i_l$ ), DC link voltage ( $V_{DC}$ ), series compensator compensation voltages ( $v_{inja}$ ,  $v_{inj b}$ , and  $v_{inj c}$ ), and shunt compensator compensation currents ( $i_{coma}$ ,  $i_{comb}$ , and  $i_{comc}$ ). A voltage sag of 0.70 p.u magnitude is observed at 0.5-0.56 s; voltage swells of 1.30 p.u amplitude at 0.6-0.66 s; and at 0.5-0.56 s a supply voltage corrupted from the  $-11^{\text{th}}$  to the  $+13^{\text{th}}$  order harmonic, with amplitudes of  $1/15^{\text{th}}$  and  $1/20^{\text{th}}$  of the fundamental voltage, is imposed on the grid voltages ( $v_s$ ). At 0.5-0.6 s the load is adjusted from three- to two-phase, when “phase c” is removed from the supply line. This caused an unbalanced load state in the network. From the implementation results, it is observed that the shunt compensator part of the UPQC compensates for unbalanced loading. Similarly, it balances the sinusoidal source current ( $i_s$ ) and maintains it as in phase with the source voltages ( $v_s$ ). The UPQC series compensator serves as compensation for the voltage sag/swell and distortion and results in distortion free load voltage ( $v_l$ ), as shown in Fig. 8. It also compensates for the load voltage ( $v_l$ ) from all the PQ perturbations and is sinusoidally balanced with the desired magnitude. Therefore, it maintains constant

voltage at the load side common coupling point. Simultaneously, the shunt compensator maintains the balanced supply current and regulates the power factor at unity. The SSLKF-FLL control algorithm keep up the DC link voltage close to a reference level under the PQ perturbations mentioned above. The harmonic spectrums of supply voltage ( $v_s$ ), supply current ( $i_s$ ), load voltage ( $v_l$ ), and load current ( $i_l$ ), are expressed in Tab. 2. The “line to line” signals are listed here for the harmonic spectrum study but due to the symmetrical phase results they are practically identical to the other phases of the system. The total harmonic distortion (THD) of the source current is 3.63%, filtered from the load current THD of 26.83%. Similarly, the THD of the load voltage is 3.16%, also filtered from a supply voltage THD of 16.85%. The harmonic range supports the restriction of harmonic levels below 5% for medium level grid voltage as per, the IEEE standards on SSLKF-FLL control of UPQC systems.

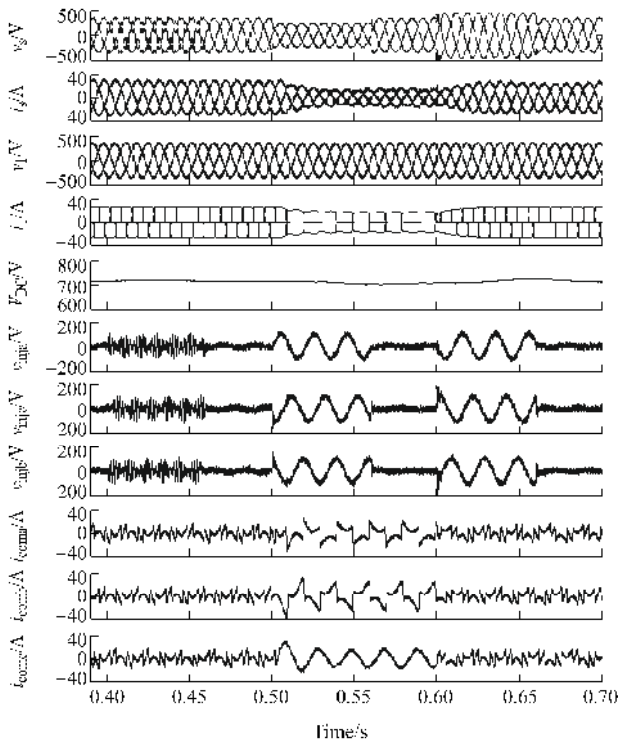


Fig. 8 Steady state and dynamic response of UPQC with SSLKF-FLL

Tab. 2 Performance of UPQC under harmonics

Operating mode	System parameters	%THD and peak magnitude values
Harmonic compensation	Source voltage $v_s$	16.85%, 585.8 V
	Supply current $i_s$	3.63%, 31.70 A
	Load voltage $v_l$	3.16%, 586.1 V
	Load current $i_l$	26.83%, 30.16 A

## 5 Test results

The SSLKF-FLL control algorithm is built on a three wire UPQC system for non-linear loads. The SSLKF-FLL is designed and programmed using OP-5142 real time simulator with 60  $\mu$ s sampling time. The four channel digital storage oscilloscope (DSO) is used to capture all waveforms. A switching frequency of 10 kHz is chosen during the implementation for both APFs. The dynamic behavior of the UPQC system is tested with PQ disturbances described previously. A PQ analyzer, FLUKE-4B, is used to evaluate the THD during harmonic distortion. Both the internal signal and steady-state response of the UPQC are measured in “phase to ground” values. The entire performances of the waveforms are shown in Figs. 9-11, with identical references to phase ‘a’ and other phases. The system parameter and control algorithm values are given in Tab. 3.

Tab. 3 Parameters used for test performance

Parameter	Value	
PCC voltage $V_s$	110 V, 50 Hz	
Non-linear load: 3- $\phi$ bridge rectifier	$R = 20 \Omega$ , $L = 200$ mH	
DC-link voltage $V_{DC}/V$	200	
Injecting DVR transformer	120/120 V, 4 kVA	
Interfacing inductance for shunt side $L_{sh}/mH$	3	
Interfacing inductance for series side $L_{se}/mH$	1.5	
RC filter	$R_f = 5 \Omega$ , $C_f = 20 \mu F$	
PI-controller gains	$K_p = 80$ , $K_i = 1.0$	
Selected cut off frequency of LPF/Hz	10	
Switching frequency of both APFs/kHz	10	
Sampling time $T_s/\mu s$	60	
SSLKF-FLL internal gains	$k_1$	$100\sqrt{2}\pi$
	$k_2$	-141.2
	$\lambda$	-1 000

### 5.1 Reference supply current generation for shunt compensator

The primary task of the SSLKF-FLL circuit is to estimate the FPSCs during steady-state and under PQ perturbations. On the basis of these in-phase ( $v_{f\alpha}^+$ ) and quadrature ( $v_{f\beta}^+$ ) FPSCs, the load voltage reference and supply current reference signals are generated. The FPSC voltage ( $v_{f\alpha}^+$ ,  $v_{f\beta}^+$ ) is evaluated from the Kalman filters during sag in the supply voltage ( $v_{sa}$ ), as seen in subplot 1 of Fig. 9a. The DC-link voltage ( $V_{DC}$ ) in

subplot 2 of Fig. 9a illustrates its stability during transient conditions. It is regulated by instantaneous active power loss components ( $P_{loss}$ ), as demonstrated in Fig. 4. The active powers ( $P_{lavg}$ ) in subplot 3 are needed for generating the reference signal for the shunt APF at the load side. During sag conditions, the reference power ( $P_{ref}$ ) in subplot 4 is obtained when  $P_{loss}$  is added to  $P_{lavg}$ , represented in Fig. 9a. The internal signals depicted during sag voltage in Fig. 9b are reference power ( $P_{ref}$ ), reference supply voltage ( $v_{sa}^+$ ), and FPSC voltage ( $v_{f\alpha}^+$ ,  $v_{f\beta}^+$ ), shown in subplots 1, 2, 3, and 4, respectively, used to generate the reference supply current for the shunt compensator. Fig. 9c depicts the reference source current ( $i_{sa}^*$ ) in subplot 1 generated for the shunt APF with the help of signals shown in Fig. 9b. In Fig. 9c, it is noted that the sensed source current ( $i_{sa}$ ) in subplot 1 follows the reference source current ( $i_{sa}^*$ ) in subplot 2, during sag deviation. In the SPWM controller, the errors ( $i_{er}$ ) in signals derived between the difference of the sensed actual and reference supply current, subplot 3 of Fig. 9c, are utilized to procure gating pulses ( $G_{1a}$  in subplot 4) for the shunt APF.

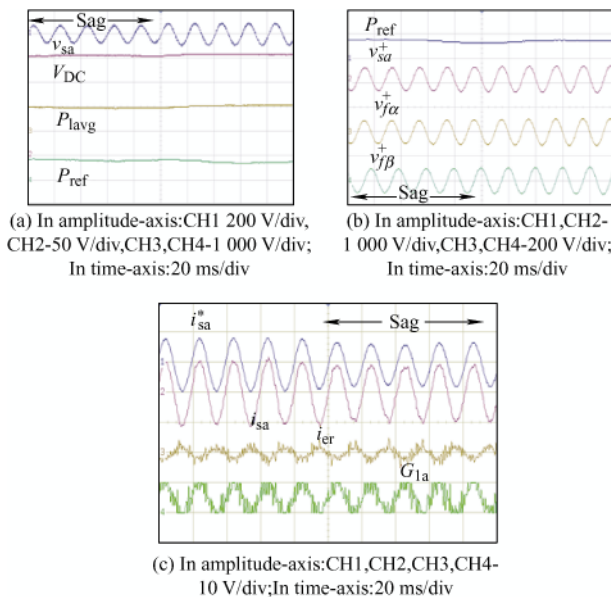


Fig. 9 Reference supply current generation for UPQC using SSLKF-FLL control algorithm

## 5.2 Dynamic performance of UPQC

Figs. 10-11 illustrate UPQC's dynamic performance analysis to compensate the above mentioned PQ disruption using an SSLKF-FLL based control technique. These signals are taken for "phase a" at

occurrence when the dynamic PQ disruptions are adjusted to nominal conditions. Figs. 10a-10d depicts the information regarding the supply voltage ( $v_{sa}$ ), supply current ( $i_{sa}$ ), load voltage ( $v_{1a}$ ), and load current ( $i_{1a}$ ) during voltage swells, sags, harmonics distortions and load unbalancing, respectively. In these figures, a voltage swell of 20%, sag of 20%, and 11<sup>th</sup> and 13<sup>th</sup> order voltage distortions are superimposed on the initial supply voltages, as shown in Figs. 10a-10c. The UPQC provides alleviation for voltage harmonics and manages distortion free load voltage, as indicated in Fig. 10c.

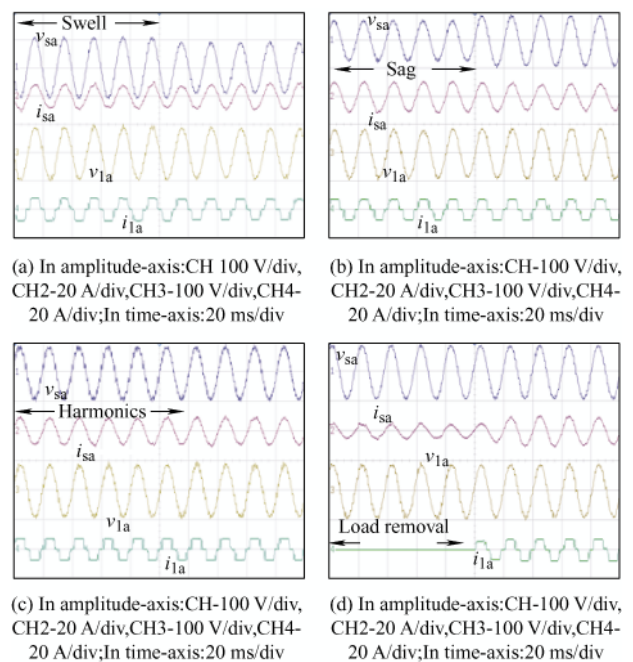


Fig. 10 Dynamic of UPQC during swell, sag, harmonics disturbances and load unbalancing

The supply current magnitude decreases or increases in conjunction with the change in input voltages, as seen in Figs. 10a-10b, subplot 2, during voltage sag and swell deviations. Simultaneously, load voltage is sustained in a sinusoidal wave-shape with a fixed magnitude, independent of PQ disturbances. As shown in subplot 4 of Fig. 10, the load current tends to be extremely distorted and the supply current retains a sinusoidal wave-shape via the UPQC. Phase 'a' of the load is disconnected to cause an unbalanced load condition (in subplot 4), which is shown in Fig. 10d. The sinusoidal feature of the supply current is also sustained at the desired level. Simultaneously, sinusoidal load voltage is maintained throughout various PQ disturbances. From close observation of

Figs. 10a-10d during these disruptions and nominal situations, the load voltages ( $v_{la}$ ) in subplot 3 are seen to be in-phase with the supply currents ( $i_{sa}$ ) in subplot 2, indicating that the UPQC maintains a unity power factor and preserves the balanced load voltage. Figs. 11a-11c shows the behavior of the DC link voltage ( $V_{DC}$ ), in subplot 4, with supply voltage ( $v_{sa}$ ) in subplot 1, load voltage ( $v_{la}$ ) in subplot 2, and the compensating voltage of “phase a” ( $v_{ca}$ ) in subplot 3 at various PQ disruptions. Figs. 11a-11c clarifies that the compensated voltage injected by the series transformer is in-phase during sag and harmonic distortion and in-quadrature during swell conditions. Similarly, Fig. 11d shows the supply current ( $i_{sa}$ ) in subplot 1; load current ( $i_{la}$ ) in subplot 2; compensating current of phase A ( $i_{ca}$ ) in subplot 3, injected during the unbalance loading situation; and the DC link voltage ( $V_{DC}$ ) in subplot 4. It is seen that the sinusoidal supply current is preserved and the shunt compensator injects a current with the required wave-shape. The fluctuations of the DC link voltage can be seen in Figs. 11a-11d in subplot 4, during dynamic disturbance and the DC link voltage is regulated at the required level over one cycle. All figures indicated that the UPQC’s dynamic performance with the SSLKF-FLL based control algorithm successfully mitigates all of the PQ problems.

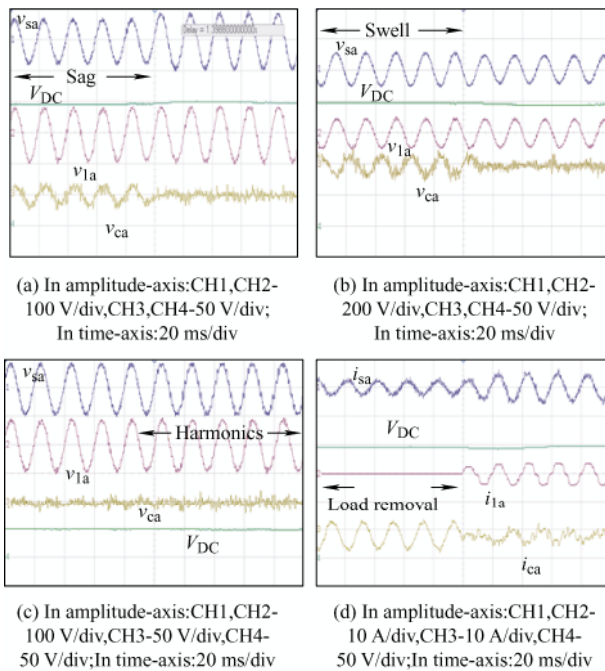


Fig. 11 Dynamics of UPQC during sag, swell, harmonics, and unbalanced load with DC link

### 5.3 UPQC performance at steady state condition

Fig. 12a and Fig. 12b illustrates the waveforms recorded when the supply voltage distortions are present in-line with nonlinear loads. Fig. 12a displays the supply voltage ( $v_{sa}$ ) waveforms with voltage distortion of the above mentioned conditions and supply current ( $i_{sa}$ ) after mitigation. The source current (THD) in Fig. 12b has been improved to 3.8% from the load current THD of 18.20%.

The summarized results relating to steady-state analysis for harmonic distortion are given in Tab. 4. Tab. 4 illustrates the recorded results of “phase a” during uncompensated supply voltage ( $v_{sa}$ ), compensated load voltage ( $v_{la}$ ), mitigated source current ( $i_{sa}$ ), and distorted load current ( $i_{la}$ ) under non-linear loads on the UPQC system. These performance results are studied with aforesaid harmonic distortions in the supply side voltage and load current. The results refer to knowledge concerning the distorted supply voltage with 11.30% THD and an RMS value of 110.70 V. It is clarified that the load voltage ( $v_{la}$ ) is compensated for, having a 109.3 V RMS value and 4.7% THD.

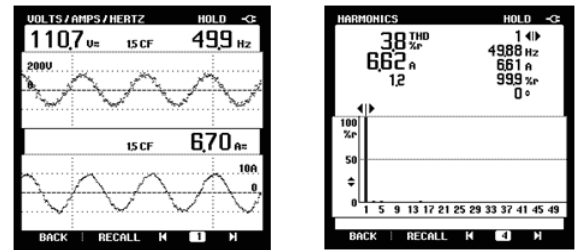


Fig. 12 UPQC performance at steady-state

Tab. 4 Performance summary of UPQC during harmonic disturbance

Nature of disturbance	Parameter	Quantity in RMS
Distortion	Source voltage $v_{sa}$	110.70 V with THD 11.3%
	Load voltage $v_{la}$	109.3 V with THD 4.7%
	Source current $i_{sa}$	6.62 A with THD 3.8%
	Load current $i_{la}$	5.75 A with THD 18.2%

Similarly, the supply current has an RMS value of 6.62 A with 3.8% THD, after mitigation. The nonlinear load is known to have an RMS value of 5.75 A and a THD of 18.20%. It is evident that  $v_{la}$  and  $i_{la}$  are within

the acceptable THD limits provided by IEEE-519-2014. This result proves the capability of the UPQC system to compensate for harmonic disturbances.

## 6 Conclusions

SSLKF based control is conducted for a three-phase UPQC system under a nonlinear load to achieve PQ compensation. SSLKF control is able to identify the FPSCs (in-phase and quadrature) and grid frequency accurately for the UPQC system, providing fast and smooth steady-state and dynamic responses. The combination of FLL with steady state linear Kalman filters demonstrates superior behavior when compared to other types of single phase PLL techniques published in the literature. It shows that the phase angle and amplitude of a distorted waveform can be precisely and rapidly determined via the Kalman filters. The PI controller parameters, which are tuned in this study using BA optimization, seek minimized DC bus voltage variations, even with upset value of current or voltage. After the 20 iterations, the PI controller proportional ( $K_p$ ) and integral ( $K_i$ ) gain are obtained as 200.15 and 1.0, respectively, which maintains the DC bus voltage levels at their desired magnitude. The simulation and test results determine the validity of the proposed UPQC algorithm. The proposed UPQC and BA demonstrates the potential for performance enhancement of the system and PQ improvement of the distribution networks. The presented work can be investigated and evaluated in the future with different linear (or a combination of both linear and nonlinear) loads via the same control algorithm. Similarly, soft computing techniques, such as fuzzy control, artificial neural networks, or intelligent control algorithms, can be used for three-phase UPQCs to improve the system's effectiveness. Renewable energy sources, such as wind and solar power can be integrated with this (or other) topologies of UPQC.

## References

- [1] H Hafezai, G D Antona, A Dede, et al. Power quality conditioning in LV distribution networks: Results by field demonstration. *IEEE Transactions on Smart Grid*, 2017, 8(1): 418-427.
- [2] B Singh, A Chandra, K I A Haddad. Power quality: Problems and mitigation techniques. West Sussex: John Wiley and Sons, 2014.
- [3] V Kavitha, K Subramanian. Investigation of power quality issues and its solution for distributed power system. *Proc. International Conference on Circuit, Power and Computing Technologies (ICCPCT)*, Kollam, 2017: 1-6.
- [4] M H Bollen. Understanding power quality problems: voltage sags and interruptions. New York: Wiley-IEEE Press, 2000.
- [5] S S Reddy. Determination of optimal location and size of static VAR compensator in a hybrid wind and solar power system. *International Journal of Applied Engineering Research*, 2016, 11(23): 11494-11500.
- [6] S S Reddy. Congestion management and voltage profile improvement in a hybrid power system with FACTS controllers. *International Journal of Applied Engineering Research*, 2017, 12(9): 2095-2103.
- [7] S S Reddy. Solving the power system state estimation problem embedded with UPFC using glow worm swarm optimization algorithm. *International Journal of Applied Engineering Research*, 2017, 12(10): 2361-2369.
- [8] E Hossain, M R Tür, S Padmanaban, et al. Analysis and mitigation of power quality issues in distributed generation systems using custom power devices. *IEEE Access*, 2018, 6: 16816-16833.
- [9] A A Abdou, S Kamel, M A Akher, et al. Voltage stability analysis of distribution network in egypt including UPQC device. *Proc. 20<sup>th</sup> International Middle East Power Systems Conference (MEPCON)*, Cairo, Egypt, 2018: 1115-1120.
- [10] R A Wanjari, V B Savakhande, M A Chewale, et al. A review on UPQC for power quality enhancement in distribution system. *Proc. International Conference on Current Trends Towards Converging Technologies (ICCTCT)*, Coimbatore, 2018: 1-7.
- [11] S S Bhosale, Y N Bhosale, U M Chavan, et al. Power quality improvement by using UPQC: A review. *Proc. International Conference on Control, Power, Communication and Computing Technologies (ICCPCT)*, Kannur, 2018: 375-380.
- [12] M Prasad, A K Akella. Mitigation of power quality problems using custom power devices: A review. *Indonesian Journal of Electrical Engineering and Informatics*, 2017, 5(3): 207-235.
- [13] H Akagi, E H Watanabe, M Aredes. Instantaneous power theory and applications to power conditioning. New York: John Wiley & Sons, 2017.
- [14] A Patel, P Chaturvedi. Performance of SRF-UVTG based UPQC-DG for integration of solar PV with non-linear loads. *Proc. IEEE International Conference on Power*

- Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, 2016: 1-5.
- [15] J Sukumaran, A Thomas, A Bhattacharya. A reduced voltage rated unified power quality conditioner for harmonic compensations. *Proc. IEEE 7<sup>th</sup> Power India International Conference (PIICON)*, Bikaner, 2016: 1-5.
- [16] A S Kumar, K Prakash. Analysis of split capacitor based D-STATCOM with LCL filter using instantaneous symmetrical components theory. *Proc. 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)*, Chennai, 2016: 103-108.
- [17] Y Hoon, M A M Radzi, M K Hassan, et al. Three-phase three-level shunt active power filter with simplified synchronous reference frame. *Proc. IEEE Industrial Electronics and Applications Conference (IEAC)*, Kota Kinabalu, 2016: 1-6.
- [18] S Devassy, B Singh. Discrete SOGI based control of solar photovoltaic integrated unified power quality conditioner. *Proc. National Power Systems Conference (NPSC)*, Bhubaneswar, 2016: 1-6.
- [19] P Rodriguez, R Teodorescu, I Candela, et al. New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions. *Proc. 37<sup>th</sup> IEEE Power Electronics Specialists Conference*, Jeju, 2006: 1-7.
- [20] J Matas, M Castilla, J Miret, et al. An adaptive prefiltering method to improve the speed/accuracy tradeoff of voltage sequence detection methods under adverse grid conditions. *IEEE Transactions on Industrial Electronics*, 2014, 61(5): 2139-2151.
- [21] T Ngo, Q Nguyen, S Santoso. Improving performance of single-phase SOGI-FLL under DC-offset voltage condition. *Proc. IECON 40<sup>th</sup> Annual Conference of the IEEE Industrial Electronics Society*, Dallas, TX, 2014: 1537-1541.
- [22] J V Valls, P Closas, C F Prades. On the identifiability of noise statistics and adaptive KF design for robust GNSS carrier tracking. *Proc. IEEE Aerospace Conference*, Big Sky, MT, USA, 2015: 1-10.
- [23] S Golestan, J M Guerrero, J Vasquez, et al. Single-phase FLLs based on linear kalman filter, limit-cycle oscillator, and complex band-pass filter: Analysis and comparison with a standard FLL in grid applications. *IEEE Transactions on Power Electronics*, 2019, 34(12): 11774-11790.
- [24] S S Reddy, M S Kumari, M Sydulu. Congestion management in deregulated power system by optimal choice and allocation of FACTS controllers using multi-objective genetic algorithm. *Proc. IEEE PES T&D 2010*, New Orleans, LA, 2010: 1-7.
- [25] S R Paital, P K Ray, A Mohanty. BAT algorithm optimized SVC for power system stability enhancement. *Proc. Progress in Electro-magnetics Research Symposium-Fall (PIERS-FALL)*, Singapore, 2017: 1977-1983.
- [26] N A N Azlan, N A Selamat, N M Yahya. Multivariable PID controller design tuning using bat algorithm for activated sludge process. *IOP Conference Series: Materials Science and Engineering*, 2018: 012030.
- [27] O B Haddad, S Mohammad, H A Loaiciga. Meta-heuristic and evolutionary algorithms for engineering optimization. New Jersey: John Wiley & Sons, 2017.
- [28] X S Yang. Bat algorithm: Literature review and applications. *Journal of Bio-Inspired Computation*, 2013, 5(3): 141-149.
- [29] B V Kumar, N V Srikanth. Bat algorithm and firefly algorithm for improving dynamic stability of power systems using UPFC. *International Journal on Electrical Engineering & Informatics*, 2016, 8(1): 164-187.



**Sayed Javed Alam** received the bachelor of technology in electrical engineering from Rajasthan Institute of Engineering & Technology Jaipur, India, in 2012 and M.Tech degree in electrical engineering with specialization in power electronics and electrical drives from Birla Institute of Technology, Mesra, India in 2015. In February 2016, he joined the department of electrical engineering, Global Institute of Technology, Jaipur, India, as an assistant professor. From July 2017 onwards, he is currently pursuing the Ph.D. degree in electrical engineering from Sardar Vallabhbhai National Institute of Technology Surat, India. His research area includes power electronics, power quality and design of custom power devices, multilevel inverter and DC-DC converters.



**Sabha Raj Arya** (M'12, SM'15) received bachelor of engineering degree in electrical engineering from Government Engineering College Jabalpur, in 2002, master of technology in power electronics from Motilal National Institute of Technology, Allahabad, in 2004 and Ph.D. degree in electrical engineering from Indian Institute of Technology (I.I.T) Delhi, New Delhi, India, in 2014. He is joined as assistant professor, Department of Electrical Engineering, Sardar Vallabhbhai National Institute of Technology, Surat. January 2019, he is promoted as associate professor in same institute. His fields of interest include power electronics, power quality, design of power filters and distributed power generation.

He received two national awards namely INAE Young Engineer Award from Indian National Academy of Engineering, POSOCO Power System Award from Power Grid Corporation of India in the year of 2014 for his research work. He is also received Amit Garg Memorial Research Award-2014 from I.I.T Delhi from the high impact publication in a quality journal during the session 2013-2014. At present, he has published more than hundred research papers in internal national Journals and conferences in field of electrical power quality.

He also serves as an associate editor for the IET (U.K.) Renewable Power Generation.