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ABSTRACT

Gallium nitride (GaN) is one of the front-runner materials among the so-called wide bandgap semiconductors that can provide devices having high breakdown voltages and are capable of performing efficiently even at high temperatures. The wide bandgap, however, naturally leads to a high density of surface states on bare GaN-based devices or interface states along insulator/semiconductor interfaces distributed over a wide energy range. These electronic states can lead to instabilities and other problems when not appropriately managed. In this Tutorial, we intend to provide a pedagogical presentation of the models of electronic states, their effects on device performance, and the presently accepted approaches to minimize their effects such as surface passivation and insulated gate technologies. We also re-evaluate standard characterization methods and discuss their possible pitfalls and current limitations in probing electronic states located deep within the bandgap. We then introduce our own photo-assisted capacitance–voltage (C–V) technique, which is capable of identifying and examining near mid-gap interface states. Finally, we attempt to propose some directions to which some audience can venture for future development.

I. INTRODUCTION

Gallium nitride (GaN) and its related ternary alloys form one of the most important III–V compound semiconductor systems well-suited for high-power, high-frequency, and high-temperature applications. Recent years have witnessed GaN-based devices fulfilling their promise of achieving unprecedented performance, otherwise difficult, if not impossible, to achieve using the ubiquitous silicon. Also, great strides have been made in overcoming major drawbacks for the widespread use of GaN in the fields of optoelectronics, RF, and power electronics, although this was achieved with less advanced technology than that used for its Si and GaAs predecessors. For instance, with tremendous advances in crystal growth technology, free-standing GaN substrates with low dislocation densities as low as $10^6\,\mathrm{cm}^{-2}$ are becoming commercially available. Furthermore, quartz-free hydride vapor phase epitaxy (QF-HVPE) has realized highly pure homo-epitaxial GaN with low densities of unintentional Si and C impurities.[1] Fujikura *et al.*[2] have successfully reduced the C concentration to less than $5\times10^{14}\,\mathrm{cm}^{-3}$ in the n-GaN epitaxial layer using QF-HVPE and reported a record high electron mobility of $1470\,\mathrm{cm}^2/\mathrm{V\,s}$ for a GaN layer with an electron carrier density of $1.2\times10^{15}\,\mathrm{cm}^{-3}$. In addition, Narita *et al.*[3] have developed state-of-the-art metal-organic vapor phase epitaxy systems for high-quality p-GaN epitaxial layers that can accommodate a wide Mg-doping range from 2×10^{16} to $8\times10^{19}\,\mathrm{cm}^{-3}$.

Progress in homo-epitaxial growth technologies has stimulated the development of vertical-type GaN metal-oxide-semiconductor field-effect transistors (GaN MOSFETs),[4–9] applicable to power converter/inverter systems.

On the other hand, GaN high-electron-mobility transistors (HEMTs) capable of high-frequency and high-power performances are very attractive for the fifth generation (5G) communication system for which an output power of over 1 W will be required for power amplifier transistors operating in W- and E-bands.[10,11] At present, because of several advantages, including simplicity, ease of fabrication, and high transconductance, the Schottky gate (SG) structure is generally used in GaN HEMTs. In the high input RF power regime, however, SG GaN HEMT may suffer from marked leakage currents due to input swings high enough to drive the gate to forward bias.[12] In addition, Gao *et al.*[13] recently reported that the forward gate-bias stress applied to SG AlGaN/GaN HEMT significantly increased gate leakage currents. To overcome these problems related to an SG structure, a metal–insulator–semiconductor (MIS) structure provides a straightforward solution applicable even to state-of-the-art GaN HEMTs.

However, problems related to surface/interface states remain, adversely impacting the performance of GaN MISFETs and MIS-HEMTs.[14,15] For example, vertical MOSFETs showed an unexpectedly low value of the threshold voltage (V_{TH}), which was much lower than the calculated value from the doping concentration and the oxide capacitance.[4,6] Excess charge induced from MOS interface states probably impedes the gate control of potential modulation at the GaN surface. In MIS-HEMTs, problems relating to V_{TH} instability remain unsolved. In particular, higher positive gate biasing of the MIS-HEMTs induces a larger V_{TH} shift toward the forward bias direction.[16,17] The charging state of the interface traps varies with the gate bias, and excess interface charges, particularly at deeper electronic states, are responsible for such V_{TH} fluctuation. The varying occupation state of the interfacial traps makes the operating point of the device dependent on the history of the bias voltage applied. Meanwhile, current collapse is one of the most important problems encountered in HEMT devices. According to the virtual gate model,[18] a high OFF-state drain bias voltage can induce electron trapping at the AlGaN surface states via a tunneling injection at the gate edge on the drain side. Subsequently, surface trapping depletes the underlying 2DEG and increases the drain resistance, leading to an increased dynamic ON resistance, i.e., current collapse. To overcome these problems, understanding their underlying mechanism is of great importance and of practical interest. Consequently, we need appropriate characterization methods and guiding principles for controlling surface/interface states in GaN-based MIS structures.

In this Tutorial, we introduce models of interface (surface) states, effects of interface states on device performances, a guiding principle for controlling interface states, capacitance–voltage (C–V) characterization of MIS HEMT structures, surface passivation, and a comparison of MOS interfaces between GaN and conventional III–V semiconductors. In Sec. II, we describe models of intrinsic and extrinsic surface/interface states, the charging conditions of interface states, and pinning of the surface Fermi level. In Sec. III, we discuss GaN MOS conventional characterization methods including their limitations and possible pitfalls. We also underline some guiding principles to consider for the effective control of surface and interface electronic states. The first half of Sec. IV explains the impact of surface states in device access regions on the current–voltage (I–V) characteristics of SG-HEMTs, while the second half presents the adverse effects of insulator/semiconductor interface states in MIS-HEMTs on V_{TH} instability, current linearity, and channel mobility. Characterization and interpretation of the rather complicated AlGaN/GaN MIS-HEMT C–V profiles are presented in Sec. V. Here, we also describe the photo-assisted C–V measurement method that we have developed, as well as explain the important relevant information that can be extracted out of these measurements. In Sec. VI, we compare the MOS interfaces in the GaN system with those in other III–V compound semiconductor families.

We also attempt to shed light on some confusion and misconceptions related to III-nitride/insulator interfaces in published literature. Finally, we will highlight some aspects that need further investigations for better understanding and control of surface and interface states haunting GaN-based devices as well as attempt to guide researchers of the same field on what direction their research should take next.

II. MODELS OF SURFACE AND INTERFACE STATES

A. Intrinsic and extrinsic surface states

Since the surface is the termination of a bulk crystal, i.e., breakdown of the crystalline periodicity, the electronic structure in the vicinity of the surface is markedly different from that of the bulk. Even if the surface atomic configuration is completely ordered, the bonding partners on one side are missing for the topmost atoms (dangling bonds), as illustrated in Fig. 1. This means that their wave functions have less overlap with those of neighboring atoms, as compared with the bulk atomic configuration. The stronger the perturbation caused by the surface, the greater the deviation of surface energy states from the bulk electronic state (Bloch state). Such surface states are often called "intrinsic" states.[19]

Tersoff[20] proposed that surface states in the bandgap originally emanate from the valence and conduction bands of

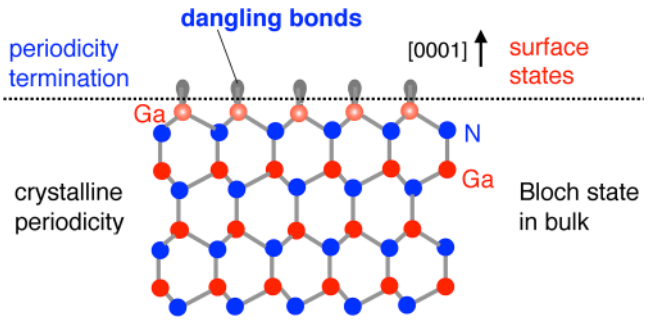


FIG. 1. Schematic illustration of a GaN (0001) surface. Even if the surface atomic configuration is completely ordered, the bonding partners on one side are missing for the topmost atoms (dangling bonds).

semiconductors, and that the density of gap states take weights from those bands, as schematically shown in Fig. 2(a). Therefore, the charging character of surface states also reflects those of the valence and conduction bands. Namely, a negative charge appears in the conduction band if a state is occupied by an electron. Thus, the upper portion of states derived from the conduction band exhibits an acceptor-like character. On the other hand, the lower part of states derived from the valence band has a donor-like character, because the valence band state is positively charged when unoccupied, as shown in Fig. 2(b). Thus, it can be assumed that the surface state continuum consists of a mixture of acceptor- and donor-like states, and their branch point acts as a charge-neutral level (E_{CNL}).[20]

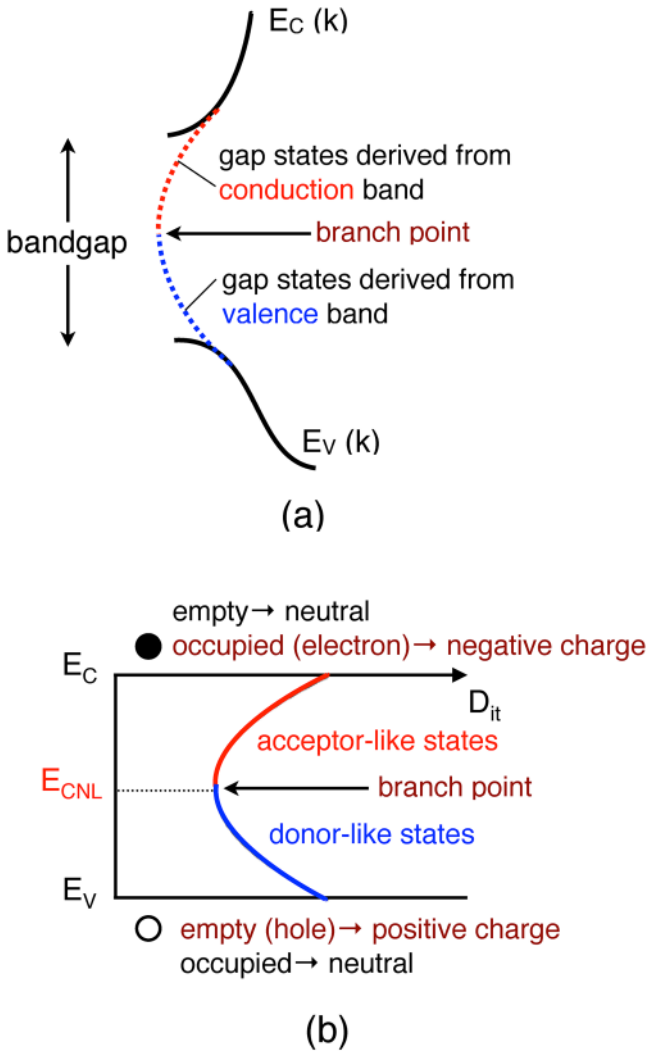


FIG. 2. Intrinsic surface state model. Surface states in the bandgap originally emanate from the valence and conduction bands of semiconductors. (b) Acceptor-like and donor-like surface states, arising from charging characters of conduction and valence bands, respectively.

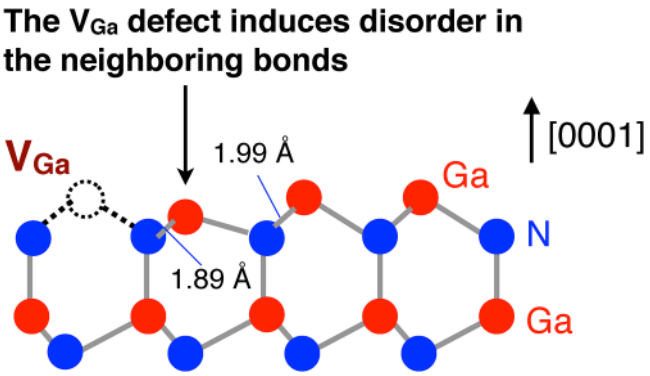


FIG. 3. V_{Ga}-induced lattice disorder at the GaN(0001) surface.

An actual semiconductor surface involves vacancies, adatoms, dimers, etc., causing peculiar energy levels within the bandgap. These levels are called "extrinsic" surface states. For example, it was reported from theoretical calculations that the vacancies (V_{Ga} and V_N) in GaN induce discrete levels in the vicinity of the valence- and conduction-band edges,[21–23] respectively. For the m-plane GaN surface, theoretical calculations predicted the formation of the Ga–N dimer, creating corresponding gap levels.[24–26] In addition, surface defects can enhance lattice disorder in bond lengths and angles. In the case of Ga vacancy on the GaN(0001) surface, Xue *et al.*[27] theoretically pointed out that a change in the charging state of the N dangling bond of a second layer N atom induces a downward relaxation of the neighboring Ga atom along with the c axis, as schematically shown in Fig. 3. The disorder-induced gap state (DIGS) model[28] proposed that such bond disorder on semiconductor surfaces produces electronic states with density distributions in both energy and space. Figure 4 shows an example of surface (interface) state density distribution from a practical semiconductor

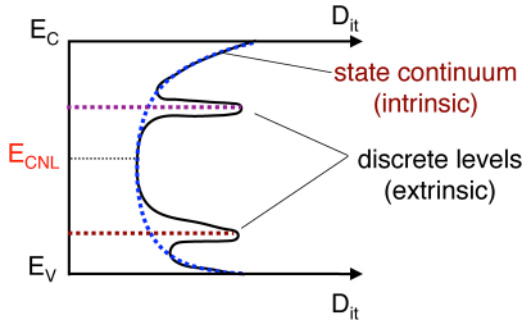


FIG. 4. An example of surface (interface) state density distribution at a practical semiconductor surface (interface), consisting of intrinsic state continuum and extrinsic discrete levels originating from surface defects and/or specific atomic bonding.

surface (interface), consisting of intrinsic state continuum and extrinsic discrete levels originating from surface defects and/or specific atomic bonding.

B. Interface state charge as a function of the surface Fermi level

Since the surface (interface) state continuum consists of a mixture of acceptor- and donor-like states, the charging condition of the surface (interface) states greatly depends on the E_F position. An MOS band structure with an n-type semiconductor is illustrated in Fig. 5. When a positive gate voltage V_{G1} is applied to the MOS structure, the surface Fermi level (E_{FS1}) is located above E_{CNL}, as shown in Fig. 5(a). In this case, the donor-like states occupied with electrons are neutral, while the acceptor-like states with energies between E_{FS1} and E_{CNL} capture electrons, resulting in "negative" interface charges with density D_{itA}^- as follows:

$$D_{itA^-} = \int_{E_{CNL}}^{E_{FS1}} D_{itA}(E)dE. \quad (1)$$

If the surface Fermi level is coincident with E_{CNL} at a given V_{G2} ($E_{FS2} = E_{CNL}$), as shown in Fig. 5(b), the acceptor-like states are fully empty, while all donor-like states are occupied with electrons, leading to the neutral condition for both interface states, as stated earlier. When the surface Fermi level is positioned below E_{CNL} [Fig. 5(c)], the empty donor states at energies between E_{CNL} and E_{FS3} generate "positive" charges with density D_{itD}^+, as follows:

$$D_{itD^+} = \int_{E_{FS3}}^{E_{CNL}} D_{itD}(E)dE. \quad (2)$$

As a result, the negative acceptor charges (D_{itA}^-) and positive donor charges (D_{itD}^+) screen the applied gate electric field at the positive and negative gate biases, respectively. This leads to the well-known "stretch-out" behavior in a C–V curve of an MOS diode, as schematically shown in Fig. 6.

C. Pinning of the surface Fermi level at free semiconductor surfaces

For a "free" semiconductor surface, surface states generally induce band bending. As shown in Fig. 7(a), the flat-band condition for an n-type semiconductor would induce only negative surface charges, because the acceptor-like surface states at energies below the surface Fermi level (E_{FS}) easily capture electrons. However, this is prohibited by the charge neutrality law, because there is no counterpart of positive charge in the bulk region. To preserve the charge neutrality condition, the bulk semiconductor has to produce positive charges balancing with surface negative charges. An upward band bending is then necessary to generate ionized donors (N_D^+) in the semiconductor depletion layer. The resultant downward shift of E_{FS} decreases surface acceptor charges. Finally, as shown in Fig. 7(b), the E_{FS} is fixed at the specific position for maintaining the charge balance between surface acceptor states and shallow donors in the depletion layer. In the case of a p-type semiconductor surface, the charge balance between surface

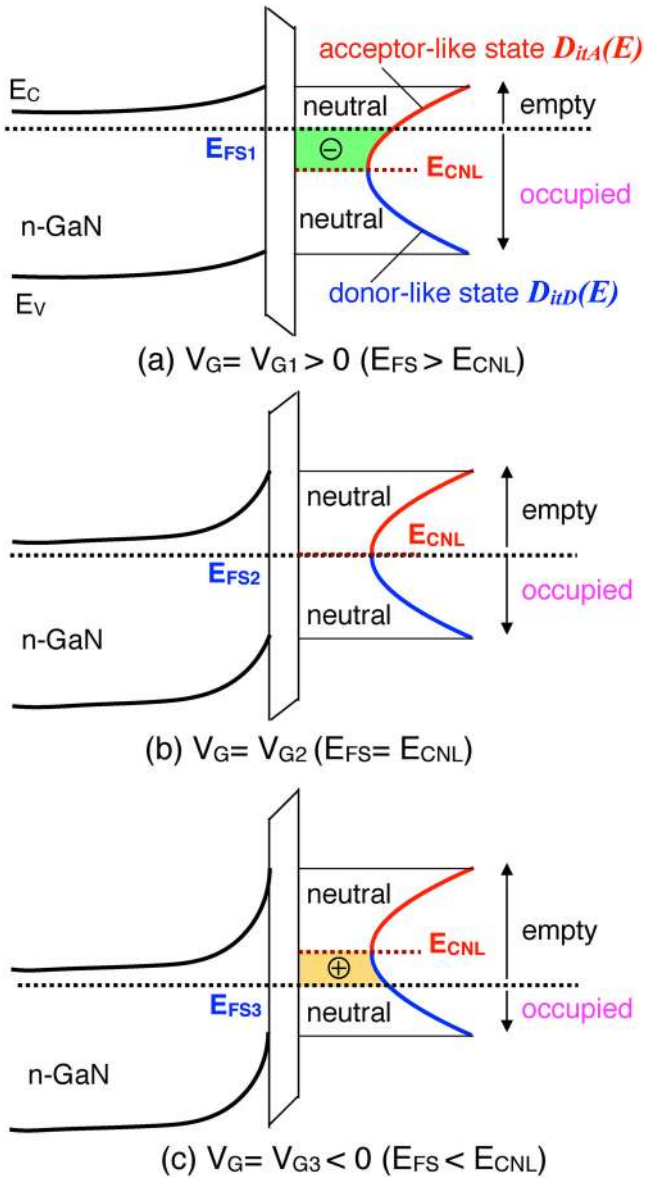


FIG. 5. Charging conditions of interface states as a function of surface Fermi level (E_{FS}) relative to the charge neutrality level (E_{CNL}) for an MOS structure using an n-type semiconductor. (a) Negative interface charge induced by the ionization of acceptor states, (b) neutral condition, and (c) positive interface charge induced by the ionization of donor states.

donor states and shallow acceptors in the depletion layer (N_A^-) causes a downward band bending, as shown in Fig. 7(c). When a semiconductor surface has a relatively low state density with a wide distribution, the band bending is rather small, as shown in Fig. 8(a). On the other hand, a high density of surface state with a narrow distribution fixes the E_{FS} position near E_{CNL}, as shown in

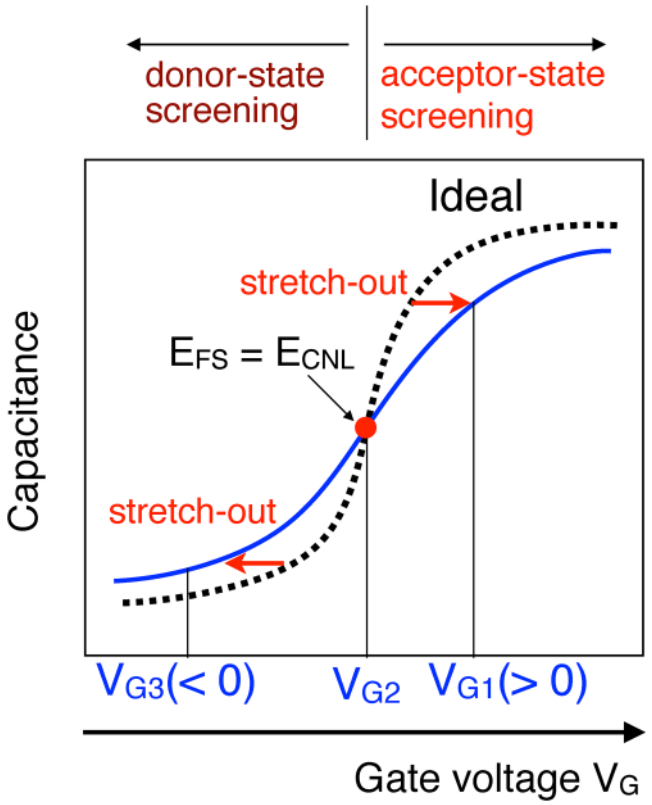


FIG. 6. Stretch-out behavior in a *C–V* curve of an MOS diode caused by screening charges of donor- and acceptor-like interface states.

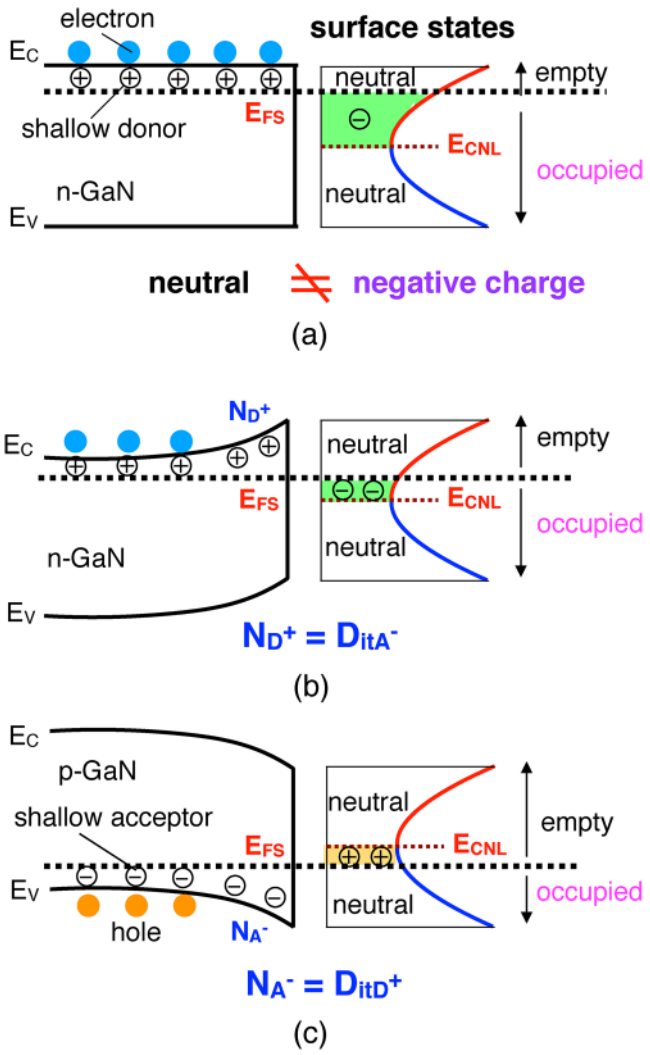


FIG. 7. Band-bending effect at a free semiconductor surface, originating from charge balance between surface state charges and an ionized shallow donor/acceptor in the semiconductor depletion layer.

Fig. 8(b), resulting in large band bending. Namely, the "surface pinning" of E_{FS} takes place at the semiconductor surface. In the case of GaN and AlGaN surfaces, the strong pinning of the surface potential can act as a virtual gate, causing the famous "current collapse" effects on GaN-based HEMTs,[18] which will be discussed in detail in Sec. IV.

III. CHARACTERIZATION AND CONTROL OF GaN MOS INTERFACES

A. Energy range for interface states detectable in admittance measurement

Having a wide bandgap, GaN can contain electronic states located deeper from band edges so much so that some of them can remain insensitive to probing external bias. It is, therefore, crucial to identify the energy range that can contribute to admittance measurements. From Shockley–Read–Hall (SRH) statistics, the time constant τ of electron emission from the interface state to the conduction band is given as follows:

$$\tau = \frac{1}{\nu_{TH}\sigma_{TH}N_C}\exp\left(\frac{E_T}{kT}\right), \tag{3}$$

where E_T, σ_{TH}, ν_{TH}, and N_C are the energy of the interface states measured from E_C, the capture cross-section of interface states, the electron thermal velocity, and the effective density of states at the conduction band edge, respectively. Assuming a typical value of $1 \times 10^{-16}\,\mathrm{cm}^2$ for σ_{TH}, we can obtain a plot of E_T vs T, as shown in Fig. 9(a). According to Eq. (3), the time constants of interface states near midgap or at deeper energies can be extremely long ($\geqq 10^{20}$ s) at RT. This means that electrons, once captured at such deep states, can remain trapped even when their state energies are far greater than the surface Fermi level (E_{FS}), as schematically shown in Fig. 9(b). If we assume 10^3 s for the detectable limitation time in admittance measurements, interface states at energies below $E_C - 0.7$ eV behave like "frozen states."

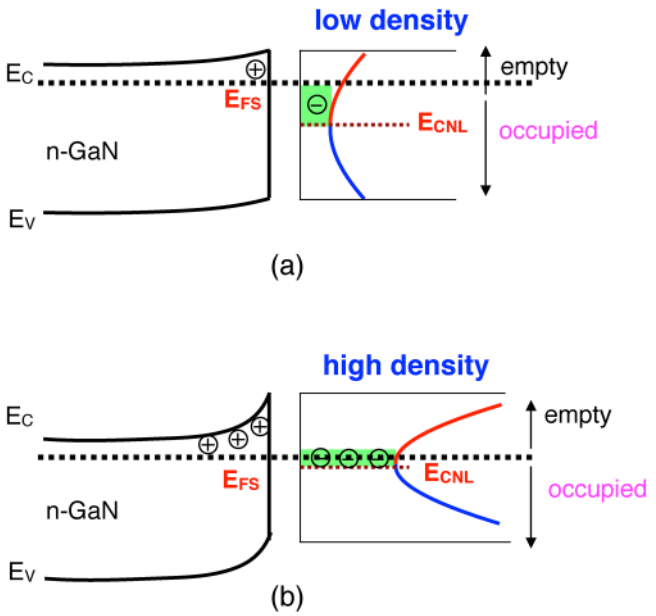


FIG. 8. Surface band bendings for (a) low surface state density with a wide distribution and (b) high density of surface states with a narrow distribution. The latter case fixes the E_{FS} position near E_{CNL}, namely, the Fermi level pinning at a semiconductor surface.

Thus, the detectable energy range is very limited using admittance measurements at RT.

To circumvent this limitation, it is very useful to carry out admittance measurements at elevated temperatures. At 200 °C, for example, the detectable energy depth is extended to around E_C − 1.3 eV, as shown in Fig. 9(c). Since GaN transistors are intended to be employed in high power operations, an increase in the channel temperature up to 100 °C or higher is not uncommon.[29–31] From this viewpoint, a high-temperature admittance measurement is also meaningful for evaluating the device performance and operation stability of a practical MOS device. An example of temperature-dependent *C*–*V* characteristics from an Al_2O_3/n-GaN diode is shown in Fig. 10. No interface control process was performed on the MOS diode (as-prepared condition). At RT, relatively good *C*–*V* characteristics with small hysteresis were observed. When the measurement temperature was raised to 200 °C, however, the drastic transformation of the *C*–*V* characteristics was observed, i.e., significant hysteresis emerged together with the decrease in the *C*–*V* slope (stretch-out). This indicates that the electron emission rates at deeper interface states are enhanced at higher temperatures and that their charging/discharging behavior significantly degraded *C*–*V* characteristics at 200 °C. Matocha *et al.*[32] and Bae *et al.*[33] also pointed out that the interface state charges at deeper energies play a part at high temperatures, leading to a degradation of *C*–*V* characteristics.

In addition to the high-temperature method, admittance measurements using low-frequency ac signals are also capable of characterizing interface states at relatively deep energies. By lowering

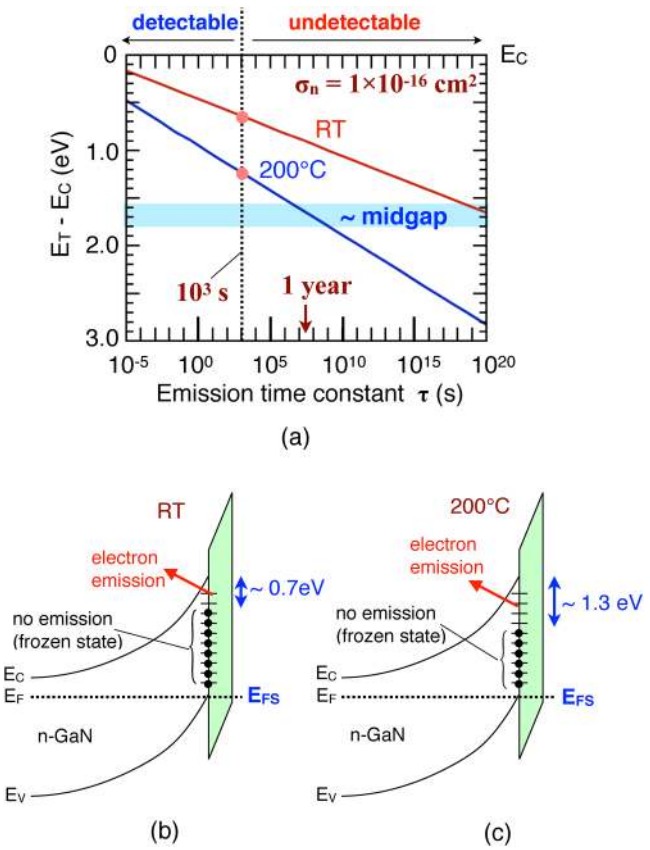


FIG. 9. (a) Time constant τ of electron emission from the interface state to the conduction band as a function of the energy depth from the conduction band edge. For calculation, we used a typical value of 1×10^{-16} cm^2 to capture cross section σ_{TH} of interface states. Estimated ranges for electron emission from interface states at the GaN MOS interface at (b) RT and (c) 200 °C.

the frequency of the ac measurement signal, deeper interface states are expected to respond accordingly to an ac signal, contributing to an additional component to the measured capacitance. To illustrate this phenomenon, *C*–*V* curves of the Al_2O_3/n-GaN structure without an interface control process (the as-prepared sample) are shown in Fig. 11. In a reverse bias regime, significant frequency dispersion with ledge-like features was observed, arising from high densities of interface states.[32] From Terman's analysis of the data, it was found that the as-deposited sample had high interface state densities in the order of 10^{12} cm^{-2} eV^{-1} at around E_C–0.5 eV.

In frequency-dependent *C*–*V* measurements, we have to pay attention to the apparent frequency dispersion of capacitance at forward bias. To clarify this point, we introduce an experimental example for a planar-type MOS sample. In this case, the Al_2O_3 MOS structure was fabricated on a thin GaN layer (0.7 μm) grown on an insulating sapphire substrate, as shown in Fig. 12(a). The sample had a non-optimized layout design with a long distance (400 μm) between the gate and the ohmic electrodes. As shown in

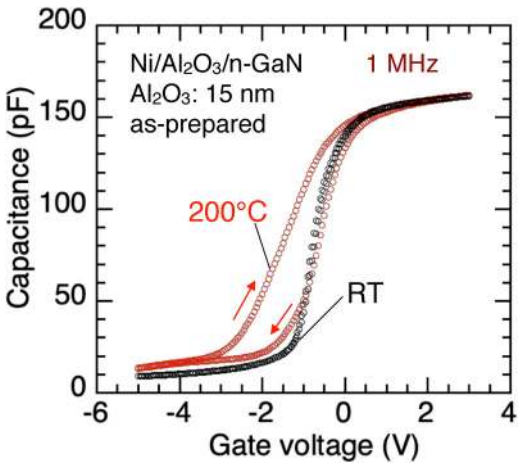


FIG. 10. An example of temperature-dependent *C–V* characteristics of the Al_2O_3/n-GaN diode. No interface control process was performed on the MOS diode (the as-prepared condition).

Fig. 12(b), the *C–V* characteristics showed anomalous frequency dispersion at a forward bias, i.e., a decrease in the accumulation capacitance at high frequencies over 100 kHz. Such an apparent effect is caused by the high equivalent resistance connected in series with the intrinsic MOS capacitor, arising from the access resistance, R_S, between the gate and the ohmic electrodes, as shown in Fig. 13(a). To verify this, a simple calculation of ideal *C–V* characteristics was carried out on the basis of an equivalent circuit

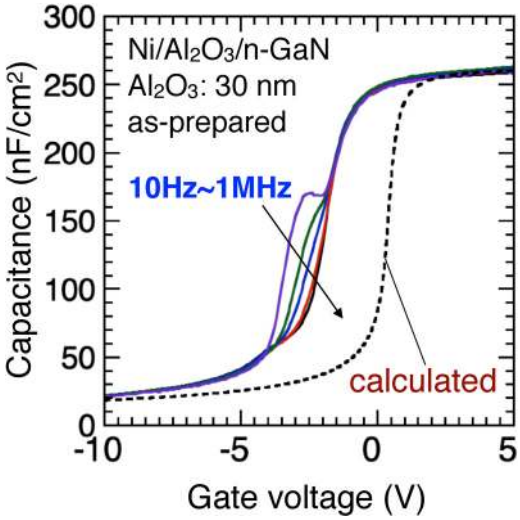
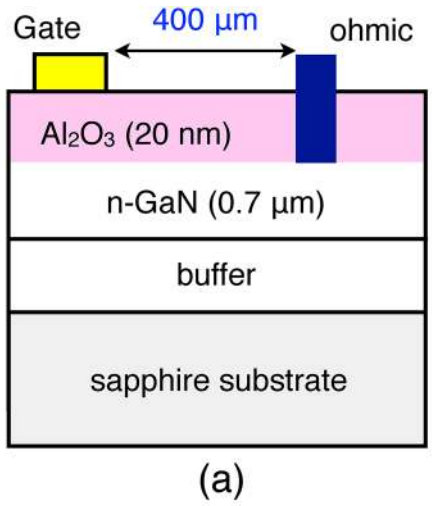


FIG. 11. *C–V* curves of the Al_2O_3/n-GaN structure without an interface control process (the as-prepared sample). At a reverse bias, a significant frequency dispersion and a ledge-like feature were observed, arising from the high densities of interface states.



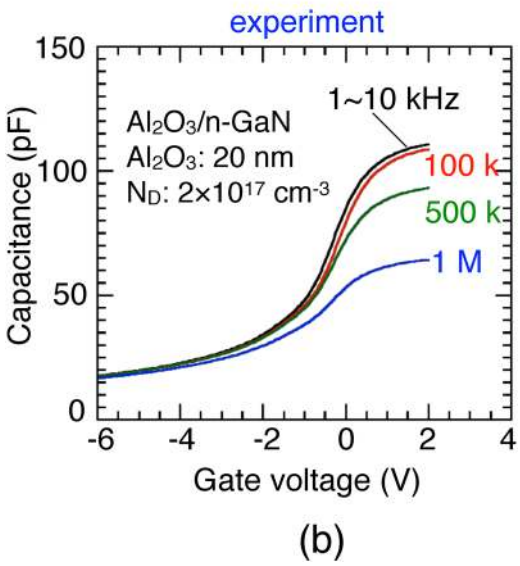


FIG. 12. (a) A planar-type Al_2O_3 MOS structure fabricated on a thin GaN layer (0.7 μm) grown on an insulating sapphire substrate. (b) Experimental *C–V* characteristics with anomalous frequency dispersion at a forward bias, i.e., a decrease in the accumulation capacitance at high frequencies over 100 kHz.

shown in Fig. 13(a). Calculation results using $R_S = 1.2\,k\Omega$ reasonably replicated apparent frequency dispersion of capacitance at an accumulation bias, as shown in Fig. 13(b). This value of $R_S = 1.2\,k\Omega$ is close to the access resistance between the gate and the ohmic electrodes, estimated from the electron density and mobility of the thin GaN layer. Therefore, if a peculiar frequency dispersion of capacitance is observed at high frequencies, as shown in Fig. 12(b), one has to carefully inspect the non-negligible and appreciable value of R_S due to high access resistance or even due to the degradation of the ohmic electrode. To check such effect of the series

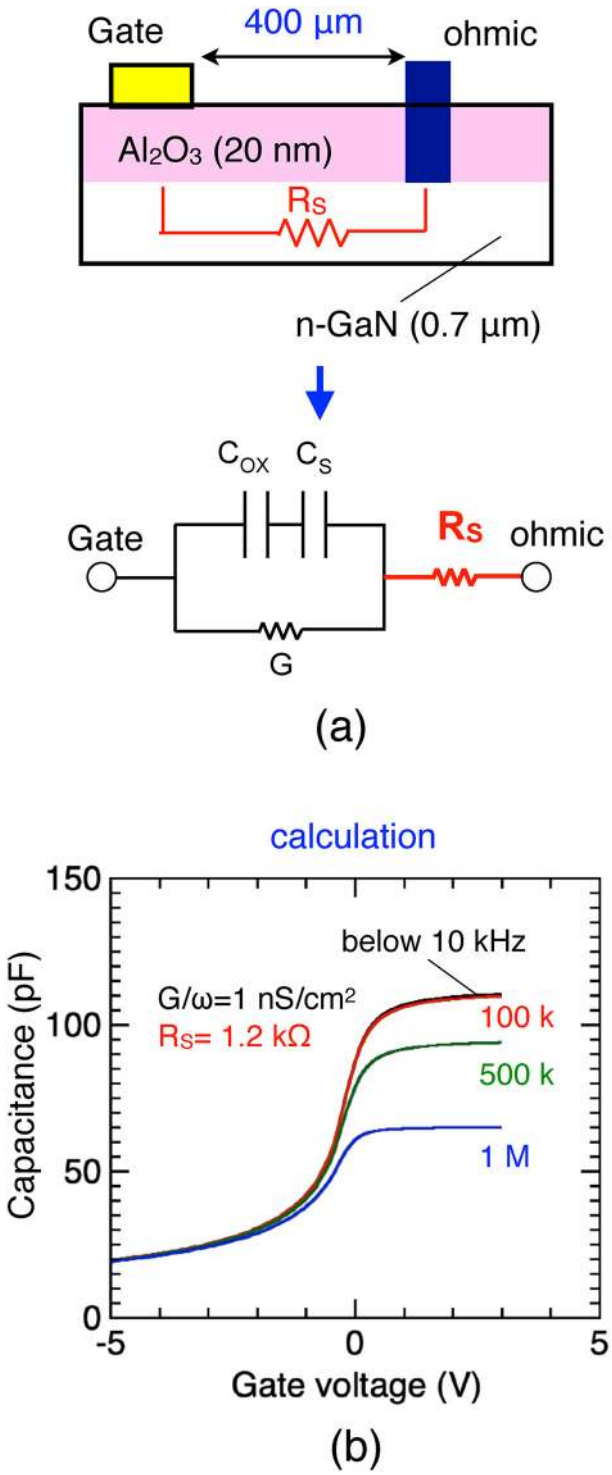


FIG. 13. (a) Schematic illustration of access resistance R_S between the gate and the ohmic electrodes, and the equivalent circuit of the MOS structure. (b) Calculated *C–V* curves assuming R_S = 1.2 kΩ.

resistance experimentally, it is useful to measure *C–V* characteristics by selecting the "series circuit mode" in an impedance analyzer. In this case, if the disappearance of the frequency dispersion is confirmed, then it can be concluded that a relatively high resistance connected in series to the MOS capacitance impedes normal *C–V* measurements using a standard "parallel circuit mode."

B. Choice of gate dielectric for GaN MIS devices

To build up a stable MIS gate structure applicable to GaN-based power transistors, we have to consider the basic properties of insulators such as bandgap, permittivity, breakdown field, and chemical stability. In addition, an understanding and control of insulator/semiconductor interface properties is a requisite for realizing high-performance GaN MIS transistors. Figure 14 shows the relationship between bandgap and permittivity for major insulators. For sufficient suppression of the gate leakage current even at a forward bias, a gate insulator with a wide bandgap causing large band offsets at the insulator/semiconductor interface is needed. This is indispensable for a robust operation of power switching transistors applicable to power conversion systems. In this regard, materials having an E_G of over 6 eV can function as a suitable gate insulator. On the other hand, high-κ (κ > 10) materials are attractive for the fabrication of MIS-HEMTs with high transconductance (g_m), leading to high f_T in RF amplifier devices.

Although a SiO_2 film has a low permittivity (3.9), it is still of particular interest for MOS power transistor applications because of its large bandgap and chemical stability. Yamada *et al.*[34] and Yamamoto *et al.*[35] demonstrated that state densities at SiO_2/GaN interfaces were remarkably reduced by utilizing a thin GaO_x interlayer. Al_2O_3 is also suitable as a gate insulator in power MIS-HEMTs, because it possesses a relatively high permittivity (8 ~ 9). However, it is well known that a polycrystalline structure is generated in the Al_2O_3 layer when it is subjected to process

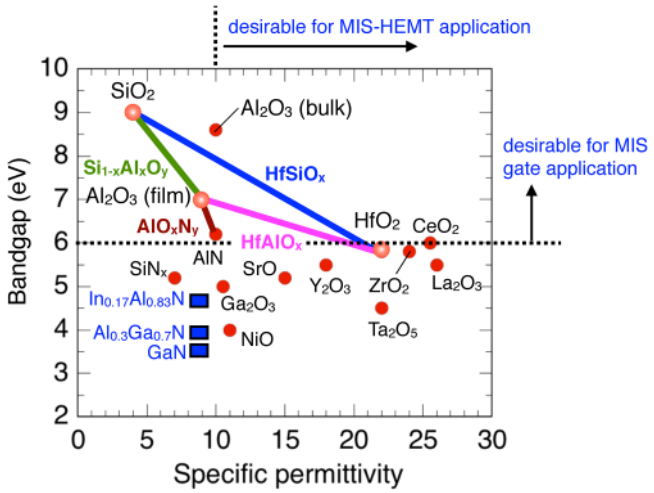


FIG. 14. Relationship between bandgap and permittivity for major insulators, $HfSiO_x$, $HfAlO_x$, AlO_xN_y, and $Si_{1-x}Al_xO_y$.

temperatures reaching 800 °C.[36,37] Grain boundaries in polycrystalline Al_2O_3 can lead to a significant increase in the leakage current in Al_2O_3/GaN structures.[37,38] To mitigate this problem, an aluminum oxynitride (AlO_xN_y) gate has been applied to AlGaN/GaN MOS-HEMTs.[37] Good *C*–*V* curves with a typical two-step behavior and negligible frequency dispersion were observed in those devices, indicating relatively low trap densities at the AlO_xN_y/AlGaN interface. Kikuta *et al.*,[39] on the other hand, developed an ALD process for Al_2O_3/SiO_2 nanolaminate structures, equivalently corresponding to $Al_{1-x}Si_xO_y$ films on GaN. When compared with Al_2O_3, they reported a higher breakdown field for $Al_{1-x}Si_xO_y$ with equivalent SiO_2 composition in the 0.21–0.69 range. Meanwhile, hafnium silicate ($HfSiO_x$) films with Hf-rich composition are expected to exhibit a high permittivity value (over 10), as indicated by the blue line in Fig. 14, while maintaining an amorphous structure even at an annealing temperature of 800 °C. In this regard, Nabatame *et al.*[40] have developed and investigated $HfSiO_x$ as a gate dielectric for GaN-based devices. After post-deposition annealing (PDA) of a HfO_2/SiO_2 laminate structure at around 800 °C, they achieved a chemically stable amorphous $HfSiO_x$ layer with a high permittivity (~13) and a high breakdown field (~8.6 $MVcm^{-1}$). The subsequent application of $HfSiO_x$ to AlGaN/GaN HEMTs resulted in a high transconductance and excellent operation stability even at high temperatures up to 200 °C.[41]

C. Guiding principle for controlling surface states

A general guiding principle for controlling surface states is to reduce surface defects and to terminate surface dangling bonds by a stable atomic configuration together with a chemically stable insulating film. This absolutely decreases the total energy of the surface, sweeping the DOS from the gap toward the conduction and valence bands. Hashizume *et al.*[42] have developed an interface control process of GaN MOS structures utilizing ALD Al_2O_3 and a post-metallization annealing (PMA) at 300 °C, as schematically shown in Fig 15(a). The *C*–*V* characteristics of Ni/Al_2O_3/n-GaN diodes with and without PMA are shown in Fig 15(b). The as-prepared sample (without PMA) showed *C*–*V* curves with notably evident frequency dispersion and ledge-like features at a reverse gate bias. On the other hand, excellent *C*–*V* characteristics without frequency dispersion were observed in a frequency range from 10 Hz to 1 MHz after PMA under N_2 ambient at 300 °C for 10 min. This indicates that the PMA process had realized low state densities, which was confirmed by conductance method analysis to be ranging from as low as 1 to 4×10^{10} $cm^{-2}eV^{-1}$ at the Al_2O_3/GaN interface.[42]

To gain insight into the bond strain of GaN near the Al_2O_3/GaN interface, the geometric phase analysis (GPA) was conducted to high-resolution transmission electron microscopy (HRTEM) images of the Ni/Al_2O_3/n-GaN structures,[42] generating maps of relative lattice constants along with the c-axis GaN, as shown in Fig. 16(a). The relative value of 1.00 corresponds to the c-axis lattice constant of 0.5186 nm. The MOS sample without PMA showed a scattering of lattice constants near the Al_2O_3/GaN interface, indicating a disorder in the atomic bonding configuration on the GaN surface. As schematically shown in Fig. 16(b), an actual semiconductor surface has dangling bonds and vacancies, causing

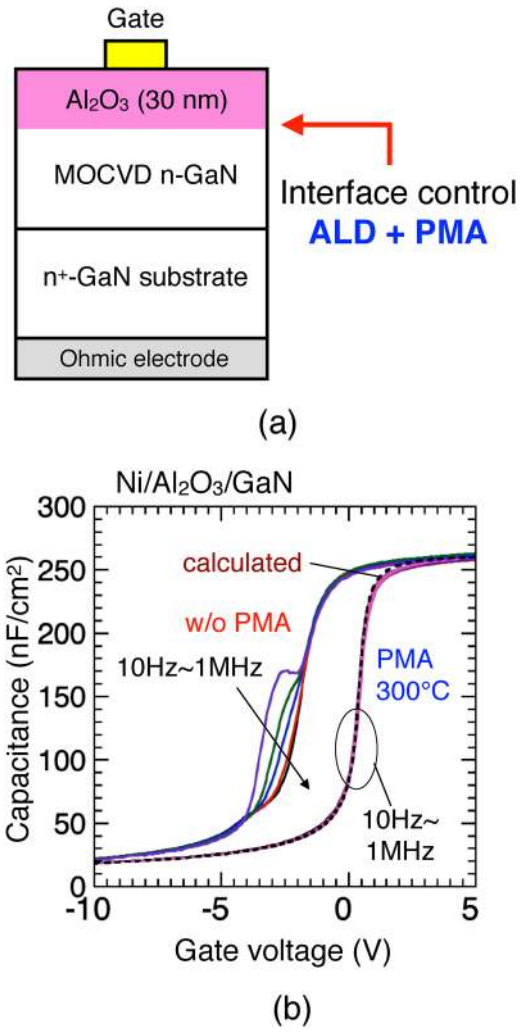
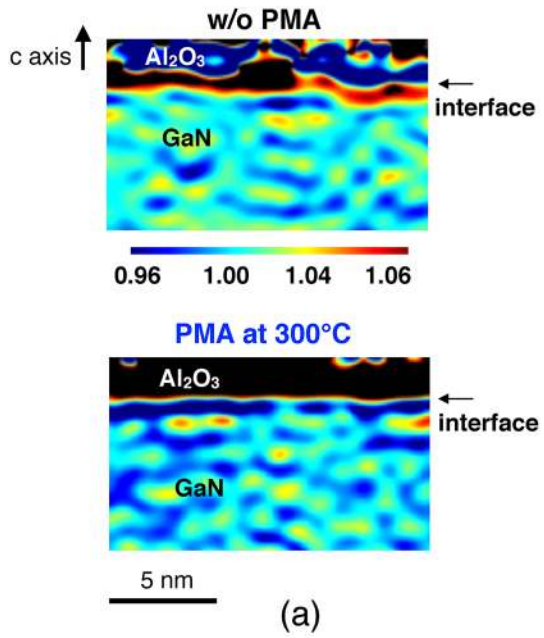


FIG. 15. (a) GaN MOS structure utilizing ALD Al_2O_3 and a post-metallization annealing (PMA) at 300 °C. (b) *C*–*V* characteristics of Ni/Al_2O_3/n-GaN diodes with and without PMA.

lattice disorder in bond lengths and angles. On the other hand, a uniform distribution of the lattice constant near the interface was observed for the sample with PMA at 300 °C, as shown in Fig. 16(a). This indicates that PMA is effective for the relaxation of surface defects and termination of dangling bonds with O atoms, as schematically shown in Fig. 16(b). Zywietz *et al.*[43] and Chokawa *et al.*[44] predicted from theoretical calculations that the termination of Ga dangling bonds with O atoms effectively reduced the density of states (surface states) within the GaN bandgap.

Interestingly, there is also a possibility that a peculiar atomic-bonding configuration at a semiconductor surface contributes to the successful control of interface states. Figure 17 shows a comparison of state densities at the Al_2O_3/GaN interfaces fabricated on c-plane and m-plane GaN surfaces. Even without undergoing the



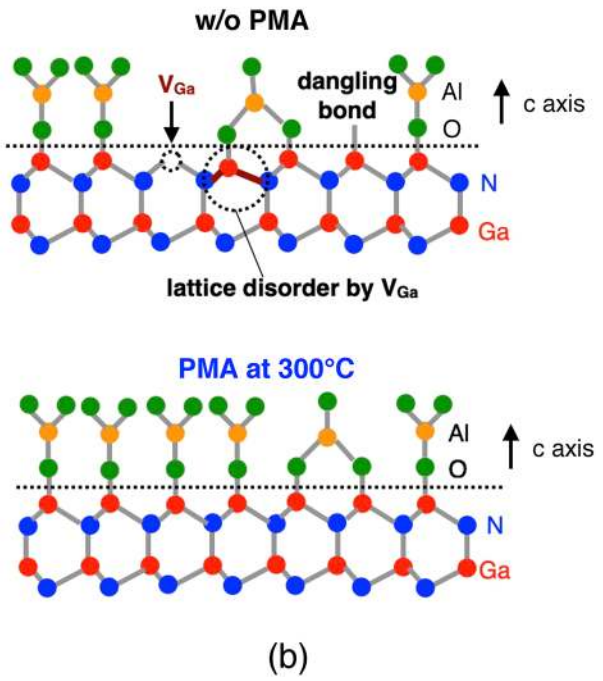


FIG. 16. (a) Maps of relative lattice constants along the c-axis GaN near the Al_2O_3/GaN interfaces. The relative value of 1.00 corresponds to the c-axis lattice constant of 0.5186 nm. The geometric phase analysis was applied to high-resolution transmission electron microscopy images of the Al_2O_3/n-GaN structures. (b) Schematic models of atomic bonding configuration at Al_2O_3/GaN interfaces before and after PMA. Reproduced with permission from Hashizume *et al.*, Appl. Phys. Express **11**, 124102 (2018). Copyright 2018 Japan Society of Applied Physics.

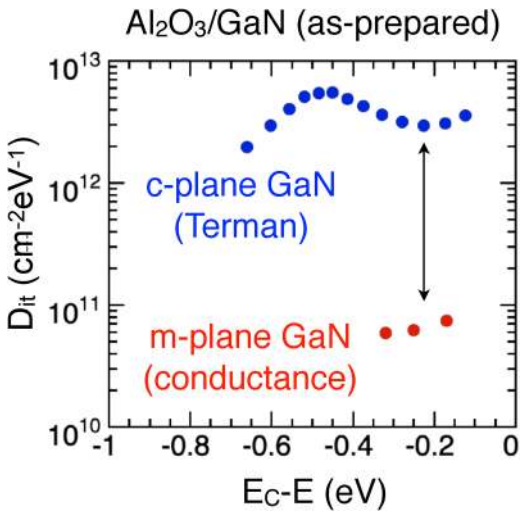


FIG. 17. Comparison of state densities at the Al_2O_3/GaN interfaces fabricated on c-plane and m-plane GaN surfaces.

PMA process (the as-prepared condition), the MOS sample on the m-plane GaN surface showed low interface state densities in the order of $10^{10}\,cm^{-2}\,eV^{-1}$, which are significantly lower than those of the Al_2O_3/c-plane GaN interface. Very recently, Ando *et al.*[45] also provided proof that D_{it} at the Al_2O_3/GaN interface for the m plane is lower than that for the c plane. Several theoretical studies demonstrated that the Ga–N dimer structure is most stable on the m-plane GaN surface.[24,25,26,46] In addition, the specific electronic states originating from the Ga–N dimer were detected on the m-plane GaN surfaces by *in situ* photoelectron spectroscopy[47] and scanning tunneling spectroscopy.[48] Therefore, it is likely that the m-plane GaN surface has a stable atomic bonding configuration consisting of Ga–N dimers, as illustrated in Fig. 18(a). The stable dimer structure is beneficial for controlling dangling bonds and vacancy defects on the m-plane GaN surface. During the initial stage of the ALD Al_2O_3 deposition, bond breaking of the Ga–N dimer at an elevated temperature of 300 °C could occur, as shown in Fig. 18(b). The subsequent ALD process can terminate the topmost bonds with O–H radicals, followed by the formation of the Al_2O_3 layer, as schematically shown in Figs. 18(c) and 18(d), leading to low state densities at the Al_2O_3/GaN interface even for the sample without PMA (the as-prepared sample). The PMA process at 300 °C further lowered D_{it} to $2.0 \times 10^{10}\,cm^{-2}\,eV^{-1}$, as in the case of the MOS sample on the c-plane GaN.

A thin GaO_x layer was also reportedly utilized as an interface control layer for SiO_2/GaN structures.[34,35] Yamada *et al.*[34] deposited a 2-nm-thick GaO_x layer on GaN by sputtering, followed by a deposition of thick SiO_2 and subsequent post-deposition annealing (PDA) at 800 °C. Yamamoto *et al.*[35] deposited 20-nm SiO_2 on the O_2-plasma-treated GaN surface by remote plasma CVD and carried out PDA at 600–800 °C. Both MOS diodes exhibited good *C–V* characteristics without frequency dispersion, resulting in low interface state densities in the order of $10^{10}\,cm^{-2}\,eV^{-1}$. In these

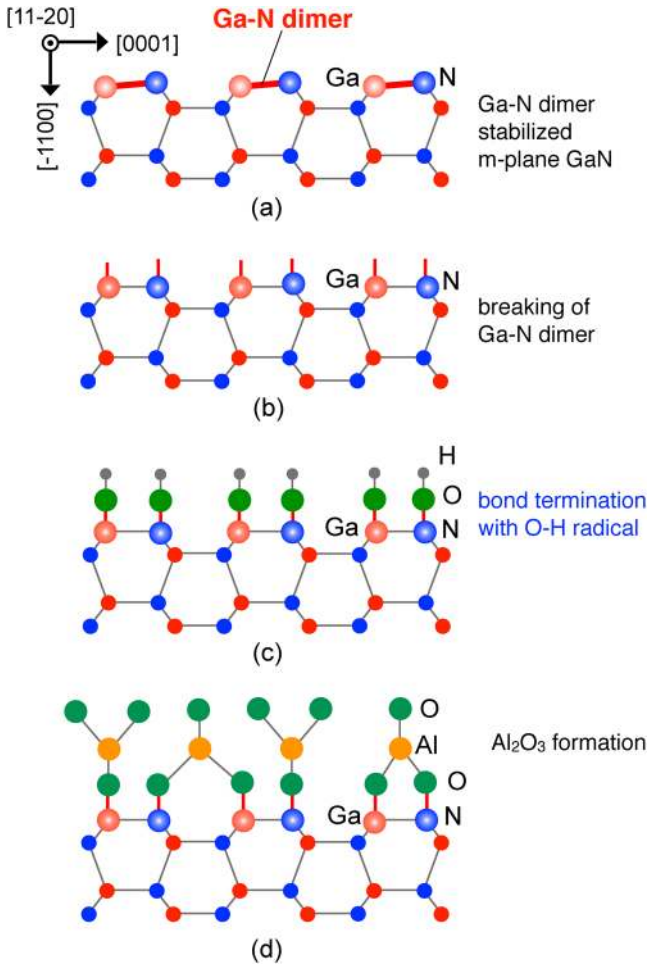


FIG. 18. Models of atomic bonding configuration of m-plane GaN surfaces: (a) Ga–N dimer stabilization, (b) bond breaking of the Ga–N dimer at the elevated temperature of 300 °C in the initial stage of the ALD Al_2O_3 deposition, (c) termination of topmost bonds with O–H radicals, and (d) subsequent deposition of the Al_2O_3 layer.

cases, the topmost bonds are likely terminated with O atoms and/or Ga–O radicals.

IV. IMPACT OF SURFACE AND INTERFACE STATES ON DEVICE PERFORMANCE

A. Trapping and current collapse phenomena

The performance of a semiconductor device is highly sensitive to the quality of the surface as well as interfaces between the materials from which it was fabricated. Some instability issues such as V_{TH} fluctuation and current degradation greatly hindered the development of AlGaN/GaN HEMTs during their infancy. Among current degradation issues, the so-called current collapse phenomenon, which is a temporary drain current reduction after the

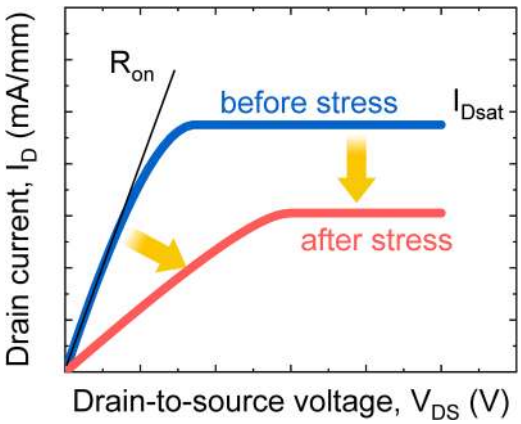


FIG. 19. Schematic illustration of current collapse showing the increase in on-resistance R_{on} and decrease in I_{Dsat} after a bias stress.

application of an electrical bias stress, has been a major obstacle for the realization of highly stable power devices. A simple graphical explanation of this phenomenon is given in Fig. 19, which shows a decrease in the saturation current I_{Dsat} accompanied by an increase in on-resistance, following a DC off-state bias stress.[49,50] The increase in R_{on} is undesirable, because it diminishes the efficiency of the device when used in power-switching and amplifier applications. Another closely related issue is the drain current compression during large signal operations at RF frequencies, known as DC-to-RF dispersion illustrated in Fig. 20. An achievement of 1.1 W/mm power density,[51] a value for state-of-the-art silicon-based LDMOS, in early AlGaN/GaN HEMT prototypes, had raised the expectation for these devices. However, it was found that at high frequencies, AlGaN/GaN HEMTs do not deliver the power output expected from its measured swept DC drain curves.[52]

For sinusoidal signals, the maximum linear output power $P_{o,max}$ is given by

$$\begin{aligned} P_{o,max} &= \frac{1}{T}\int_0^T \frac{\Delta I_D}{2}\sin(\omega t)\frac{\Delta V_{DS}}{2}\sin(\omega t)dt \\ &= \frac{1}{2\pi}\int_0^{2\pi} \frac{\Delta I_D}{2}\frac{\Delta V_{DS}}{2}\left\{\frac{1}{2}[1-\cos(2\omega t)]\right\}dt \\ &= \frac{1}{8}\Delta I_D \Delta V_{DS} = \frac{I_{D_{max}}(V_{Br}-V_K)}{8}. \end{aligned} \quad (4)$$

Here, I_{Dmax}, V_{BR}, and V_K are the maximum drain current, breakdown voltage, and knee voltages, respectively. As can be seen from Fig. 20, the effective RF drain current I_{Dmax}' is lower, while the effective RF knee voltage V_K' is higher, compared with their corresponding values in DC, giving the limited output power.

Both current collapse and DC-to-RF dispersion are believed to be due to the loss of channel electrons due to traps situated anywhere within the device. Traps are energy states within the bandgap capable of capturing carriers, which once captured, the probable subsequent event is the emission of these carriers to their

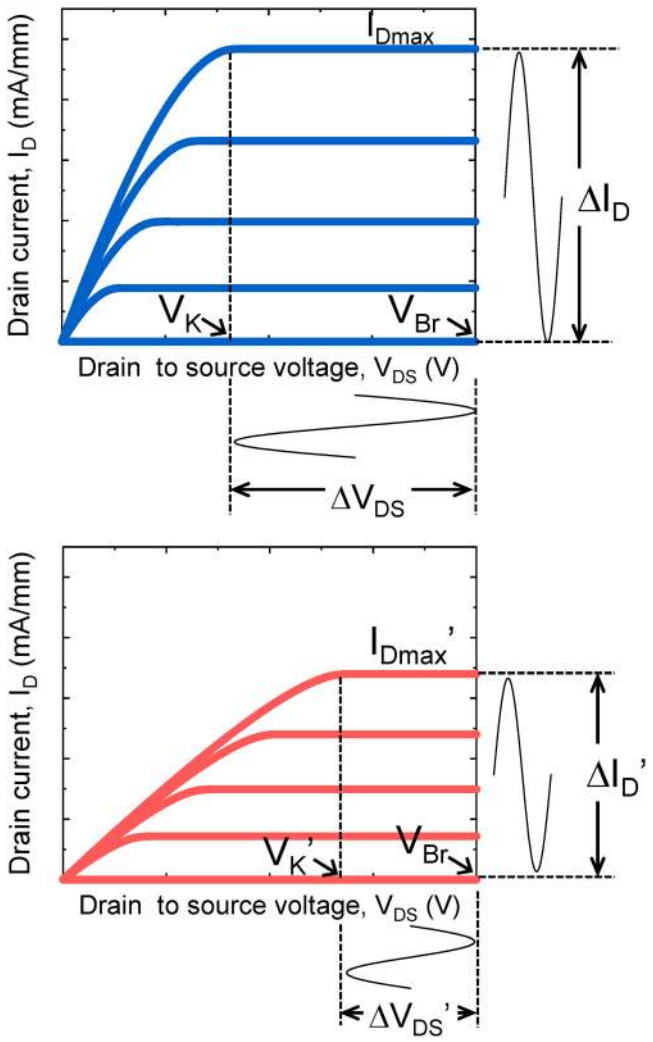


FIG. 20. Schematic illustration of drain curves (I_D–V_{DS}) DC-to-RF dispersion: (top) DC and (bottom) RF large signal I_D–V_{DS} curves.

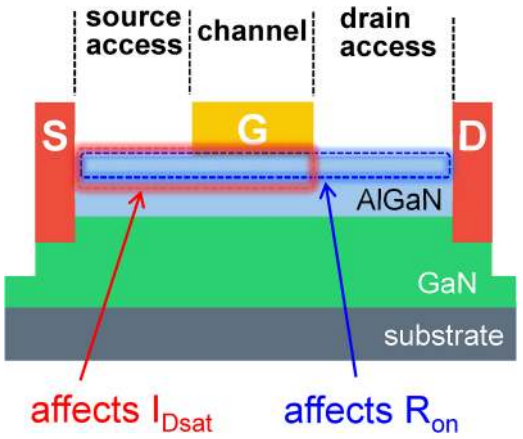


FIG. 21. Cross-sectional schematic illustration of an AlGaN/GaN HEMT showing the possible location of traps and their effect on drain current.

original state, instead of recombination with their opposite pair.[53] Surface states, discussed in Secs. III A–C, located at energy levels more than kT away from band edges fall under this definition. The spatial location of these traps has varying effects on the drain current, as illustrated in Fig. 21. In principle, trapping anywhere within the device increases total resistance between the drain and the source electrodes, and, therefore, increases R_{on}. On the other hand, trapping below the gate and source access region also decreases I_{Dsat}.

In the same way that the established knowledge and technology gained from silicon-based devices have aided the development of GaAs-based devices,[54] studies for identifying and controlling the trapping effects in GaN-based devices have been guided by experience gained from GaAs. The term "collapse" appeared to have been first used to describe the distortion in the form of compression of AlGaAs/GaAs HEMT I_D-V_{DS} curves at liquid nitrogen temperature after the application of a drain bias greater than 1 V.[55] This instability issue was earlier shown to be temporary and recoverable by shining light on the device.[56] It is for this historical reason that current collapse is defined as temporary drain current reduction after the application of an electrical bias stress. Some groups have also acceptably used the term "current degradation" in the literature. It should be pointed out, however, that "degradation" sometimes connotes a permanent unrecoverable change in current.[57,58]

After the ground-breaking demonstration of AlGaN/GaN HEMTs by Khan *et al.*,[59] it did not take long before an analogous current–voltage characteristic collapse was also reported in these wide bandgap semiconductor devices.[60] One of the most successful models in explaining current collapse is the "virtual gate" model proposed by Vetury *et al.*[18] This is schematically illustrated in Fig. 22. With a positive drain bias V_{DS} and negative gate bias V_{Goff}, the drain access region is subjected to a high bias stress equal to the algebraic sum of V_{DS} and V_{Goff}. It is for this reason that trapping is considered to happen predominantly in the drain access region, particularly near the gate edge, where the maximum electric field is located. Electrons from the metal gate can then tunnel toward the AlGaN surface where they can be trapped by the surface states [Fig. 22(a)]. After the negative gate bias V_{Goff} is removed, the trapped electrons cannot instantaneously be emitted from the surface states and instead collectively form a "virtual gate" adjacent to the actual physical gate [Fig. 22(b)], partially depleting the underlying 2DEG. While a 2DEG channel readily forms under the actual gate in response to an applied V_{Gon}, it will take a certain characteristic time constant for the trapped electrons forming the virtual gate to be emitted from surface states. This leads to the apparently reduced drain current, i.e., current collapse, which is actually a delayed response of drain current to the gate voltage. Using scanning kelvin probe microscopy, Koley *et al.*[61] have observed a correlation of drain current and surface potential profile slow transient in AlGaN/GaN HEMTs subjected to bias stress,

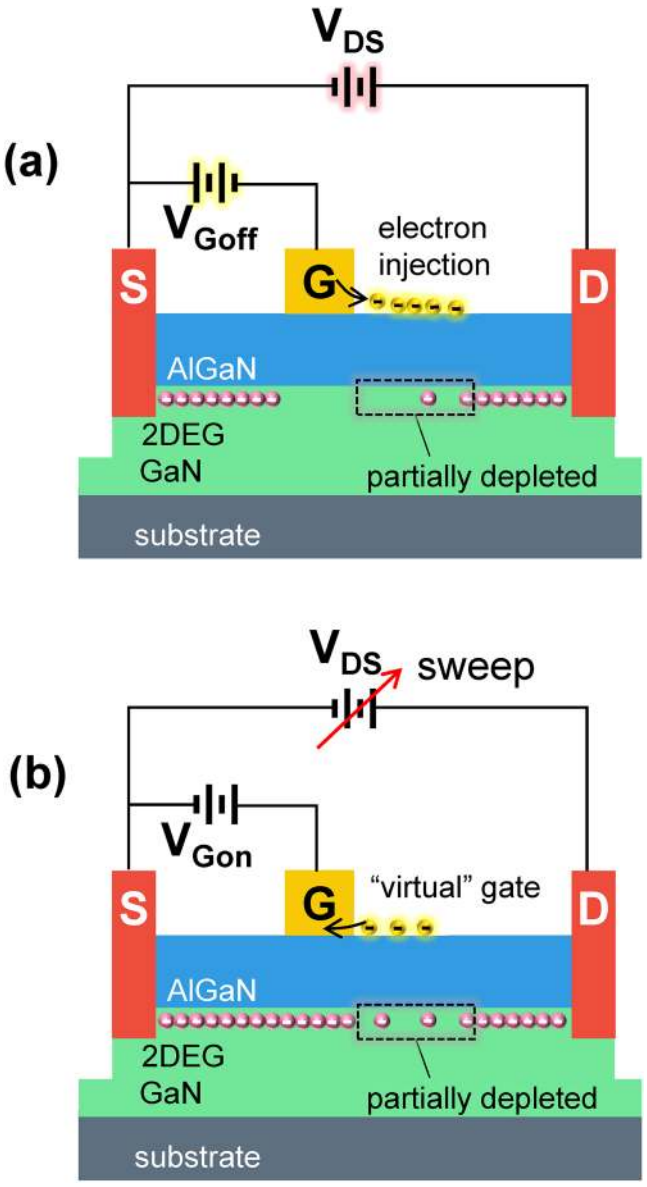


FIG. 22. Schematic illustration of virtual gate formation: (a) AlGaN/GaN HEMT under bias with positive drain bias V_{DS} and gate to source bias V_{Goff} that is more negative than V_{TH}, (b) immediately after replacing V_{Goff} with a gate to source voltage V_{Gon} that is more positive than V_{TH} and sweeping the drain to source voltage V_{DS} from zero.

supporting the idea of electron trapping/detrapping and, therefore, virtual gate formation on the drain access region close to the gate edge. Furthermore, Hasegawa *et al.*[62] explained that the slow response of drain current is due to the emission of trapped electrons from the intrinsic U-shaped surface state continuum, previously discussed in Sec. II A.

B. Surface passivation

It has been known, even for ubiquitous Si-based devices, that surfaces are extremely sensitive to contaminants even in a controlled environment.[63] To make matters worse, surface properties, which are generally unstable and unpredictable, can dictate the electrical characteristics of the devices. This susceptibility of semiconductor devices to ambient contaminants has made passivation one of the standard technologies for achieving stable performance in such devices. It is, therefore, not surprising that one of the initial and most successful methods of mitigating current collapse in AlGaN/GaN HEMTs is by surface passivation. Generally, the passivation layer is an insulating material deposited over a semiconductor device to protect its surface from contamination and further reaction, as illustrated in Fig. 23. Silicon nitride (SiN_x) is one of the earliest well-understood insulating materials, having been used as chemical barrier coatings at different stages of the Si-based device fabrication process.[64]

Using a SiN_x passivation layer, Green *et al.*[65] were able to reduce surface trapping in AlGaN/GaN HEMTs, consequently achieving a state-of-the-art record power density of 4 W/mm at 4 GHz. Since then, the widespread implementation of SiN passivation had raised the standard of output power densities to over 10 W/mm.[66] SiN passivation layer deposition is generally the final step in the device fabrication process and, as such, is usually performed *ex situ*, i.e., in a deposition chamber different from the growth chamber where the epitaxy of the main epitaxial layers is done. To avoid modification of the AlGaN surface from ambient air exposure during chamber to chamber transfer at different stages

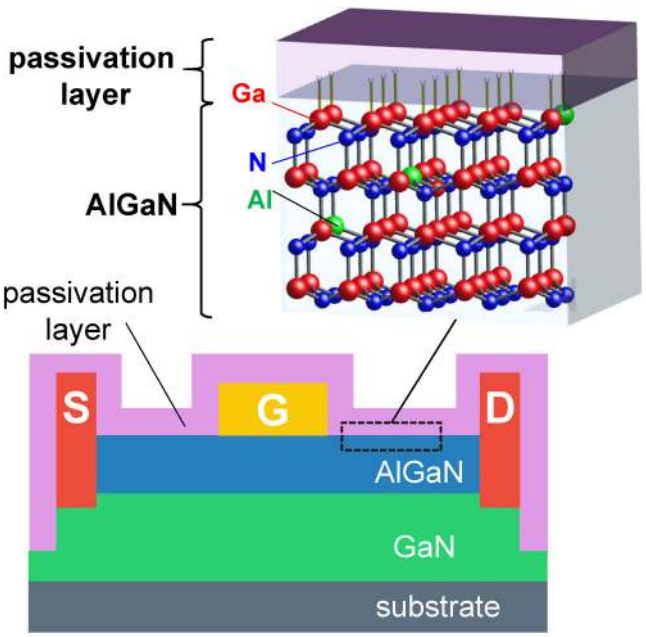


FIG. 23. Schematic illustration of passivation protecting the access region surface from contamination and further reaction.

of fabrication, Derluyn *et al.*, deposited the SiN passivation *in situ*, i.e., immediately following AlGaN growth in the same metal-organic vapor phase epitaxy (MOVPE) chamber.[67] Consequently, superior characteristics including an almost twofold increase in maximum drain current and transconductance were achieved over the un-passivated device.

While universal and substantial improvement in device performance as a result of passivation had been reported, a general mechanism by which passivation effects, such as reduced surface trapping and increased drain current, can be explained has yet to be devised. It has been suggested that the positively charged surface donors, postulated to be the source of 2DEG[68] as well as one of the sources of extrinsic surface states, are buried by passivation, making them inaccessible to electrons injected from the metal gate.[69] On the other hand, an increased positive charge at the passivation layer/AlGaN interface has also been proposed to account for the increased drain current after passivation.[61,65,70–72] Meanwhile, it has also been shown by simulation that passivation relaxes the electric field along the gate edge on the drain side,[73,74] weakening electron injection and eventual trapping on the adjacent AlGaN surface. Finally, as discussed in Sec. III C, we also believe that passivation decreases the total energy of the surface, sweeping the DOS from within the gap toward conduction and valence band edges, effectively reducing the density of states.

C. Role of the gate-to-source access region

Up to this point, current collapse has been mainly attributed to electron injection from the metal gate onto the drain access region, where the maximum electric field is located under a negative gate bias. However, there was proof that trapping is not confined to this region. Arulkumaran *et al.*[71] and Sun *et al.*[75] independently reported that AlGaN/GaN HEMTs with passivation only on the drain access region suffered a much severe current collapse than the device with full passivation including the source access region. On the other hand, with the aid of pulsed I_D–V_{DS} measurements using different quiescent bias conditions that can deliberately induce stress on either the drain access region or only in the source access region, DiSanto *et al.*[76] demonstrated a significant impact on the current collapse of trapping in the source access region.

It is to be noted that the source access resistance R_S forms a loop with the input voltage V_{GS} in such a way that the voltage drop across R_S decreases the effective forward voltage applied to the intrinsic channel region directly under the metal gate. It is for this reason that trapping in the source access region not only increases R_{on} but also decreases I_{Dsat}, as indicated in Fig. 21.

Using a second gate G2 that can intentionally induce surface charging exclusively on the drain access region of the main gate G1, Tajima *et al.*[74] and Nishiguchi *et al.*[77] provided evidence that current collapse can indeed be explained by surface charging and the eventual formation of virtual gates on both drain and source access regions. Figure 24(a) compares the pre- and post-stress I_D–V_{DS} curves measured at gate voltage $V_{G1} = -2$ V. Regardless of the gate terminal used in stressing the device, R_{on} increased after the application of an off-state bias stress consisting of $V_{DSstress} = 30$ V simultaneously applied with $V_{GSstress} = -10$ V. However, G1 and G2

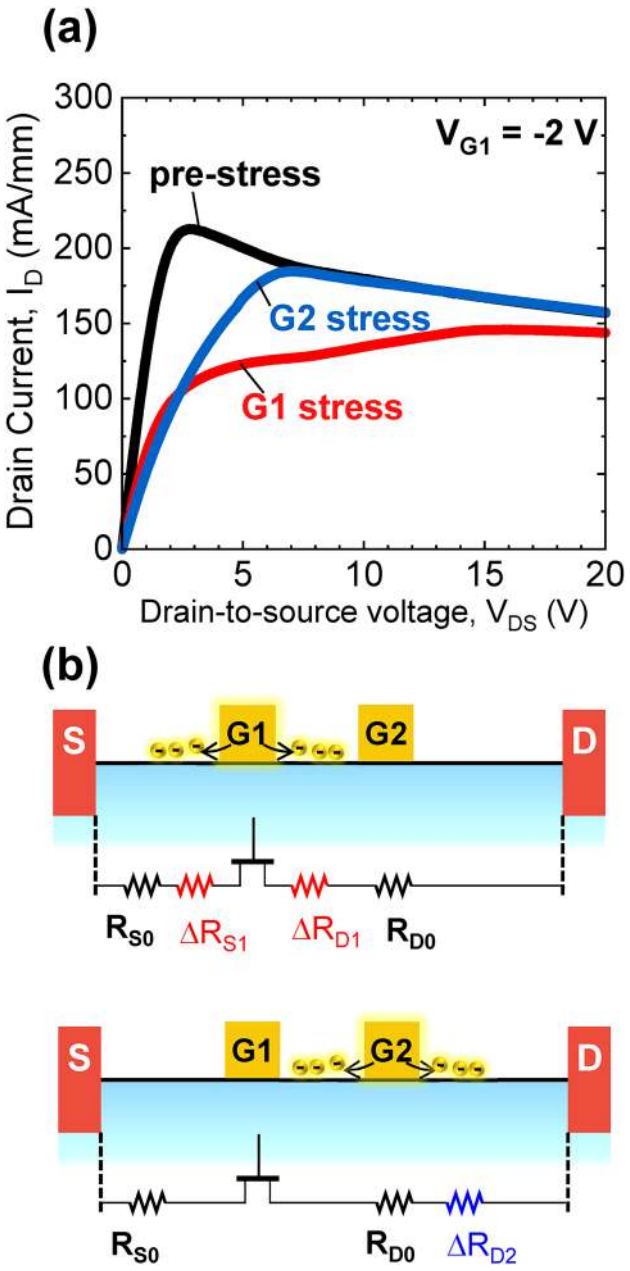


FIG. 24. (a) Pre- and post-stress I_D–V_{DS} curves measured with $V_{G1} = -2$ V. (b) Proposed model showing the increase on access resistances due to surface charging on both sides of the gate used in stressing. Reproduced with permission from Tajima and Hashizume, Jpn. J. Appl. Phys. **50**, 061001 (2011). Copyright 2011 Japan Society of Applied Physics.

stresses have a different impact on I_{Dsat}. While the off-state stress on G1 considerably decreased I_{Dsat}, the off-state stress on G2 had practically no effect on I_{Dsat}. These results can be understood within the framework of the proposed model illustrated in

Fig. 24(b). After stressing the device using G1, "virtual gates" on both sides of G1 increased both drain and source access resistances, collectively increasing R_{on}. In addition, however, the increase in R_S also reduced I_{Dsat} as explained earlier. Similarly, stressing the device using G2 can lead to virtual gate formation on both its drain and source sides. However, these virtual gates are effectively confined to the drain side of the main gate G1 and thereby causing an increase only in the drain access resistance. Accordingly, stressing the device using G2 increased only R_{on} without changing I_{Dsat}. From the above discussion, therefore, current collapse can be explained by electron trapping on both drain and source access regions.

D. Threshold voltage instabilities

A majority of early AlGaN/GaN HEMT devices are based on the Schottky gate (SG) architecture, where a metal with an appropriately high work function, usually nickel (Ni), is deposited on the AlGaN surface to form a rectifying contact. Aside from being relatively easy to fabricate, SG-HEMT devices offer high transconductance, i.e., efficient channel current controllability, because only the AlGaN barrier layer separates the metal gate from the 2DEG channel. However, SG-HEMT devices suffer from high gate leakage current especially when a positive voltage is applied on the gate. This shortcoming renders SG-HEMT unusable in enhancement mode technology, where drain current flows only by applying positive gate voltage. Furthermore, it has been reported recently that a forward gate stress can reduce the Ni/AlGaN Schottky barrier height, which then leads to an increased leakage current[13] as mentioned in the Introduction. To address this problem of gate leakage current, an insulator material can be inserted between the metal gate and the AlGaN barrier layer to form the so-called MIS structure. The insulator material deposited on the AlGaN surface before the gate metal also naturally acts as a passivant because it covers both drain and source access regions.

A good insulator material should have a high bandgap to effectively suppress gate leakage current and should have a high permittivity to facilitate good control of the gate over the 2DEG channel. Unfortunately, however, there is a common trade-off between bandgap and permittivity, namely, insulators with high bandgap have usually low permittivity and vice versa, as shown in Fig. 14. For instance, while SiO_2 has a wide bandgap of 9 eV, it suffers from a low relative permittivity of only 3.9. On the other hand, HfO_2 has relative permittivity as high as 20, but a bandgap of only ~5.7 eV. Having a high bandgap of 7 eV and sufficient relative permittivity of 9, Al_2O_3 has become one of the most accepted and most widely used insulator materials for GaN-based devices.[78–80]

While the MIS structure can reduce the gate leakage current by several orders of magnitude, insulator–semiconductor interfaces can harbor electronic states that can introduce additional concerns such as V_{TH} instabilities in AlGaN/GaN MIS-HEMTs. These interface states whose origin was discussed in the previous sections can trap and emit electrons, and being directly underneath the metal gate, can lead to V_{TH} transient.

To understand V_{TH} instability, it will be helpful to first derive the equation for V_{TH}. A band diagram of a typical Ni/Al_2O_3/AlGaN/GaN MIS-HEMT with applied gate voltage equal to V_{TH} is shown in Fig. 25(a). The associated interfacial charges are also shown in Fig. 25(b). In the diagram, V_{TH} is defined as the gate voltage at which there is no band bending in the GaN layer, i.e., the flat band condition. With $V_G = V_{TH}$, the conduction band edge E_C of the GaN channel at the AlGaN/GaN interface lies above E_F, indicating the absence of 2DEG under the metal gate. From Fig. 25, we can relate the potential terms as follows:

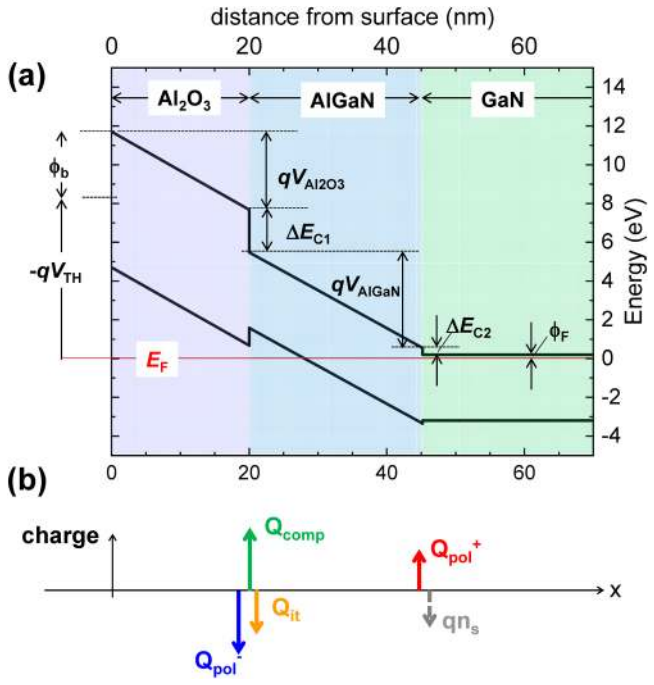


FIG. 25. (a) Band diagram of Al_2O_3(20 nm)/AlGaN(25 nm)/GaN MIS-HEMT with an applied gate voltage equal to threshold voltage V_{TH}, (b) schematic distribution of charges within the device.

$$-qV_{TH} + \phi_b - q\Delta V_{Al_2O_3} - \Delta E_{C1} - q\Delta V_{AlGaN} - \Delta E_{C2} - \phi_F = 0. \tag{5}$$

By invoking electric flux continuity law along with the AlGaN/GaN and Al_2O_3/AlGaN interfaces, respectively, we can obtain

$$\Delta V_{AlGaN} = \frac{d_{AlGaN}}{\varepsilon_{AlGaN}} Q_{pol^+} \tag{6}$$

and

$$\Delta V_{Al_2O_3} = \frac{d_{Al_2O_3}}{\varepsilon_{Al_2O_3}} (Q_{pol^-} + Q_{it} + Q_{comp} + Q_{pol^+}). \tag{7}$$

Substituting Eqs. (6) and (7) to Eq. (5), we can finally arrive at the V_{TH} equation given below:

$$V_{TH} = \left(\frac{\phi_b - \Delta E_{C1} - \Delta E_{C2} - \phi_F}{q}\right) - \frac{d_{Al_2O_3}}{\varepsilon_{Al_2O_3}}(Q_{pol^-} + Q_{comp} + Q_{it}) - \left(\frac{\varepsilon_{AlGaN} d_{Al_2O_3} + \varepsilon_{Al_2O_3} d_{AlGaN}}{\varepsilon_{Al_2O_3}\varepsilon_{AlGaN}}\right) Q_{pol^+}. \quad (8)$$

In the above-mentioned equation, ϕ_b is the Ni/Al_2O_3 barrier height, ΔE_{C1} is the Al_2O_3/AlGaN conduction band offset, ΔE_{C2} is the AlGaN/GaN conduction band offset, ϕ_F is E_C–E_F where E_F is the Fermi level, Q_{pol}^- is the negative polarization charge due to the sum of spontaneous and piezoelectric polarization of AlGaN, Q_{pol}^+ is the net positive polarization charge due to the sum of spontaneous and piezoelectric polarization of AlGaN minus GaN spontaneous polarization, Q_{comp} is the compensating charge that typically cancels out the effect of Q_{pol}^-,[81] and Q_{it} is the interface charge caused by interface states. The origin of Q_{comp}, referred to as surface donors by some groups,[81,82] is still under debate. Nevertheless, it seems necessary to explain to model the experimentally observed V_{TH} dependence on insulator thickness.[83,84] In the V_{TH} equation, Q_{it} represents the ionized interface states, whose magnitude can vary during one measurement run, and, therefore, is the main culprit of V_{TH} instability.

Figure 26 shows an illustration of a typical bi-directional C–V profile of Ni/Al_2O_3/AlGaN/GaN MIS-HEMT. Here, V_G is increased from −8 V [point (a)] to +3 V [point (b)] and then reduced back to −8 V [point (c)]. A difference in V_{TH} for the up-sweep and down-sweep is evident, illustrating the V_{TH} hysteresis loop (ΔV_{hys}). The origin of this ΔV_{hys} is explained graphically in Fig. 27. Initially, when $V_G = -8$ V is applied, the energy of the entire interface states is above E_F [Fig. 27(a)]. Acceptor-like interface states below E_C – 0.8 eV, having long emission time constants, remain filled with electrons and behave like negative frozen states[85] having a cumulative negative charge of $Q_{it\_up\text{-}sweep} = -q \times D_{itA}^- \times dE_a$. As V_G is swept positively, interface states go down approaching E_F, and, eventually, a portion of the upper half of acceptor-like states goes below E_F, when $V_G = +3$ V. At this point, interface states below E_C −0.5 eV [Fig. 27(b)] are filled with electrons coming from the AlGaN/GaN interface, giving a cumulative negative charge of $-q \times D_{itA} - \times dE_b$. When V_G is returned and swept back to −8 V [Fig. 27(c)], some of the electrons trapped in the interface states may not have sufficient time to be emitted, resulting in a cumulative negative charge of $Q_{it\_down\text{-}sweep} = -q \times D_{itA}^- \times dE_c$. Obviously, the down-sweep, $Q_{it\_down\text{-}sweep}$, is more negative than the up-sweep, $Q_{it\_up\text{-}sweep}$, resulting in a more positive V_{TH} for down-sweep, as described in Eq. (8). This leads to the well-known hysteresis problem in AlGaN/GaN MIS-HEMTs. The higher the density of interface states, the higher will be ΔV_{hys}, and more unstable will be the operation of MIS-HEMT. It is, therefore, of utmost importance to control the insulator/semiconductor interface to obtain the density of minimal interface states and consequently stable V_{TH}.

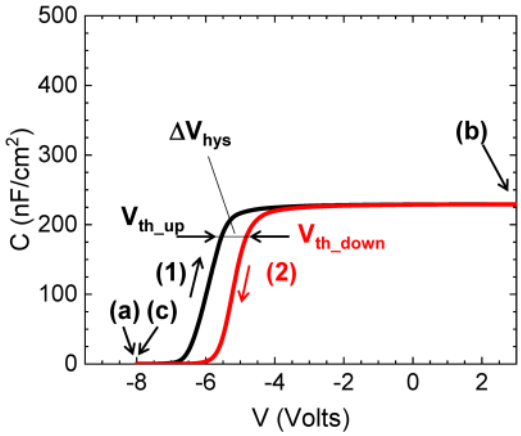


FIG. 26. Schematic illustration of a C–V profile hysteresis loop from an Al_2O_3(10 nm)/AlGaN(20 nm)/GaN MIS-HEMT formed by sweeping the voltage from (a) to (b) and back to (c).

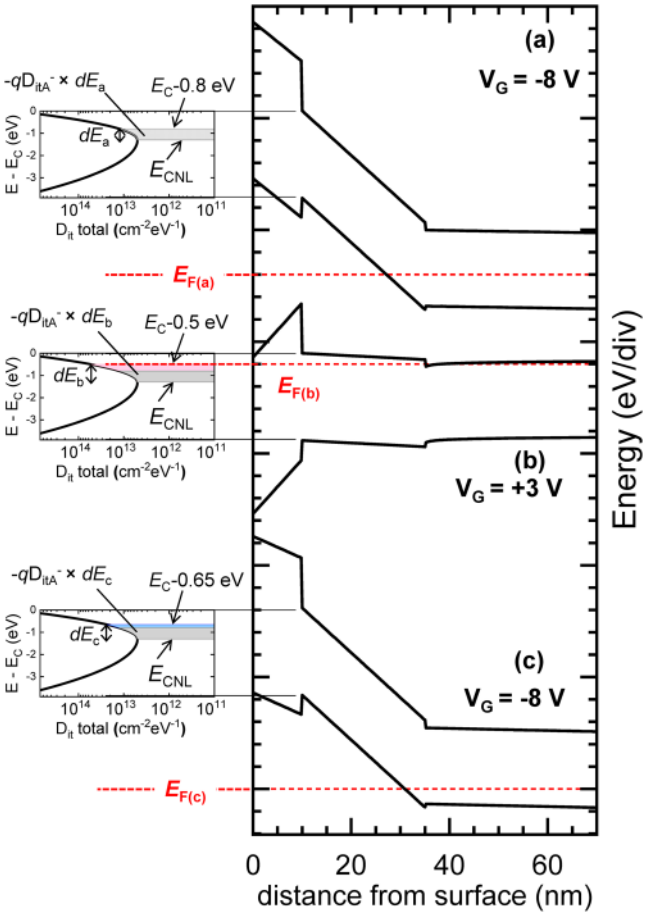


FIG. 27. Schematic energy band diagrams together with charge condition of interface states corresponding to points (a), (b), and (c) in a double sweep C–V profile illustrated in Fig. 26.

E. Effects of interface states on the current linearity of MIS-HEMTs

While GaN-based transistors can provide exceptional power and efficiency, they still suffer from reduced linearity at high input voltage swings. The growing stringent demand posed by new generation wireless communication systems necessitates highly linear amplifiers. Non-linearity in the device characteristics of GaN-based transistors can result in a severe distortion of the output signal, which may require complex circuit-level linearization solutions. Identifying and understanding the sources of this non-linearity in GaN-based HEMTs are, therefore, crucial for implementing a more cost-effective device-level approach.

Figure 28 illustrates a typical transfer characteristic of AlGaN/GaN MIS-HEMTs. At V_G, which is sufficiently more positive than V_{TH}, the rate of increase of I_D with increasing V_G tends to decrease, resulting in the sudden drop of g_m. For an ideal linear device, I_D should increase linearly with V_G, giving a flat dI_D/dV_G, i.e., a flat g_m. The sudden drop in g_m is usually attributed to decreasing saturation velocity with increasing 2DEG density.[86,87] Here, we show that the compromised linearity of AlGaN/GaN MIS-HEMTs at a high V_G regime can also be explained by the presence of D_{it} along with the insulator/AlGaN interface.

Figure 29 illustrates the band diagram of an Al_2O_3/AlGaN/GaN structure under (a) $V_G = 0$ and (b) $V_G = \Delta V_G$. For convenience, we have chosen $V_G = 0$ as the starting gate voltage V_G that is sufficiently more positive than V_{TH}. This is a valid assumption considering that conventional planar GaN-based MIS-HEMTs are normally-on devices with negative V_{TH}. From the band diagram shown on the left-hand portion of Fig. 29(a), with $V_G = 0$, E_C at the AlGaN/GaN interface is lower than E_F, indicating the presence of a 2DEG channel confined by a triangular quantum well formed by the AlGaN/GaN heterojunction. Also, with $V_G = 0$, acceptor-like states D_{itA}^- below E_F are populated with electrons with density corresponding to the shaded area $D_{itA}^- \times dE$ indicated on the D_{it} distribution shown on the right-hand figure. By applying $+\Delta V_G$ on the gate [Fig. 29(b)], the entire band diagram adjusts so as to increase the electric field within the device, namely, the slopes of E_C and E_V in Al_2O_3 change positively. Consequently, E_C at the AlGaN/GaN interface dips lower, increasing the 2DEG sheet density. Also, E_C along the Al_2O_3/AlGaN interface descends by $q\Delta V_s$, pulling down the entire D_{it} distribution and increasing the number of populated acceptor-like states, as shown in Fig. 29(b). In terms of electrostatics, $+\Delta V_G$ applied on the gate, induces positive charges on the gate metal, which is then balanced by an increase in both negatively charged 2DEG and negatively charged populated acceptor-like states, with the density represented by the hatched area $D_{itA}^- \times q\Delta V_S$ [the right-hand portion of Fig. 29(b)]. Here, it is to be noted that, to induce the same amount of populated negative acceptor-like states, a higher D_{itA}^- will require a smaller $q\Delta V_S$ to maintain the same shaded area. Accordingly, a smaller $q\Delta V_S$ also limits the downward movement of E_C at the Al_2O_3/AlGaN interface, inhibiting the increase in 2DEG, finally leading to the reduced rate of I_D increase and abrupt drop in g_m.

The more pronounced I_D saturation behavior in AlGaN MIS-HEMTs with an increased D_{it} is schematically illustrated in Fig. 30. Within the above-mentioned scheme, clearly, a high-quality insulator/AlGaN interface with a low D_{it} is desirable to obtain highly linear GaN-based MIS-HEMTs. On a final note, with a

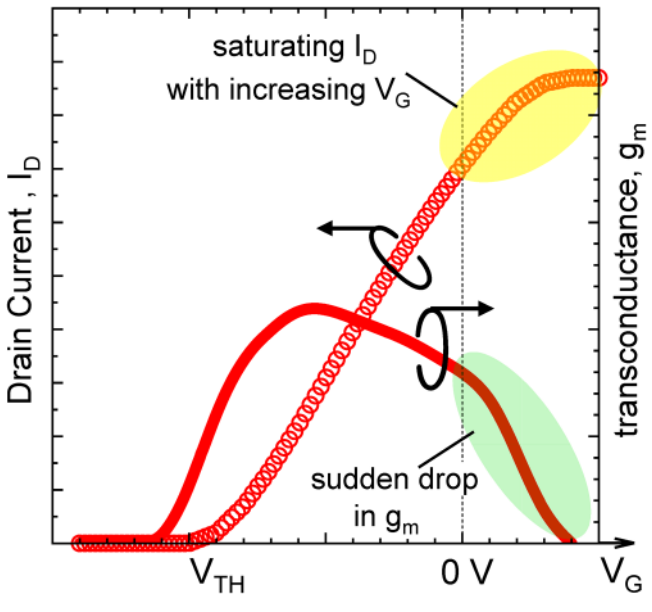


FIG. 28. Schematic illustration of drain current saturation behavior with an increasing gate voltage in AlGaN MIS-HEMTs.

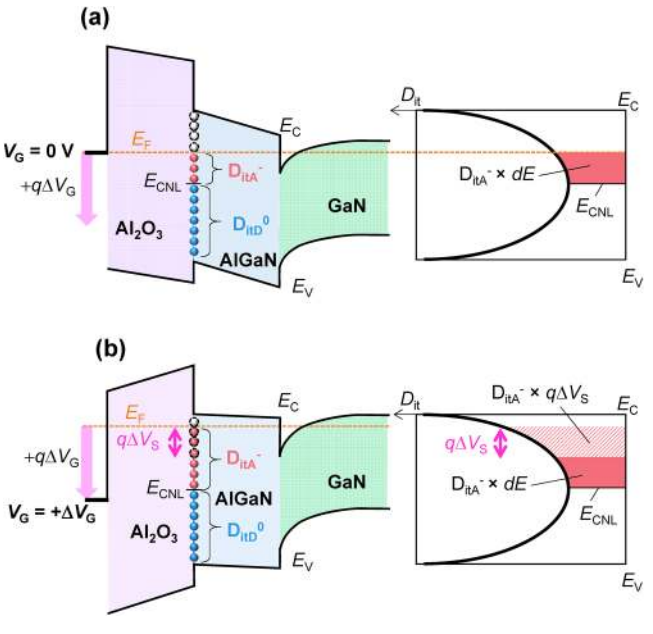


FIG. 29. Schematic illustration of band diagram and D_{it} distribution at (a) $V_G = 0$ and (b) $V_G = \Delta V_G$.

lower D_{it}, the same ΔV_G can also cause a deeper dip in $q\Delta V_S$, which can create a triangular quantum well below E_F adjacent to the insulator/AlGaN interface. This, in turn, impels some of the electrons forming the 2DEG to spill from AlGaN/GaN over to the Al_2O_3/AlGaN interface, i.e., the "spill-over" phenomenon. Thus, the "spill-over" phenomenon is an indicator of a high-quality insulator/AlGaN interface. This spill-over channel formed along the Al_2O_3/AlGaN interface parallel to the AlGaN/GaN 2DEG channel, which is capable of being modulated by V_G, can also partially alleviate the I_D saturation and abrupt g_m drop at a high V_G.

F. Effects of interface state charges on channel transport in MOSFETs and MIS-HEMTs

As described in Sec. II B, the charging condition of interface states greatly depends on the surface E_F position relative to E_{CNL}. In general, the occupied acceptor-like states carry negative charges at a forward bias, while the unoccupied donor-like states carry positive charges under depletion conditions. The resultant excess charges lead to channel mobility degradation due to Coulomb scattering in MOSFETs and MIS-HEMTs.

Yamaji *et al.*[88] investigated a correlation between interface state densities and channel mobilities in GaN MOSFETs with a lightly doped n-channel and a SiO_2 gate insulator. The interface state density was detected in the range of $(6–10)\times10^{11}\,cm^{-2}\,eV^{-1}$ at an energy level of 0.2 eV from the conduction band edge. They demonstrated that the reduction of state densities at the SiO_2/GaN interface resulted in increased channel mobility. Fiorenza *et al.*[89] reported the transport properties of the SiO_2/GaN channel using a recessed gate structure on AlGaN/GaN HEMTs. A high interface state density in the range of $(3–5)\times10^{12}\,cm^{-2}\,eV^{-1}$ limited the channel mobility to less than 110 cm^2/Vs. Based on a standard mobility model, they proposed that a one order magnitude reduction of the interface state density can lead to an effective mitigation of Coulomb scattering, resulting in an enhancement of the peak mobility to 220 cm^2/Vs. Meanwhile, Hosoi *et al.*[90] reported a high peak mobility over 250 cm^2/V s in the AlO_xN_y/GaN channel using a recessed gate AlGaN/GaN structure. They demonstrated that excellent interface properties with low trap densities can indeed attenuate the Coulomb scattering effect on the channel mobility.

In the above-mentioned devices employing a typical MOS channel, the accumulation electron channel is directly adjacent to the interface state charges. For the MIS HEMTs, on the other hand, the 2DEG channel is separated by the AlGaN barrier from the insulator/AlGaN interface, and, therefore, a weakened scattering effect from the interface state charges is expected. Hung *et al.*[91] investigated the interfacial charge effects on the 2DEG mobility in AlGaN/GaN MIS HEMTs. Figure 31 presents their calculation results showing the dependence of channel mobility on interface charge density computed for different 2DEG densities for an ultrathin AlGaN barrier. The figure suggests that, if the interface charge density can be kept under $1\times10^{12}\,cm^{-2}$, for a typical 2DEG density range $(5–10\times10^{12}\,cm^{-2})$ in AlGaN/GaN HEMTs, Coulomb scattering will be insignificant, as evidenced by the almost constant mobility plateau for interface charge density $<1\times10^{12}\,cm^{-2}$. This highlights the advantage of MIS gate application to HEMT structures.

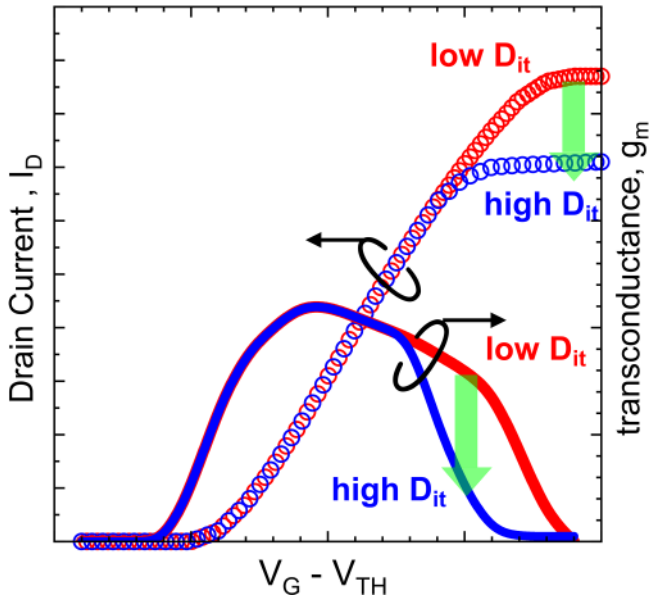


FIG. 30. Schematic illustration of a more pronounced drain current saturation behavior in AlGaN MIS-HEMTs with an increased D_{it}.

V. CHARACTERIZATION AND CONTROL OF GaN-BASED MIS-HEMT INTERFACES

A. Interpretation of MIS-HEMT *C–V* characteristics

Understanding the behavior of electronic states along the insulator/semiconductor interfaces is one of the prerequisites for undertaking measures to improve gate controllability and device performance of an MIS-HEMT. Figure 32 shows a schematic

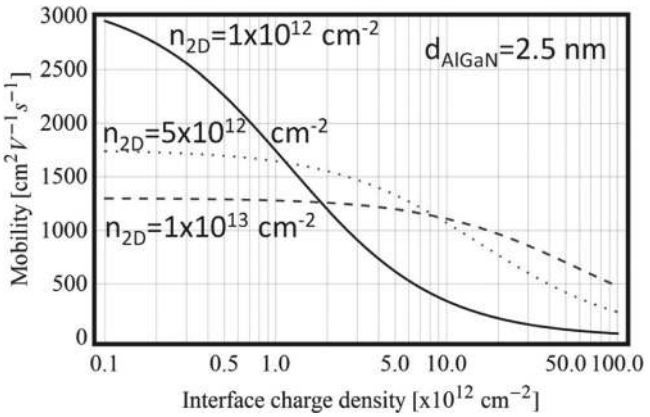


FIG. 31. Calculated mobility vs dielectric/AlGaN interface charges density for various 2DEG densities. Reproduced with permission from Hung *et al.*, Appl. Phys. Lett. **99**, 162104 (2011). Copyright 2011 AIP Publishing LLC.

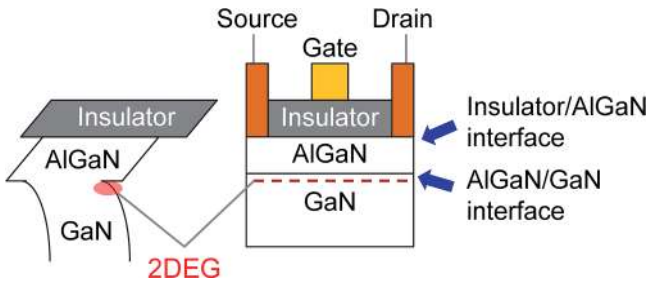


FIG. 32. Schematic illustrations of an insulator/AlGaN/GaN structure and the corresponding band diagram.

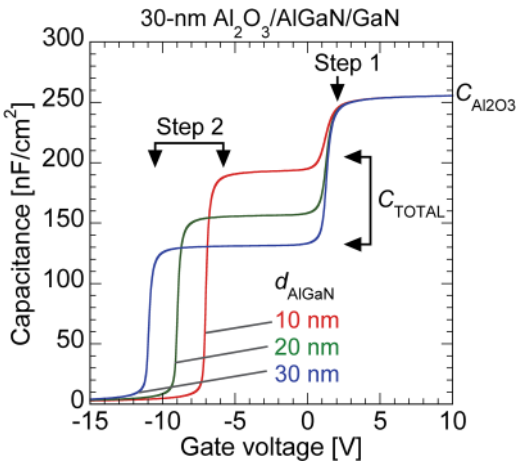


FIG. 33. Calculated *C–V* curves with different AlGaN thicknesses initially without considering interface state density (ideal curves).

illustration of the AlGaN/GaN HEMT MIS structure and its band diagram. In an MIS-HEMT structure, a gate insulator is formed on the AlGaN/GaN heterostructure, resulting in two interfaces under the gate electrode. Compared with an MIS structure having a single semiconductor layer (e.g., insulator/GaN), those two interfaces, insulator/AlGaN and AlGaN/GaN, make the potential control rather complicated during *C–V* measurements. In fact, an MIS-HEMT structure typically shows a two-step *C–V* behavior,[85] one, at the so-called spill-over regime discussed earlier, and two, around the depletion-accumulation transition. This is completely different from that of a simple MIS diode structure. Moreover, the emission efficiency of electrons from the near mid-gap interface states to the conduction band is very limited at RT, as already discussed in Sec. III. To estimate the interface state properties of an MIS-HEMT structure, these difficulties should be considered in the characterization.

To understand typical *C–V* behaviors, we show numerically calculated ideal *C–V* curves. The calculation was carried out using a numerical solver of the Poisson equation, taking into account the bound charges along the AlGaN/GaN interface originating from spontaneous and piezoelectric polarization as well as charge in the electronic states at the Al_2O_3/AlGaN interface.[92] Following the results of Ambacher *et al.*[93] and Miczek *et al.*,[92] a polarization-related bound charge Q^+_{pol} [Fig. 25(b)] at the AlGaN/GaN interface of 10^{13} cm^{-2} and an Al_2O_3 thickness of 30 nm were assumed in the calculation. The other parameters used in the calculation are described in Ref. 92. Figure 33 shows calculated *C–V* curves with different AlGaN thicknesses initially without considering interface state density (ideal curves). The two-step behavior is reproduced in the calculation, as observed in experimental *C–V* curves.[85,94] The constant capacitance in the spill-over regime corresponds to the Al_2O_3 capacitance, whereas that at the reverse bias is determined by the total capacitance (C_{TOTAL}) of the Al_2O_3 and AlGaN layers connected in series. At a reverse bias (Step 2), the capacitance steeply decreases to nearly zero, indicating the 2DEG depletion at the AlGaN/GaN interface. This voltage in an MIS diode structure approximately corresponds to V_{TH} in an actual three-terminal MIS transistor device. With decreasing the AlGaN barrier thickness, as shown in Fig. 33, the C_{TOTAL} increases and the V_{TH} at Step 2 shifts toward the positive voltage direction, as expected.

Note that the calculated curves without D_{it} show almost the same steep slope at both Steps 1 and 2. This is completely different from the observed experimental results, where the presence of electronic states along the Al_2O_3/AlGaN interface modifies the *C–V* characteristics, decreasing the slope of the Step 1 relative to Step 2. To see the effect of the electronic states, *C–V* curves were calculated assuming interface state density $D_{it}(E)$ at the Al_2O_3/AlGaN interface consisting of acceptor- and donor-like states [$D_{itA}(E)$ and $D_{itD}(E)$] separated by the E_{CNL},[85,94] as explained in Sec. II and shown in Fig. 34(a). For the calculation, D_{it} distributions using the following equations were used:[92]

$$D_{itA} = D_{it0}\exp\left[\left(\frac{E - E_{CNL}}{E_{0A}}\right)^{n_A}\right],$$
$$D_{itD} = D_{it0}\exp\left[\left(\frac{E_{CNL} - E}{E_{0D}}\right)^{n_D}\right], \quad (9)$$

where D_{it0} is the minimum state density, and E_0 and n define the curvature of the D_{it} distribution. We used the E_{CNL} values calculated by Mönch.[95] In addition, we took into account the time constants for electron emission from the interface state density using the aforementioned SRH statistics.

The calculated *C–V* curves are shown in Fig. 34(b). The *C–V* slope at a positive gate bias drastically decreases with an increasing interface state density, similar to reported experimental curves.[94,96,97] Figure 35 shows band diagrams of the Al_2O_3/AlGaN/GaN structure at different gate voltages. At a forward bias, the nearly flat potential of the AlGaN layer shown in Fig. 35(a) can lead to an electron transfer from the AlGaN/GaN interface to the Al_2O_3/AlGaN interface. Moreover, there is a high possibility of electron trapping at the Al_2O_3/AlGaN interface due to the increased probability of electron occupation of acceptor-like states, because a vast majority of them are below E_F. The acceptor-type states result in negative charges, while donor-type states are neutral

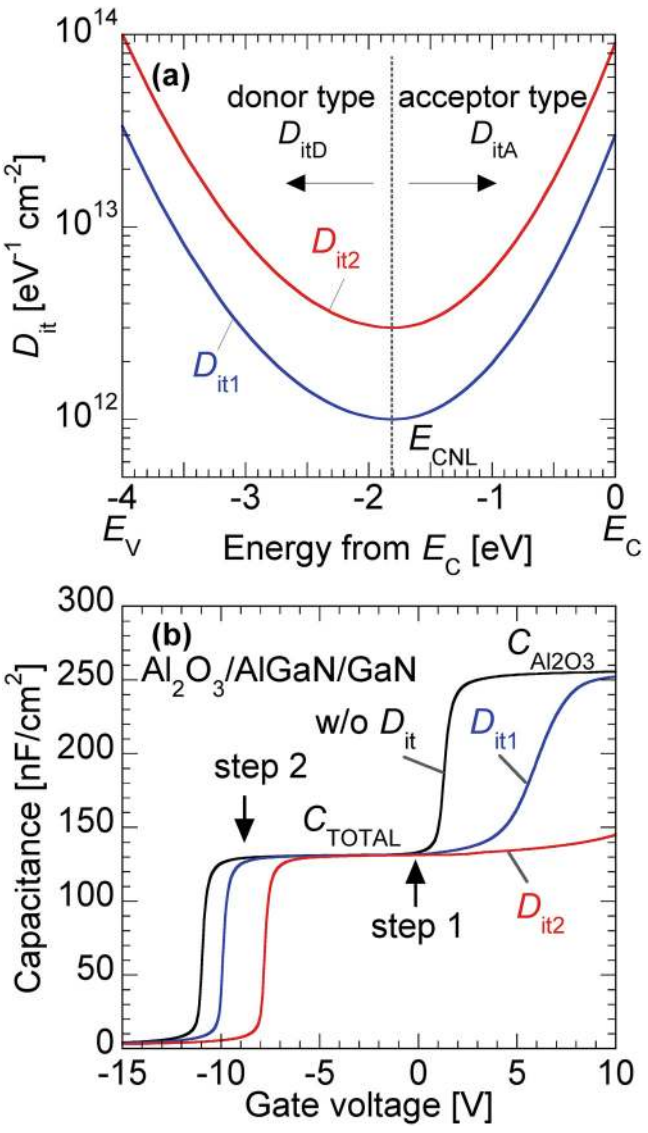


FIG. 34. Interface state density distributions at the Al_2O_3/AlGaN interface used for the calculation. (b) The calculated *C–V* curves without and with interface states.

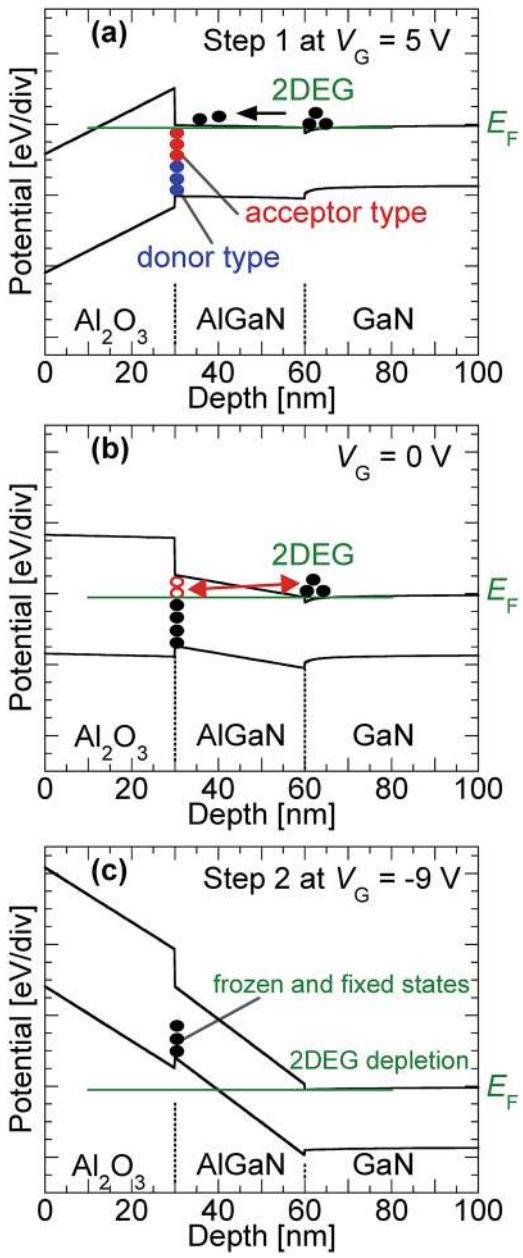


FIG. 35. Calculated band diagrams of the Al_2O_3/AlGaN/GaN structure at (a) V_G = 5 V, (b) 0 V, and (c) −9 V.

when they are populated by electrons. Such negatively charged interface states can screen an applied gate electric field, suppressing the potential modulation of the AlGaN layer. Furthermore, the electron occupation rate of the interface states is a function of V_G, because the E_F moves within the bandgap of AlGaN according to the V_G swing, as shown in Fig. 35(b). The equivalent trapping effect is manifested as a stretch out of the *C–V* curve at the forward bias region, as shown in Fig. 34(b). For an extreme case of an MIS-HEMT structure having very high interface state densities at the insulator/AlGaN interface, Step 1 is not observed even at a high forward bias.[98,99] Several reports showed *C–V* curves without the characteristic first step at the forward bias regime. In this case, it is likely that high-density states at the insulator/AlGaN interface impede the control of the gate over the AlGaN surface potential. An incorrect analysis of such a peculiar *C–V* behavior often gives rise to a misleadingly low interface state density at the insulator/AlGaN interfaces.[100–102]

Figure 35(c) shows the band diagram at $V_G = -9$ V. The Fermi level E_F is located far below E_V of AlGaN at the Al_2O_3/AlGaN interface, which makes electron occupation of interface states no longer responsive to the gate bias, leading to the absence of stretch-out behavior in the C–V curve at Step 2, as shown in Fig. 33. Furthermore, it is estimated from SRH statistics that the time constants of electron emission at RT from near mid-gap states can exceed 10^{20} s. Thus, electrons captured at deep states remain unaffected even when a large negative bias is applied to the gate electrode. Under these circumstances, interface states act as "fixed and frozen" charges, and, thus, the parallel C–V shift (V_{TH} shift) at Step 2 toward the positive bias direction with respect to the ideal C–V curve,[94] as shown in Fig. 33.

B. Characterization of interface state density using an MIS-HEMT structure

Characterization of state densities at the insulator/AlGaN (or InAlN) interface in MIS-HEMT systems is rather challenging. Since an MIS-HEMT structure includes a localized 2DEG and two interfaces, the Terman method[103] based on the analysis of a depletion layer capacitance is not applicable to the MIS-HEMT structure. Thus, several methods to determine state density distribution near E_C at the insulator/AlGaN (or InAlN) interface in MIS-HEMT systems are proposed. The curve fitting between the experimental C–V curve is one way of determining state density distribution near E_C at the insulator/AlGaN (or InAlN) interface in MIS-HEMT systems.[94,104]

Figure 36 shows a flow chart for estimation of state density distribution near E_C at the insulator/AlGaN (or InAlN) interface in MIS-HEMT systems by curve fitting between experimental and calculated C–V curves. First, an experimental C–V curve is measured. Then, using an intelligent guess for arbitrary $D_{it}(E)$ distribution given by Eq. (9), we carry out the calculation of potential distribution at a given V_G by numerically solving the Poisson equation, as mentioned above. In this relation, we have to take into account interface state charges and polarization charges. Interface state charges can be calculated from the assumed $D_{it}(E)$ distribution, the Fermi Dirac occupation function, and the effective energy range of states according to the SRH statistics, as described in the Sec. III A. Based on the calculated potential distribution at a given V_G, we can easily obtain a differential capacitance ($C = \Delta Q/\Delta V_G$), followed by the calculation of a C–V curve corresponding to the experimental one. If the calculated C–V curve well fits the experimental result, then we can judge that the assumed $D_{it}(E)$ is correct. If not, after the appropriate readjustment of the $D_{it}(E)$, the calculation process will be repeatedly carried out until a good fit between the measured and the calculated C–V curves is attained.

Figure 37(a) shows the example of best-fitting curves between the calculated and the experimental C–V curves of the Al_2O_3/AlGaN/GaN structures with and without the inductively coupled-plasma (ICP) assisted dry etching of the AlGaN surface.[94] The estimated state density distributions near E_C at the Al_2O_3/AlGaN interface from the fitting are given in Fig. 37(b). Note that only the state density distribution near E_C at the insulator/AlGaN interface can be determined from the fitting results. Due to the associated long emission time of interface, only the acceptor-like traps in the energy range indicated by solid lines in Fig. 37(b) can change their charge state accordingly with the gate voltage sweep at RT. Nevertheless, the extracted distribution near E_C can provide a ballpark estimate of the remaining intrinsic deeper states assuming U-shape continuity.

Conductance method is one of the most reliable measurement techniques extracting interface states in MOS structures. However, one should be carefully aware of the E_F position at the AlGaN (or InAlN) interface when using this method. Some papers reported conductance analysis in the reverse bias range on MIS-HEMT structures.[105–107] However, due to the associated long emission time constants of interface states, the interface states are irrelevant and, therefore, could not be responsible for the conductance peak in the conductance–frequency (G–f) curve at the reverse bias range. Thus, the conventional conductance method is only efficient in a forward bias regime. Alternatively, there is a unique characterization method using forward-bias G–f characteristics at high temperatures.[108] From the analysis based on the G–f–T (T: temperature) mapping, an energy range of interface states responding to the G–f measurement and gate-control efficiency related to an interface state density can be estimated. The frequency dependence of C–V curves is also one of the characteristic features of an insulator/AlGaN interface. The MIS interface electronic state densities near the conduction-band edge for MIS-HEMT structures can be obtained by investigating the frequency dispersion characteristics of the C–V curves in the positive bias range.[109–113]

C. Photo-assisted C–V characterization

Since near mid-gap electronic states having long emission time constants contribute to slow V_{TH} fluctuation, it is meaningful to determine their distribution along the insulator/AlGaN (or InAlN) interface in MIS-HEMT systems. However, it is extremely difficult to detect interface states by a conventional C–V measurement at RT, as previously discussed. Thus, a photo-assisted C–V method using monochromatic lights with photon energies less than the bandgap is proposed to detect near mid-gap electronic states at insulator/AlGaN interfaces at RT.[85]

Figure 38(a) shows the schematic illustrations of photoionization effects of interface states under a monochromatic light with energy less than the bandgap of GaN. First, under dark conditions, a forward gate voltage high enough to observe the insulator capacitance is applied. In this case, almost all interface traps are filled with electrons under a nearly flat band condition. The gate bias is then swept toward a value more negative than the threshold voltage, as shown in Fig. 38(b). After reaching a sufficiently negative gate bias, a sub-E_g monochromatic light with a photon energy of $h\nu_1$ is illuminated to the sample surface. Consequently, we are effectively inducing photo-assisted electron emission from the interface states within the energy range corresponding to the photon energy range, as schematically shown in Fig. 38(a). After switching the light off, the gate voltage is then swept toward 0 V under dark conditions. As shown in Fig. 38(b), we can observe the C–V curve shift toward the reverse bias direction, corresponding to the change in the interface state charge Q_{it} ($h\nu_1$). Using different sub-E_g photon energies, we can induce a systematic C–V shift, as shown in Fig. 38(b). The voltage shift difference (ΔV) between two

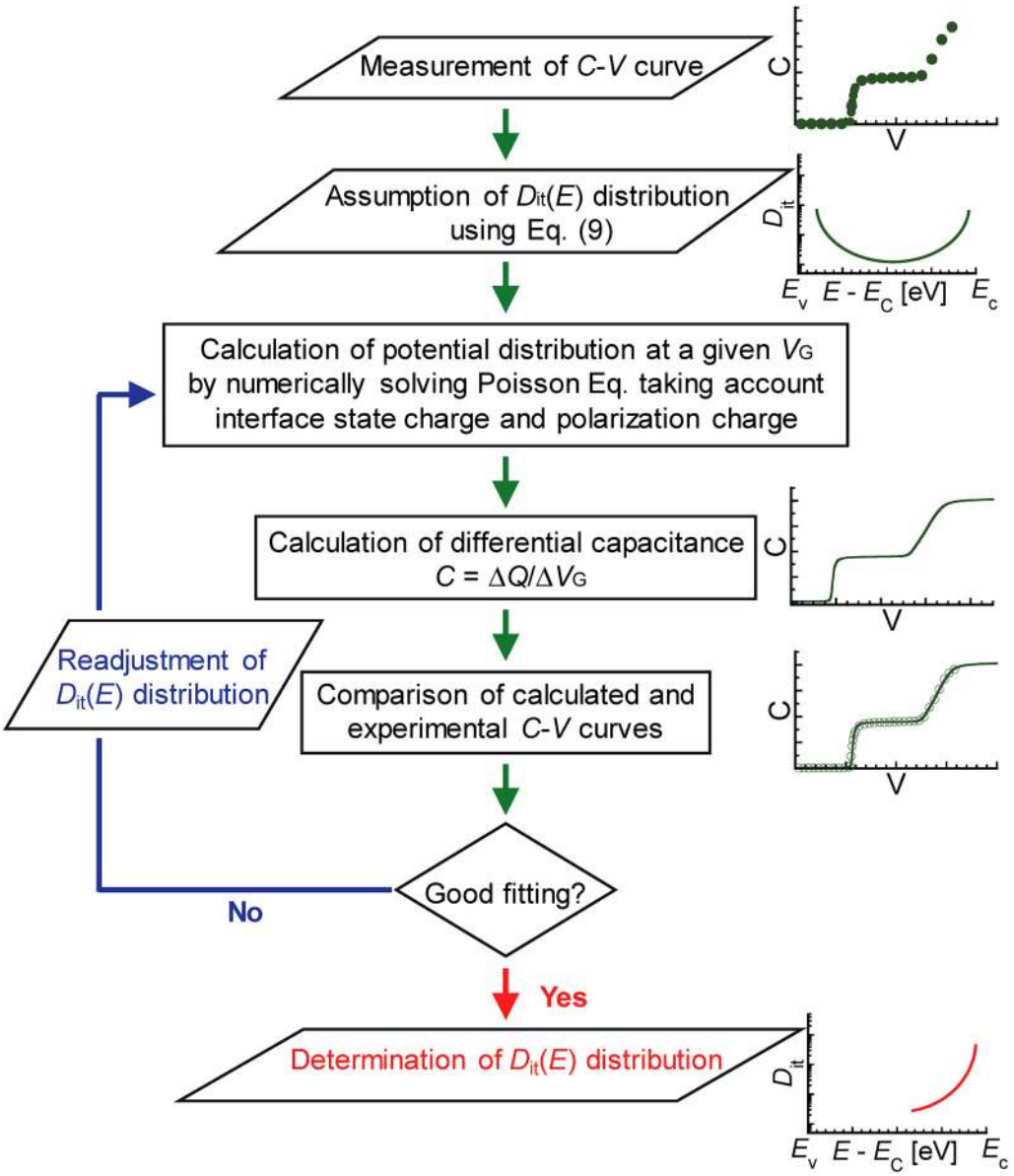


FIG. 36. A flow chart for estimation of state density distribution near E_C at the insulator/AlGaN (or InAlN) interface in the MIS-HEMT systems by curve fitting between experimental and calculated *C–V* curves.

photon energies corresponds to the interface charge difference, ΔQ_{it}, in the energy range $\Delta h\nu$ shown in Fig. 38(c). The state density can be simply estimated using the observed ΔV in the following equation:

$$D_{it}(E = E_{AV}) = \frac{C_{TOTAL}\Delta V}{q\Delta h\nu}, \tag{10}$$

where C_{TOTAL} is the total capacitance of Al_2O_3 and AlGaN and E_{AV} is the average interface energy schematically shown in Fig. 38(c).

Figure 39(a) shows an example of the measured photo-assisted *C–V* curves for the Al_2O_3/AlGaN/GaN structure.[94] *C–V* profiles shift systematically toward the reverse bias direction with an increasing photon energy, as mentioned above. The completely parallel *C–V* shift toward the negative direction indicates that the interface states near midgap or at deeper energies act as fixed charges in this bias range. Using a combination of the numerical fitting of *C–V* characteristics previously described and the present photo-assisted *C–V* technique, the state density distribution of the

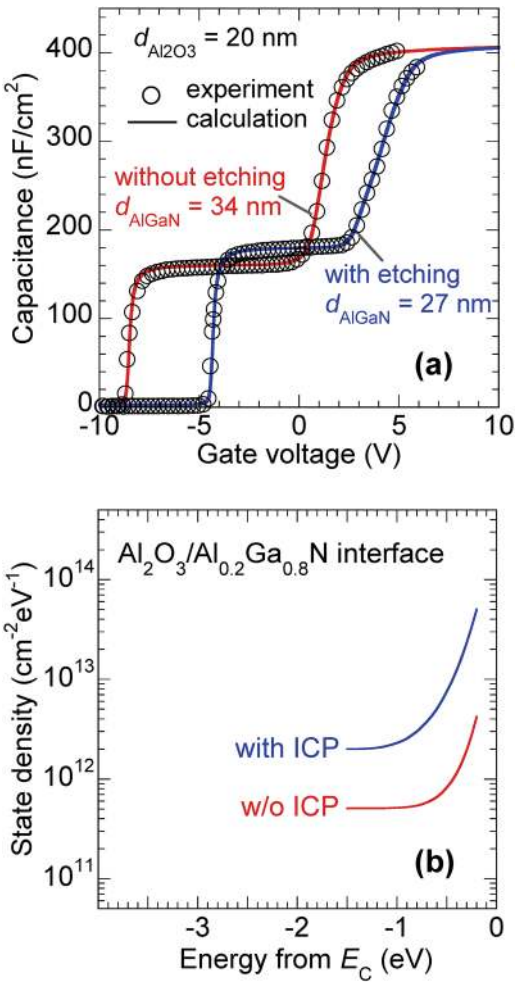


FIG. 37. An example of best fitting curves between the calculated and the experimental *C–V* curves of the Al_2O_3/AlGaN/GaN structures with and without the ICP dry etching of the AlGaN surface. Reproduced with permission from Yatabe *et al.*, Jpn. J. Appl. Phys. **53**, 100213 (2014). Copyright 2014 Japan Society of Applied Physics.

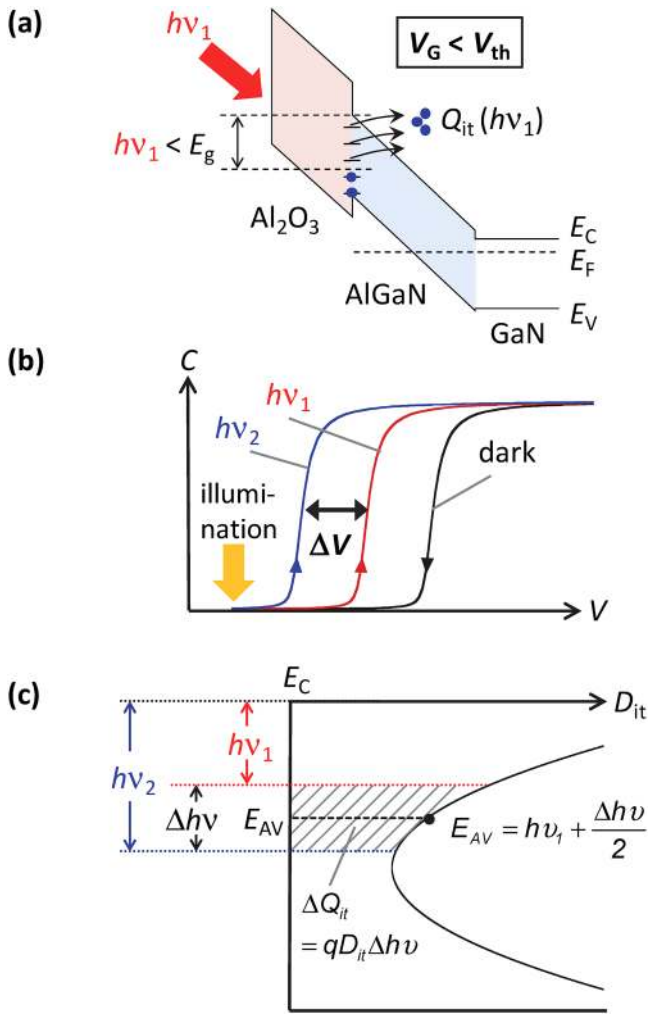


FIG. 38. Schematic illustration of (a) photo-assisted electron emission at the insulator/AlGaN interface, (b) photo-assisted *C–V* curves, and (c) interface state charge and energy range corresponding to the voltage shift, ΔV, in photo-assisted *C–V* characteristics. Reproduced with permission from Yatabe *et al.*, Jpn. J. Appl. Phys. **53**, 100213 (2014). Copyright 2014 Japan Society of Applied Physics.

Al_2O_3/AlGaN interfaces can be estimated within a wide energy range,[94] as shown in Fig. 39(b).

A key issue for GaN-based MIS-HEMT is the control of MIS interfaces. Here, we introduce an example of excellent operation stability of $HfSiO_x$/AlGaN/GaN HEMT on a free-standing GaN substrate.[41] The $(HfO_2)/(SiO_2)$ laminate structure was deposited on the AlGaN surface by plasma-enhanced atomic layer deposition, followed by a post-deposition annealing at 800 °C. The $HfSiO_x$-gate HEMT showed good transfer characteristics with a high transconductance expected from its κ value and a subthreshold swing of 71 mV/decade. The detailed *C–V* analysis on the corresponding MOS HEMT diode showed low state densities in the order of $10^{11}\,cm^{-2}\,eV^{-1}$ at the $HfSiO_x$/AlGaN interface. The temperature dependence of transfer characteristics is shown in Fig. 40. The fabricated MOS HEMT showed a stable operation with a V_{TH} drift of only 150 mV from its RT value even at 150 °C, indicating excellent gate controllability. It is likely that the PDA process at 800 °C is effective in recovering surface defects such as vacancies and in terminating dangling bonds with O atoms at the AlGaN surface.[42,43]

VI. COMPARISON OF MOS INTERFACES BETWEEN GaN AND CONVENTIONAL III–V SEMICONDUCTORS

The development of high-performance MISFETs has been an important subject for conventional III-V semiconductors such as

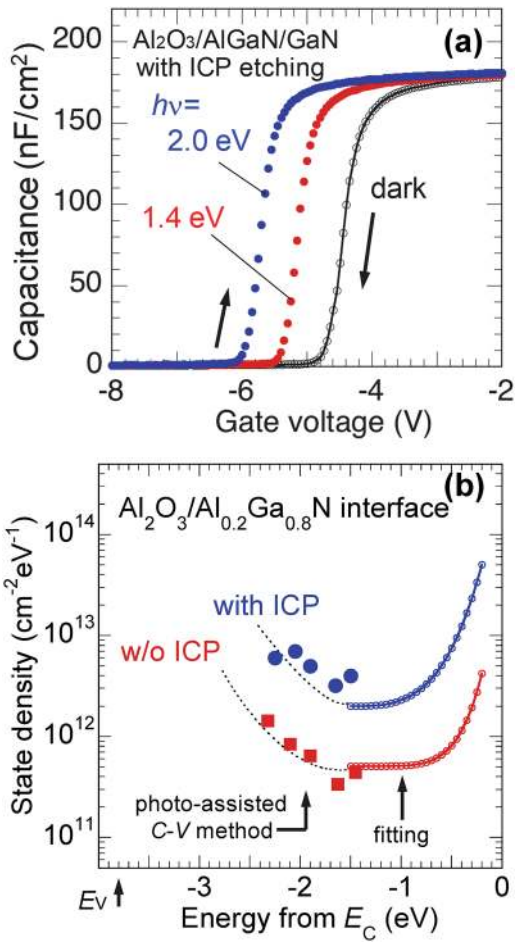


FIG. 39. (a) An example of the photo-assisted *C–V* characteristics of an Al_2O_3/AlGaN/GaN structure and (b) $D_{it}(E)$ distributions at the Al_2O_3/AlGaN interface obtained by a combination of the photo-assisted *C–V* method and the *C–V* fitting analysis. Reproduced with permission from Yatabe *et al.*, Jpn. J. Appl. Phys. **53**, 100213 (2014). Copyright 2014 Japan Society of Applied Physics.

GaAs, InP, and InGaAs. However, instability issues related to interface states still remain in the corresponding MIS systems.[114] In this regard, a characteristic feature is the marked frequency dispersion at an accumulation bias in the experimental *C–V* characteristics of MOS structures using GaAs,[115,116] InP[117,118] and InGaAs.[118–120] In particular, it is surprising that the maximum capacitance sometimes exceeds the insulator capacitance at low frequencies,[118] as shown in Fig. 41.

To explain this anomalous *C–V* behavior at an accumulation bias, we have to consider traps (electronic states) in the vicinity of the insulator/semiconductor interfaces, interacting with electrons in the conduction band via tunneling. Yuan *et al.*[121] proposed the border trap (BT) model assuming a trap inside the gate insulator (an oxide trap), as shown in Fig. 42. Here, the trap energy level nearly aligns with the conduction band minimum (CBM) of a

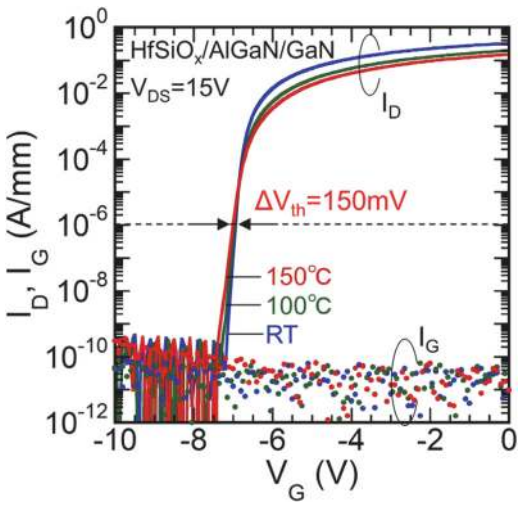


FIG. 40. Temperature-dependent transfer characteristics of $HfSiO_x$/AlGaN/GaN HEMT on a free-standing GaN substrate. Reproduced with permission from Ochi *et al.* AIP Adv. **10**, 065215 (2020). Copyright 2020 AIP Publishing LLC.

semiconductor. In this case, we can observe long time constants for electron capture/emission processes via tunneling between a border trap and the conduction band, resulting in large frequency dispersion even at an accumulation bias,[118,120] as shown in Fig. 41. However, the stringent assumption required by the BT model is that the trap energy level should nearly align with the CBM of a semiconductor. This is too critical for a wide variety of III–V MOS systems, i.e., a lot of combinations exist between oxides and semiconductors.

The disorder-induced gap state (DIGS) model,[28,122] as schematically shown in Fig. 43(a), can also explain well this frequency

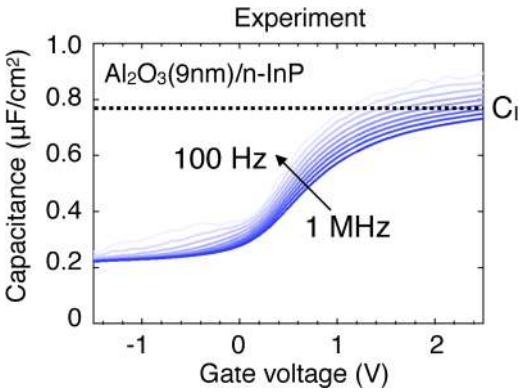


FIG. 41. Frequency dispersion at an accumulation bias in the experimental *C–V* characteristics of an Al_2O_3/n-InP MOS structure. Reproduced with permission from Brammertz *et al.*, IEEE Trans. Electron Dev. **58**, 3890 (2011). Copyright 2011 IEEE Publishing.

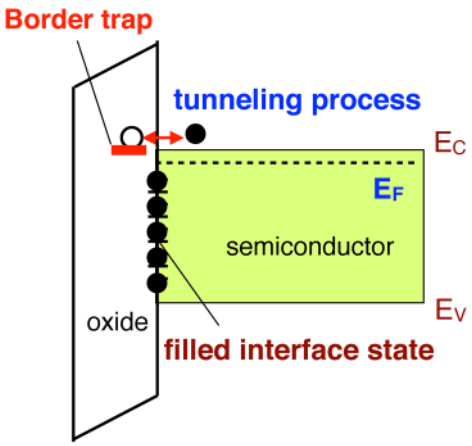


FIG. 42. The border trap (BT) model assuming a trap inside the gate insulator (an oxide trap).

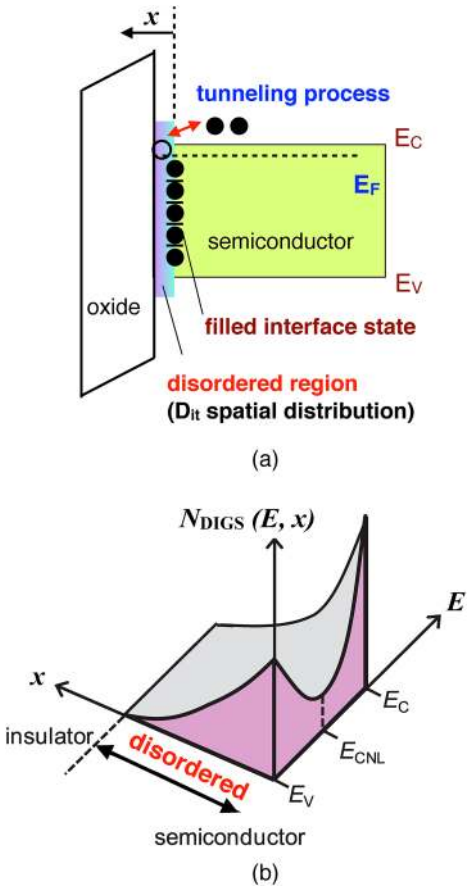


FIG. 43. (a) The disorder-induced gap state (DIGS) model and (b) the corresponding electronic states with density distributions in both space and energy.

dispersion at an accumulation bias. The DIGS model assumes a disordered region within several monolayers at a semiconductor surface, consisting of defects, dangling bonds, and lattice displacement. Such surface disorder produces electronic states with density distributions in both space and energy, as shown in Fig. 43(b). When interface states have space distribution, the tunneling effect can be involved in electron capture/emission processes. This particularly causes an additional capacitance component at low frequencies, resulting in a large accumulation capacitance exceeding the insulator capacitance, as shown in Fig. 41. Galatage *et al.*[120] reported that frequency dispersions of accumulation capacitances observed in InP and InGaAs MOS diodes were successfully replicated with the calculations based on the DIGS model by assuming the disorder depth within 0.8 nm from the crystalline semiconductor surface. They also demonstrated from photoemission spectroscopy analysis that the oxidation-induced bond disorders with several monolayers at III-V semiconductor surfaces are responsible for interface states with a spatial density distribution. In addition to oxidation, a high process energy can introduce bond disorders with a depth distribution on conventional III–V semiconductor surfaces, as schematically shown in Fig. 44(a), causing anomalous frequency dispersion of accumulation capacitance observed in mainstream III–V MOS *C*–*V* characteristics.

In the case of the GaN MOS system, on the other hand, frequency dispersion of capacitance in *C*–*V* characteristics has not

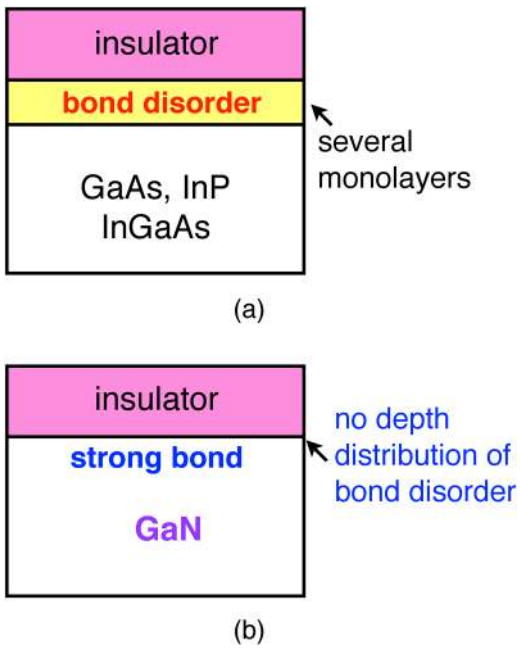


FIG. 44. Schematics of MIS interfaces: (a) conventional III–V semiconductor interfaces have a bond disordered region, causing an anomalous frequency dispersion of accumulation capacitance observed in MOS *C*–*V* characteristics. (b) A strong Ga–N bonding can restrain the spread of bond disorder to the bulk region, leading to no depth (spatial) distribution of interface states.

been observed in the forward bias region, as shown in Fig. 11. In the "reverse bias" regime, the as-deposited sample (without PMA) showed a significant frequency dispersion and a ledge-like feature, arising from high densities of interface states.[118] However, frequency dispersion of capacitance was not observed at a "forward bias," as shown in Fig. 11. These features were also reported for SiO_2/GaN and Al_2O_3/GaN structures.[34,123–126] The topmost GaN surface probably includes a bond-disorder configuration due to dangling bonds, adatoms, and surface defects, responsible for high-density electronic states at the insulator/GaN interfaces, as described in Sec. II A. However, a strong Ga-N bonding nature can restrain the spread of bond disorder to the bulk region, leading to a depthless (no spatial) distribution of interface states, as schematically shown in Fig. 44(b). By controlling the topmost surface with successful bond termination,[42] we can achieve excellent MOS interface properties, like the Si MOS system, practically applicable to various types of GaN MOS transistors. This is definitely different from MOS interfaces using conventional III–V semiconductors.

VII. SUMMARY

In summary, we introduced and discussed the models of interface (surface) states, the effects of these states on device performances, a guiding principle for controlling interface states, capacitance–voltage (C–V) characterization of MIS-HEMT structures, surface passivation, and a comparison of MOS interfaces between GaN and conventional III–V semiconductors. In Sec. II, we described the origin and models of intrinsic and extrinsic surface/interface states, their charging conditions, and the related Fermi level pinning of the surface, typically observed in wide bandgap semiconductors. In Sec. III, we reexamined GaN MOS conventional characterization methods and pointed out their limitations and possible pitfalls that one should be aware of when carrying out these measurements. We also underlined some guiding principles to consider for the effective and enhanced control of surface and interface electronic states. The impact of surface states in device access regions on the current–voltage (I–V) characteristics of SG-HEMTs was discussed in the first half of Sec. IV, while the adverse effects of insulator/semiconductor interface states in MIS-HEMTs on V_{TH} instability were presented in the latter half of the section. Characterization and interpretation of the rather complex AlGaN/GaN MIS-HEMT C–V profiles were presented in Sec. V. We then described the photo-assisted C–V measurement method that we have developed, using sub-E_G illumination, for probing near mid-gap electronic states, which are otherwise difficult if not impossible to detect under normal conditions. In Sec. VI, we also compared the MOS interfaces in the GaN system with those of more mature III–V compound semiconductor families. Furthermore, we also shed light on some confusions and misconceptions related to III-nitride/insulator interfaces in published literature. Finally, we highlighted some aspects that need further investigations for better understanding and control of surface and interface states haunting GaN-based devices as well as attempted to guide present and future researchers of the same field for setting the next stage of development.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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