Coordination of MMCs With Hybrid DC Circuit Breakers for HVDC Grid Protection

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***Abstract*—A high-voltage direct-current (HVDC) grid protection strategy to suppress dc fault currents and prevent overcurrent in the arms of modular multilevel converters (MMCs) is proposed in this paper. The strategy is based on the coordination of half-bridge MMCs and hybrid dc circuit breakers (DCCBs). This is achieved by allowing MMC submodules to be temporarily bypassed prior to the opening of the DCCBs. Once the fault is isolated by the DCCBs, the MMCs will restore to normal operation. The performance of the proposed method is assessed and compared to when MMCs are blocked and when no corrective action is taken. To achieve this, an algorithm for fault detection and discrimination is used and its impact on MMC bypassing is discussed. To assess its effectiveness, the proposed algorithm is demonstrated in PSCAD/EMTDC using a four-terminal HVDC system. Simulation results show that the coordination of MMCs and DCCBs can significantly reduce dc fault current and the absorbed current energy by more than 70% and 90%, respectively, while keeping MMC arm currents small.**

***Index Terms*—Modular multi-level converters, dc circuit breakers, high-voltage direct-current grids, protection.**

I. Introduction

VOLTAGE source converter (VSC) based high-voltage direct-current (HVDC) grids are expected to facilitate the large-scale integration of renewable energy generation into electricity grids and to enable cross-border energy trading [1]. Presently, only two multi-terminal VSC-HVDC systems are in operation: the Nan'ao three-terminal HVDC system and the Zhou Shan five-terminal network [2]. Another four-terminal dc grid pilot project interconnecting Beijing and Zhangjiakou will be commissioned in 2018 [3]. In Europe, several HVDC grid topologies have been proposed to represent the building blocks of a future pan-European grid [4], [5]. Other notable VSC-based multi-terminal system projects include the Tres Amigas Superstation and the Atlantic Wind Connection, which are still under construction [6].

Manuscript received October 12, 2017; revised January 6, 2018 and March 16, 2018; accepted April 15, 2018. Date of publication April 27, 2018; date of current version January 22, 2019. This work was supported by the EU's FP7 Programme through the project "Beyond State of the art Technologies for re-Powering AC corridors & multi-Terminal HVDC Systems" (BEST PATHS) under Grant 612748. Paper no. TPWRD-01249-2017. *(Corresponding author: Sheng Wang.)*

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Digital Object Identifier 10.1109/TPWRD.2018.2828705

The deployment of HVDC grids and their reliable operation will depend on the adequate performance of their protection schemes during dc faults. This is challenging as a dc network has a lower inductance than an ac system of equivalent rating and, thus, exhibits a higher rate of change in fault currents and a faster fault propagation [7]. A dc grid protection system should have the ability to interrupt fault currents when their magnitude is low not only to prevent damaging power system equipment, but also to bring down the rating and, hence, the cost of protection devices such as dc circuit breakers (DCCBs). There are three alternatives to reduce the magnitude of the fault current: 1) to limit the rate of fault current rise; 2) to increase the speed of fault isolation; and 3) to limit the energy sources which feed the fault current before fault isolation.

Existing methods to limit the rate of fault current rise require the deployment of additional components. A simple approach is to connect large reactors in series with DCCBs [8], [9] or at the ac side of the converter to form an LCL circuit [10]. However, series reactors will significantly increase the foot-print and cost of the protection device or of converter stations. Moreover, they could reduce the voltage stability of the dc system [11]. Alternatively, an extra energy dissipation circuit [12] or a resistive superconducting fault current limiter [13] could be added to reduce the fault current. Nevertheless, the inclusion of such devices will increase investment costs.

The second option is to increase the speed of fault isolation, which is restricted by fault detection, fault discrimination and the operation of DCCBs. Algorithms have been proposed for a fast fault detection and discrimination based on local measurements of voltage and current (and their derivatives) without using communications [14]–[16]. Other fast relaying algorithms are based on traveling wave analysis [17] and signal processing [18]. Unconventional methods such as 'Open Grid' change the protection sequence order to reduce the delay before fault isolation [19]. Despite their advantages, the previous schemes do not minimize the requirements on fault current interruption and, moreover, the delay caused by the opening of DCCBs is inevitable. For instance, the hybrid DCCB, which is a widely accepted alternative for HVDC applications, incurs a delay of 2–3 ms to isolate a dc fault [20]. The fault current will rise with a high rate during this time.

The third option is to limit the energy sources contributing to the dc fault current. If MMCs take no action prior to fault isolation, the sources shown in Fig. 1 that will contribute to the fault current include (*i*) submodule (SM) capacitors within

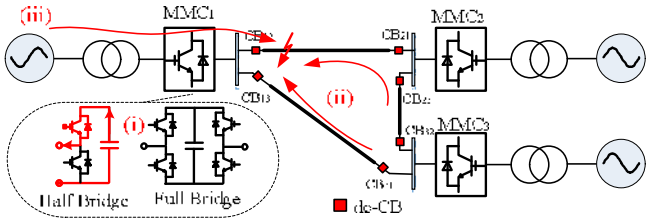

Fig. 1. Sources feeding a dc fault.

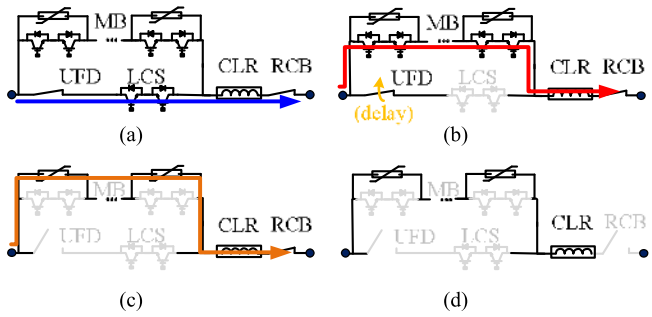

Fig. 2. Operation of a hybrid DCCB.

the MMCs; (*ii*) capacitive components of dc lines; and (*iii*) the connected ac system. The amount of fault current contributed by each source has been analyzed in [21], [22]. Notice that if MMCs take an action, such as blocking, the SM capacitors will become floating and stop contributing to the fault current.

MMCs with full-bridge (FB) SMs may be blocked to prevent the discharge of SM capacitors and to interrupt the fault current contributed by a connected ac system [22], [23]. However, such topologies have a larger number of semi-conductor devices and are subjected to higher conduction losses than half-bridge (HB) MMCs. Since HB-MMCs are more widely implemented in VSC-HVDC applications than FB-MMCs, the latter are out of the scope of this paper.

The blocking of FB-MMCs cannot prevent the current flowing through the IGBTs' diodes from feeding a dc fault.

To fully stop the energy sources at the converter side from contributing to a fault, an alternative is to bypass the SMs within the MMC. In [25], [26], MMCs are bypassed to transform a dc fault into a balanced ac short-circuit so that the dc current will gradually be cleared and MMCs can then recover. However, the ac system will be exposed to a large ac current due to the long fault clearance duration. Additional thyristors are required to form the bypass circuit. The advantage of using thyristors is their capability to withstand large ac currents. These methods could also be implemented for HVDC grids. However, as thyristors cannot be turned off when their currents are different from zero, the recovery of an MMC station from a bypassing operation is slow and would cause a more severe disturbance to both ac and dc systems.

An alternative is to bypass an MMC using its own IGBTs. This concept has been tested in a point-to-point link in [27]. This work provides significant insight into DCCB switching modeling and the impact of circulating current controllers on the recovery of an MMC. However, its application in HVDC grids and a coordinated operation with multiple DCCBs have not been studied. It should be remarked that since IGBTs have a low current capability, a detailed analysis of the maximum arm and ac currents of an MMC during bypassing is required. This has not been covered in previous work.

Considering that future HVDC grids will likely employ DCCBs, this paper proposes a new protection strategy to coordinate the operation of hybrid DCCBs and HB-MMCs. MMCs are bypassed prior to the opening of the DCCBs so that fault currents can be interrupted at much smaller magnitudes, followed by an immediate recovery of the MMCs after fault isolation. For completeness, analytical expressions describing the suppression of currents are provided. More importantly, arm and ac currents during the coordination of MMCs and multiple DCCBs are also analyzed for different values of system inductance and bypassing duration so that the safety of devices is ensured during operation. A fault detection and discrimination algorithm has been included alongside the proposed method to evidence, via simulation studies, the benefits brought by the method compared to when MMCs are blocked and when no corrective action is taken.

II. Coordination of MMCs With Hybrid DCCBs

A. Operation of Hybrid DCCBs

A hybrid DCCB is composed of a load commutation switch (LCS) built using several IGBTs, an ultrafast disconnector (UFD) and a main breaker (MB) which consists of several hundreds of IGBTs and surge arresters [8] (see Fig. 2). Current flows through the LCS and the UFD during normal operation [see Fig. 2(a)]. Losses are small as the LCS consists only of a few IGBTs.

Once a tripping signal is received, the LCS will be first switched off. It immediately blocks to commutate the fault current into the MB [see Fig. 2(b)]. The voltage rating of LCS must exceed the on-state voltage of the MB [8]. The UFD can then open following the action of the LCS, although its operation typically takes several milliseconds. The dc fault current flowing through the MB will keep rising with a very high rate during this time. A current limiting reactor (CLR) is therefore used to mitigate the rise of dc fault current. It should be noticed that the voltage rating of the MB and UFD is typically designed as 1.5 p.u. of the dc system voltage to withstand fast voltage transients during current breaking [8]. This rating much higher compared to that of LCS.

After the UFD fully opens, the MB will trip to isolate the fault and the fault energy is absorbed by the surge arresters [see Fig. 2(c)]. The residual current breaker (RCB) will also open after the fault current is reduced to zero [see Fig. 2(d)].

B. HB-MMC Bypassing

In the proposed method, the MMCs can be temporarily bypassed (for ≈2–3 ms) to suppress the fault current before the opening of DCCBs. This is achieved by opening the upper IGBTs in all SMs and by keeping the lower IGBTs closed in the

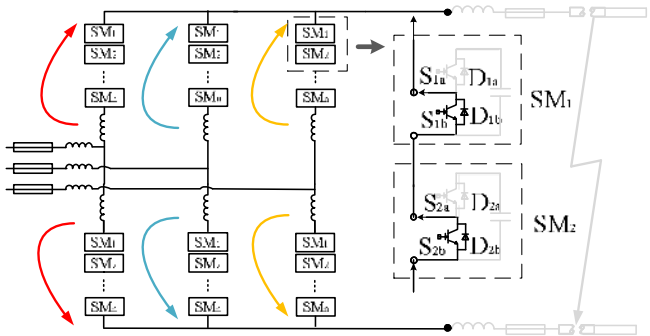

Fig. 3. MMC bypassing operation.

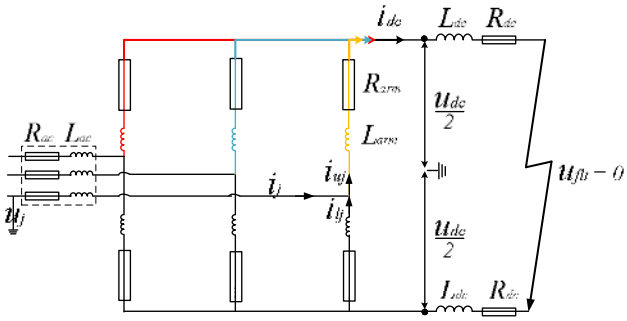

Fig. 5. Equivalent circuit after bypassing all SMs.

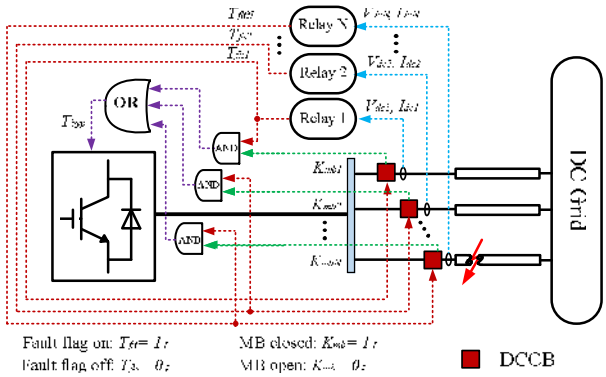

Fig. 4. Algorithm for coordinating operation.

event of a dc fault (see Fig. 3). For instance, S_{1a} of SM_1 and S_{2a} of SM_2 are opened while S_{1b} of SM_1 and S_{2b} of SM_2 keep closed.

A solid dc fault is then converted into a balanced ac short circuit during bypassing. Consequently, the SM capacitors will stop discharging and the current flowing within the three phases is balanced. This prevents the fault current contributed from the MMC side from increasing, resulting in a large reduction in the interrupted dc fault current (see Section III for details). Moreover, since the SM capacitors will not discharge, the rise in the MMC arm current will be also mitigated and the internal protection of IGBTs (based on overcurrent) will be unlikely triggered to block the MMCs. Given that the ac short circuit lasts for several milliseconds only, it will not cause a significant disturbance to connected ac systems and will be automatically cleared after MMC recovery [28].

C. Sequence of Actions for MMC and DCCB Coordination

The detailed sequence of actions for the coordination of MMC bypassing and DCCB operation are given below:

Step 1: A dc fault occurs. The transducers at the line ends continue measuring voltages (V_{dc1}, $V_{dc2} \ldots V_{dcN}$) and currents (I_{dc1}, $I_{dc2} \ldots I_{dcN}$) and sending these measurements to the relays at the local busbar (see Fig. 4).

Step 2: The relays detect and discriminate the fault based on the input measurements. The relay at the faulty circuit will turn on its fault flag ($T_{fltN} = 1$) while the fault flags for relays on healthy circuits remain off ($T_{flgt1} = 0$).

Step 3: The MB of the DCCB on the faulty circuit is in a closed state ($K_{mbN} = 1$) and its LCS is open as the respective fault flag is turned on. The fault current is then commutated to the MB. The DCCB starts to open its UFD in a relatively slower manner than the LCS. Meanwhile, the local MMC is immediately bypassed as one of the fault flags is on ($T_{fltN} = 1$) and the respective MB is in closed state ($K_{mbN} = 1$).

Step 4: The UFD is fully opened immediately after the opening of the MB ($K_{mbN} = 0$). The MMC will hence resume to normal operation.

Step 5: The fault energy is absorbed by the surge arrester of the DCCB. The fault current is drawn to zero followed by the opening of the RCB.

The coordination of DCCBs and MMCs mainly happens at Step 3, where the UFD of the DCCB on a faulty circuit starts to open. As a result of this coordination, the interrupted dc current magnitude is significantly reduced and an overcurrent within MMC arms is prevented. Unlike other bypassing strategies, no additional circuitry is needed to protect the semiconductor devices within the MMCs due to the fast speed of the method. Moreover, given that the coordination occurs at a bus level, no communications are required.

III. Impact of MMC Coordination on System Currents

A. Mathematical Analysis of MMC Bypassing

A mathematical model is used to analyze the fault current reduction using the proposed method. Fig. 5 shows the equivalent circuit of an MMC in bypass mode due to a dc fault. This is a first-order RL circuit where L_{ac} and R_{ac} form the ac system reactance; R_{arm} is the switching-on resistance of the semiconductor devices in each arm; L_{arm} the arm inductance; L_{dc} the dc inductance per pole (including the current limiting reactor within the DCCB), and R_{dc} the dc resistance per pole.

The dc current flowing through the positive pole (i_{dc}) and the upper arm currents (i_{uj}) has the following relationship:

$$i_{dc}(t) + \sum i_{uj}(t) = 0 \tag{1}$$

where "j" represents phases a, b, c. The upper arm currents are driven by the difference between the ac phase voltage (u_j) and

the converter dc pole-to-ground voltage ($u_{dc}/2$):

$$\frac{u_{dc}\left(t\right)}{2}-u_{j}=R_{arm}i_{uj}\left(t\right)+L_{arm}\frac{di_{uj}\left(t\right)}{dt}+R_{ac}i_{j}\left(t\right)+L_{ac}\frac{di_{j}\left(t\right)}{dt} \tag{2}$$

Substituting (2) into (1) yields the relationship between dc voltage and dc current:

$$R_{arm}i_{dc}\left(t\right)+L_{arm}\ \frac{di_{dc}\left(t\right)}{dt}=\ -\frac{3}{2}u_{dc}\left(t\right) \tag{3}$$

The voltage at the faulty point is ideally zero (i.e., $u_{flt}=\ 0$, see Fig. 5). Therefore, the dc voltage can be expressed as:

$$u_{dc}\ \left(t\right)=\ 2\left[L_{dc}\frac{di_{dc}\left(t\right)}{dt}+R_{dc}i_{dc}\left(t\right)\right] \tag{4}$$

By combining (3) and (4), dc current $i_{dc}(t)$ is obtained:

$$i_{dc}\ \left(t\right)=I_{dc}^{-}\ \times e^{-\left(\frac{R_{arm}+3R_{dc}}{L_{arm}+3L_{dc}}\right)\left(t-t_{0}\right)} \tag{5}$$

where I_{dc}^{-} is the initial dc current prior to MMC bypassing and t_0 the instant at which the MMC starts to bypass.

Equation (5) mathematically illustrates the effectiveness of bypassing an MMC for dc current suppression. The dc current only depends on its initial value and on the system reactance and resistance; hence, the SM capacitors will not discharge and the ac current will not flow through the dc circuit. Also, the converter dc current will exponentially decay to zero if the SM bypass mode is permanently activated.

The ac phase current (i_j), upper arm current (i_{uj}) and lower arm current (i_{lj}) shown in Fig. 5 can be represented as:

$$\begin{cases} i_{j}\left(t-t_{0}\right)=i_{j}^{+}\left(t-t_{0}\right)+\left[i_{j}^{-}\left(t_{0}\right)-i_{j}^{+}\left(t_{0}\right)\right]e^{-(R/L)(t-t_{0})} \\ i_{uj}\left(t-t_{0}\right)=i_{uj}^{+}\left(t-t_{0}\right)+\left[i_{uj}^{-}\left(t_{0}\right)-i_{uj}^{+}\left(t_{0}\right)\right]e^{-(R/L)(t-t_{0})} \\ i_{lj}\left(t-t_{0}\right)=i_{lj}^{+}\ \left(t-t_{0}\right)+\left[i_{lj}^{-}\left(t_{0}\right)-i_{lj}^{+}\left(t_{0}\right)\right]e^{-(R/L)(t-t_{0})} \end{cases} \tag{6}$$

where superscript "$-$" denotes a pre-bypassing steady-state operating condition and "$+$" denotes a post-bypassing steady-state condition. R and L are the total resistance and inductance of the bypassed ac circuit and are given as:

$$R\ =\frac{R_{arm}}{2}\ +R_{ac}\ ,\ L\ =\frac{L_{arm}}{2}\ +L_{ac}. \tag{7}$$

During normal operation, the MMCs use a circulating current suppression control strategy [29]. The current of the upper and lower arms consists of a third of the dc current (I_{dc}) and half of the ac phase current:

$$\begin{cases} i_{j}^{-}\left(t\right)=I_{j}^{-}\ \sin\left(\omega t+\alpha\right),\ i_{uj}^{-}\left(t\right)=\ \frac{I_{j}^{-}\sin\left(\omega t+\alpha\right)}{2}+\frac{I_{dc}^{-}}{3}, \\ i_{lj}^{-}\left(t\right)=\frac{I_{j}^{-}\sin\left(\omega t+\alpha\right)}{2}-\frac{I_{dc}^{-}}{3}, \end{cases} \tag{8}$$

where I_j^-, ω and α represent the magnitude, angular speed and phase angle of the steady-state ac phase current during normal SM operation (i.e., before the SM bypass mode is enabled).

During the MMC bypass mode, the IGBTs in the upper and lower arms of the MMCs are connected in parallel; hence, the current flowing through them will be identical in the post-bypassing steady-state and equal to half the ac phase current:

$$\begin{cases} i_{j}^{+}\ \left(t-t_{0}\right)=I_{j}^{+}\ \sin\left[\omega\left(t-t_{0}\right)+\beta\right] \\ i_{uj}^{+}\ \left(t-t_{0}\right)=i_{lj}^{+}\ \ \left(t-t_{0}\right)=\frac{i_{j}^{+}\left(t-t_{0}\right)}{2} \end{cases} \tag{9}$$

I_j^+ and β are the magnitude and phase angle of the steady-state ac phase current due to the SM bypass mode and depend on the ac system impedance and voltage magnitude U_j:

$$\begin{cases} I_{j}^{+}=\frac{U_{j}}{\sqrt{R^{2}+\left(L\omega\right)^{2}}},\ \beta\ =\ -\arctan\left(\frac{L\omega}{R}\right) \end{cases} \tag{10}$$

Substituting (8) and (9) into (6) yields:

$$\begin{cases} i_{j}\ \left(t-t_{0}\right)=I_{j}^{+}\ \sin\left(\omega\left(t-t_{0}\right)+\beta\right) \\ \quad+\left[I_{j}^{-}\sin\left(\omega t_{0}+\alpha\right)-I_{j}^{+}\sin\left(\omega t_{0}+\beta\right)\right]e^{-(R/L)(t-t_{0})} \\ i_{uj}\ \left(t-t_{0}\right)=\frac{I_{j}^{+}\sin\left(\omega\left(t-t_{0}\right)+\beta\right)}{2} \\ \quad+\left[\frac{I_{j}^{-}\sin\left(\omega t_{0}+\alpha\right)-I_{j}^{+}\sin\left(\omega t_{0}+\beta\right)}{2}+\frac{I_{dc}^{-}}{3}\right]e^{-(R/L)(t-t_{0})} \\ i_{lj}\ \left(t-t_{0}\right)=\frac{I_{j}^{+}\sin\left(\omega\left(t-t_{0}\right)+\beta\right)}{2} \\ \quad+\left[\frac{I_{j}^{-}\sin\left(\omega t_{0}+\alpha\right)-I_{j}^{+}\sin\left(\omega t_{0}+\beta\right)}{2}-\frac{I_{dc}^{-}}{3}\right]e^{-(R/L)(t-t_{0})} \end{cases} \tag{11}$$

which shows the dynamic characteristics of the ac and arm currents due to the MMC bypass operation. In a transient regime, these depend on the bypass start time t_0, the bypass duration, and the system impedance. The dc current does not influence the value of the instantaneous ac current but it affects the arm currents during transients. The SM capacitors do not contribute to the arm currents during MMC bypassing.

B. Mathematical Analysis of MMC Blocking

If an MMC is blocked instead of being bypassed, the dc fault current contributed from SM's capacitors is also eliminated. However, fault current is still contributed from the ac sides through the diodes of the MMC. The current flowing through it can follow two possible paths [see Fig. 6(a) and (b)] [30], [31]: (a) through a three-diode rectifier, and (b) through a four-diode rectifier. Notice that the ac side of the MMC is an equivalent star connection which was converted from a delta connection.

In the path with the three-diode rectifier, the circuit in Fig. 6(a) can be re-drawn as Fig. 6(c), where L_{dc} is the converter dc terminal inductance, L_{arm} is the arm reactance, $L_{ac,e}$ is the equivalent ac inductance and u_j is the phase-to-ground ac voltage. Resistances are much smaller than inductances and hence are ignored. The Laplace transform can be used to obtain the expression of the dc current (i_{dc}). The solution is given as

$$i_{dc}\left(t\right)=\left|\frac{2\sqrt{3}U_{j,ll}}{4L_{dc}+3\left(L_{arm}+L_{ac,e}\right)}\sin\left[\omega\left(t-t_{0}\right)+\alpha\right]\right|+I_{dc3d}^{-} \tag{12}$$

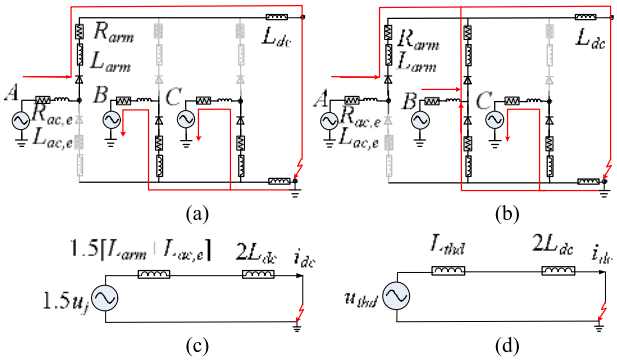

Fig. 6. Current flowing within a MMC after blocking operation. (a) Through a three-diode rectifier. (b) Through a four-diode rectifier. (c) Equivalent circuit of three-diode rectifier. (d) Equivalent circuit of four-diode rectifier.

where ω is the frequency of the ac system, $U_{j,ll}$ is the phase to phase voltage and I_{dc3d}^{-} is the dc current before this stage [31].

For the four-diode rectifier stage, the circuit in Fig. 6(b) can be represented as the Thevenin equivalent circuit shown in Fig. 6(d), where L_{thd} and U_{thd} are the equivalent inductance and voltage. The solution of the i_{dc} in this stage is given as

$$\begin{cases} i_{dc}(t) = \left| \dfrac{L_{arm} U_{j,ll}}{2\left(L_{thd}+2L_{dc}\right)\left(L_{arm}+L_{ac,e}\right)} \sin\left[\omega\left(t-t_0\right)+\beta\right] \right| \\ \qquad +I_{dc4d}^{-} \\ L_{thd} = \dfrac{2L_{arm} \times \left(L_{arm}+L_{ac,e}\right) \times \left(L_{arm}+L_{ac,e}\right)}{L_{ac,e} \times \left(L_{arm}+2L_{ac,e}\right)+L_{arm} \times \left(2L_{arm}+3L_{ac,e}\right)} \end{cases} \tag{13}$$

where I_{dc4d}^{-} is the dc current before the stage of the four-diode rectifier [31].

It should be noticed that both (12) and (13) have a sinusoidal ac component. As the diodes can only conduct current in a forward direction, the ac component will always make the dc current larger after blocking. If the initial dc current prior to MMC blocking or bypassing is the same ($I_{dc3d}^{-} = I_{dc}^{-}$ or $I_{dc4d}^{-} = I_{dc}^{-}$), the performance dc current suppression using blocking is always worse than that of MMC bypassing. According to (5), the dc current after bypassing will become smaller.

C. MMC Bypassing for the Suppression of DC Fault Current

A simulation is performed in PSCAD to illustrate the effectiveness of a bypass operation to suppress the fault current contributed from the converter side. All results are given in per unit. The selected base values are 1 kA for dc current, 400 kV for dc voltage, 0.4 MJ for dc energy and 1.67 kA for both ac phase and arm currents. A solid pole-to-pole fault was applied at 1 s at the terminals of an MMC operating at a rated dc voltage of ±200 kV (± 0.5 p.u.) and a rated dc current of 1 p.u. The technical parameters of the MMC are listed in Table I and correspond to the Zhou Shan converter station in the Zhou Shan five-terminal dc network [2]. The ac system is rated at 220 kV and has a total impedance of 0.12 H to have a short circuit current level under 3 p.u.

Results are shown in Fig. 7. To facilitate the understanding, MMC bypassing is enabled when the fault current exceeds

TABLE I
ZHOU SHAN MMC DATA

Component	Attribute	Description
MMC	Power rating	400 MW
	Voltage rating	± 200 kV
	SMs per arm	250
	SM capacitance	12 mF
	Arm inductor	90 mH
	IGBT rated current	1.67 kA (1 p.u.)
	IGBT peak current	3 kA (1.8 p.u.) for 10 μs
	Diode peak current	3 kA (1.8 p.u.) for10 ms
	DC inductor	20 mH
AC transformer	Ratio	230 kV / 205.13 kV
	Power rating	450 MW
	Impedance	15%
	Peak ac current	20 kA (11.98 p.u.) for 2s
AC system	Nominal voltage	220 kV
	Impedance	0.12 H

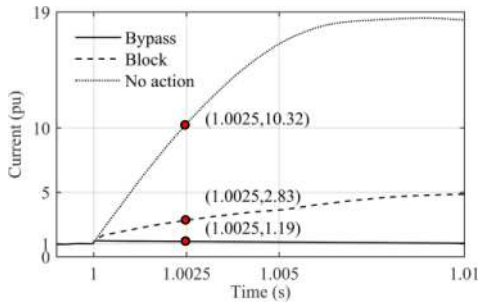

Fig. 7. DC fault current caused by a solid pole-to-pole fault.

1.2 p.u., which is sensed by the relay after 250 μs. It should be highlighted that the total delay for sensing the fault could be larger in practical applications as there will be delays caused by data acquisition and coding/decoding of analogue-digital signals. In addition, noise may need to be filtered for data acquisition, which in turn may incur in extra delays. Such delays are neglected in this study. For comparison, the fault currents when no action is taken and when the MMC is blocked are also given. The DCCBs are kept closed to clearly show the differences between the MMC operation modes. As it can be observed, the fault current increases to 18 p.u. within 10 ms if the MMC keeps operating. If the MMC is blocked, the fault current rises to 5 p.u. but at a smaller rate. However, it decays exponentially from 1.2 to 1 p.u. within 10 ms if the MMC is bypassed.

Assuming a total operation delay of 2.25 ms for a hybrid DCCBs (2 ms to open the UFD and 250 μs to open of LCS) [8], the MMC should bypass for the same amount of time if a coordinated operation is desired. In this case, the interrupted current magnitude is 1.19 p.u. – still much smaller compared to when the MMC is blocked (2.83 p.u.) or when no action is taken (10.32 p.u.). It is worth to mention that the blocking operation also reduces the dc current to a level which can be interrupted by DCCBs [8]. However, with the bypassing operation, a further reduction in dc current will decrease the current rating requirements of protection devices and of the cooling system of the DCCBs. Considering that DCCBs are expensive devices, their cost can be significantly reduced by using IGBTs with smaller

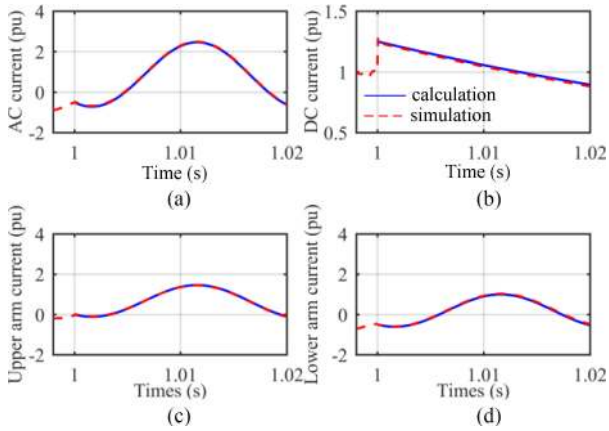

Fig. 8. Impact of MMC bypass operation on (a) ac current, (b) dc current, (c) upper arm current, and (d) lower arm current.

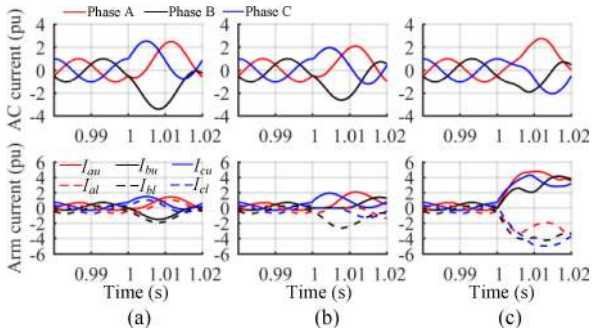

Fig. 9. Comparison of the impact on ac and arm currents for three MMC modes of operation. (a) Bypass action. (b) Blocking action. (c) No action.

current rating or by reducing the number of IGBTs being employed. In addition, smaller reactors could be used, which would further reduce the cost and footprint of the protection system.

D. Analysis of Arm and AC Currents

The coordinated operation also aims to reduce the rate of rise in the arm current while avoiding significant disturbances to ac currents. Fig. 8 shows the impact of MMC bypassing on the ac current (phase A), arm currents (phase A), and dc current due to a pole-to-pole dc fault at 1 s. The results shown with a blue solid line were obtained using (11) and the red dashed lines show PSCAD results. As it can be observed, both set of results show a good agreement. The ac current rises to a peak value of 2.49 p.u. within 12 ms while the upper and lower arm currents increase to a maximum of 1.457 and 1.043 p.u., respectively. According to the data in Table I, neither the semiconductors within the MMC nor the ac transformer will be damaged as a result of the bypassing operation.

Fig. 9 shows the three-phase ac and arm currents for an MMC in bypassing and blocking modes and when no action is taken. It should be emphasized that no additional action is applied throughout each test to clearly show the impact of the three different operations on ac and arm current over a long time (20 ms). The ac and upper arm currents are represented by solid lines while the lower arm currents are given as dashed lines. It is clearly shown that the rise of arm current is limited when the MMC is bypassed. This is because the ac phase current is shared by the upper and lower arms during MMC bypassing. The maximum magnitude of the arm currents is 1.78 p.u., which occurs in the lower arm of phase B at 1.008 s. When the MMC is blocked, this value is higher (2.69 p.u. in phase B at 1.008 s) as one of the arm currents will be equal to the ac phase current. In practice, thyristors could be used to protect the MMC as the arm current exceeds the capability of IGBTs and diodes [31]. However, MMC blocking still significantly lower than when no action is taken (4.79 p.u. in phase C at 1.012 s).

Although the benefits brought by the bypassing operation are clear, the maximum magnitude of the ac current (3.47 p.u. at 1.008 s in phase B) is higher when compared to a blocking operation (2.53 p.u.) or when no action is taken (2.82 p.u.). However, considering that the bypassing action would be coordinated with the operation of DCCBs, the fault would be isolated in 2.25 ms and followed by the restoration of the MMC. This coordination will result in much smaller ac phase and arm currents due to the fast operation of DCCBs and the MMC. The maximum arm and ac currents when the MMC is bypassed are only 1.239 p.u. (2.07 kA) and 2.059 p.u. (3.44 kA) before 1.00225 s. In addition, according to (11), the magnitude of these currents not only depends on the duration of the MMC bypassing, but also on the instant when the action is taken and on the ac system impedance. To provide additional insight, these aspects are further analyzed next.

1) Impact of MMC Bypass Instant and Duration: The bypass instant will affect the peak values of the ac and arm currents following bypassing. In a dc fault, the post-bypass currents will have a maximum peak magnitude if the MMC is bypassed when the instantaneous currents have their nominal positive or negative peak values. To examine this behavior, a sensitivity study is carried out for dc faults occurring at different instants within one full ac cycle (i.e., 0° to 360°). The bypass operation is enabled and the DCCBs start to open when the dc current sensed by the relay exceeds 1.2 p.u. The operation speed of DCCBs is varied between 0 ms (no operation delay) to 2.25 ms and hence a bypass duration up to 2.25 ms is considered.

Fig. 10(a), (c) and (e) shows results using analytical calculations. Different instants of fault occurrence and bypass durations are shown. The red area in Figs. 10(a), (c) and (e) shows the magnitudes of ac and arm currents increase as the delay in the operation of DCCBs (and hence the bypass duration) increases from 0 to 2.25 ms. The maximum magnitude of ac current is only 2.063 p.u. [see the dashed red line in Fig. 10(a) which occurs for dc faults taking place when the ac current phase angle is 85.5° or 265.5° (i.e., 4.5° prior to its nominal positive or negative peak value]. This occurs since it takes 0.25 ms (i.e., 4.5°) for the dc current to reach 1.2 p.u. and the MMC bypassing is enabled when the ac current reaches its peak value. Similarly, the maximum magnitudes of upper and lower arm currents are both 1.277 p.u. (occurring at the same instant).

Fig. 9(b), (d) and (f) shows the ac and arm currents obtained through time-domain simulations. In Fig. 9(b) and (d), the fault is applied at 1.00475 s (i.e., 85.5°) to generate the maximum ac and upper arm currents. In Fig. 10(f), the fault is applied at

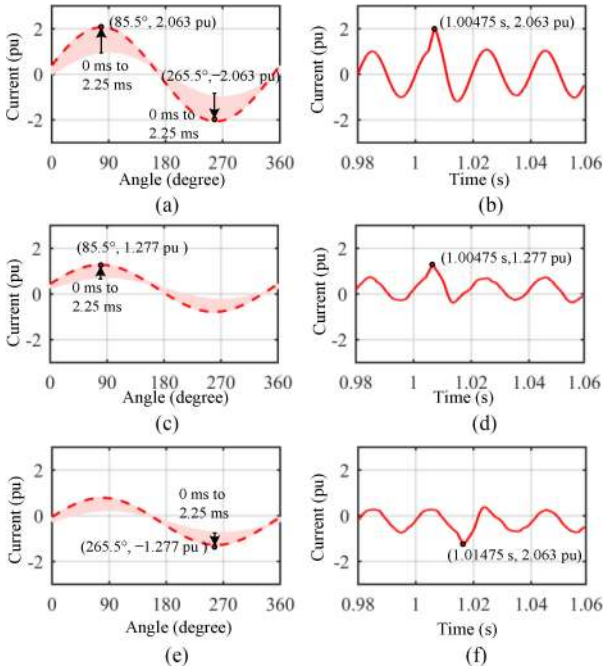

Fig. 10. Analysis of maximum ac and arm currents. (a) Analytical ac current. (b) Simulated ac current. (c) Analytical upper arm current. (d) Simulated upper arm current. (e) Analytical lower arm current. (f) Simulated lower arm current.

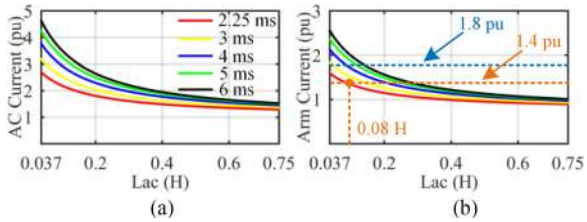

Fig. 11. AC system impedance and bypassing period analysis. (a) Maximum ac current. (b) Maximum arm current.

1.01475 s (i.e., 265.5°) to obtain the maximum magnitude for the lower arm current. These results agree with the analytical calculations: the maximum ac and arm currents are 2.063 and 1.277 p.u. respectively when the MMC is bypassed for 2.25 ms [see Fig. 9(a), (c) and (e)].

It should be highlighted that the peak currents shown in Fig. 10 are within the overcurrent limits of the IGBTs and the ac components according to Table I. Hence, MMC bypassing will neither drastically affect ac system performance nor damage the semiconductor devices. The bypass operation is completed when the DCCBs isolate the fault. The MMC then recovers smoothly without causing significant disturbances.

2) Impact of AC System Impedance and Bypass Duration: A sensitivity analysis is performed to investigate the impact of different ac system impedances (L_{ac}) on the maximum values of ac-side currents. Different delays in the operation of DCCBs, and hence the required bypassing durations, are considered. Figs. 11(a) and 10(b) show results using analytical calculations. The maximum ac and arm currents decrease from 4.671 to 1.257 p.u. and from 2.695 to 0.898 p.u., respectively, as L_{ac} increases from 0.037 to 0.75 H and as the bypass duration reduces from 6 to 2.25 ms.

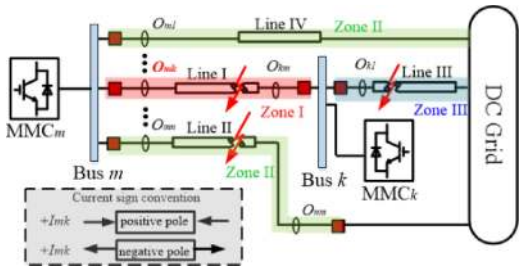

Fig. 12. Fault discrimination in a generic HVDC grid.

Considering that the semiconductor devices within the MMCs can withstand a current up to 1.8 p.u. (3 kA) and that the operation of DCCBs is fast, the proposed coordinated protection strategy can be used on HVDC grids linked to ac systems when $L_{ac} \geq 0.037$ H. However, the semiconductors could feature internal self-protection to block the converters if the arm current exceeds a threshold of typically 1.4 p.u. of its rated value. To ensure the benefits of bypassing, the arm currents should not exceed this threshold either. Fig. 11(b) shows the operation range if the threshold is set to 1.4 p.u. (2.35 kA). As it can be observed, the method is suitable for HVDC systems interconnecting ac grids with $L_{ac} \geq 0.08$ H.

IV. Relaying Algorithm for Coordinated Operation

When a coordinated operation is employed, relays should quickly detect and discriminate a dc fault using local measurements only and hence avoid communication delays. This section considers the use of an algorithm based on the local measurement of both dc current and voltage. The criteria used are the same as in [33], with discussions on the impact of MMC bypassing on the threshold design for each criterion included here for completeness. In a generic HVDC grid as in Fig. 12, the relay at location O_{mk} connected to Bus m should be able to detect and discriminate an internal fault (in Zone I) from external faults at a dc line connected to the same busbar (in Zone II) and at a dc line connected to the remote Bus k (in Zone III).

Let the current measured at O_{mk} be I_{mk} and its derivative be dI_{mk}/dt. The criterion for discriminating faults at Zone I from Zone II is given as

$$\text{If } \left(\frac{dI_{mk}}{dt} > \frac{dI_{thr}}{dt}\right), \text{then } T_{n2mk} = 1, \tag{14}$$

where dI_{thr}/dt is the threshold for the derivative of the first current wavefront and T_{n2mk} is a flag that will be turned on to confirm that the fault is not at Zone II if the measured dI_{mk}/dt is larger than the threshold. A fault at Zone I should induce a positive dI_{mk}/dt and at Zone II a negative dI_{mk}/dt is expected. If MMC$_m$ is bypassed following an external fault in Zone II, I_{mk} will still flow from Line I to Bus *m* and, as a result, dI_{mk}/dt will be negative. The bypassing operation will not change the sign of dI_{mk}/dt and hence will not affect fault discrimination of the relay at O_{mk}.

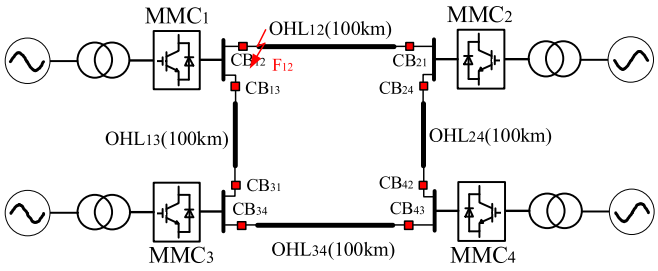

Fig. 13. One-line diagram of the meshed dc test system.

The discrimination of faults at Zone I from Zone III is designed based on the voltage measurement at O_{mk} (U_{mk}) and its derivative (dU_{mk}/dt). The CLRs of DCCBs (located at O_{km} and O_{kl}) are large and hence the electrical distance between two dc lines is increased by their inclusion. This significantly facilitates fault discrimination. The increase in fault current will result in a significantly enough voltage difference across the CLRs. A fault at Zone I will hence cause a larger decrease in U_{mk} with a steeper negative rate dU_{mk}/dt compared to that at Zone III. Hence, the criterion is given as:

$$\text{If } (U_{mk} < U_{thr}) \text{ and } \left(\frac{dU_{mk}}{dt} < \frac{dU_{thr}}{dt}\right), \text{ then } T_{n3mk} = 1. \tag{15}$$

where U_{thr} and dU_{thr}/dt in (15) are the thresholds for voltage and its derivative, respectively, and T_{n3mk} is a flag that will be turned on to confirm the occurrence of a fault outside Zone III if the inequalities in (15) are met. If an external fault happens at Zone III, MMC$_k$ will also bypass, leading to a lower voltage at Bus k and hence lower U_{mk} with a faster rate of change compared to the case without MMC bypassing. Therefore, to ensure that the relay at O_{mk} does not turn on its fault flag for a fault in Zone III, the values of U_{thr} and dU_{thr}/dt should be set lower than those for U_{mk} and dU_{mk}/dt for faults at Zone III followed by the bypassing of MMC$_k$, but still higher than those for faults at Zone I [see (15)].

Combining (14) and (15), the final criterion for fault discrimination can be expressed as:

$$\text{If } (T_{n2mk} = 1) \text{ and } (T_{n3mk} = 1), \text{then } T_{fltmk} = 1. \tag{16}$$

To further increase the discrimination reliability, five consecutive samples are used. In other words, the relay at O_{mk} will only turn a final fault flag (T_{fltmk}) on when five consecutive samples of T_{n2mk} and T_{n3mk} meet criterion (14). The fault flag will then be sent to MMC$_m$ and the DCCB at O_{mk} for a coordinated operation.

V. Simulation Studies

A. Test System

The performance of the coordination scheme is assessed in the four-terminal HVDC system shown in Fig. 13. The system is rated at ±200 kV. Overhead lines (OHLs) generally experience a larger number of faults than cable-based systems and dc fault propagates faster in OHLs [25]. Therefore, OHLs are used in this paper for the simulation studies. The proposed method is not limited to HVDC systems connected by OHLs since an MMC bypassing action significantly reduces the fault current through DCCBs contributed from MMCs and ac systems. Moreover, the current contributed by MMCs is the most dominant. The DCCBs are located at dc line ends. The ac systems are rated at 220 kV. Converter MMC$_1$ regulates the dc voltage to ±200 kV, while MMC$_2$, MMC$_3$ and MMC$_4$ operate in power control mode to regulate power to 200, −200 and 200 MW, respectively. Other relevant data is listed in Table I.

TABLE II
Thresholds for Protection

Relays	CB_{12}	CB_{21}	CB_{13}	CB_{31}	CB_{24}	CB_{42}	CB_{34}	CB_{43}
U_{thr} (p.u.)	0.8	0.69	0.5	0.5	0.56	0.56	0.69	0.69
dU_{thr}/dt (p.u./ms)	0.5	1.25	1.25	1.25	1.25	1.25	0.95	1.25
dI_{thr}/dt (p.u./ms)	> 0.15							

B. Modeling of DC Components

All OHLs are represented using the frequency dependent model available in PSCAD/EMTDC. The conductor (type AAAC-806-A4-61) and ground wire (type AFL CC-75-528) data for OHL model can be found in [34], [35], respectively. The structure of the tower is provided in [36]. All DCCBs are modeled as hybrid, with an operation delay of 2.25 ms. The limiting reactors are set to 0.05 H and surge arrester banks are rated at 0.75 p.u. (300 kV). All MMCs are represented as Thévenin equivalent models [37].

C. Case Studies

Due to its severity, a solid pole-to-pole fault is applied to the test system to assess the effectiveness of the proposed coordination algorithm. Fault F_{12} is applied at 1 s at the end of OHL_{12} connected to MMC$_1$ (i.e., at CB_{12}, see Fig. 13). Table II shows the selected thresholds for the criterion developed in Section IV. The internal self-protection of SMs will be activated if the arm current is larger than 1.4 p.u. Two studies are performed:

- *Study 1:* DCCBs act **without** coordination of MMCs;
- *Study 2:* DCCBs act **with** coordination of MMCs.

Simulation results are given from Figs. 14–16. In both studies, fault detection and discrimination is fast, taking 0.24 ms at CB_{12} and 0.4 ms at CB_{21}. The DCCBs at CB_{12} and CB_{21} then start to open and MMC$_1$ and MMC$_2$ bypass their SMs to suppress dc fault currents. The MMCs will recover after the MBs of the DCCBs on the faulty circuit open. The remote MMCs (i.e., MMC$_3$ and MMC$_4$) do not bypass as the relays of their DCCBs discriminate fault F_{12} as an external fault. They will also not block as their arm currents are under 1.4 p.u.

Fig. 14 shows the interrupted currents and absorbed fault energy of DCCBs at CB_{12} and CB_{21} for both studies. It can be observed that the MMC bypassing can significantly reduce the currents' magnitude and absorbed fault energy. Taking CB_{12} in Study 2 as an example (with coordination of MMCs), the

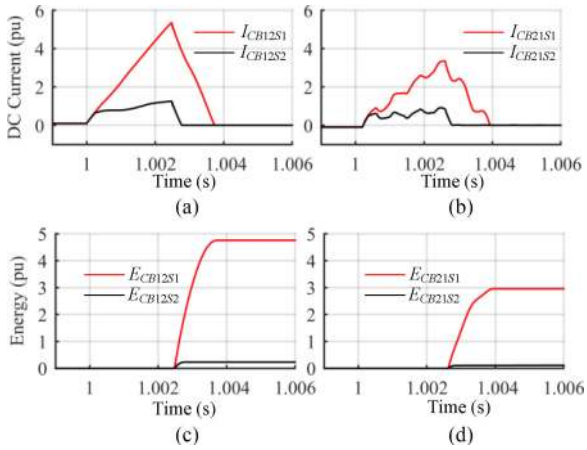

Fig. 14. Simulation results. Current and energy at DCCBs at faulty circuit. (a) Fault current at CB_{12}. (b) Fault current at CB_{21}. (c) Absorbed energy of CB_{12}. (d) Absorbed energy of CB_{21}.

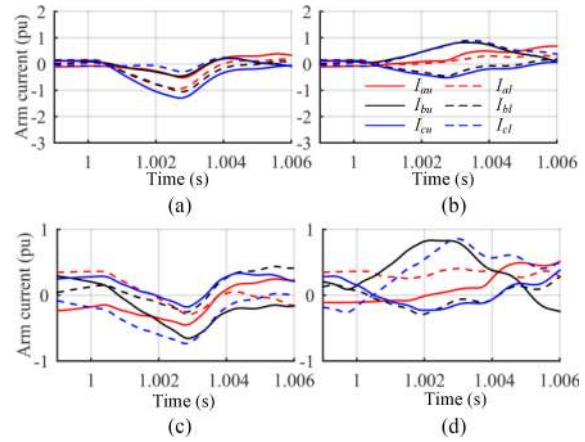

Fig. 15. Simulation results. Three-phase arm currents. (a) MMC1 in Study 1. (b) MMC1 in Study 2. (c) MMC2 in Study 1. (d) MMC2 in Study 2.

interrupted current (I_{CB12S2}) is significantly reduced by 74.5% (to 1.5 p.u.) compared to that in Study 1 (I_{CB12S1}) without the coordination of MMCs (5.9 p.u.). The absorbed energy is reduced by 95.2%, from 4.76 p.u. (1903.2 kJ) (E_{CB12S1}) to 0.23 p.u. (91.5 kJ) (E_{CB12S2}) with MMC bypassing. This significant reduction would allow DCCBs to be designed at a much lower rating. These results clearly demonstrate the benefits of the proposed method.

Fig. 15 shows the arm currents of MMC_1 and MMC_2. I_{au}, I_{bu}, I_{cu} are the upper arm currents for the three phases and I_{al}, I_{bl}, I_{cl} the lower arm currents. For MMC_1 in Study 1, the maximum arm current reaches -1.32 p.u. due to the fast discharge of SM capacitors before the MBs of DCCBs open. In Study 2, the bypassing of MMC_1 prevents the SM capacitors from discharging and hence stops the ac source contributing to the dc current. Consequently, the magnitude of the maximum arm current is reduced to 0.88 p.u. For MMC_2, the maximum magnitudes of arm currents are similar and are smaller compared to those in MMC_1 for both studies. This is because MMC_2 has a large electrical distance to the fault point and will be

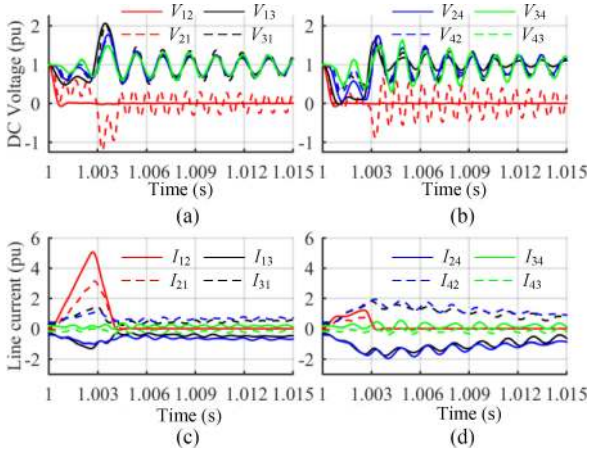

Fig. 16. Simulation results. Measurements of dc voltages and currents. (a) DC voltage in Study 1. (a) DC voltage in Study 2. (c) DC current in Study 1. (c) DC current in Study 2.

less affected than MMC_1. All arm currents are below 1.4 p.u. and the internal self-protection of SMs will not be triggered to block the MMCs. In addition, the ac currents are the superposition of upper and lower currents. In Study 1, the maximum ac current is -1.03 p.u. at 1.00238 s at MMC_1. In Study 2, the bypassing of MMC_1 causes a slightly larger maximum ac current (-1.24 p.u. at 1.00256 s at MMC_1).

Fig. 16 shows the dc voltages and currents measured at all line ends. The voltage and current measured at $CB_{12}, CB_{21} \ldots CB_{43}$ are denoted as $V_{12}, V_{21} \ldots V_{43}$ and $I_{12}, I_{21} \ldots I_{43}$, respectively. As it can be noticed, the bypassing of MMC_1 and MMC_2 allows the dc system to temporarily operate at lower dc voltages. This mitigates the system overvoltage after the DCCBs isolate the fault (i.e., maximum voltage reduced from 2.02 to 1.69 p.u.). In addition, the fault current is significantly reduced when the proposed method is employed. Although the damping of current following system recovery is slower, the duration is still short (about 15 ms) and the currents are small enough to not cause significant disturbances.

VI. Discussion

A. Bypassing Using Thyristors

The Study 2 in Section V-C has been repeated when the MMC bypassing action is achieved using extra thyristors instead of IGBTs [25]. Simulation results at MMC_1 are given in Fig. 17. Fig. 17(a) shows that if thyristors are employed for the bypassing action the dc fault current of CB_{12} ($I_{CB12-thyristor}$) can be reduced. The thyristors' gate signals are removed immediately following the fault isolation. However, the arm currents flowing through the thyristors (e.g., I_{auT}, I_{buT}) do not all come to zero [see Fig. 17(b)]. Those thyristors where current flows must keep conducting and hence the MMC cannot be restored. As a result, the MMC's dc current ($I_{mmc-thyristor}$) keeps decreasing down to -7.2 p.u. during this time due to the in-feeding of the rest of the dc system [see Fig. 17(c)]. As it can be observed, the

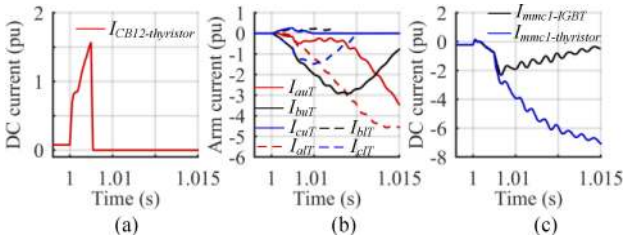

Fig. 17. Bypassing operation using thyristors. (a) Fault current at CB_{12}. (b) Arm currents flowing through thyristors. (c) DC current of MMC_1.

magnitude of $I_{mmc-thyristor}$ is much higher than that when IGBTs are used, which is only -2.1 p.u. $(I_{mmc-IGBT})$ as the IGBTs can turn off at any current and hence the MMC can immediately restore. Therefore, the thyristors based method may not be as suitable as the IGBT based method for HVDC grid applications.

B. Different Approaches for Protecting HVDC Grids

There are also other methods for protecting HVDC grids relying on different technologies. The first method is to use ACCBs with HB-MMCs and fast dc disconnectors (FDs). All MMCs of the HVDC grid should be blocked immediately once a dc fault is detected. The ACCBs then open, taking about 50 ms. As a result, the fault current naturally decays to zero and all FDs open. This process takes a very long time (e.g., 200 ms) [7]. The ACCBs can then re-close, followed by the de-blocking of MMCs and re-closing of FDs at the healthy circuits. As it can be appreciated, the operation of the ACCBs-based method is slow, and the dc system will be exposed to high fault currents. Moreover, the entire HVDC grid must be de-energized during fault clearance. The advantage of using ACCBs is their low investment cost as they constitute a mature technology based on mechanical components.

The second approach is to use MMCs having FB or clamp-double (CD) SMs plus FDs. This type of MMCs can effectively regulate dc fault current to a low magnitude by reversing the dc voltage while keep providing reactive power support to the connected ac systems [23], [38]. The FDs at the faulty circuit can then isolate the dc fault. However, delivery of active power amongst all MMCs is interrupted during fault clearance. Although the duration is much shorter ($<$60 ms) compared to the method based on ACCBs, the power in-feed loss in this period is still not desirable. MMCs using FB or CD SMs also comprise more semiconductor devices compared to HB-MMCs, which increases the conduction losses.

The third approach is to use hybrid DCCBs only. With the DCCB-based method, only those DCCBs at the faulty circuit are required to open and the fault can be isolated within several milliseconds. Active power is still being transmitted by MMCs and will not be interrupted, although there could be some disturbances due to the dc fault. The major shortcoming of using this approach is the high investment cost of hybrid DCCBs due to the need of many semiconductors devices.

The fourth method is to coordinate the operation of both hybrid DCCBs and HB-MMCs as proposed in this paper. While the DCCBs ensure the fast dc fault isolation, the bypassing of MMCs can significantly reduce the dc fault current magnitude. Compared to the method based on ACCBs or FB-MMCs, the delivery of dc power will not be fully interrupted. The system will be recovered immediately after the bypassing of MMCs, taking several milliseconds only. Compared to the protection using DCCBs only, the fault current is significantly reduced and this would reduce the cost of the dc protection devices.

It should be mentioned that [27] proposes to bypass an MMC using IGBT units during a fault to reduce the magnitude of the fault current. However, the method from [27] has the following main differences compared to the approach presented in this paper: (a) the method in [27] has been developed for point-to-point link protection, while this paper aims to provide a general solution for HVDC grid protection; (b) one MMC coordinates with multiple DCCBs in the study presented in this work (see Fig. 4); (c) the algorithm and duration for MMC bypassing is different in [27] compared to this work. In this study, the MMC bypassing is based on both fault detection and the position of the MB of the DCCB. A bypassed MMC will recover immediately after the MB of the DCCBs open. Conversely, in [27] the MMC is bypassed based on the fault signal only and the bypass duration is based on the duration of the fault.

Another method incorporating bypassing is also proposed in [39], where thyristors are used for bypassing plus the use of a slow DCCB. The method can be well implemented in point-to-point links, with the slow-acting DCCB helping to reduce the cost compared to the method presented in this paper. However, as previously discussed, the bypassing based on IGBTs is more suitable for protecting HVDC grids and the use of hybrid DCCBs can achieve faster system recovery while causing less disturbances to neighboring ac systems.

Other coordination methods also rely on MMC blocking during the operation of DCCBs. For instance, in [40], the MMCs are blocked during fault clearance and recover once the DCCBs open. Compared to the proposed method, the fault clearance flags for MMC restoration are also based on the opening of DCCBs as in [40]. However, the flags for corrective actions of the MMCs (bypass or block) are different. In this paper these flags are based on measurements of dc line current and voltage and its derivatives while in [40] they are based on the converter's arm current, terminal current and voltage. The MMC blocking can also depend on the MMCs' arms overcurrent only and the DCCBs can act to isolate the dc fault. If there is an overcurrent present, the MMC will be blocked, or otherwise, the MMC will stay de-blocked during fault clearance. The MMC blocking strategy also reduces the dc current but not as much as the bypassing operation (as analyzed in previous sections).

VII. Conclusion

System protection upon dc faults remains a key technical issue preventing the widespread deployment of HVDC grids. To contribute to this, this paper proposes the coordination of HB-MMCs with hybrid DCCBs to reduce the fault current magnitudes and to mitigate the rise of MMC arm current following dc faults. A coordination sequence for DCCBs and MMCs has

been established. To provide further insight, an analysis of the impact of MMC bypassing on dc current and on arm and ac currents has been performed. For completeness, a comparison has been made when MMCs are blocked and when no corrective action is taken.

To assess the effect of the coordination scheme, a method for fault detection and discrimination has been also considered. The algorithm for MMC bypassing has been evaluated and its effectiveness to reduce dc fault current and absorbed energy has been tested using a four-terminal HVDC system. It has been shown that if dc fault isolation by DCCBs takes place while the SMs of the MMCs are temporarily bypassed, a substantially lower fault current is produced. In particular, the results show that the bypassing of MMCs significantly reduces the interrupted current and the absorbed energy if the coordinated operation is activated. Moreover, the arm currents are kept small during operation and hence the overcurrent protection of SMs will not be triggered.

The proposed coordination scheme constitutes a promising alternative to protect HVDC grids by interrupting dc fault currents at a significantly reduced magnitude without additional costs. By achieving this, a significant reduction in the current rating of dc protection devices may be possible.

Future work needs to be carried out on the back-up protection for the proposed coordination scheme, where malfunction of MMC and DCCBs is considered and solutions are provided to avoid damages to the dc protection devices.

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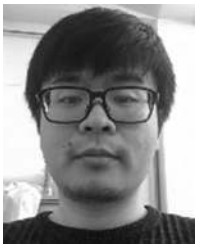

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