Copper-Encapsulated Silicon Micromachined Structures

J.-L. Andrew Yeh, Hongrui Jiang, Hercules P. Neves, *Member, IEEE*, and Norman C. Tien, *Member, IEEE*

***Abstract*—Selective copper encapsulation on silicon has been used to fabricate micromachined devices such as inductors with quality factors over 30 at frequencies above 5 GHz. The devices are fabricated using either polysilicon surface micromachining, or integrated polysilicon and deep reactive ion etching bulk silicon micromachining. Their exposed silicon surfaces are selectively activated by palladium activation, which allows the subsequent copper deposition on the activated silicon surfaces only. This silicon-encapsulated-with-copper technique takes advantage of both the excellent mechanical properties of silicon (to maintain structural integrity), and the high conductivity of copper (for electrical signal transmission). Furthermore, the process not only minimizes interfacial forces typical of physical metal deposition on silicon, but also balances the forces by metal encapsulation on all sides of the silicon structures. [498]**

***Index Terms*—Conformal metal deposition, DRIE bulk silicon micromachining, electroless copper plating, integrated polysilicon, metal encapsulation, selective metal deposition, quality factor.**

I. INTRODUCTION

HIGHLY conductive metals are usually required to improve the electrical quality factors (Q) of micromachined devices such as capacitive sensors, microrelays/switches, RF passive elements, and through-hole interconnects [1]–[8]. The high-Q factors can only be achieved with metals that reduce the output impedence in capacitive sensors, the contact resistance in microrelays, the insertion loss in microswitches, or the series resistance in RF elements. High-Q devices are commonly fabricated using metal surface micromachining or silicon micromachining with metals sputtered or evaporated on top. However, there are manufacturing challenges in stress control on metal surface micromachined structures. In addition, thermal expansion mismatch occurs in the silicon micromachined structures where metal films are deposited on top of silicon.

Metal surface micromachining has been used to fabricate devices such as mirrors, switches, inductors, and tunable capacitors [4], [7], [9]–[11]. In general, the technology has constraints on the size of feasible devices for practical applications because of warping on metal films [7]. The warping can result from various factors, including stress gradients, internal stresses, and thermal expansion mismatches between metals and sacrificial materials such as photoresist, polyimide, and oxide. Stress gradients in metal films (structures) result in either wavy or curved metal surfaces. Compressive internal stresses may lead to buckling on clamped–clamped structures. Thermal expansion mismatch between clamped–clamped structures and the underlying sacrificial layers results in interfacial forces. Removing the sacrificial layers would induce forces on the structures as they relax, but are still restricted by the anchors.

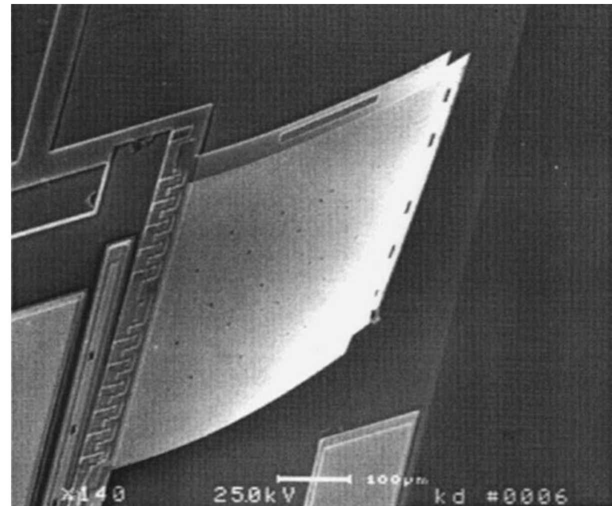

Fig. 1. Hinged membrane bent due to thermal expansion mismatch between gold and polysilicon. 0.5-μm Au is deposited on a 2-μm polysilicon membrane. This SEM picture is taken before annealing.

Compared to the majority of metal surface micromachinings, silicon micromachinings are more mature technologies. Polysilicon surface micromachining has demonstrated the ability to create not only large-size low-stress structures, but also complex multiple-level devices. deep reactive ion etching (DRIE) bulk silicon micromachining can produce high-aspect-ratio structures out of a single-crystal silicon substrate. The drawback is that silicon has a high electrical resistivity, although it can be minimized by depositing metals on the silicon through evaporation or sputtering. However, the resulting bimorph metal/silicon structures tend to warp due to thermal expansion mismatch (see Fig. 1). In addition, buckling may occur in DRIE bulk silicon micromachined structures because of compressive thermal stress in metal/oxide/silicon

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sandwich structures (SCREAM process) and in metal/silicon bi-layer structures (SOI process) [12], [13]. The thermal stress can be estimated by

$$\sigma = f_s \frac{E}{1-v} \Delta\alpha \Delta T$$

where ΔT is the temperature difference between the room and deposition temperatures and $\Delta\alpha$ is the difference of the thermal expansion coefficients between metal and the surrounding material. E and v are the Young's modulus and Poisson's ratio of metal, respectively. The term f_s is a constant factor that depends on the geometry and elasticity of each material [14].

To take advantage of both the electrical properties of metals and mechanical properties of silicon, a technique to selectively encapsulate silicon micromachined structures with copper is proposed. Electroless copper deposition with selective activation on silicon surface is applied for metallization on all sides of silicon micromachined structures [15]–[21]. Palladium is used to selectively activate silicon and not insulation layers (including silicon nitride and silicon dioxide) in preparation for subsequent copper deposition [18]. Using this technique, some fabrication difficulties of metal surface micromachining are overcome, and the stresses induced by bimorph metal-on-silicon structures are minimized and are further balanced due to metal encapsulation on the silicon structures. This process of encapsulating silicon with copper (see Fig. 2) keeps the mechanical properties of silicon and the electrical properties of copper, and minimizes thermal stresses in the structures due to low-temperature copper deposition. Furthermore, the encapsulation also balances any stresses that may arise across the metal–silicon interface.

Silicon has been widely used in the microelectromechanical systems (MEMS) field as well as in the integrated-circuit (IC) industry. The mechanical properties of silicon (including polysilicon) have been extensively studied; thus they are more controllable than those of the majority of metals that are used in metal surface micromachining. Copper has a higher conductivity than aluminum that makes it attractive for high-Q elements. The mechanical stresses in electroless-plated copper are lower than those in evaporated films [22]. This method is compatible with silicon IC fabrication, as copper is currently used in IC interconnects. Using this technique, one obtains the merits of both fabrication methods while avoiding their drawbacks.

II. Basics of Selective Electroless Copper Plating

Electroless copper deposition can be performed on a catalytic surface due to anodic oxidation of a reducing agent and cathodic reduction of copper ions. Catalytic metal (palladium) activates the silicon surface through the mechanism of contact displacement, while the surfaces of silicon dioxide and silicon nitride remain inert. The contact displacement deposition (also known as immersion deposition, galvanic deposition, conversion, etc.) is a reaction in which electrons are supplied not by an oxidation (as in electroless deposition), but by the substrate itself [23]. Since silicon is not thermodynamically favorable for the initiation of electroless copper deposition, contact displacement deposition

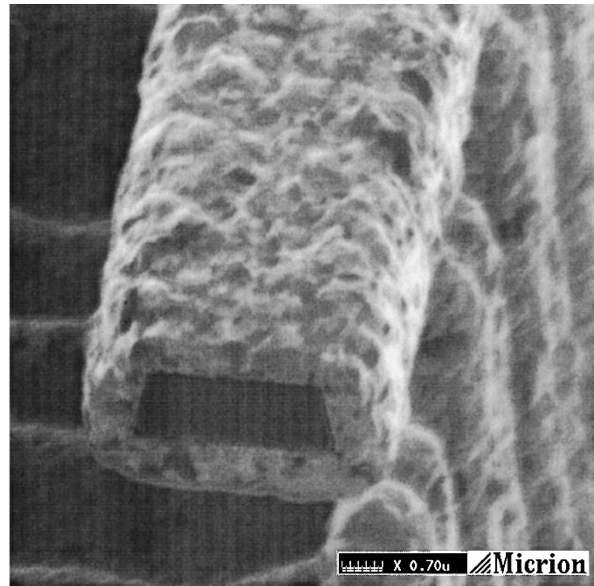
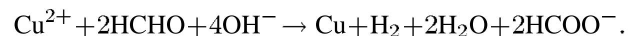


Fig. 2. Copper encapsulation of a 1.5-μm-thick polysilicon freestanding beam. Approximately 1-μm of copper is deposited on the whole surface of polysilicon. The beam is cut using focus ion beam (FIB).

of palladium is done to form a seed layer where the electroless process can begin.

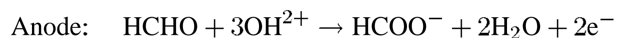
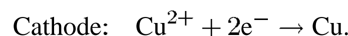
The palladium activation creates catalytic sites (nucleation centers) on the silicon surface, enabling subsequent electroless copper deposition. The activation bath consists of diluted HF (100–250 ml/L), which removes the native oxide on the silicon surface at the etch rate of less than 100 nm/min. Typically, HF is present at such high concentrations; i.e., the etching is usually faster than the palladium nucleation process, which is needed for an adequate electron exchange between the substrate and reducing reaction. The diluted HF has no impact on the electrical isolation because silicon nitride and/or buried silicon dioxide of SOI wafers are used as insulators.

The plating process is autocatalytic; in other words, the deposition continues once it starts. Using formaldehyde as the reducing agent, the main reaction of copper deposition can be expressed as [24]



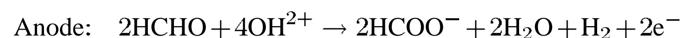
$$Cu^{2+} + 2HCHO + 4OH^- \rightarrow Cu + H_2 + 2H_2O + 2HCOO^-.$$

The electrochemical mechanism can be resolved into the following two steps, which take place simultaneously at two electrodes. Initially, the copper deposition occurs at the palladium surface [25]

$$\text{Anode:} \quad HCHO + 3OH^{2+} \rightarrow HCOO^- + 2H_2O + 2e^-$$
$$\text{Cathode:} \quad Cu^{2+} + 2e^- \rightarrow Cu.$$

On the deposited copper surface, the reaction at the anode becomes



$$\text{Anode:} \quad 2HCHO + 4OH^{2+} \rightarrow 2HCOO^- + 2H_2O + H_2 + 2e^-$$

with hydrogen being produced [26].

The electroless copper plating bath composition used in this paper consists of a cupric salt [5-g/l $CuSO_4 \cdot H_2O$), a reducing agent (5-ml/l HCHO), and a complexing agent

(15-g/l Ethylenediaminetetraacetic acid (EDTA)]. Potassium hydroxide is added to adjust the plating bath pH value to 12–13. Additives to the deposition solutions are surfactant RE610, brightener 2,2′-dipyridyl and surfactant Triton X-100.

RE-610 is proprietary surfactant, which consists of a nonionic surfactant (ethoxylated nonyl phenol) associated with an anionic surfactant (phosphate ester). Its role is to increase the wettability of the substrate by reducing surface tension, making the copper surface smooth and shining. Like all surfactants, it is at higher concentration at the liquid/solid interface than at the bulk of the solution (known as *adsorption*) [27]. 2,2′-Dipyridyl works as a brightening agent; it causes the randomization of the crystal growth and, therefore, reduces the roughness average. Triton X-100 consists of octoxynol-9, which acts as a leveling agent (i.e., it allows a more efficient filling of crevices and trenches). It reduces the defect density and enhances the electrical uniformity of Cu films.

III. Device Fabrication

The devices were fabricated at the Cornell Nanofabrication Facility (CNF), Cornell University, Ithaca, NY, using silicon-based micromachining technologies including polysilicon surface micromachining [28] and integrated polysilicon and DRIE bulk silicon micromachining [29]. The fabrication processes used to manufacture the demonstration devices for copper plating are described as follows.

A. Polysilicon Surface Micromachining

The process begins with the passivation layers on p-type silicon wafers including 0.5-μm thermal oxide and 0.2-μm low-stress low-pressure chemical vapor deposition (LPCVD) nitride. This is followed by the deposition of a 0.5-μm LPCVD p-type boron-doped polysilicon film that acts as an electrical ground layer. This layer is lithographically patterned and then etched by a chlorine-based reactive-ion etch (RIE). Next, a 2-μm low-temperature oxide (LTO) is deposited at the temperature of 400 °C as the first sacrificial layer, which is to be removed at the end of the process to free the first structural polysilicon layer. Dimples and anchor openings are lithographiclly transferred into the sacrificial layer with a CHF_3-based plasma etcher.

Another 2-μm *in situ* boron-doped polysilicon layer is deposited and functions as the first structural material (poly1). An annealing step is performed at 1000 °C for1 h in N_2 to reduce the residual stresses built in the poly1, which is subsequently etched using oxide as a hard mask. A second LTO sacrificial layer of a thickness 1.2 μm is deposited and etched for the formation of anchor openings and poly1–poly2 vias. The last step of fabrication is to deposit, pattern, and etch the second structural layer (poly2), which is made of a 2-μm-thick p-type polysilicon layer.

B. Polysilicon Surface Micromachining Structures with Deep Cavities in Bulk Silicon

The process starts with a 600-nm-thick silicon nitride deposition on a bare silicon wafer as the isolation layer [30]. Next, sacrificial oxide blocks that define the cavities are created in the silicon substrate. These are created via the following steps: etching 30-μm-deep narrow beams using DRIE, thermally oxidizing the beams, and filling the trenches between the oxidized beams with silicon dioxide, and planarizing the rippled oxide surface with chemical mechanical polishing (CMP). A 1-μm LPCVD oxide layer is deposited, in which anchor openings are patterned and etched. The anchors allow polysilicon structures to be fixed onto the nitride isolation layer on top of the stationary silicon chunk. The subsequent polysilicon surface micromachining follows the same procedure as described in Section III-A.

C. Integrated Polysilicon Surface and DRIE Bulk Silicon Micromachining

The integrated polysilicon surface and DRIE bulk silicon micromachining is distinct from regular silicon wafers used as substrates in the process described in Section III-B [29]. The integrated silicon process begins with a silicon-on-insulator (SOI) wafer that has a top silicon layer of 20 μm and a buried oxide of 1 μm. The procedure for the formation of oxide blocks is the same as that in Section III-B. The oxide blocks transform unwanted silicon into silicon dioxide, which is removed during the HF release. CMP used in the formation of the oxide blocks creates a flat substrate surface for the following polysilicon surface micromachining in Section III-A. Finally, a deep silicon etch using the Bosch process is performed to define the structures from the single crystal silicon.

IV. Copper Plating

Post-processing following the fabrication of the samples primarily consists of HF release, copper metallization, and self-assembly monolayer (SAM) coating. The silicon micromachined structures are released in a 49% aqueous HF bath, which etches away the sacrificial oxide and oxide blocks. The samples are rinsed with de-ionized (DI) water. Prior to the wet palladium activation, the samples are bathed in DI water to prevent stiction, which may pull structures onto the substrate and cause them to stick once the samples are dried.

Next, the samples are transferred and lay immersed in a palladium solution for one minute at a temperature between 20°C–40 °C. Palladium ions selectively activate the exposed silicon on all sides of structures and enable the autocatalytic electroless copper deposition. During the activation, both the sacrificial (oxide) and passivation layers (nitride) remain inactive to the palladium ions. Right after the activation, samples are immersed in a copper plating solution bath where the solution is agitated at 100–300 r\min at a temperature between 55 °C–66 °C. Upon completion of the deposition, samples are coated with a self-assembled monolayer of octadecyltrichlorosilane (C^{18} OTS) in a process developed by Houston *et al.* [31]. The monolayer that coats the silicon structures eliminates the stiction and slows copper corrosion.

V. Device Demonstration

A. Selectivity

Fig. 3 shows that copper selectively deposits on silicon, but not on standard silicon nitride after 10 min of deposition. The 1-μm-thick electroless copper was conformally deposited on all the exposed surfaces of the polysilicon structures that are 2-μm

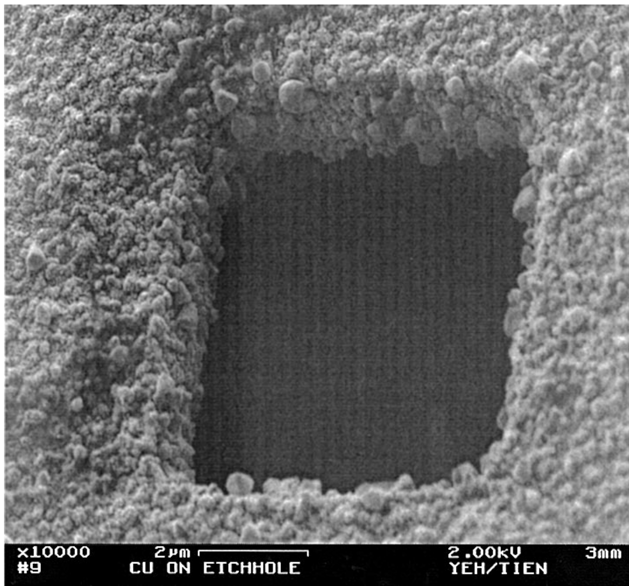


Fig. 3. Electroless deposited copper around an etch hole. A standard silicon nitride underneath the etch hole is inert to both palladium activation and copper deposition.

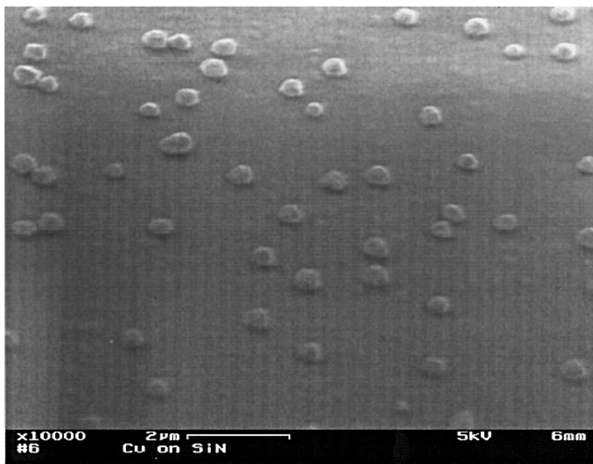


Fig. 4. Copper precipitation on low-stress silicon nitride.

thick. Some copper precipitation, shown in Fig. 4, is observed on top of the low-stress silicon nitride that is rich of silicon. However, the copper does not compromise electrical isolation. Palladium activation does not generate seed layers on the low-stress nitride, although the silicon rich nitride provides a favorable environment for the formation of copper nuclei in comparison to the stoichiometric nitride. Empirically, the precipitation can be removed by dipping samples in an aqueous HF solution for a couple of seconds. Alternatively, increasing the activation energy or required nuclei size of crystallization can reduce possibility of precipitation. Like nitride, oxide is also inactive to copper deposition (see Section V-B).

B. Selective Pattern

Copper may also be selectively deposited in only certain regions on the chip (see Fig. 5). A photolithography step is used to open areas from 5 μm $\times$ 5 μm to 1 mm $\times$ 1 mm where copper is to be deposited. Using photoresist as a mask, the oxide in the

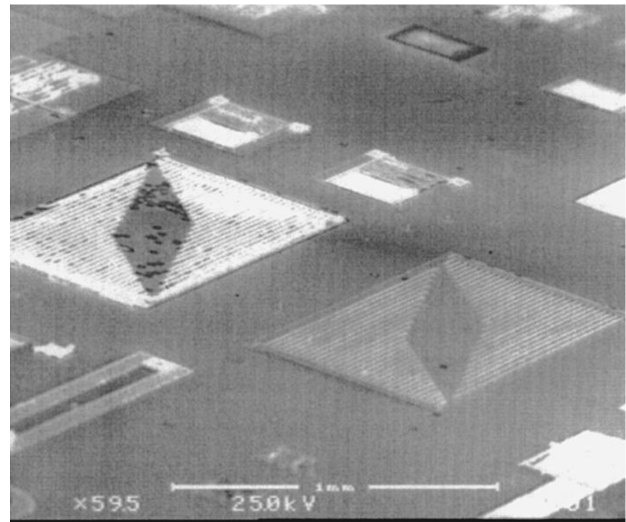


Fig. 5. Selective deposition of copper on structures in desired areas on the chip. The bright structures are where copper has been deposited on polysilicon.

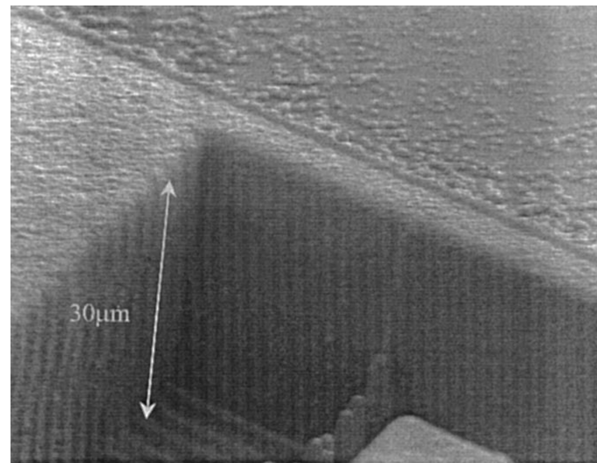


Fig. 6. Conformal copper deposition on a silicon cavity of depth 30 μm. Some copper precipitation occurs on the low-stress nitride.

window areas to be opened are wet etched using buffered HF (BHF). After the BHF release, the photoresist is removed and copper deposition is performed. The sacrificial oxide prevents the copper from depositing anywhere, except the released silicon regions. Due to lateral etch of BHF release, the minimum feature that has been resolved for copper deposition is around 10 μm $\times$ 10 μm.

C. Conformal Metal Coverage

Fig. 6 shows that copper is conformally deposited on the sidewalls and ground planes of a cavity of depth 30 μm in the silicon substrate. The copper coating on the silicon substrate can be used to minimize the substrate loss due to the high resistivity of silicon. Fig. 7 shows that the interconnection (via) between two polysilicon layers has been conformally coated with copper. Copper deposition on the undercut region between the two polysilicon layers allows electrical signals pass from the upper polysilicon layer to the lower layer through a continuous copper skin. The intrinsic nature of electroless deposition makes it possible for plating copper on high-aspect-ratio structures.

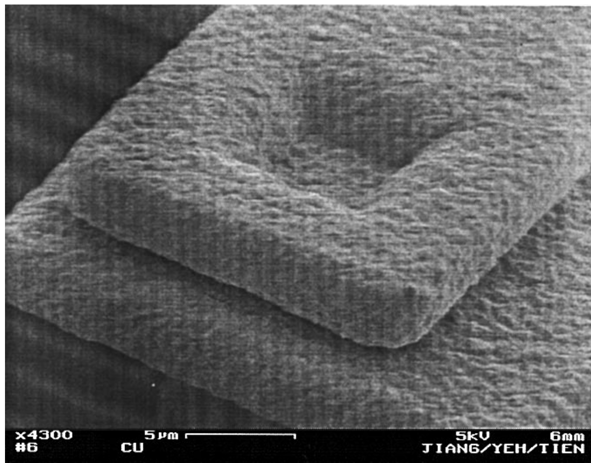


Fig. 7. Copper conformally deposits on all sides of the interconnection between two polysilicon layers including the backside and the undercut region.

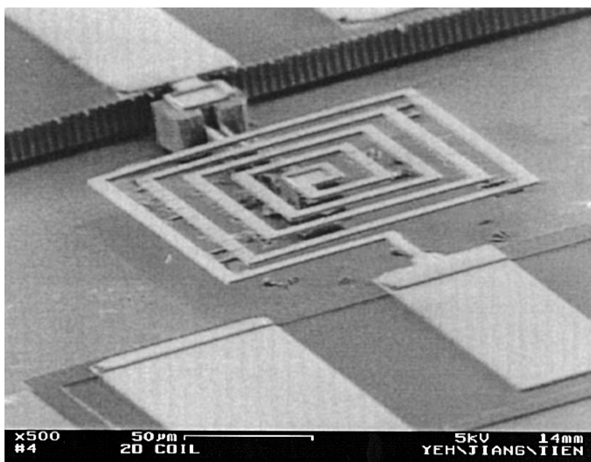


Fig. 8. Silicon micromachined structure of large topography for copper plating.

D. Topography

The selective copper plating is particularly useful for free-standing structures and complex structures with large topography (see Figs. 3 and 8). The need for a metal photolithography step over a large topography can be avoided. Etching or liftoff of the metal is not required because the copper only deposits on the layers that are activated (which, in this case, is polysilicon and not isolation layers such as nitride and oxide). Fig. 9 shows that this technique is capable of filling copper into the 1-μm-wide gap between two suspended polysilicon beams of thickness 2 μm at the temperature of 60 °C.

One possible application of this technique to is metallize a through-hole interconnection. Fig. 10 shows an SEM photograph of one end of a preliminary through-hole interconnect that consists of copper, 300-nm n^+-doped polysilicon and 830-nm oxide in addition to silicon substrate. The breakdown voltage of the interconnect is measured to be 200 V. The method has also been used to deposit copper on both sides of a hinged plate (see Fig. 11) before it was rotated out of the surface. The plate, which has 5 μm $\times$ 5 μm holes with spacing of 30 μm apart, was initially 2 μm above the nitride layer. At a deposition rate

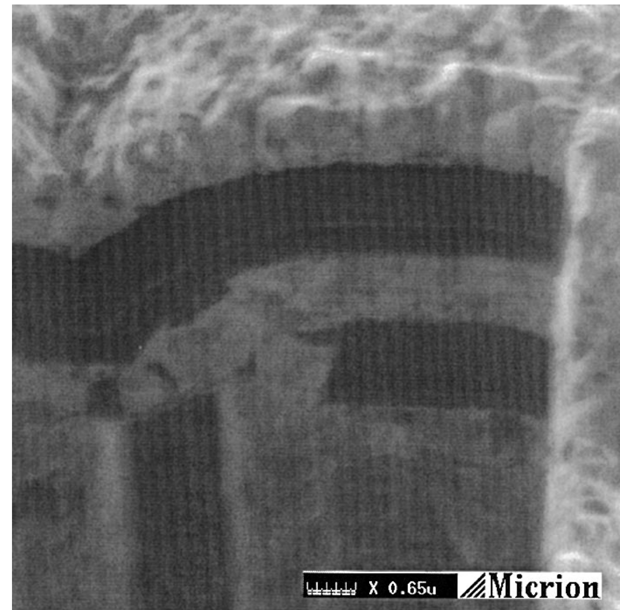


Fig. 9. Copper filling the gap between two polysilicon beams.

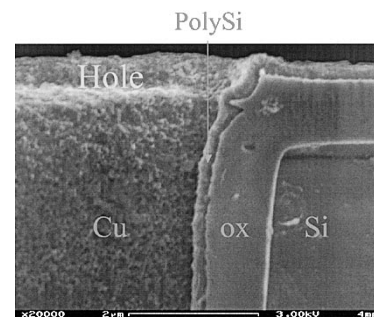


Fig. 10. One end of a through-hole interconnect that consists of copper, polysilicon, silicon dioxide, and a silicon substrate.

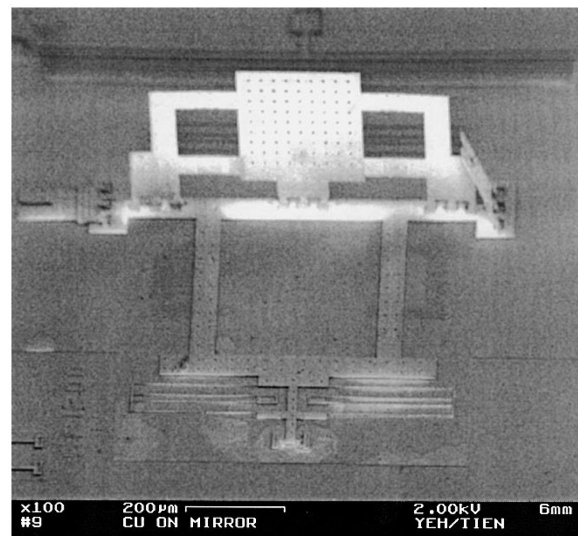


Fig. 11. Backside of a flipped-up hinged polysilicon plate encapsulated in copper.

of 100 nm/min (at 80 °C) for 2 min, copper aggregates are randomly generated within 5 μm around etch holes on the backside of the plate. The quality of the backside deposition is mainly due

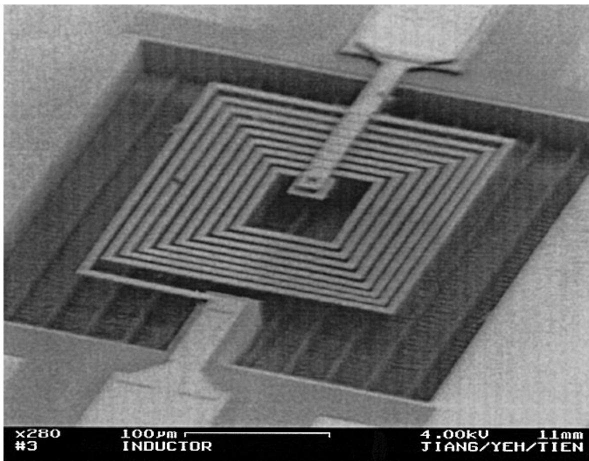


Fig. 12. High-Q silicon micromachined suspended spiral inductor encapsulated with copper.

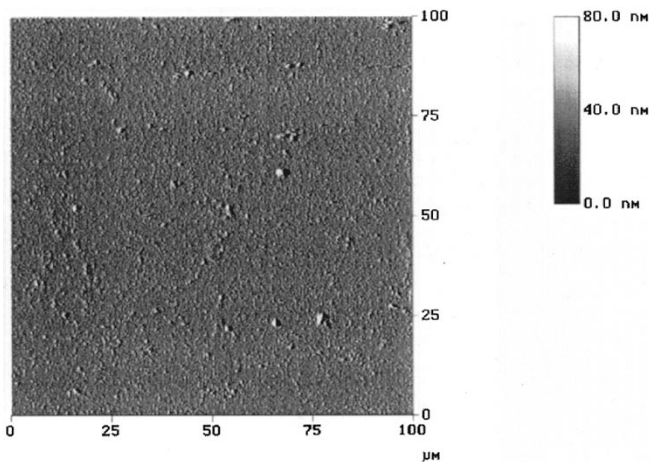


Fig. 13. AFM surface scan of a sample with 0.5-μm-thick copper on it. The large copper bumps are caused by dust in the laboratory.

to the limited amount of palladium and copper ions transported into the gap of 1.5 μm between the backside of the plate and substrate.

E. Inductor

This silicon-encapsulated-with-copper process is used to fabricate suspended spiral inductors (see Fig. 12). We have previously reported that the inductors have measured inductances of 2–12 nH and Q factors over 30 at 5 GHz [30]. In these inductors, the spiral coils are suspended above the silicon substrate by 30 μm in order to minimize the parasitic capacitance between the coils and substrate. The coils are made of 2-μm polysilicon and encapsulated with 1.5-μm electroless copper on all the surfaces of the coils. In this design, the polysilicon bearing the mechanical loading provides structural rigidity and the copper transmitting the electrical signals minimizes series resistance. The sidewalls and bottom plane of the cavity are also coated with copper, thus providing a low-resistance electrical ground line and electromagnetic shield to eliminate the effects due to the lossy silicon substrate.

VI. Characteristics of Copper

The characteristic measurements we have performed are resistivity, deposition rate, and roughness. The copper resistivity (deposited at 66 °C) is measured to be 2.1 $\mu\Omega \cdot$ cm with a Prometrix four-point probe instrument. The deposition rate is found to be 55 nm/min at the temperature of 66 °C. The surface morphology of the copper can be seen from an atomic force microscope (AFM) image of a sample with 500 nm of copper deposited (see Fig. 13). The rms surface roughness of the copper was measured to be approximately 20 nm over an area of 100 $\times$ 100 μm^2 using the contact mode of the AFM.

VII. Conclusion

The encapsulation of freestanding silicon structures with selectively electroless-plated copper will allow silicon to be used in MEMS applications that require high conductivity. This method uses silicon as the structural material and copper for electrical signal transmission, and is particularly beneficial in fabrication of high-Q devices. The activation agent (Palladium) initiates the electroless copper deposition only on silicon and not on isolation materials such as nitride and oxide, eliminating the need for metal lithographic patterning. Thus, this method simplifies the metallization of silicon micromachined structures, especially ones with large topography.

Since electroless copper deposition is a low-temperature process, thermal expansion mismatch between silicon and copper is negligible. Using this method, copper is deposited on all exposed surfaces of silicon, thus, the residual stress in copper on one side is apt to balance that on the opposite side. Furthermore, copper deposition has high conformality on the silicon surface, enabling metallization of high-aspect-ratio structures and complex structures with a variety of features.

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