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Research Article

CORDIC-Based Multi-Gb/s Digital Outphasing Modulator for Highly Efficient Millimeter-Wave Transmitters

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This paper describes a high-speed CORDIC-based digital outphasing modulator. Fixed-point Matlab model of the outphasing modulator is developed to evaluate the system performance and define the circuit design parameters. Design issues such as signal quantization error, delay mismatch, and phase overflowing are addressed to enable hardware implementation. The complete outphasing modulator is fully custom designed in 40 nm CMOS, which can be integrated in a millimeter-wave outphasing transmitter to enhance the system average efficiency. Tested with 10.56 Gb/s 64-QAM, this work achieves an EVM of 3.2% and fulfils the IEEE 802.11ad spectral mask requirements.

1. Introduction

Linearization and efficiency enhancement techniques are always the focus in the design of power amplifiers (PAs) [1]. Figure 1 shows the characteristics of a typical linear PA. The PA only achieves the peak power-added efficiency ($\mathrm{PAE}_{\mathrm{MAX}}$) near its saturated output power (P_{SAT}). However, due to the high peak-to-average power ratio (PAPR), the PA has fairly low average output power (P_{AVG}) and average power-added efficiency ($\mathrm{PAE}_{\mathrm{AVG}}$). Note that the PDF represents the probability density function of the complex modulated signals. At millimeter-wave frequencies (mm-Wave), such issue becomes even more severe as the transistor operates at a large fraction of the f_T/f_{MAX} [2]. Therefore, the key challenge of mm-Wave multi-Gb/s transmitter (TX) is the poor average efficiency when transmitting complex modulated signals (e.g., 64-QAM).

The outphasing PA achieves linear amplification using highly efficient nonlinear PAs [3, 4], potentially alleviating the linearity/efficiency trade-off issue. The concept of outphasing is shown in Figure 2 with the phasor diagram of the outphasing vectors (i.e., $S_1(t)$ and $S_2(t)$) and combined signal (i.e., $S(t)$). The signal component separator (SCS) is employed to generate the $S_1(t)$ and $S_2(t)$ based on $S(t)$ [5]. The magnitude of the $S(t)$ depends on the outphasing angle $\varphi(t)$. As a result, the outphasing PA can achieve high linearity and high efficiency simultaneously. The work in [6] first time presents the fully integrated outphasing transmitter front-end at mm-Wave. It shows that even at mm-Wave the outphasing TX is able to perform linear amplification using switching or saturated power amplifiers (PAs), achieving nearly two times better average efficiency [6] than that of a conventional I/Q TX. Therefore, it is essential to develop a high-speed outphasing modulator to facilitate a fully integrated outphasing TX [7, 8]. The work in [9] presents an outphasing TX for 2.4-GHz WLAN with a delay-based phase modulator. However, it may require a delay resolution of 0.1 ps for a phase resolution of 2° when operating at 60 GHz and inevitably consumes high power. The work in [10] presents a digital outphasing modulator based on piece-wise linear functional approximation, but its speed will be limited if high-order modulation (e.g., 64-QAM) is applied due to the increased memory size of the look-up tables (LUTs) in the system.

In this paper, we report a fully custom designed digital outphasing modulator in 40 nm CMOS. Coordinate rotation digital computer (CORDIC) [11] is employed to realize the conversion between Cartesian and Polar coordinates, and different trigonometric functions. Issues such as signal quantization error, delay mismatch, and phase overflowing are

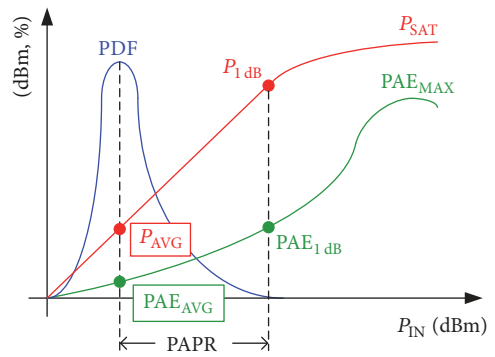

Figure 1: Characteristics of a typical linear PA.

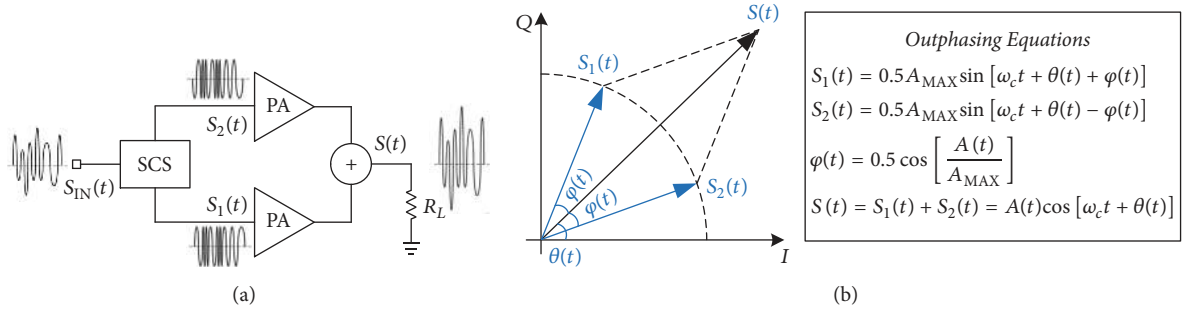

Figure 2: Outphasing system: (a) architecture and (b) phasor diagram.

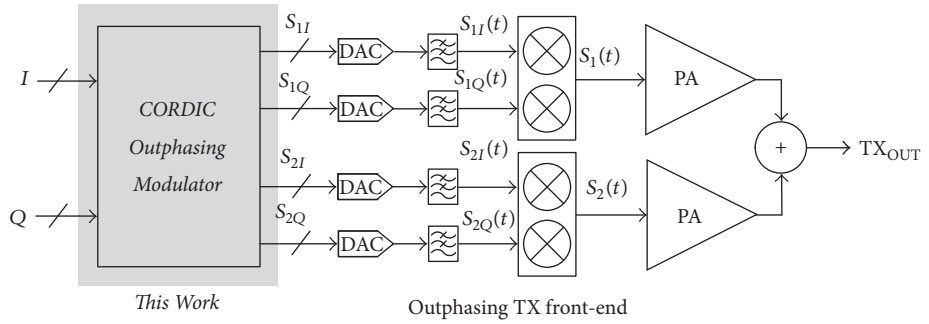

Figure 3: System architecture of the complete outphasing transmitter.

tackled to facilitate hardware implementation. The proposed outphasing modulator achieves simulated 10.56 Gb/s 64-QAM with an error-vector-magnitude (EVM) of 3.2% and fulfils the IEEE 802.11ad spectral mask requirements for 60 GHz communications. Section 2 describes the system architecture of the outphasing transmitter while Section 3 details the proposed CORDIC-based outphasing modulator. The circuit-level implementation and simulated results of the outphasing modulator are presented in Section 4 with the conclusion given in Section 5.

2. Outphasing Transmitter System Architecture

Figures 3 and 4 show the system architecture and phasor diagram of the outphasing transmitter where $A(t)$, $\theta(t)$ are the amplitude and phase modulated signals, respectively, and outphasing angle $\varphi(t)$ equals $\cos^{-1}[A(t)/A_{MAX}]$. The CORDIC-based outphasing modulator is tasked to generate the four multi-GHz digital baseband signals S_{1I}, S_{1Q}, S_{2I}, and S_{2Q}. They are converted to their analog counterparts $S_{1I}(t)$, $S_{1Q}(t)$, $S_{2I}(t)$, and $S_{2Q}(t)$ through high-speed digital-to-analog converters (DACs), and up-converted by quadrature modulators to construct the desired outphasing signals $S_1(t)$ and $S_2(t)$ at the input of the two switching PAs. The linear amplification can be achieved at TX output by vectoring summing two outphasing signals.

It is seen that the outphasing TX requires 4 DACs, 4 reconstruction filters, and 2 I/Q modulators, twice as much as that of the conventional I/Q TX. However, the linearity requirement of these analog baseband circuits is relaxed due to the low peak-to-average-power ratio (PAPR) of the

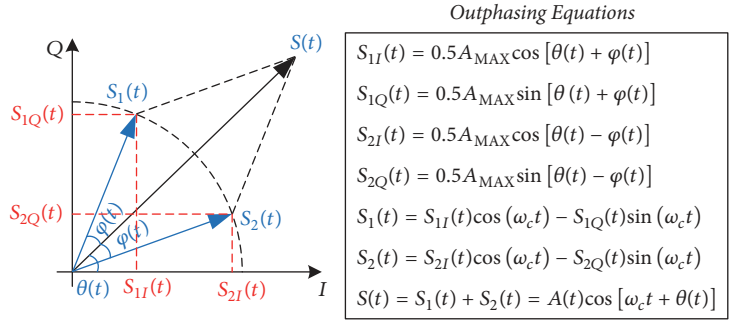

Figure 4: Phasor diagram of the outphasing transmitter with baseband signal decomposition.

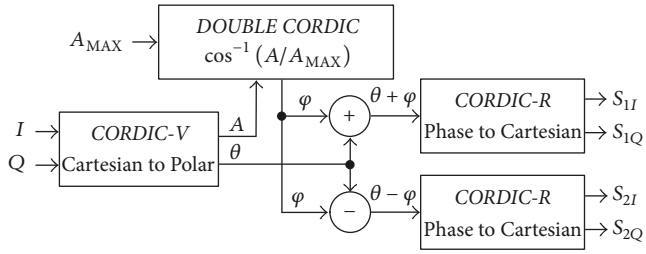

Figure 5: CORDIC-based outphasing modulator system diagram.

outphasing baseband signals [6]. Considering that the dc power of DAC is in exponential proportion to its linearity, the proposed outphasing system has no dc power penalty in its analog baseband circuits. In addition, prior-art 60 GHz outphasing TX front-end achieves 15% average efficiency for 16-QAM signals while conventional I/Q TX only has 7%. For a typical 60 GHz PA with 100 mW average output power for transmitting 16-QAM, the outphasing and IQ TXs consume 0.67 and 1.43 W, respectively. Depending on the data rates, the dc power of the proposed outphasing modulator varies between 30 and 150 mW, which gives outphasing TX huge efficiency benefit. Such benefit will be more pronounced for 64-QAM due to the increased PAPR.

3. CORDIC-Based Outphasing Modulator

CORDIC is a fast and efficient algorithm to compute common mathematical functions [11] as it only requires "add," "subtract," and "shift" operations. It is fully utilized in this work to realize high-speed outphasing modulator. Figure 5 shows the system diagram. The vectoring mode of CORDIC (CORDIC-V) is used to convert the input (I, Q) signals to the polar form (A, θ) while the rotation mode of CORDIC (CORDIC-R) is to transform the phase signals $\theta \pm \varphi$ to the four outphasing baseband signals. The most critical part of the outphasing modulator is to realize $\cos^{-1}(x)$ function. The double CORDIC iterations [11, 12] are utilized in this work to compute $\cos^{-1}(x)$, which is also straightforward to implement in circuitry.

The fixed-point model of the outphasing modulator is developed in Matlab to evaluate the performance and define the circuit design parameters. In the simulation, the outphasing TX front-end (see Figure 3) is assumed to be ideal. For hardware implementation, it is essential to determine the number of CORDIC iterations (i.e., CORDIC pipelined stages) and truncate the signals to balance the accuracy, speed, latency, and power consumption. Simulations indicate that CORDIC iterations have relatively minor impact on the system performance and eight iterations are sufficient to perform the coordinate conversions and to compute $\cos^{-1}(x)$. Quantization of each signal greatly degrades EVM and results in spectral regrowth. Regarding the number of bits required by the outphasing modulator, the limiting factor is the $\cos^{-1}(x)$ double CORDIC block, but it is reasonable to set all the CORDIC blocks with the same word length without sacrificing the speed. Tested with 10.56 Gb/s 64-QAM signals (PAPR = 7.6 dB, root-raised cosine filter with a roll-off factor of 0.35), Figure 6 shows the simulated EVM and adjacent-channel-leakage ratio (ACLR). It is observed that when the number of bits equals 10, the EVM and ACLR flatten out to 2% and −60 dBc, respectively. It leaves sufficient margin and can be budgeted for other implementation nonidealities. To simplify the input interfacing and reduce DAC resolution, the input I/Q signals and the four outphasing signals (i.e., S_{1I}, S_{1Q}, S_{2I}, and S_{2Q}) are truncated to 8 and 7 bits, respectively. Simulation predicts that the performance degradation is negligible.

4. Circuit Implementation and Simulation Results

Based on the system design and simulation, all the building blocks of the CORDIC-based outphasing modulator are

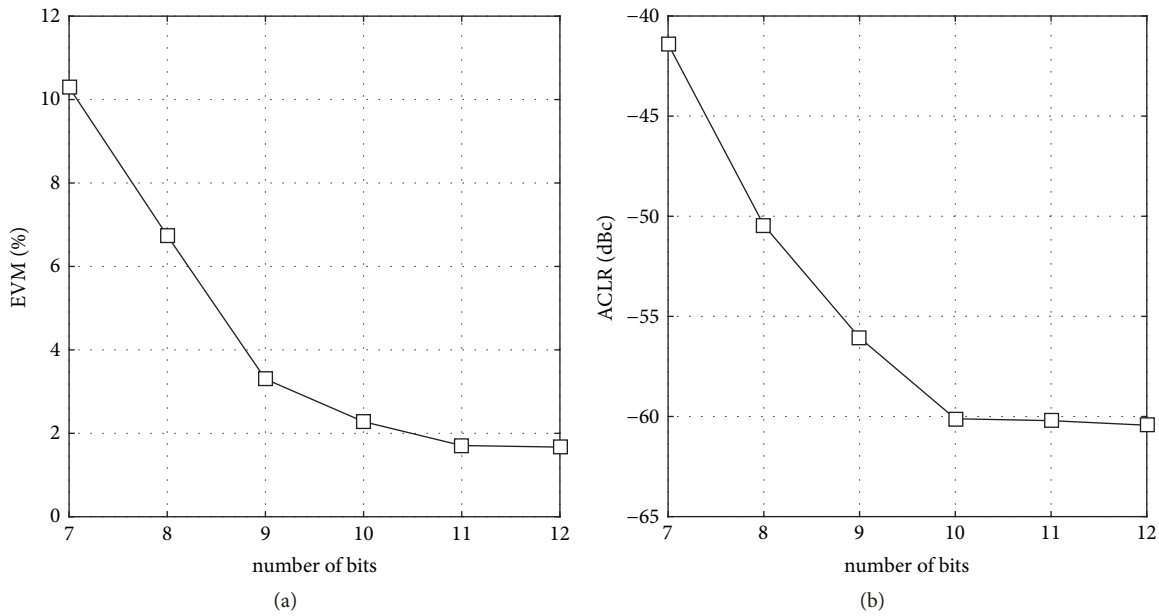

Figure 6: Simulated (a) EVM and (b) ACLR versus number of bits of the outphasing modulator.

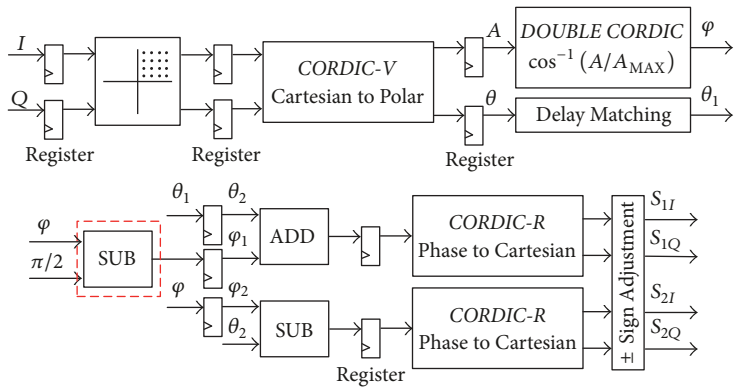

Figure 7: Top-level schematic of the CORDIC-based outphasing modulator.

migrated to the circuit level. The design is implemented in 40 nm CMOS. Figure 7 shows the top-level schematic of the outphasing modulator. In practice, the CORDIC-V and CORDIC-R only work properly when the phase of input I/Q signals is between $-\pi/2$ and $\pi/2$, so the input I/Q signals are first transformed to the first quadrant. It is feasible thanks to the symmetrical characteristics of trigonometric functions. The resulting sign issue can be easily resolved by using flag signals and recovering the "±" sign for S_{1I}, S_{1Q}, S_{2I}, and S_{2Q} at the output of the outphasing modulator. Simulation predicts that $\theta + \varphi$ may be larger than $\pi/2$. To tackle this overflowing issue, we subtract the phase by $\pi/2$ (i.e., the block in the red dashed box) and set $S_{1I} = 0.5 \cdot A_{\mathrm{MAX}} \cdot \cos(\theta + \varphi - \pi/2) = 0.5 \cdot A_{\mathrm{MAX}} \cdot \sin(\theta + \varphi)$, $S_{1Q} = 0.5 \cdot A_{\mathrm{MAX}} \cdot \sin(\theta + \varphi - \pi/2) = -0.5 \cdot A_{\mathrm{MAX}} \cdot \cos(\theta + \varphi)$. A_{MAX} is set to 1. In this design, when the input signal is small (i.e., $|x| < 0.2$), $\sin(x)$ and $\cos(x)$ are approximated by the linear functions, given by $\sin(x) = x$ and $\cos(x) = 1 - |x|/8$, which are more efficient than CORDIC-R. The delay matching block and all the registers are used to balance the latency in the signal paths.

It can be seen that the adder and the subtractor are the most critical blocks in CORDIC as well as in the complete outphasing modulator (see Figure 7), which determine the speed and power consumption. In this work, the full adder is realized by double pass-transistor logic (DPL) [13] which features relatively fast speed compared to mirror adder and complementary pass-transistor logic (CPL) adder [14] while still achieves full signal swing even at low supply voltage, as shown in Figure 8. In the design of the DPL adder, the speed of the circuit has been paid more attention. The optimum transistor size is selected upon which the delay of the critical path in the adder is minimized. In addition, the carry-select topology [14] is applied to minimize the delay of the critical path where the 10-bit adder in the $\cos^{-1}(x)$ block is split into

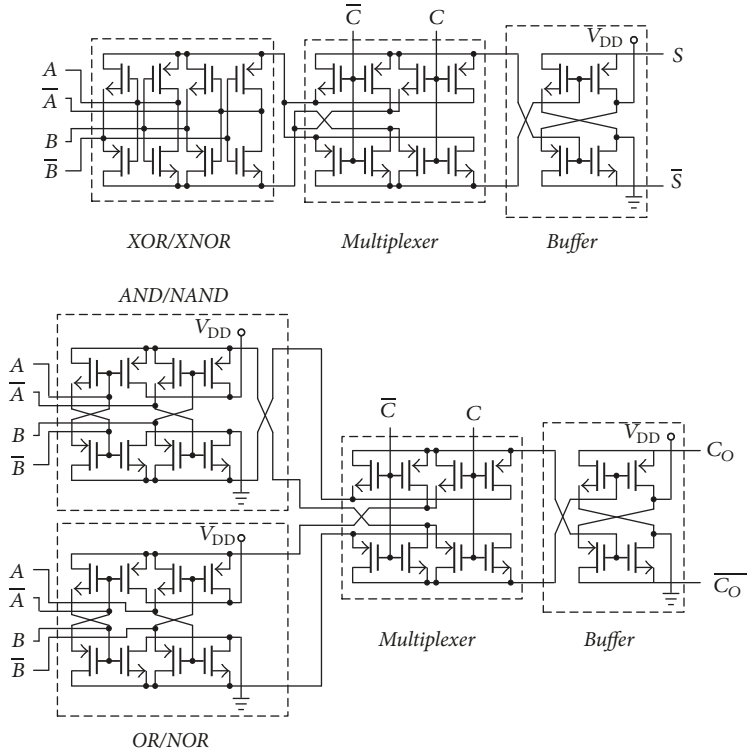

Figure 8: Schematic of full adder realized by double pass-transistor logic.

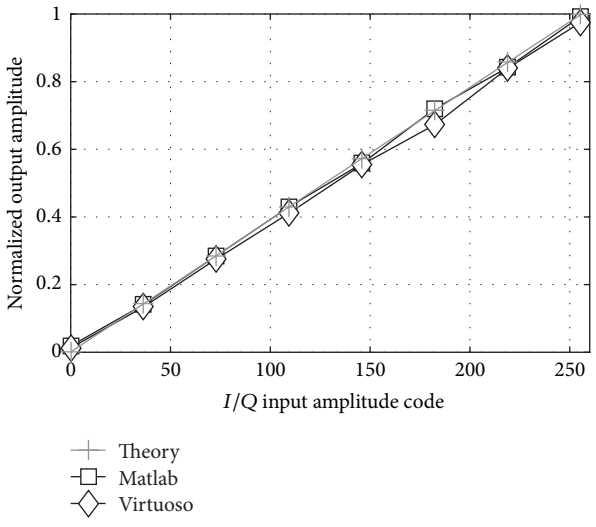

Figure 9: Simulated outphasing modulator linearity.

3-bit, 3-bit, and 4-bit adders. The 10-bit DPL-based adder features a simulated critical path delay of 180 ps in 40 nm CMOS. It means that a maximal clock frequency of 5.6 GHz can be applied.

In this work, the complete outphasing modulator is fully custom designed in 40 nm CMOS using Cadence Virtuoso in order to ensure high speed and low power. Figure 9 shows the static response of the outphasing modulator. It can be seen that the modulator can operate linearly up to the peak output amplitude. The simulated results in Virtuoso are in good agreement with the theory and Matlab results. For the dynamic response, the outphasing modulator is first simulated in Virtuoso and the results are then fed to the outphasing front-end (i.e., Matlab model) to further evaluate the system performance. The complete system is tested with 10.56 Gb/s 64-QAM (i.e., 1.76 GHz signal bandwidth). Figure 10 shows the simulated 64-QAM constellation with an EVM of 3.2% and the output spectra that well fits the IEEE 802.11ad spectral mask requirements at 60 GHz. The corresponding power consumption is 112 mW at the supply voltage of 0.9 V, well competing with [10] for the same data rates.

5. Conclusion

A high-speed digital outphasing modulator is reported to enable fully integrated efficient outphasing TX for mm-Wave applications. CORDIC algorithm is utilized to realize coordinate conversions and $\cos^{-1}(x)$ function. Issues such as signal quantization error, delay mismatch, and phase overflowing are tackled to facilitate hardware implementation. Fully custom designed in 40 nm CMOS, the proposed outphasing modulator achieves 10.56 Gb/s 64-QAM modulation with an EVM of 3.2% and meets the IEEE 802.11ad spectral mask requirement.

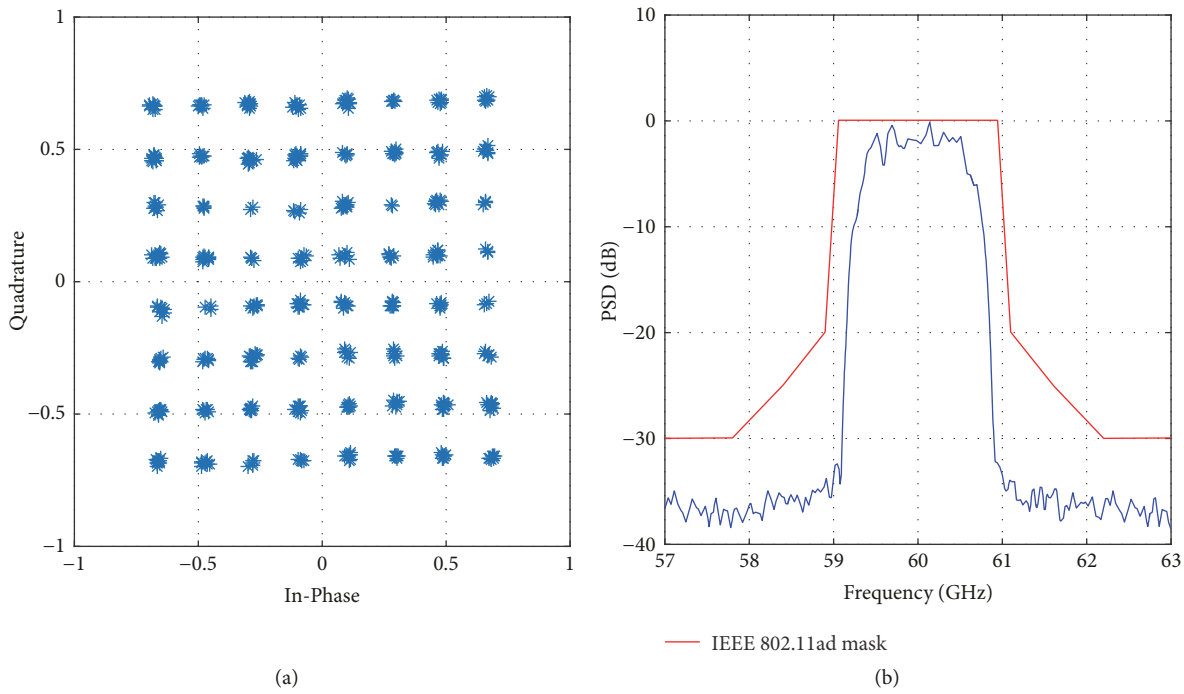

Figure 10: Simulated (a) 64-QAM constellation diagram and (b) power spectral density (PSD) of the output signals for IEEE 802.11ad.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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