Cost of Ownership Analysis for Patterning Using Step and Flash Imprint Lithography

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ABSTRACT

While the critical dimension in the microelectronics industry is continually going down due to developments in photolithography, it is coming at the expense of exponential increase in lithography tool costs and rising photomask costs. Step and Flash Imprint Lithography (S-FIL) is a nano-patterning technique that results in significantly lower cost of the lithography tool and process consumables. In this study, a comparison of S-FIL with Extreme Ultraviolet (EUV) photolithography technique is provided at the 50nm node†. Advantages and disadvantages of S-FIL for various application sectors are provided. Finally, cost of ownership (CoO) computations of S-FIL versus EUV is provided. CoO computations indicate that S-FIL may be the cost-effective technology in the sub-100nm domain, particularly for emerging devices that are required in low volumes.

1. Introduction

The unique physical and chemical phenomena at the nanoscale can lead to novel devices that potentially have significant practical value. However, in order to fabricate such devices in a cost-effective manner, nano-manufacturing techniques that substantially retain the cost benefits of wafer-scale microelectronics manufacturing are required. MEMS devices have benefited from the fact that they possess critical dimensions that are at least one order of magnitude larger than high-end microelectronic devices. However, at the nano-scale, high-throughput wafer-scale manufacturing techniques currently do not exist. Further, the cost projections of microelectronics manufacturing for devices with critical dimensions below 100nm appear to be prohibitive unless large-volume manufacturing is required. Therefore, it is imperative that novel, low-cost nano-manufacturing techniques be developed in conjunction with the study of nano-scale devices to fully benefit from the field of nanotechnology.

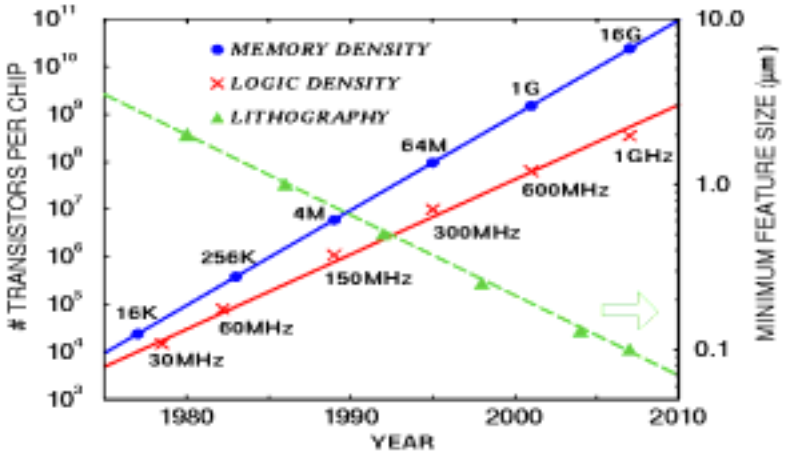


Figure 1: The Moore's Law

Figure 1 illustrates the well-known Moore's law associated with the growth of the microelectronics industry. The packing of more and more transistors per chip with smaller and smaller critical dimensions has led to a continuous advantage in cost and performance. For example, in 1987 a Cray I computer cost $8M and required 60Kwatts of power,

† In the International Technology Roadmap for Semiconductors (ITRS), the DRAM half-pitch being the most difficult device parameter to fabricate, is used to define the lithography nodes.

while today a Nintendo that draws only about 5 watts and performs 3.5x as many additions per sec only costs about $300.00! In order to keep progressing at this rate, it is essential to continually print smaller structures and devices at approximately the rate shown in the lithography plot in Figure 1. Historically, the lithography technology of choice has been photolithography. The minimum feature size (F) in photolithography is given by: $F = (k_1)(\lambda/NA)$. Here λ is the exposure wavelength, NA is the numerical aperture of the lens system in the photolithography tool with typical values of 0.5 to 0.8, and k_1 is a process related term with typical values of 0.7 to 0.4. The reduction of F has been achieved by periodically going to smaller and smaller exposure wavelengths. Photolithography is now operating at a deep UV wavelength of λ = 248 nm, while λ = 193 nm is undergoing beta testing and is expected to go into production soon. Concurrently, λ = 157 nm is being researched and is being touted as the successor to 193 nm optical lithography. Finally, the primary candidate for next generation lithography beyond 157 nm is believed to be extreme ultraviolet lithography (EUV) that operates at λ = 13.2 nm. This continuous reduction is wavelength combined with highly sophisticated designs of lenses and mirrors, design of advanced and complex masks, innovation in materials, processes, and precision machines will surely enable sub-100nm lithography, and may even result in sub-70nm lithography. However, with shorter wavelengths, there are long lists of new and substantial technical challenges. For instance, fused silica has been the established lens material in optical lithography. However, fused silica is not transparent at 157 nm. Therefore, the 157 nm research efforts are focused on using CaF_2 as the lens material, which has led to significant original research problems with respect to manufacturing of sufficient quantities of high-purity CaF_2 and circumventing the high level of birefringence that is characteristic of this material. At λ = 13.2 nm, there are no known transparent materials; therefore all the optical systems and photomasks are based on reflective optics. Further, obtaining a source with sufficient power at this EUV wavelength is still an open problem. High-resolution e-beam lithography techniques, though very precise, are too slow for high-volume commercial applications. They are believed to be best suited for directly writing photomasks used in photolithography.

2. The Exponential Cost of Going Smaller

It is not physical limits, but prohibitive costs that are likely to make the traditional approach of decreased wavelength challenging. Even today, optical lithography is an extremely expensive unit process. Historically, the cost of optical exposure tools has increasing exponentially (see Figure 2). Even if fundamental challenges are overcome at λ = 157 nm and 13.2 nm, it is believed that the historical exponential increase in tool cost could become even steeper. In addition to the cost of the tool, the recurring and consumable costs associated with process materials, environmental control, complicated photomasks, etc. makes next generation lithography a high-risk proposition. The only way to recover these costs is to have high throughputs; long tool lives; long photomask lives; and excellent feature fidelity within a chip, between chips and between wafers.

While lithography was primarily developed by the silicon microelectronics industry, it is fast becoming a key unit process for several other application areas such as micro-fluidic devices, optical switches, flat panel displays, SAW devices, etc. Emerging nano-resolution applications include sub-wavelength optical components, biochemical analysis devices, high-speed compound semiconductor chips, distributed feedback lasers, photonic crystals, and high-density patterned magnetic media for storage. The above discussion clearly indicates that there exists a need for low-cost alternatives to nano-resolution photolithography. It is believed that if a sufficiently low cost lithography solution can be developed, it will provide a major competitive edge to manufacturers of traditional and emerging devices, and enable new kinds of devices that are currently not economical. The cost and complexity trends in photolithography have motivated us to investigate and develop a non-

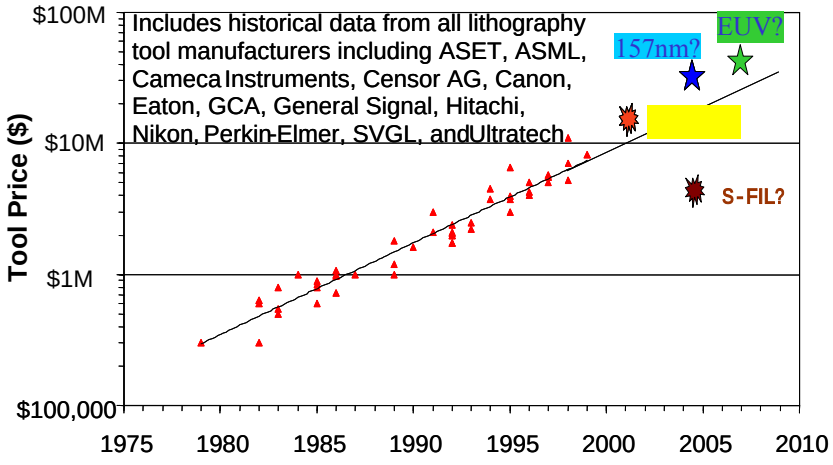


Figure 2: The Exponential Increase in Cost of Lithography Tools

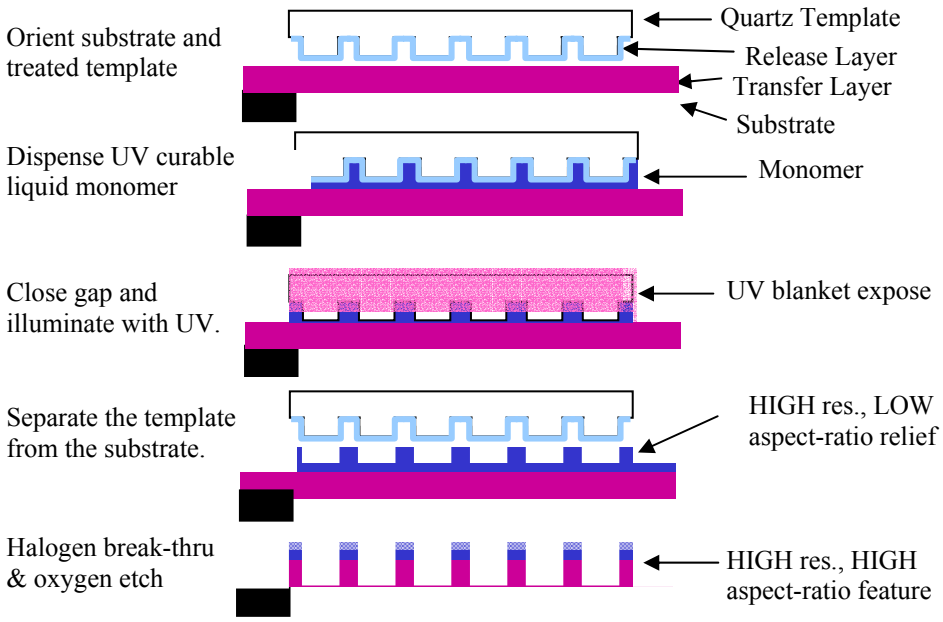


Figure 3: The Step and Flash Imprint Lithography (S-FIL) Process

optical, low-cost lithography technique known as Step and Flash Imprint Lithography (S-FIL).

3. The S-FIL Technology

While looking for low-cost lithography alternatives, our goal was to develop a technology that not only resulted in significantly lower cost of process consumables and the tool (see projected tool cost for S-FIL in Figure 2), but also ensured that other aspects of lithography were as good or better than photolithography. These other aspects include life of the tool; life of the master (used instead of the photomask); master cost; process yield; throughput; and feature fidelity within a chip, between chips and between wafers.

We have investigated imprint lithography (IL) techniques for pattern replication capable at sub-100nm resolution on silicon wafers. IL has several important advantages over conventional optical lithography and EUV lithography. The parameters in the classic photolithography resolution formula (λ, k_1, and NA) are not relevant to IL because the technology does not use reduction lenses. Investigations by others and us in the sub-100nm regime indicate that the resolution is only limited by the pattern resolution on the template, and replication of sub-20 nm features has been demonstrated using IL. The resolution of IL is a directly a function of the resolution of the template fabricating process. Therefore, the IL tools are multi-generational leading to significant cost advantages in new process development and integration. IL techniques are essentially micromolding processes in which the topography of a template defines the patterns created on a polymer film coated onto the substrate. Traditional micromolding or embossing processes require high pressures and temperatures (pressures greater than 10MPa may be required, and temperatures must be greater than the T_g of the polymer film). This leads to unpredictable distortions in the imprinted structures. Also, our experience with such high-temperature and high-pressure process illustrated another serious problem. Imprinting with varying pattern density resulted in incomplete displacement of the polymer even at elevated temperature and high pressure for long periods. In particular, it is impractical to try and replicate isolated recessed structures present in the template.

Step and Flash Imprint Lithography (S-FIL) is an improved version of traditional micromolding. S-FIL is based on a low-viscosity, UV-curable liquid etch barrier in conjunction with a bi-layer approach. The template is rigid and transparent allowing for UV curing of the etch barrier and the adaptation of traditional layer-to-layer alignment techniques. This results in a low pressure, room temperature process (Figure 3) that is:

- Multi-generational with nano-resolution capability
- Insensitive to variations in pattern density,
- Particularly suited for high-resolution layer-to-layer alignment, and
- Capable of generating high aspect ratio, high-resolution features with high throughput.

A detailed discussion of the S-FIL process including its sub-100nm resolution capability, its ability to self-clean (in-situ cleaning of contaminants from the template), and its ability to print over pre-existing topography is provided elsewhere [1, 5].

4. Comparison of S-FIL with Mainstream Next Generation Lithography (NGL) Schemes

S-FIL can potentially compete with the mainstream NGL technologies such as 157nm photolithography (PL), electron projection lithography (EPL), and extreme ultraviolet lithography (EUV) techniques. The key competitive advantages of S-FIL over the other NGL techniques include:

- Ultra-high (sub-20nm) resolution
- Resolution = *f*(template); S-FIL is a multi- node technology
- Significantly lower cost structure of S-FIL (Table 1)

The extendibility of projection lens based PL is widely believed to end with 157 nm PL. While 157 nm PL is a major variation of photolithography, any technique such as EUV or EPL will be a disruptive departure from the well-established technology of photolithography. During these transitions, a clear opportunity exists for S-FIL to become a viable solution, if it has been developed adequately. The low-cost nature of S-FIL allows its investigation in other applications to reduce the risk of inserting it for high-end Silicon manufacturing. The high-cost of the other NGL lithography techniques significantly increases the risk of inserting these technologies, particularly since these techniques cannot be investigated in a cost-effective manner for other applications.

Table1: Comparison of S-FIL and other NGL techniques

Sub-Systems	SFIL	157 nm	EPL	EUV
Tool Life	Multi-Node	Single Node	Multi-Node	Multi-Node
Imaging System	None	Expensive	Expensive	Expensive
Process Materials	Standard	Specialized	Specialized	Specialized
Source Cost	Low	High	High	Very High
Environment	Standard	Inert	Vacuum	Vacuum
Throughput	Good	Good	Low	Good
Power	Low	Medium	High	High
Master Cost	Medium to High	Medium	Medium	High

5. Comparison of S-FIL with Other Imprint Lithography Techniques

A brief discussion of two prominent research programs in the area of imprint lithography is provided next. Professor Chou of Princeton and Professor Whitesides of Harvard have made significant contributions to the development of imprint lithography techniques. Professor Chou's group has advanced the high pressure/temperature nanomolding technique to unprecedented levels of resolution [2]. This is a simple process and it is well suited for many applications. Unfortunately, the pattern dependent issues, and high operating pressures and temperatures make it difficult to adapt the technique to (i) the fabrication of multi-layer devices that require precise layer-to-layer alignment, and (ii) the processing of compound materials such as GaAs and InP.

The techniques developed in the Whitesides' group are elegant and inventive and can be used in conjunction with various functional materials; they are also suited for patterning curved surfaces with flexible templates [3]. However, the use of flexible templates makes it unsuitable for applications where distortion in the template eliminate layer-to-layer alignment potential and lead to variations in critical dimensions.

6. 1X Template Fabrication

The S-FIL templates are fabricated using processes that are similar to phase shift mask fabrication technology. We have a partnership in place with Motorola Labs, in Tempe, Arizona for the purpose of fabricating sub-50nm templates (Figure 4). We have also received sub-100nm templates from Dupont Photomask, Inc. (DPI) in Round Rock, Texas. It should be noted that the use of a thick, structurally stable template avoids problems associated with processing 1X membrane masks of the sort used in x-ray and ion projection lithography techniques.

The ultimate resolution of imprint technologies appears to be limited by the resolution of the imprint template. It is therefore desirable to extend the ability to pattern these templates to coincide with the ITRS. As an example, by the year 2005, the ITRS calls for 65nm minimum resist features for microprocessor gate length and 130nm minimum mask feature size for optical proximity correction features. Therefore, for 1X pattern transfer with imprint lithography, there would be a need to accelerate mask feature size targets in the ITRS to coincide with the resist feature targets. Perhaps the most significant challenge facing the 1X template fabrication is in inspection. Exhaustive inspection followed by repair is essential in the fabrication of high-end silicon microelectronic devices, since the presence of even a single defect in

the master could lead to zero yield in subsequent processes. 1X template inspection will likely require electron beam based inspection that could significantly increase the template cost. However, it is believed that the cost of masks of competing techniques is also likely to be high. For example, it is predicted that the cost of EUV masks is likely to be high due to the need for complex, 80 monolayer stacks required to create the reflective masks. Further, the significantly lower tool costs of S-FIL and its potential use in applications that do not require exhaustive inspection makes it attractive from a cost point of view as discussed in the next section.

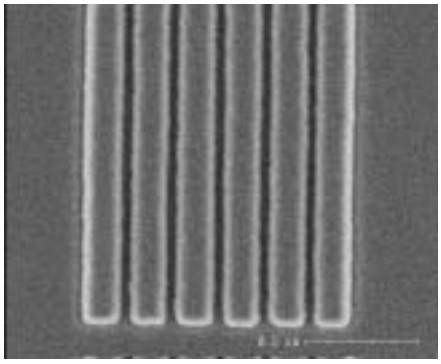


Figure 4: Sub–50nm spaces on S-FIL template fabricated by Motorola

7. Cost of Ownership Estimates: S-FIL vs. EUV at the 50nm Node

This analysis presents a comparison of the Cost of Ownership (CoO) of the S-FIL technology to that of the EUV photolithography (PL) at the 50nm node. This comparison is believed to provide a baseline for patterning cost in the sub-50nm domain. CoO represents the cost of lithography per wafer level and is widely used to compare lithography costs of various technology options. The CoO analysis presented here is derived primarily from [4]. The real technological advantage of the S-FIL technology lies in its ultra-high resolution (sub-50nm), low tool costs and long tool life (multi-node technology). The analysis investigates the variation of CoO with respect to (i) production volume or throughput (no. of wafers/hour), (ii) Template (mask) usage, (iii) Template (mask) cost reduction in applications that do not require exhaustive inspection, and (iv) Template cost uncertainty.

7.1 Basic CoO Model

The CoO model assumes that the cost per wafer level is the sum of the costs associated with mask (or template), process costs, and tool costs. Other costs such as cost of operating the fabrication facility, maintaining the environment control, the footprint of the equipment, etc. [4] have not been included in this analysis since they are comparatively small. However, all these factors should favor the S-FIL technology due to its simpler tools and environmental control requirements.

$$\text{CoO } \textbf{(in \$ per wafer level)} = P_W + \frac{M_0}{M_L} + \frac{E_0 + (D)(E_M)}{(D)(T)(U)(365)(24)}$$

Here, P_W = Process cost per wafer level (resist and etch costs)

M_0	=	Photomask/template cost in $
M_L	=	Photomask/template usage in no. of wafer levels
E_0	=	Litho & coat/bake capital equipment costs in $
E_M	=	Litho equipment annual maintenance costs in $
E_T	=	Total litho equipment costs in $ = $\{E_0 + (D)(E_M)\}$
D	=	Equipment depreciation in years
U	=	Utilization of equipment
T	=	Throughput in wafer levels per hour

7.2 Assumptions

Several assumptions have been made for the S-FIL and EUV at the 50nm node. These assumptions are representative of discussion in [4] and are listed below:

1. P_W = $7.00 is assumed to be constant for S-FIL & EUV at the 50 nm node‡
2. M_0 = With inspection and repair, M_0 is nominally assumed to be $40K for both S-FIL and EUV (Figures 6 and 7).
3. In the absence of exhaustive inspection (for applications such as optical devices and bio-chemical analysis devices), S-FIL M_0 = $15K. This cost is based on the assumption that the S-FIL template costs are dominated by inspection (Figures 6 and 7).
4. Due to uncertainty associated with M_0 for S-FIL templates, a separate analysis is performed where M_0 is assumed to vary between $30K and $50K, while M_0 for EUV is kept constant at $40K (Figure 8).
5. M_L = Variable in Figure 7 (ranges from 250 to 10,000)
6. E_T = At the 50nm node, total litho equipment cost for S-FIL = $10M, for EUV = $30M
7. D = 5 years is assumed to be a constant for S-FIL & EUV at the 50 nm node
8. U = 70% is assumed to be a constant for S-FIL & EUV at the 50 nm node
9. T = Variable in Figures 5, 6 and 8 (typical range from 10 to 80 wafers/hr.)

7.3 CoO Discussion

The results of the CoO analyses are presented in Figures 5-8. The trends clearly indicate the value of the S-FIL technology for applications that at the 50nm node. The high total litho equipment cost of EUV necessitates high throughput, while the low total litho equipment cost of S-FIL can tolerate low throughput situations. Even at high throughputs, S-FIL technology is predicted to cost lower. In Figure 7, the variation of CoO as a function of template (mask) usage is shown. In the case of very low template (mask) usage, the tool cost is dominated by the template (mask) cost. Therefore, at very low usage, if M_0 for both S-FIL and EUV is assumed to be the same ($40K), then the CoO values become very similar. Such low template (mask) usage is likely to be important for emerging devices and research applications where an exhaustive template (mask) inspection is generally not needed, and throughputs are expected to be low. In such situations, S-FIL clearly provides a cost advantage over EUV (Figures 6 and 7).

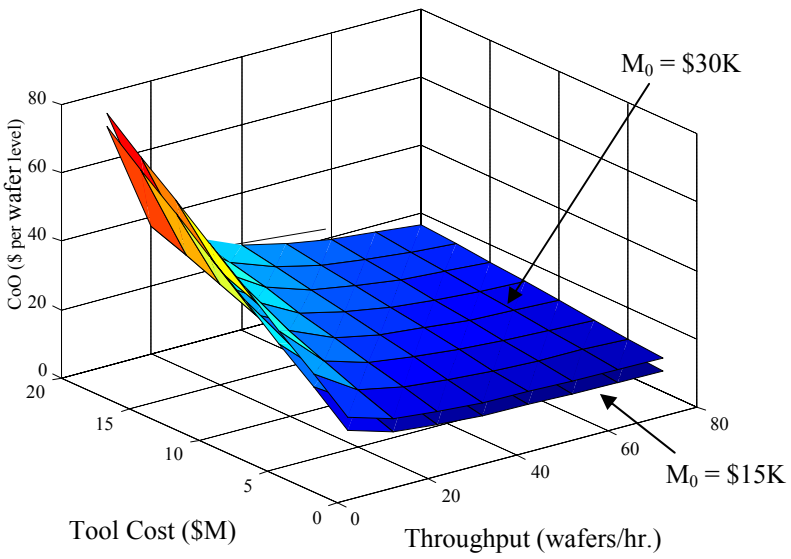


Figure 5: Overall CoO Trends as a Function of Tool Cost and Throughput

The major uncertainties associated with the S-FIL cost analyses presented here include the template inspection costs, template life and process yields. The template life and process yields require more statistical verification even though preliminary experiments suggest that these numbers are encouraging. However, the S-FIL technology lacks the large historical data available from years of practicing an established technology such as photolithography. Therefore, the analysis presented here should be treated as a best estimate based on presently available data. Factors that should favor S-FIL as compared to technologies such as EUV include significantly lower tool costs, potentially lowered mask life in EUV due to high-energy radiation exposure, and lowered tool life in EUV due to exposure of tool optics to high energy

‡ This assumption is conservative from the point of view of S-FIL since S-FIL resist costs are expected to be very small, and the etch costs are expected to be comparable to that of EUV.

radiation and contaminants that out-gas from materials used in the process. Further, due to the low cost nature of S-FIL, it is more likely to be used on emerging applications. Such applications can provide valuable statistical data for further development of the patterning process.

8. Summary

S-FIL is a nano-patterning technique that substantially maintains all the advantages of optical lithography. S-FIL tools possess significant cost advantages versus EUV in the sub-50nm domain. Finally, S-FIL has lower cost of ownership (CoO) than EUV. This is particularly true for emerging application areas such as optical communications and biochemical analysis. These applications do not require exhaustive template inspection, have low device volumes, and are not likely to support high throughput lithography.

Figure 6: S-FIL & EUV CoO Vs. Throughput at the 50nm Node

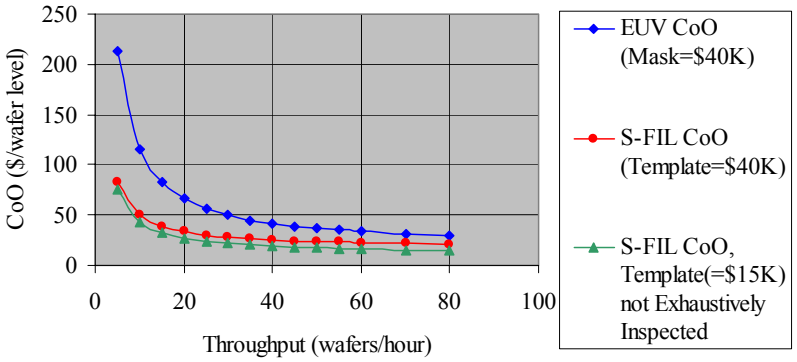


Figure 7: S-FIL & EUV CoO versus Mask Usage at the 50nm node

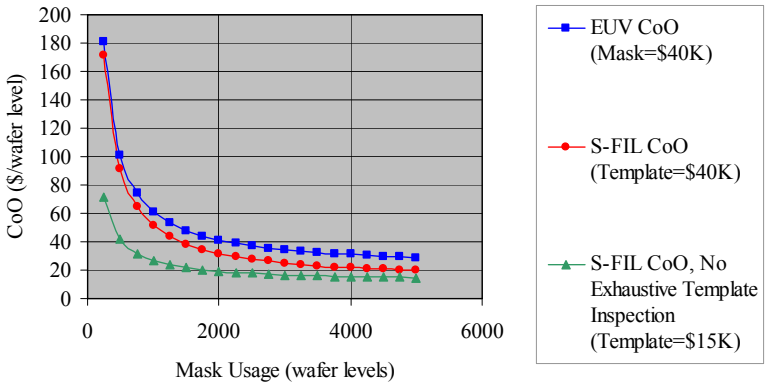
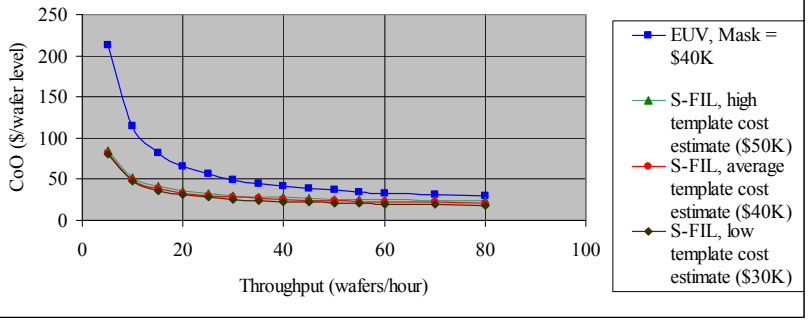


Figure 8: S-FIL (with Template Cost Uncertainty) and EUV CoO Vs. Throughput Mask Usage, M_L = 4000 Wafers



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