Coupling-Aware Dummy Metal Insertion for Lithography

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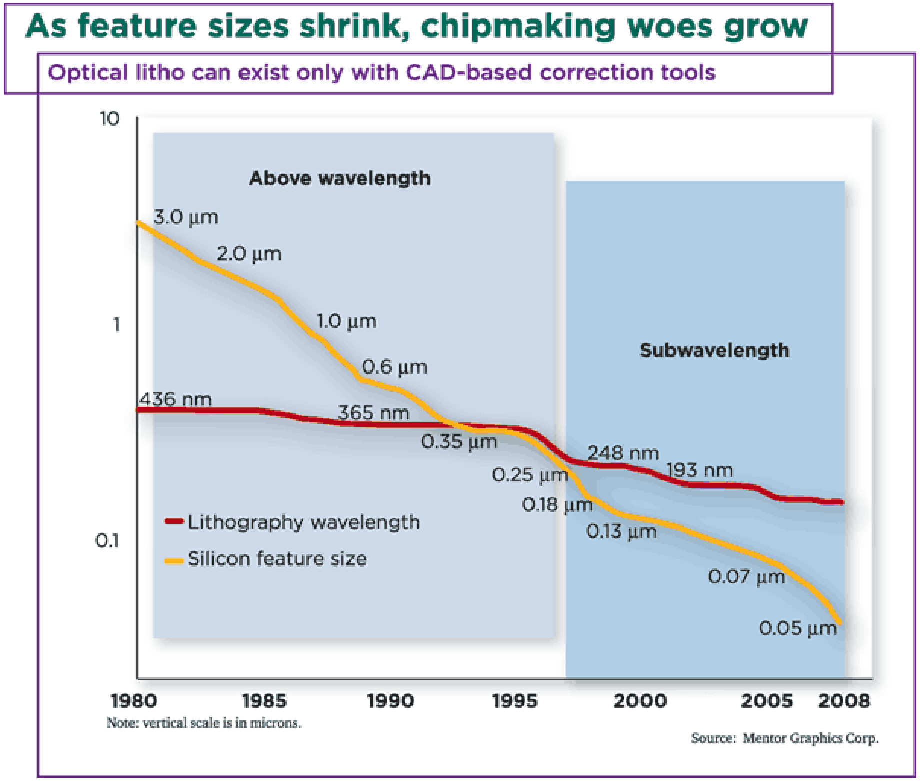
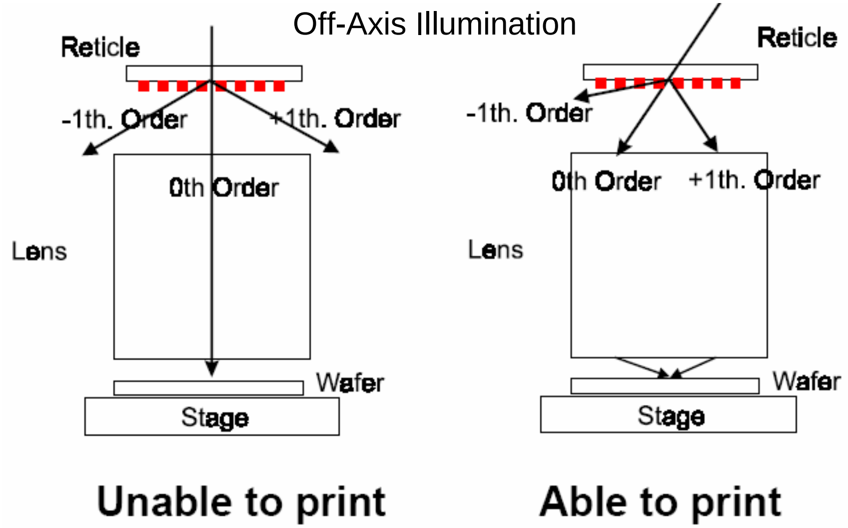
Technology Scaling and Lithography

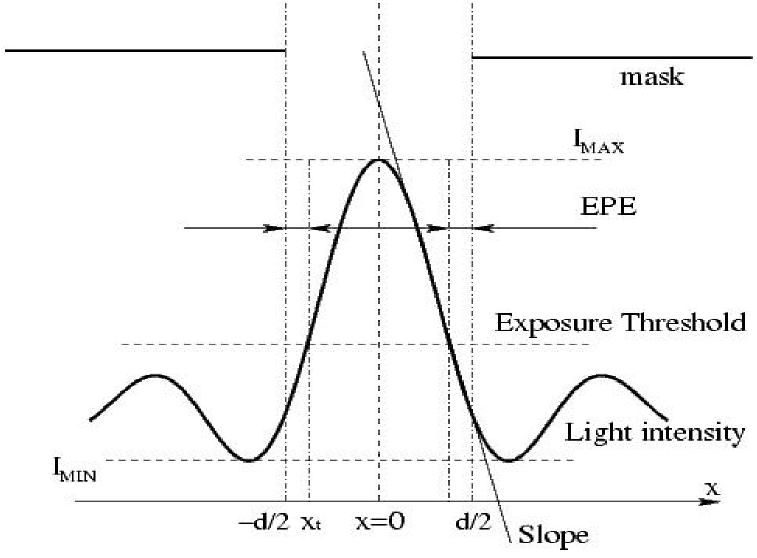
- Lithography system with 193nm wavelength will be used for future technology nodes
- The gap between feature size and wavelength increases
- Metal layer will have issues for future nodes as Poly layer have now



Resolution Enhancement Technology

- Optical Proximity Correction (OPC)
- Phase Shift Mask (PSM)
- Off-Axis Illumination (OAI) is widely used
  - Enhanced slope
  - Smaller edge placement error (EPE)



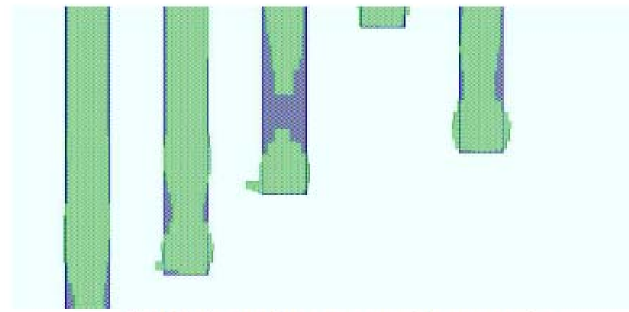


Off-Axis Illumination (OAI)

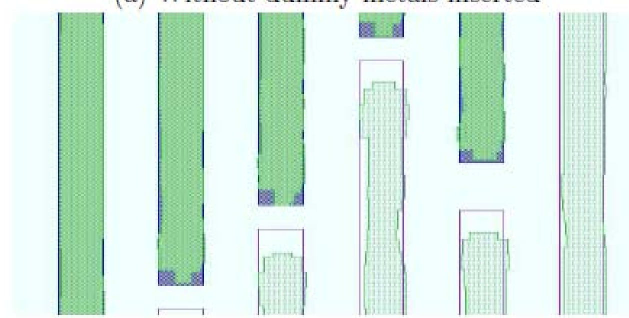
- Pros
  - Little lithography/mask cost overhead compared to OPC or PSM
  - Good printability for dense features
- Cons
  - Complicated design rules
  - High printing errors for isolated features with defocus
  - Difficult “Forbidden Pitch” problem

Dummy Metals Improve Printability

- With OAI, some features can't be printed correctly even after OPC
- Obtain layout uniformily by inserting dummy metals
- Dummy metal insertion improves printability



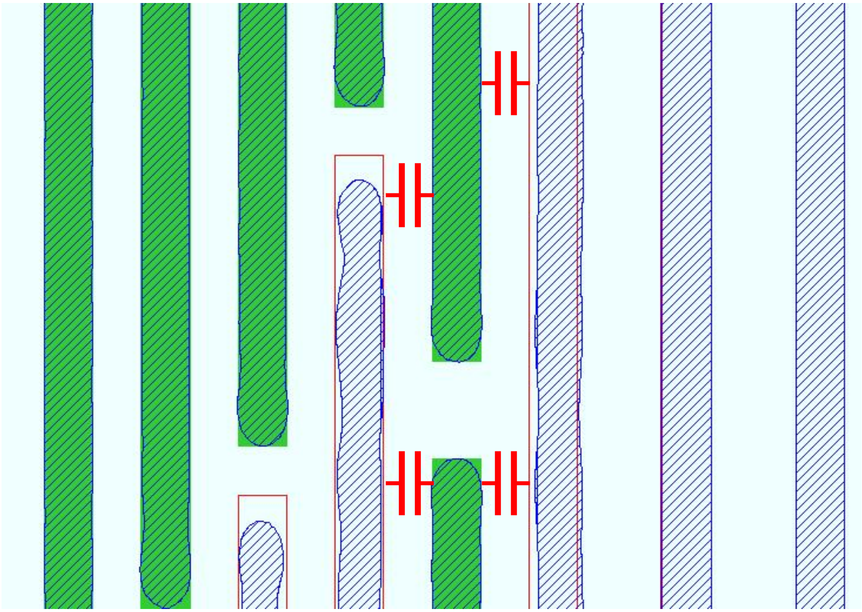
(a) Without dummy metals inserted



(b) Dummy Metals are inserted to achieve uniformity

Dummy Metals Add Coupling Capacitance

- Dummy metal insertion introduces additional metals on wafer
- Coupling capacitance is increased
- May degrade circuit performance

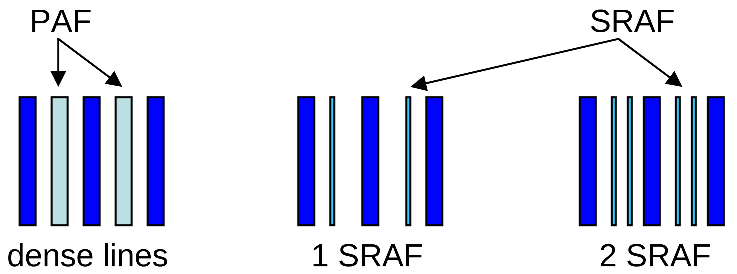


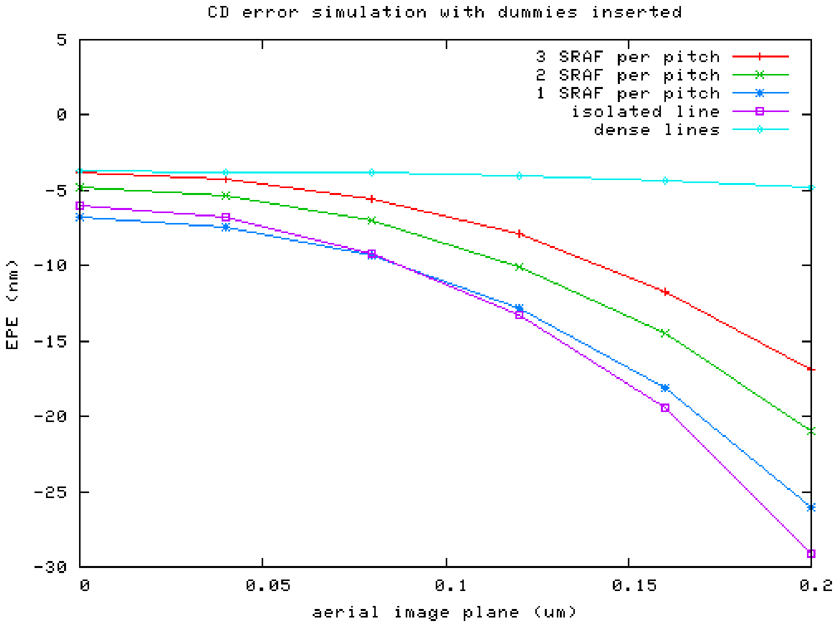
Printed image simulation from Calibre™ after dummy insertion

Two Types of Dummy for Lithography

- Printable Assist Feature (PAF)
  - Same width as metal wires
- Leaves metals on wafer
  - Higher coupling capacitance
  - Better printability

- Sub-Resolution Assist Feature (SRAF)
  - Small enough not to be printed
  - Several parallel SRAFs are needed to act as one PAF
  - Lower coupling capacitance
  - Less improvement on printability



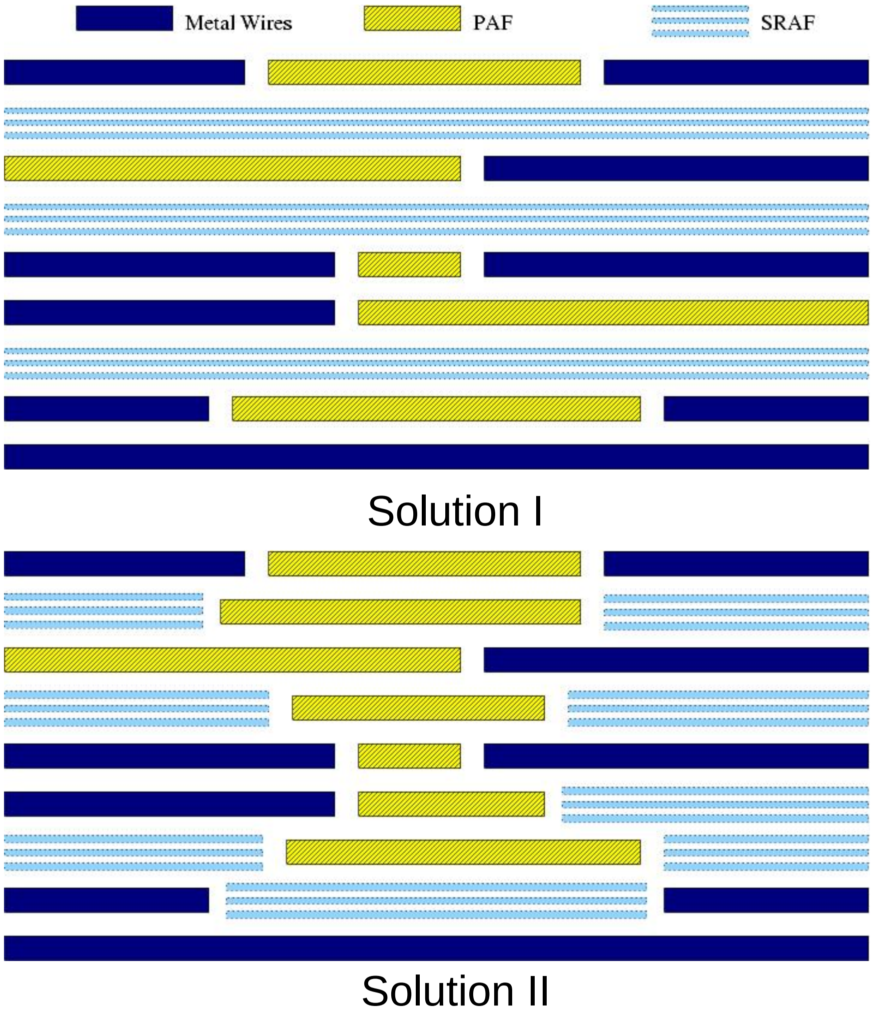


Litho Cost and Coupling Cost

- Lithography cost
  - Complexity of assist features (PAF < SRAF)
  - Printability (EPE) (PAF < SRAF)
  - Reduce lithography cost ↔ Use *more* PAFs
- Coupling Cost
  - PAFs add coupling capacitance
  - SRAFs has no coupling overhead
  - Reduce coupling cost ↔ Use *less* PAFs

Coupling-Aware Dummy Insertion

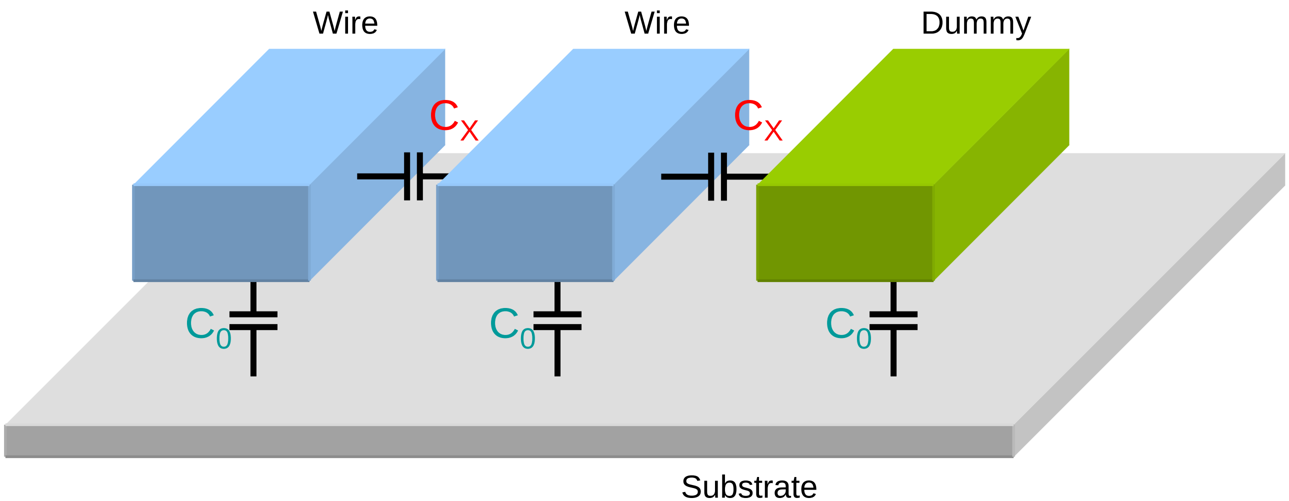
- Trade off between coupling cost and lithography cost
- Compared to inserting PAF everywhere
  - Solution I: 30% less coupling
  - Solution II: 46% less coupling with 5% less SRAFs
- Insert PAFs and SRAFs to minimize lithography cost subject to coupling cost bound

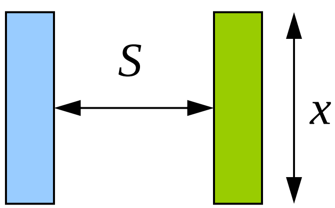


Coupling-Aware Dummy Insertion

- Given a layout with metal wires routed, find a dummy metal insertion solution (using PAFs and SRAFs) that minimizes the total amount of PAFs inserted such that total coupling capacitance is less than a given bound
- *We have designed an efficient algorithm to solve this problem optimally*

Coupling Capacitance Model

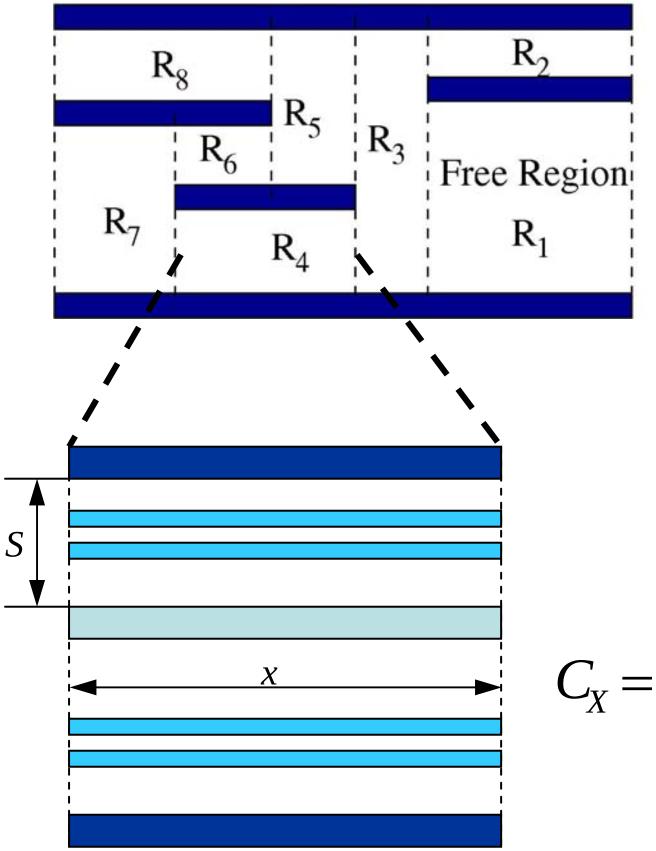




$$C_X = C_0 \frac{x}{S^{\alpha}}$$

Post-Routing Partitioning

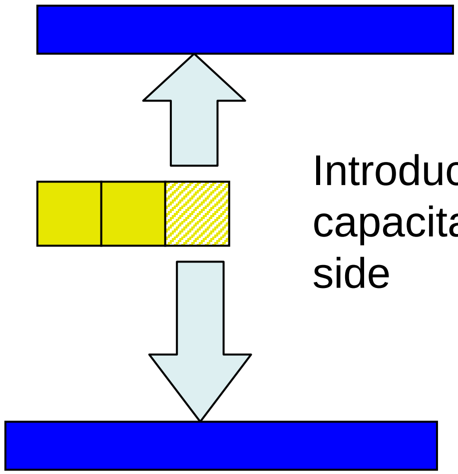
- Layout is partitioned into regions
- Each region has only top and bottom metal features
- Dummies will be inserted into the white spaces in the region
- PAFs and SRAFs give different coupling and lithography cost



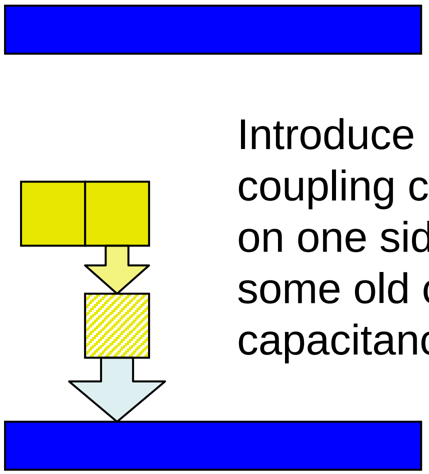
$$C_X = C_0 \frac{x}{S^{\alpha}}$$

Coupling-Lithography-Cost (CLC) Ratio

- Coupling-lithography-cost (*CLC*) ratio = *Increase in coupling capacitance per unit increase in PAFs*
- Dummy insertion with smaller *CLC* ratio is preferred



Introduce new coupling capacitances for both side



Introduce new coupling capacitances on one side and block some old coupling capacitance

Basic Algorithm

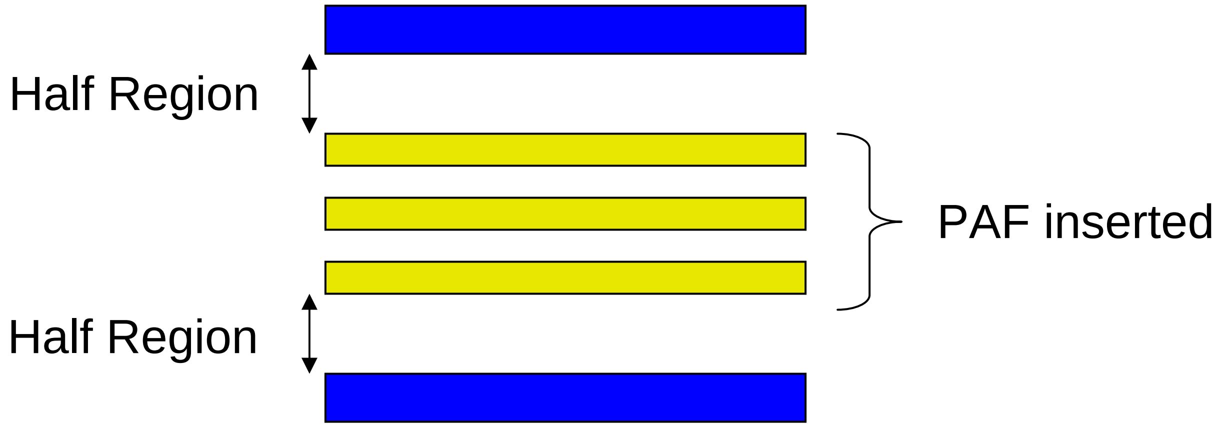
- **Goal**: Insert maximum PAFs to keep coupling capacitance within given bound
- A simple greedy algorithm
  1. Insert unit length PAF at a location which has minimum CLC ratio
  2. Update CLC ratios for all insertion locations
  3. Repeat Step 1 until coupling capacitance bound is violated
- A much faster implementation is possible

Improved Algorithm

- Pick a region with minimum CLC ratio
- Insert a suitable number of tracks of PAFs into the selected region
- New regions formed and optimal insertion of PAFs is iteratively performed on the regions to minimize CLC ratio
- Algorithm stops when no more slack on coupling capacitance constraint

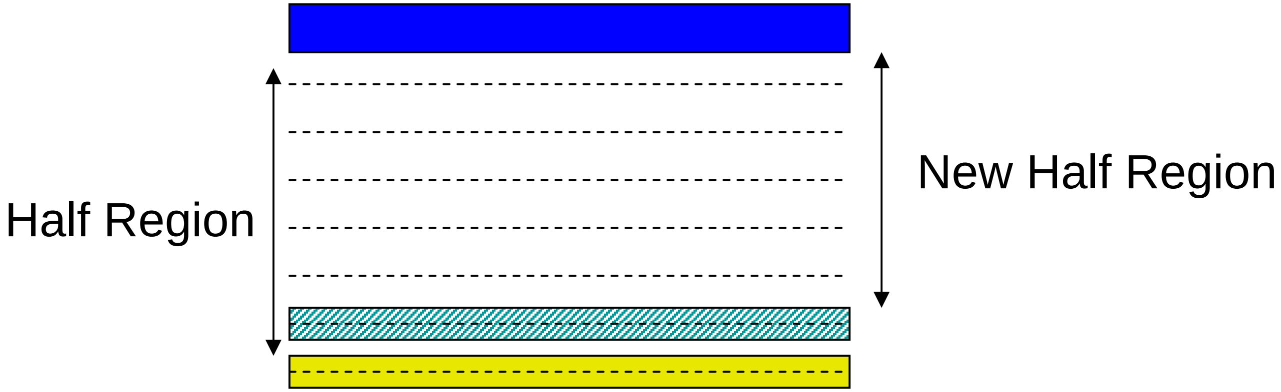
Dummy Insertion for One Region

- PAFs are inserted on tracks
- PAFs are inserted into the middle tracks first
- If coupling constraint is not reached, insert PAFs to fill all these tracks
- One region is divided by the inserted PAFs into two half regions



Dummy Insertion for Half Region

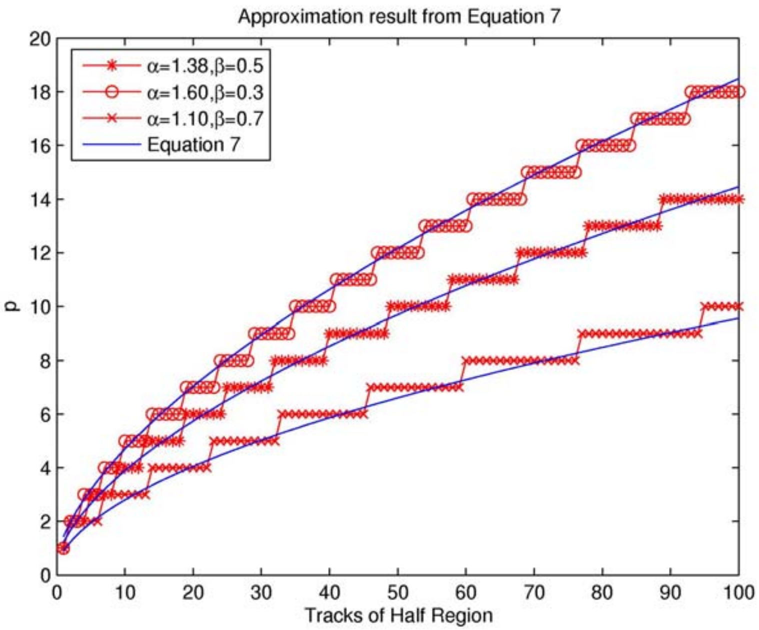
- Minimum CLC is achieved by inserting PAFs on the track nearest to the bottom
- If this track is filled, new half region with new minimum CLC will be formed



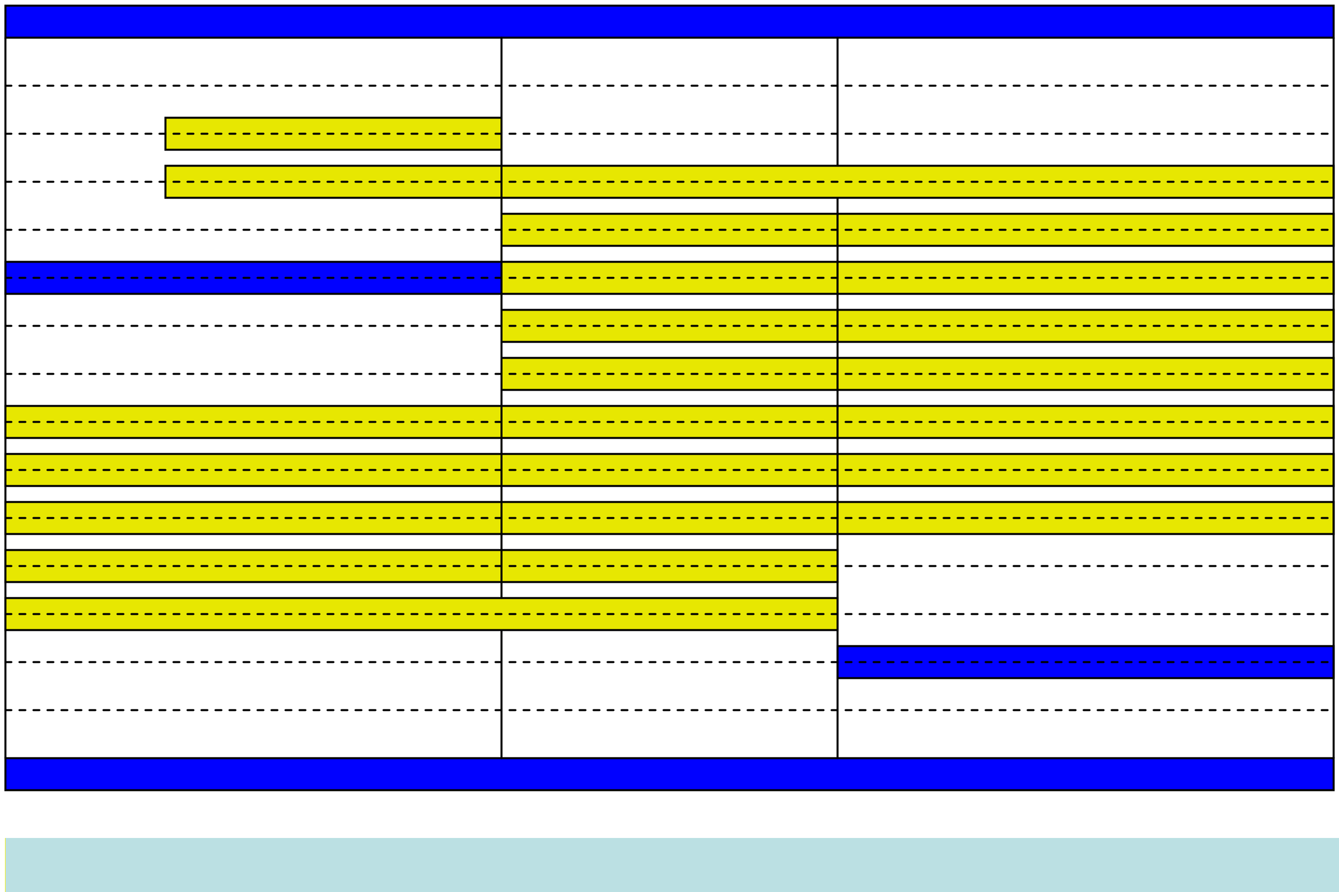
Optimal Dummy Insertion for a Region

- Given a region with m tracks
- Inserting *p* tracks of PAFs with identical length will minimize the CLC ratio
- *p* is a function of m

$$p \approx \left(\frac{\alpha}{(m+\beta)^{-\alpha} + (k+\beta)^{-\alpha}} \right)^{\frac{1}{\alpha+1}} - \beta + 0.5.$$



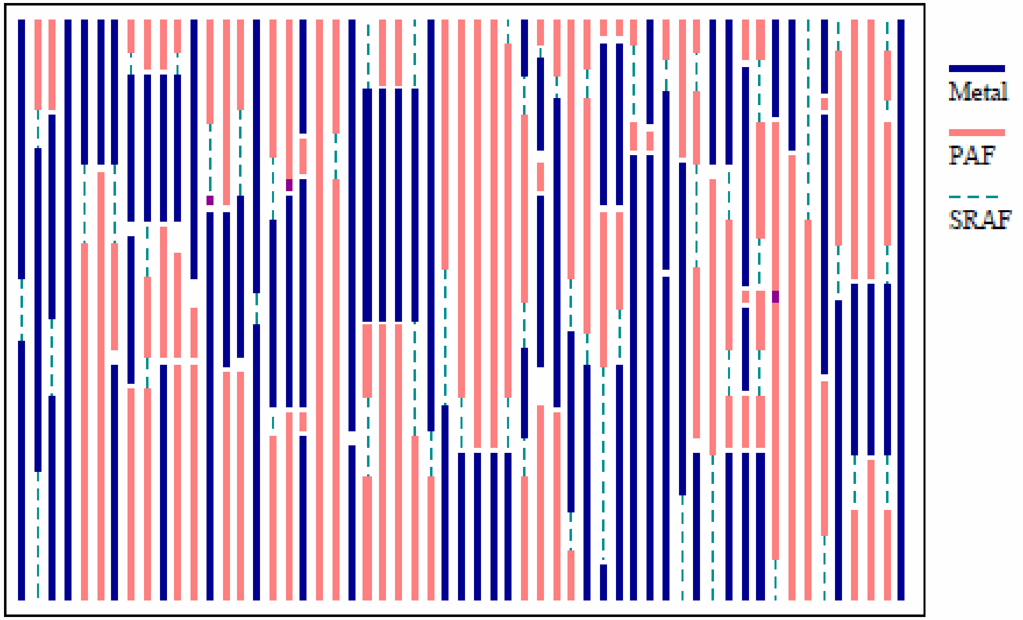
Demo



Coupling Capacitance Constraint

Experimental Results

- Insertion result is shown by our optimal algorithm with linear complexity



Conclusion

- First work on coupling-aware dummy metal insertion for lithography
- Consider the tradeoff between mask complexity, printability and coupling capacitance
- An optimal algorithm is proposed to minimize lithography cost subject to a given coupling capacitance bound