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# Coupling Between Differential Signals and the DC Power-Bus in Multilayer PCBs

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# Coupling Between Differential Signals and the DC Power-Bus in Multilayer PCBs

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***Abstract*—Differential and common-mode transfer impedances are proposed herein to analyze noise coupled to (from) the dc power-bus from (to) via transitions in differential signals. Expressions for the two transfer impedances in terms of conventional single-ended transfer impedances are derived and verified through measurements, full-wave finite-difference time-domain (FDTD) simulations and an analytical cavity model. Some properties of the differential and common-mode transfer impedances are investigated to facilitate engineering design. The impact of signal current imbalances on power-bus noise and the benefit of differential signals as compared to single-ended signals are quantified.**

***Index Terms*—Differential signaling, power-bus noise, signal imbalance, signal integrity, via transition.**

## I. Introduction

MULTILAYER printed circuit boards (PCBs) commonly employ dc power delivery structures that include entire planes or large area fills to provide current supply and return. The dc power-bus structure is essentially a parallel-plane waveguide [1], [2], and the modes excited within the planes can result in signal integrity (SI) and electromagnetic interference (EMI) problems [3]–[5]. Mitigating the dc power-bus noise is critical in high-speed digital circuit designs. Practical mitigation strategies include global decoupling [6], local decoupling [7], and embedded capacitance [8], [9]. All of these previous studies focus on a single via transition through the power delivery planes.

Differential signals are widely used in present high-speed digital systems due to the rejection of common-mode noise on the signal, as well as the reduction of the overall EMI level [10]. As in the case of single-ended signals, via transitions in differential signals can also excite the parallel planes, resulting in power-bus noise [11]. Analyses of coupled vias have been reported in the literature that have focused primarily on signal scattering effects at the discontinuity [12]–[14]. This paper proposes a systematic method to quantify noise coupled to and from differential signals transitioning through parallel planes or area fills in a multilayer PCB. In Section II, two transfer impedances, namely differential and common-mode transfer impedances, are introduced. Experimental and numerical results are presented in Section III, and engineering studies are considered in Section IV.

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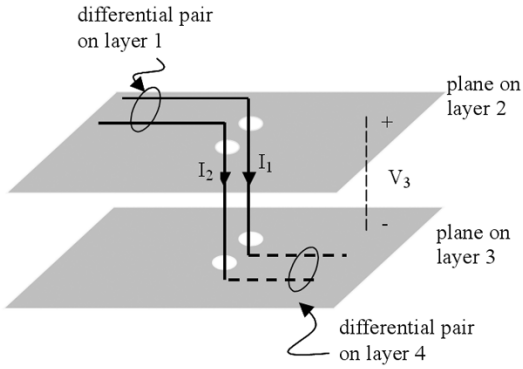


Fig. 1. Typical via transitions of a differential pair in a four-layer board.

## II. Differential and Common-Mode Transfer Impedances

A typical via transition for differential signaling in a four-layer board is shown in Fig. 1. The currents $I_1$ and $I_2$ flowing between two conducting planes or area fills can excite the parallel-plane structure, thereby developing a noise voltage $V_3$. In practice, the planes are often power and ground layer pairs, but do not necessarily need to be so. Since both $I_1$ and $I_2$ are the excitations and the system is linear, $V_3$ is the superposition of the noise voltages due to $I_1$ and $I_2$, i.e.,

$$V_3 = Z_{31}I_1 + Z_{32}I_2 \tag{1}$$

where $Z_{31}$ is the transfer impedance between the locations of $I_1$ and $V_3$, and $Z_{32}$ is the transfer impedance between the locations of $I_2$ and $V_3$. From (1), the power-bus noise voltage depends on both the excitation currents and the power-bus transfer impedances $Z_{31}$ and $Z_{32}$. With adequate models, signal integrity tools can be used to calculate the currents $I_1$ and $I_2$. This paper investigates the power-bus transfer impedances for differential signaling, and the effects of imbalances in $I_1$ and $I_2$ on the power-bus noise.

The power-bus transfer impedances are determined by the voltage across the planes (resulting from the electromagnetic field within the power planes) due to the vertical currents on the vias. In order to focus on the transfer impedances, the differential pair on layers one and four can be omitted when the skin-depth is much smaller than the thickness of the metal layers so that the current on the top surface of the metal layer is decoupled from the current on the bottom surface. The vias can

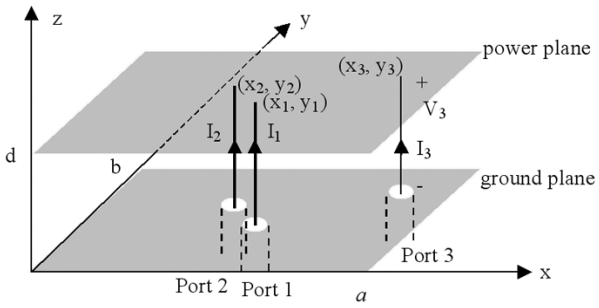


Fig. 2. A simplified two-layer structure for studying a noise voltage coupled to parallel-planes or area fills due to via transitions of differential signals.

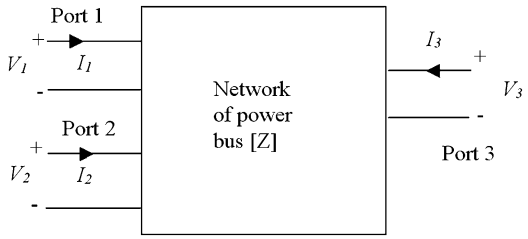


Fig. 3. A three-port network representation of a power-bus with differential feeding.

be replaced with two probes, with the center conductor of each probe connected to the power plane and the outer conductor connected to the ground plane, as shown in Fig. 2. Since the excitation mechanism of the simplified two-layer structure shown in Fig. 2 is the same as that of the original one shown in Fig. 1, i.e., the electromagnetic field within the power planes is excited by the vertical currents on the center conductors of the probes or on the vias, the simplified two-layer structure is equivalent to the four-layer one from the viewpoint of the induced noise voltage between the planes. A third probe is located at $(x_3, y_3)$ to obtain the noise voltage between the planes.

Differential and common-mode currents ($I_{\rm dm}$ and $I_{\rm cm}$), as opposed to $I_1$ and $I_2$, are used to facilitate circuit analysis in a differential system. The differential and common-mode currents, $I_{\rm dm}$ and $I_{\rm cm}$, are related to $I_1$ and $I_2$ as [15]

$$I_{\rm cm} = I_1 + I_2 \tag{2}$$

$$\text{and } I_{\rm dm} = \frac{1}{2}(I_1 - I_2). \tag{3}$$

The common-mode current $I_{\rm cm}$ is zero for an ideal differential system. However, in a practical design, $I_{\rm cm}$ is present due to various imbalances in the circuit, such as different lengths for the two traces forming the differential pair, skew in the differential driver, and mode conversion that occurs at discontinuities. Both differential- and common-mode currents contribute to the noise voltage induced between the planes. With reference to the three-port network representation in Fig. 3, the transfer impedances $Z_{3\rm cm}$ and $Z_{3\rm dm}$ due to differential and common-mode currents, respectively, are defined as

$$Z_{3\rm cm} \equiv \left.\frac{V_3}{I_{\rm cm}}\right|_{I_{\rm dm}=0, I_3=0} \tag{4}$$

$$\text{and } Z_{3\rm dm} \equiv \left.\frac{V_3}{I_{\rm dm}}\right|_{I_{\rm cm}=0, I_3=0}. \tag{5}$$

Since both $I_{\rm cm}$ and $I_{\rm dm}$ are sources of the induced noise voltage and the system is linear, superposition holds. Therefore, the noise voltage between the planes $V_3$ can be expressed in terms of $I_{\rm cm}$ and $I_{\rm dm}$ as

$$V_3 = Z_{3\rm dm} I_{\rm dm} + Z_{3\rm cm} I_{\rm cm}, \text{ for } I_3 = 0. \tag{6}$$

Equation (6) indicates that even in an ideal differential system where $I_{\rm cm}$ is zero, $I_{\rm dm}$ can still excite the power-bus if $Z_{3\rm dm}$ is nonzero. Therefore, a knowledge of $Z_{\rm dm}$ and $Z_{\rm cm}$ is essential in designing a low noise power-bus system. In the following, closed-form expressions are derived for $Z_{\rm dm}$ and $Z_{\rm cm}$.

A three-port network representation of a power-bus system being considered is shown in Fig. 3. The power-bus can be characterized by a three-port impedance matrix $[Z]$ as

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = [Z] \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{7}$$

where a port is defined by a pair of terminals located on opposite sides of the planes. The inductive behavior associated with the probes is assumed to be included in the $Z$-parameters. Applying (4) and (5) to (7), the differential and common-mode transfer impedances, $Z_{3\rm dm}$ and $Z_{3\rm cm}$, can be expressed as

$$\begin{aligned} Z_{3\rm cm} &= \left.\frac{V_3}{I_{\rm cm}}\right|_{I_{\rm dm}=0, I_3=0} = \left.\frac{V_3}{I_1 + I_2}\right|_{I_1 - I_2 = 0, I_3 = 0} \\ &= \left.\frac{Z_{31} I_1 + Z_{32} I_2}{I_1 + I_2}\right|_{I_1 - I_2 = 0, I_3 = 0} \\ &= \frac{Z_{31} + Z_{32}}{2}, \end{aligned} \tag{8}$$

$$\begin{aligned} \text{and } Z_{3\rm dm} &= \left.\frac{V_3}{I_{\rm dm}}\right|_{I_{\rm cm}=0, I_3=0} = \left.\frac{2V_3}{I_1 - I_2}\right|_{I_1 + I_2 = 0, I_3 = 0} \\ &= 2\left.\frac{Z_{31} I_1 + Z_{32} I_2}{I_1 - I_2}\right|_{I_1 + I_2 = 0, I_3 = 0} \\ &= Z_{31} - Z_{32}, \end{aligned} \tag{9}$$

where the equivalences $I_1 - I_2 = 0 \rightarrow I_1 = I_2$ and $I_1 + I_2 = 0 \rightarrow I_1 = -I_2$are used. Equations (8) and (9) show that $Z_{3\rm cm}$ and $Z_{3\rm dm}$ can be expressed in terms of $Z_{31}$ and $Z_{32}$.

## III. Experimental and Numerical Results

A double-sided rectangular test board with parallel conducting planes was constructed, as shown in Fig. 2, to validate the expressions for $Z_{3\rm cm}$ and $Z_{3\rm dm}$ in (8) and (9). The dimensions of the PCB in the $x$–$y$ plane were 15 × 10 cm, and the FR-4 dielectric layer was 1.1-mm (45-mil) thick. Three probes were constructed. The two feeding probes (ports 1 and 2) were located at (3, 4 cm) and (3, 4.23 cm) in the $x$–$y$ plane. The probes were closely spaced to form a differential feed with a spacing of 0.23 cm in the $y$ direction from center to center. The third probe (Port 3) was located at (10, 6.9 cm) to measure the voltage induced on the planes as a result of the currents $I_1$ and $I_2$ on the probes. All three probes were constructed using 0.047-in semirigid coaxial cables. The diameter of the inner conductors of the cables was 0.28 mm (11 mil), and the diameter of the outer shields was 1.2 mm (47 mil). The outer

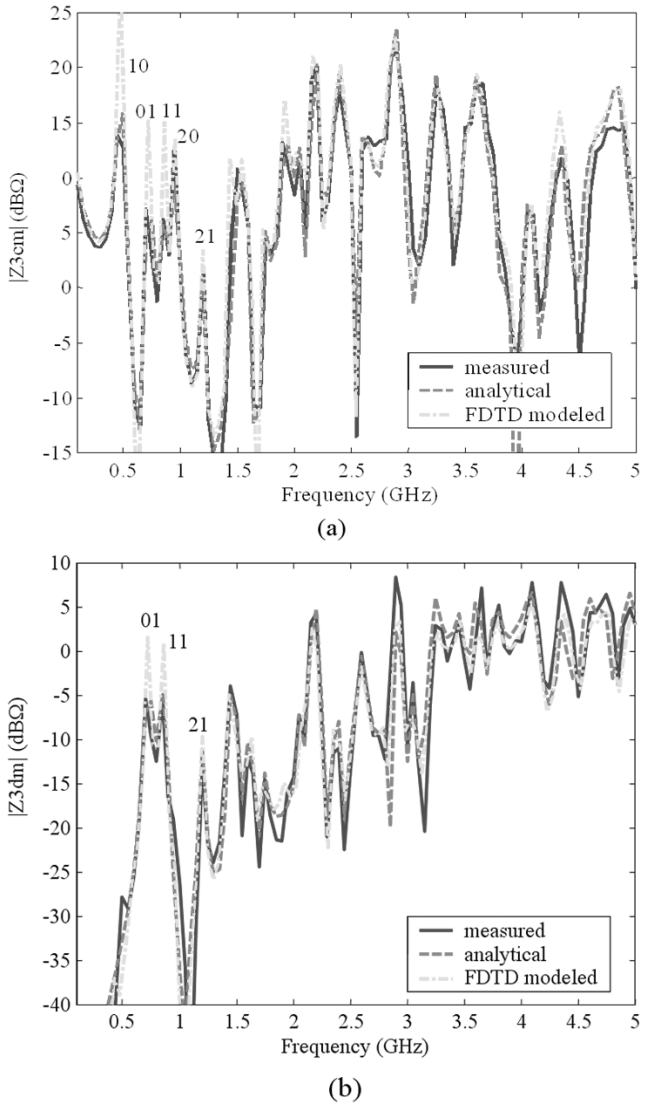


Fig. 4. Differential and common-mode transfer impedances of a 15 × 10 × 0.11 cm test board. (a) Common-mode transfer impedance. (b) Differential transfer impedance.

shields were soldered to the ground plane of the test board with a 360° connection, and the center conductors were soldered to the upper plane. On the other end of the cables, SMA connectors were attached. The SMA connectors were connected to an ATN-4112A multiport test system, combined with an HP8720ES network analyzer enabling three-port $S$-parameter measurements. The $Z$-parameters were calculated from the measured $S$-parameters using [16]

$$[Z] = z_0\left([U] + [S]\right)\left([U] - [S]\right)^{-1} \tag{10}$$

where $[U]$ is the identity matrix, and $z_0$ is the characteristic impedances assumed to be 50 Ω for all ports. The common-mode and differential-mode transfer impedances were obtained using (8) and (9), as shown in Fig. 4(a) and (b). The peaks in both $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$ correspond to the power-bus resonances. The first few distinguishable $\mathrm{TM}_{mn}$ modes are identified in Fig. 4. Employing a cavity model, all matrix elements $Z_{ij}$ in (7) can be calculated analytically for a rectangular parallel-plate area fill or power-bus as [17]–[20],

$$Z_{ij}(\omega) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{N_{mni}N_{mnj}}{\frac{1}{(j\omega L_{mn})} + j\omega C_0 + G_{mn}} \tag{11}$$

with $L_{mn} = (d/(\varepsilon ab\omega_{mn}^2))$, $C_0 = ((ab\varepsilon)/d)$, $G_{mn} = C_0\omega_{mn}(\tan\delta + (r/d))$, the dielectric loss factor given by $\tan\delta$, the skin depth given by $r = \sqrt{(2/(\omega\mu\sigma))}$, and the angular resonance frequencies $\omega_{mn} = (1/\sqrt{\varepsilon\mu})\sqrt{((m\pi)/a)^2 + ((n\pi)/b)^2}$ for mode indexes $m$ and $n$. The plane dimensions in the $x$ and $y$ directions are denoted as $a$ and $b$, respectively, and $d$ is the separation between the planes. From (11), a lumped equivalent circuit can be developed as shown in Fig. 5 [17], where the coefficient $N_{mni} = c_m c_n \cos((m\pi x_i)/a)\cos((n\pi y_i)/b)\mathrm{sinc}((m\pi W_{xi}/2a))\mathrm{sinc}((n\pi W_{yi})/2b))$ denotes the turns ratio of ideal transformers, considering the location of the port $(x_i, y_i)$ and the port widths $W_{xi}$ and $W_{yi}$ in the $x$ and $y$ directions, respectively. The constant $c_m, c_n = 0$ if $m, n = 0$, and $c_m, c_n = \sqrt{2}$ if $m, n \neq 0$.

The port geometry in (11) is assumed to be rectangular. In this paper, a coaxial feed was approximated as a square port with the same effective cross-sectional area as that of the circular feed port [21]. Therefore, the 0.047-in coaxial feed was approximated as a square port with each side equal to 0.1 cm. The FR4 material between the ground and power planes was approximated with a dielectric constant of 4.3 and a loss tangent of 0.02. A conductivity of $5.8 \times 10^8$ S/m (copper) was used for the ground and power planes. Analytical expressions for the differential and common-mode transfer impedances of a rectangular power-bus, $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$, can be obtained by substituting (11) into (8) and (9), respectively. The analytical results agree well with measurements in the frequency range from 100 MHz to 5 GHz, as shown in Fig. 4(a) and (b). Comparing results from the analytical expressions to those from measurements, the resonances agree within 5% for both $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$; the magnitude of $Z_{3\mathrm{cm}}$ agrees within 3 dB; and the magnitude of $Z_{3\mathrm{dm}}$ agrees within 5 dB of the measured value. It is more difficult to achieve agreement for the differential transfer impedance because imbalances may be introduced in the measurement. In addition, tolerances in the position of the two feeding probes on the test board which alter $Z_{3\mathrm{dm}}$ cannot be completely eliminated.

The finite-difference time-domain (FDTD) method was also employed to obtain the transfer impedances. The algorithm of perfectly matched layers (PML) was used for the absorbing boundary conditions [22]. A uniform cell size of 1.5 × 1.0 × 0.38 mm was employed such that the thickness of the board was discretized into three cells. The ground and power planes were modeled as perfect electric conductors (PEC). A Debye model was used to account for the loss of the dielectric material of the PCB, i.e., [23], [24]

$$\varepsilon_r(\omega) = \varepsilon_{r\infty} + \frac{\varepsilon_{rs} - \varepsilon_{r\infty}}{1 + j\omega\tau_r} - \frac{j\sigma_e}{\omega\varepsilon_0} \tag{12}$$

where $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m, $\varepsilon_{rs}$ and $\varepsilon_{r\infty}$ are the relative permitivity at zero frequency and at infinite frequency, respectively, and $\tau_r$ is the relaxation time constant. The FDTD simulation was conducted with $\varepsilon_{rs} = 4.3$, $\varepsilon_{r\infty} = 4.1$, and $\tau_r =$

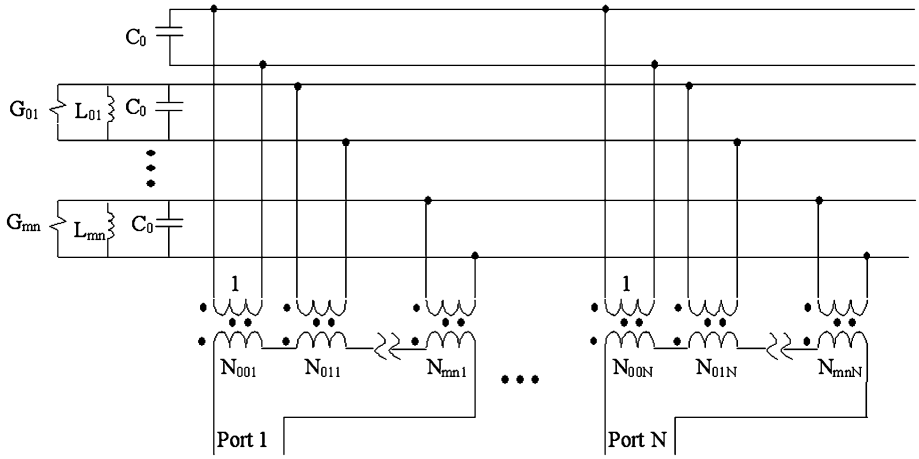


Fig. 5. Lumped equivalent circuit of a multiport power-bus system.

$4.19 \times 10^{-11}$ s. The conductivity of the dielectric material was set to $\sigma_e = 1.7 \times 10^{-3}$ S/m. The exposed center conductors of the probe cables from the ground plane to the power plane were modeled using a thin-wire subcellular algorithm [25]. A 1 MΩ lumped resistor was introduced at Port 3 between the ground and power plane to account for the open status of Port 3 for the transfer impedance calculation. The lumped resistor was modeled using a subcellular algorithm [26], with the encircling magnetic field components modified in the same fashion as for the thin-wire algorithm to give it specified cross-sectional dimensions. Two sinusoidally modulated Gaussian voltage sources, with a 50 Ω resistance incorporated into the source cell, were employed at ports 1 and 2. As with the thin-wire and resistive loads, the magnetic field components encircling the source cell were modified to give the source cell a specified cross-sectional dimension [27]. The source, the lumped resistor, and the thin-wire dimensions used in the FDTD modeling were 0.28 mm (11 mil), corresponding to the diameter of the center conductor of the 0.047-in coaxial cable.

Two simulations were conducted, one with the voltage sources at ports 1 and 2 of the same magnitude and the same sign to provide a common-mode excitation, and the other with the voltage sources of the same magnitude but opposite in sign to provide a differential excitation. The time history of the currents $I_1$ and $I_2$ on the thin-wires at ports 1 and 2, and the voltage drop $V_3$ across the resistor at Port 3 were simulated and recorded. The transfer impedances $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$ were obtained from FDTD using definitions (4) and (5), respectively. The dash-dotted curves in Fig. 4 from the FDTD simulations, agree well with the measurements and the analytical results. The higher peaks at lower frequencies may be because the dielectric loss was not sufficiently large in the Debye model. The transfer impedances $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$ from the FDTD simulations were calculated using definitions (4) and (5), as opposed to (8) and (9), and provides a further check on (8) and (9).

A four-layer board was also simulated with the FDTD method to verify that the via transition problem in a four-layer board can be reduced to the problem of a two-layer board shown in Fig. 2. Fig. 6 shows the geometry of the four-layer board with dimensions of $54 \times 33.5 \times 1.1$ mm. Layers 1 and 4 are the signal layers, while layers 2 and 3 are the power and ground layers, serving as reference layers for the signals.

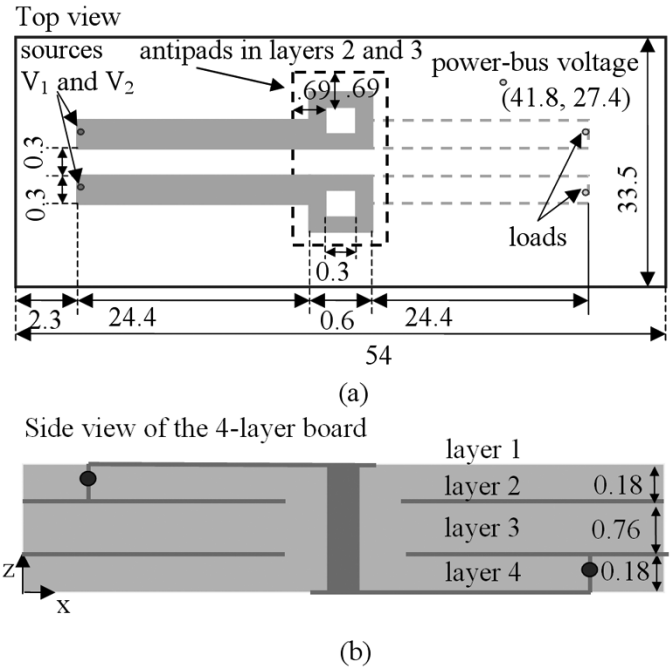


Fig. 6. Geometry of a four-layer board with via transitions in differential lines. (a) Top view. (b) Side view. Units: mm.

The spacing between the signal layer and its reference layer is 0.18 mm, while the spacing between the power layer and the ground layer is 0.76 mm. A pair of microstrip differential lines of length 24.4 mm was routed on layer 1, then transitioned to layer 4 through a pair of vias for another 24.4 mm, as shown in Fig. 6. The width and the edge-to-edge distance of the lines were 0.3 mm. For a substrate with a relative dielectric constant of $\varepsilon_r = 4.3$, the resulting differential impedance was approximately 100 Ω. The dimensions of the via hole were $0.3 \times 0.3$ mm, and the dimensions of the via pads on layers 1 and 4 were $0.6 \times 0.6$ mm. The edge of the antipad on the reference layers was 0.69 mm from the closest wall of the via hole. All dimensions were chosen to approximate current design parameters. The usual circular via cross section was approximated as a square cross section in the FDTD model for convenience. This approximation will not affect the physics of the excitation of the power-bus due to via transitions.

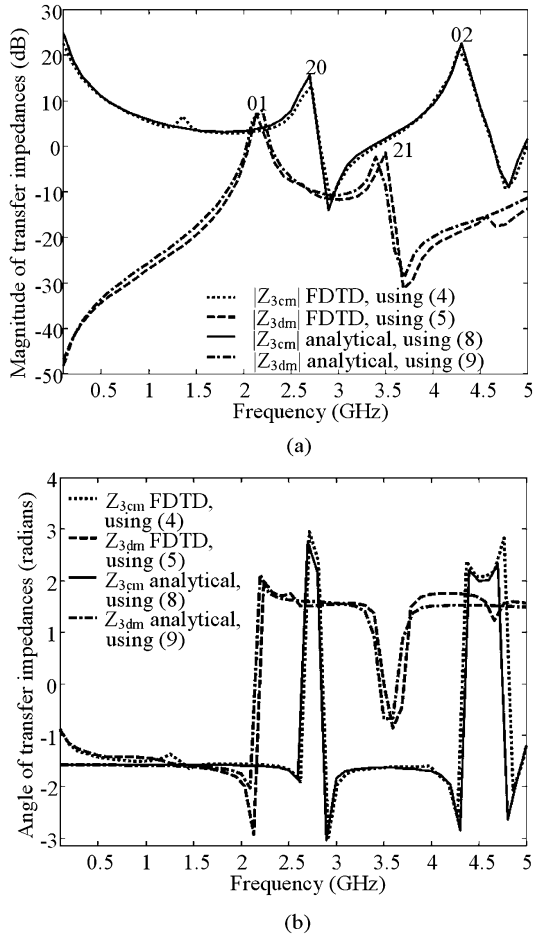


Fig. 7. Frequency responses of a four-layer board. (a) Common-mode transfer impedance. (b) Differential-mode transfer impedance.

A uniform cell size of $0.075 \times 0.075 \times 0.045$ mm was employed in the FDTD modeling, such that the spacing between the signal layer and its reference layer was discretized into four cells. Each trace width was also discretized into four cells. Since the focus here is to understand the physics of the power-bus noise due to differential via transitions, the dielectric loss is not critical and it was included in the FDTD modeling by simply using an effective conductivity [23]. The differential transmission lines were excited by two voltage sources at the source end. Each voltage source was a sinusoidally modulated Gaussian pulse with a 50-$\Omega$ internal impedance. Each line was terminated with a lumped resistor of 50 $\Omega$. Algorithms previously described in the two-layer FDTD simulation example were employed in the present case for modeling the sources, thin-wires, and lumped resistors. Two FDTD simulations were conducted, one with differential excitation ($V_1 = -V_2$) and the other with common-mode excitation ($V_1 = V_2$). The time history of the currents flowing through the two vias and the voltage between the power and ground planes at $(x, y) = (41.8,\ 27.4$ mm) were recorded. The time-domain signals were converted to the frequency-domain using a fast Fourier transform (FFT). The transfer impedances $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$ were calculated using (4) and (5), and are shown in Fig. 7. The $\mathrm{TM}_{mn}$ mode indexes associated with the rectangular power-bus resonances are marked in Fig. 7. The agreement between the results from the four-layer

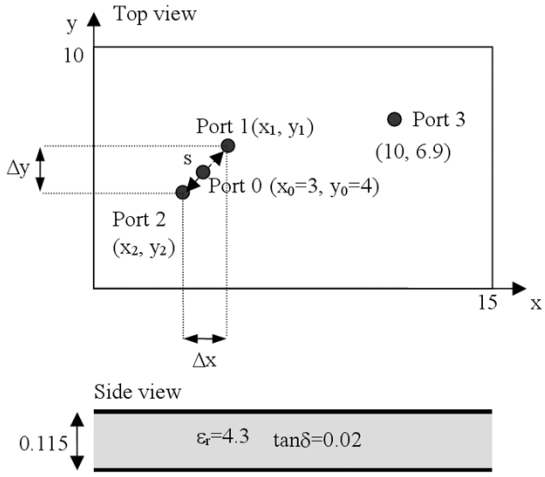


Fig. 8. Board geometry for engineering studies. Units: cm.

full-wave FDTD modeling using the definitions (4) and (5), and those from (8) and (9) using (11) is in general good. Therefore, the power-bus noise voltage due to via transitions in differential signaling on multilayer boards can be characterized through the differential and common-mode transfer impedances, which can be conveniently calculated using (8) and (9).

## IV. Design Applications

Two transfer impedances, $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$, were introduced to characterize the power-bus noise due to via transitions in differential signaling in the preceding section. In this section, the properties of $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$ are studied for design purposes. All the following studies are based on the geometry shown in Fig. 8.

### A. Influence of via Spacing on $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$

Equations (8) and (9) represent the general expressions for $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$ in terms of $Z_{31}$ and $Z_{32}$. However, from these expressions, the influence of via spacing is not directly visible. Fig. 8 shows the general configuration with the two vias at ports 1 and 2, and the observation point at Port 3. The transfer impedances $Z_{31}$ and $Z_{32}$ can be expanded into a Taylor series in the $x$ and $y$ directions, with respect to $Z_{30}$, which is the transfer impedance associated with Port 0 at the center point $(x_0, y_0)$ between the two vias (Fig. 8). Assuming that the via spacing $s = \sqrt{\Delta x^2 + \Delta y^2}$ is sufficiently small, the two transfer impedances can be approximated by the first-order Taylor expansion as

$$Z_{31} \approx Z_{30} + \frac{\partial Z_{30}}{\partial x}\frac{\Delta x}{2} + \frac{\partial Z_{30}}{\partial y}\frac{\Delta y}{2} \tag{13}$$

$$Z_{32} \approx Z_{30} - \frac{\partial Z_{30}}{\partial x}\frac{\Delta x}{2} - \frac{\partial Z_{30}}{\partial y}\frac{\Delta y}{2}. \tag{14}$$

Substituting (13) and (14) into the general expressions (8) and (9), $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$ can be approximated as

$$Z_{3\mathrm{cm}} = \frac{Z_{31} + Z_{32}}{2} \approx Z_{30}, \tag{15}$$

$$Z_{3\mathrm{dm}} = Z_{31} - Z_{32} \approx \frac{\partial Z_{30}}{\partial x}\Delta x + \frac{\partial Z_{30}}{\partial y}\Delta y. \tag{16}$$

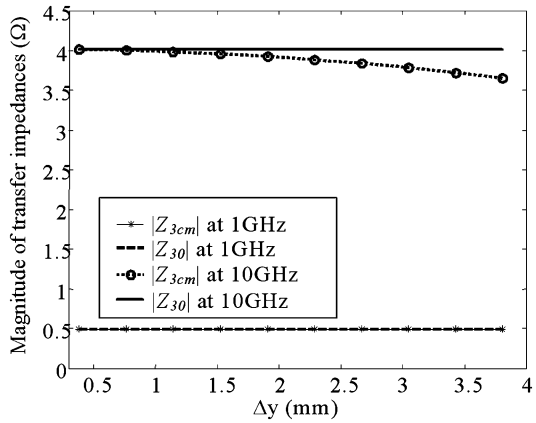


Fig. 9. $|Z_{3\mathrm{cm}}|$ as a function of via spacing.

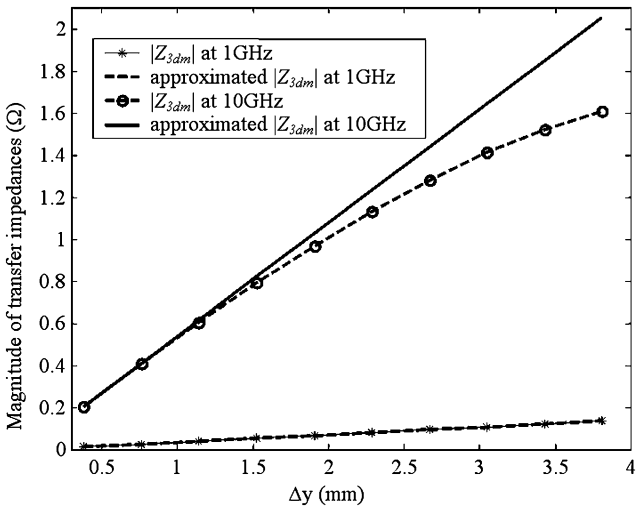


Fig. 10. $|Z_{3\mathrm{dm}}|$ as a function of via spacing.

Equations (15) and (16) indicate that $Z_{3\mathrm{cm}}$ is approximated by $Z_{30}$, which is independent of the spacing $s$, whereas the differential transfer impedance $Z_{3\mathrm{dm}}$ is proportional to the via spacing, expressed by $\Delta x$, $\Delta y$.

Expressions (8) and (9) together with (11) were employed to verify the approximations (15) and (16). Referring to Fig. 8, $\Delta x$ was set to zero and $\Delta y$ varied from 0.381 mm to 3.81 mm. Figs. 9 and 10 show the results for $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$, respectively, as a function of the via spacing, $\Delta y$. At 1 GHz, corresponding to a wavelength of 14.5 cm in the dielectric of $\varepsilon_r = 4.3$, $|Z_{3\mathrm{cm}}|$ is nearly constant as $\Delta y$ varies from 0.381 mm to 3.81 mm, while $|Z_{3\mathrm{dm}}|$ increases linearly with $\Delta y$. At 10 GHz, corresponding to a wavelength of 1.45 cm, the approximation in (15) is valid up to a spacing of $\Delta y < 1.5$ mm, with regard to an error limit of 10%. The linear approximation in (16) for $|Z_{3\mathrm{dm}}|$ holds up to $\Delta y = 1.5$ mm. Then, the validity of the approximations (15) and (16) is limited to a via spacing in the range of a tenth of the smallest wavelength of interest.

### B. Influence of Current Imbalance

The intentional differential current $I_{\mathrm{dm}}$ is usually known with sufficient accuracy from signal integrity analysis in a practical design, whereas the common-mode current $I_{\mathrm{cm}}$ is dominated by parasitics and by imbalances. The common-mode current $I_{\mathrm{cm}}$ depends on a number of different effects, such as driver-phase skew, termination imbalance, signal-path discontinuities and asymmetries, etc. It is determined by the specific design and is typically difficult to quantify. To study the influence of signal imbalance on the power-bus noise produced by differential via transitions, an imbalance factor $\kappa = I_{\mathrm{cm}}/I_{\mathrm{dm}}$ is introduced [10]. This factor is known to be at least in the range of a few percent in a practical design [28]. To assess the impact of signal imbalance on the noise voltage $V_3$, a total transfer impedance defined as

$$Z_t \equiv \frac{V_3}{I_{\mathrm{dm}}} = Z_{3\mathrm{dm}} + \kappa Z_{3\mathrm{cm}} \tag{17}$$

is considered. This general definition requires a knowledge of the magnitude and phase of $\kappa$. Therefore, an upper bound, in the sense of a worst-case estimate, is more suitable, i.e.,

$$|Z_t| = |Z_{3\mathrm{dm}} + \kappa Z_{3\mathrm{cm}}| < |Z_t|_{\max} = |Z_{3\mathrm{dm}}| + |\kappa|\,|Z_{3\mathrm{cm}}|\,. \tag{18}$$

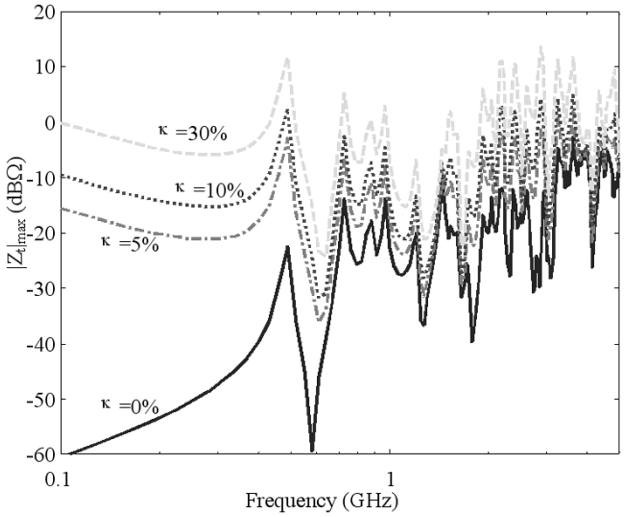


Fig. 11. The total transfer impedance for different current-imbalance factors k.

Fig. 11 shows an evaluation of the upper bound (18) of the total transfer impedance for different values of the imbalance factor $\kappa$ based on the geometry shown in Fig. 8 with $\Delta x = \Delta y = 0.381$ mm. An imbalance factor of only a few percent adds considerably to the noise-voltage level on the power-bus. For practical estimates, $|Z_t|_{\max}$ can be multiplied by the differential-mode current $|I_{\mathrm{dm}}|$ to obtain an upper bound of the noise voltage $|V_3|$. As an example, assuming a differential-voltage amplitude of 1 V and a differential-line characteristic impedance of 100 Ω, then the $I_{\mathrm{dm}}$ is in the range of 10 mA. Assuming an imbalance factor $\kappa = 10\%$, which is a representative value when dealing with imbalances on PCBs [28], $|Z_t|_{\max}$ is approximately 0 dB Ω from Fig. 11 at the $\mathrm{TM}_{10}$ resonance at around 480 MHz. This corresponds to a noise voltage $V_3 \approx 10$ mV, which is a relatively high value. In comparison, for a perfectly balanced differential signal, the noise voltage at this frequency would be 20 dB lower.

The noise voltages induced on the parallel planes due to differential signaling can also be compared to that due to single-ended routing to quantify the benefits of differential signaling relative to single-ended signaling. Consider a single-ended trace with a via transition located at Port 0 (the center between two differential vias), as shown in Fig. 8. The

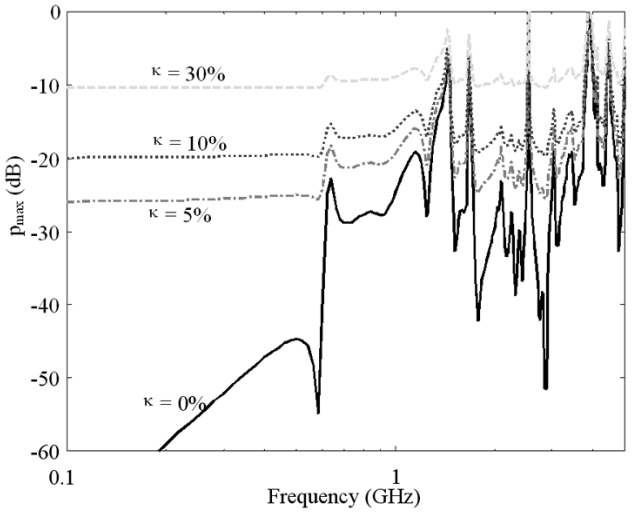


Fig. 12. The upper bound of differential-to-single ratio versus k.

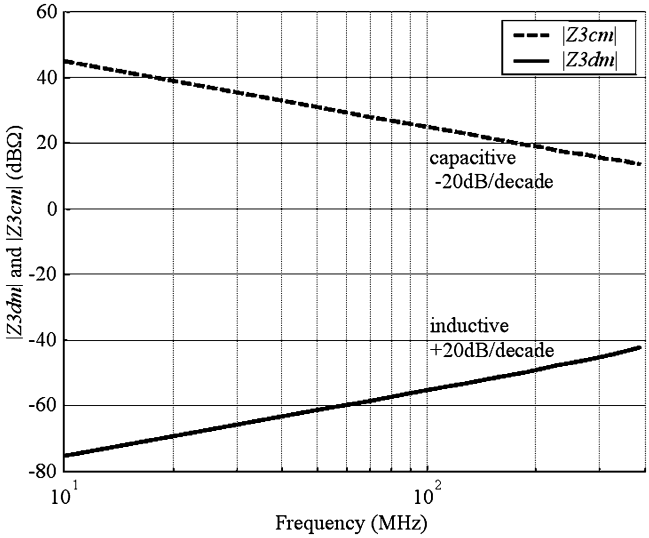


Fig. 13. $|Z_{3\mathrm{dm}}|$ and $|Z_{3\mathrm{cm}}|$ at low frequencies.

power-bus noise voltage due to the trace current $I_0$ flowing through a via transition is

$$V_{3\mathrm{sngl}} = I_0 Z_{30}. \tag{19}$$

Assuming equal currents ($I_0 = I_{\mathrm{dm}}$), the differential-to-single ratio of noise voltages $p$ can be defined as

$$p \equiv \left|\frac{V_3}{V_{3\mathrm{sngl}}}\right| = \left|\frac{Z_{3\mathrm{dm}} + \kappa Z_{3\mathrm{cm}}}{Z_{30}}\right| \approx \left|\frac{Z_{3\mathrm{dm}} + \kappa Z_{3\mathrm{cm}}}{Z_{3\mathrm{cm}}}\right| = \left|\frac{Z_{3\mathrm{dm}}}{Z_{3\mathrm{cm}}} + \kappa\right|. \tag{20}$$

In the above definition, $Z_{30}$ was replaced by $Z_{3\mathrm{cm}}$, according to the approximation (15). The upper limit of $p$ is then

$$p_{\max} \approx \left|\frac{Z_{3\mathrm{dm}}}{Z_{3\mathrm{cm}}}\right| + |\kappa|. \tag{21}$$

An evaluation of (21) is shown in Fig. 12 based on the same board geometry used to evaluate (18). It is indicated that when the imbalance ratio exceeds a few percent, the differential to single-ended ratio is approximately constant over frequency, neglecting the sharp peaks at the parallel-plane resonant frequencies. Referring again to an imbalance factor of $\kappa = 10\%$, the noise-voltage reduction due to differential signaling is between 10 and 20 dB. Fig. 12 is useful in comparing power-bus noise from the differential via transition with a single via transition or with the delta-I noise due to the switching-noise current through a supply via for a digital integrated circuit.

### C. Low-Frequency Behavior of $Z_{3\mathrm{cm}}$ and $Z_{3\mathrm{dm}}$

The transfer impedance $|Z_{3\mathrm{cm}}|$ is capacitive with capacitance equal to $C_0 = ab\varepsilon/d$, whereas $|Z_{3\mathrm{dm}}|$ is inductive, at frequencies much lower than the first resonance, as shown in Fig. 13 for $\Delta x = \Delta y = 0.38$ mm. Assuming the loss in the low-frequency range is negligible, the spacing between the two vias is much smaller than one tenth of the wavelength and $1/(\omega L_{mn}) \gg \omega C_0$, the impedance $|Z_{3\mathrm{dm}}|$ can be approximated as (22) at the bottom of the page Therefore, the associated inductance of $|Z_{3\mathrm{dm}}|$ at low frequency can be approximated as

$$L_{\mathrm{low\_freq}} \approx \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[L_{mn}N_{mn3}c_m c_n \mathrm{sinc}\left(\frac{m\pi W_x}{2a}\right) \times \mathrm{sinc}\left(\frac{n\pi W_y}{2b}\right)\begin{pmatrix} -\frac{n\pi\Delta y}{b}\cos\frac{m\pi x_0}{a}\sin\frac{n\pi y_0}{b} \\ -\frac{m\pi\Delta x}{a}\sin\frac{m\pi x_0}{a}\cos\frac{n\pi y_0}{b}\end{pmatrix}\right]. \tag{23}$$

The inductive behavior of $Z_{3\mathrm{dm}}$ can be interpreted using the equivalent circuit in Fig. 5 with the two via ports denoted as Port 1 and Port 2. Injecting two counter directed currents in Port 1 and Port 2 induces two voltage contributions on the circuit with $C_0$, representing the $\mathrm{TM}_{00}$ mode. Since the excitation of this mode is independent of the feeding position, i.e., $N_{001}$ and $N_{002}$ in (11) are equal and not a function of $(x_i, y_i)$, the two voltages across $C_0$ are also counter directed and cancel. Therefore, the $\mathrm{TM}_{00}$ mode, which is responsible for the capacitive behavior at

$$\begin{aligned} Z_{3\mathrm{dm}} &= Z_{31}(\omega) - Z_{32}(\omega) \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{N_{mn3}}{\frac{1}{(j\omega L_{mn})} + j\omega C_0 + G_{mn}}c_m c_n \mathrm{sinc}\left(\frac{m\pi W_x}{2a}\right)\mathrm{sinc}\left(\frac{n\pi W_y}{2b}\right) \times \begin{pmatrix} -2\cos\frac{m\pi x_0}{a}\cos\frac{\frac{m\pi\Delta x}{2}}{a}\sin\frac{n\pi y_0}{b}\sin\frac{\frac{n\pi\Delta y}{2}}{b} \\ -2\sin\frac{m\pi x_0}{a}\sin\frac{\frac{m\pi\Delta x}{2}}{a}\cos\frac{n\pi y_0}{b}\cos\frac{\frac{n\pi\Delta y}{2}}{b}\end{pmatrix}\right] \\ &\approx \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[j\omega L_{mn}N_{mn3}c_m c_n \mathrm{sinc}\left(\frac{m\pi W_x}{2a}\right)\mathrm{sinc}\left(\frac{n\pi W_y}{2b}\right)\begin{pmatrix} -\frac{n\pi\Delta y}{b}\cos\frac{m\pi x_0}{a}\sin\frac{n\pi y_0}{b} \\ -\frac{m\pi\Delta x}{a}\sin\frac{m\pi x_0}{a}\cos\frac{n\pi y_0}{b}\end{pmatrix}\right]. \end{aligned} \tag{22}$$

low frequencies, is eliminated. All other parallel circuits representing the other modes are inductive, as long as the frequency is below their resonances. Their excitation depends on feeding position and they add up to a total impedance that is inductive.

## V. Conclusion

Differential and common-mode transfer impedances, $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$, are proposed to facilitate analysis of dc power-bus noise that results from via transitions in differential signals. The properties of $Z_{3\mathrm{dm}}$ and $Z_{3\mathrm{cm}}$ are investigated. When the spacing between the two vias is less than one tenth of the wavelength at frequencies of interest, $Z_{3\mathrm{dm}}$ is linearly dependent on the spacing while $Z_{3\mathrm{cm}}$ remains constant with respect to the spacing. At frequencies below the first resonance of the power-bus, $Z_{3\mathrm{cm}}$ behaves as a capacitor while $Z_{3\mathrm{dm}}$ behaves as an inductance. A set of curves with various degrees of imbalances in the signal currents is generated to estimate the power-bus noise for practical designs. The benefit of differential signals compared to single-ended signals is also quantified.

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