Coupling Noise Analysis and High Frequency Design Optimization of Power/Ground Plane Stack-up in Embedded Chip Substrate Cavities

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Abstract

Future electronic systems demand faster, smaller, lighter and thinner products. Embedding Active and Passive components in package size boards is one of the major steps in accomplishing system level miniaturization and multifunctionality. All multifunctional system packages should pay attention to Signal and Power integrity for ensuring proper operation of the system. Predominant challenge encountered with respect to power integrity in mixed signal systems is coupling through the power distribution network. This coupling which is a form of noise affects power integrity if left unchecked, especially in case of embedded actives where there are large apertures (die sized) in the metal planes and cavities in dielectric to accommodate the chips. This paper for the first time brings out coupling noise analysis for different power/ground plane stack-ups in embedded chip substrate cavities.

1. Introduction

Embedded Actives is an enabling technology for ultra-miniaturization and system integration. Embedded actives are preferred compared to the surface mounted device technology as they are expected to reduce the parasitic effects of interconnects (reduced interconnect length) resulting in lower power dissipation and provide better electromagnetic shielding. They also offer smaller and thinner package profiles.

Embedded actives can be broadly classified into Chip first and Chip last approaches. Published works in the field of embedded actives focus mainly on the thin film embedded passives technologies and embedding actives using chip first approach [1 - 4]. Authors introduced the embedded actives using chip last approach for the first time and the preliminary design and process technologies were discussed in [5, 6]. In the Chip First approach, the wiring and build-up layers are formed above the chip. In the Chip Last approach the chip is placed in a cavity after all the wiring and build-up layers have been completed. The cavity which is formed in the substrates incase of Chip Last method is very important from design and process points of view. The characteristics of the cavity and the influence it will have on other package structures like transmission lines and power/ground planes need to be investigated and analyzed to understand the complete behavior of Chip last embedded chip module.

The authors introduced the concepts of electrical design involved in Chip last embedded actives and transmission line behavior in substrates with cavities by developing suitable high frequency models [6].

This paper has two sections: In the first section, the behavior of transmission lines in cavities (figure 1) is demonstrated with the help of transmission line loss response measurements validating the simulation model results. There is good model to measurement correlation with the insertion loss.

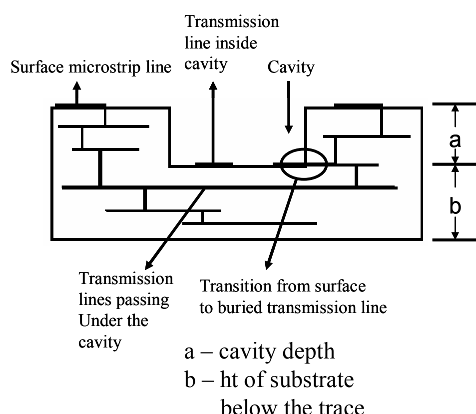

Fig1. Cross-section of Substrate with Cavity

The second section of the paper discusses power/ground plane stack-up in substrates with cavities. Test vehicles are fabricated to demonstrate the coupling effects in the different power/ground stack-up structures considered here. The test vehicles involve a 3 metal layer structure with Power/Ground/Power plane arrangement and uses photo-dielectric material for build-up layers. The cavities are opened by photo-via process and frequency domain measurements are performed on these to validate the simulations.

The paper also presents scope for further analysis on decoupling requirements needed to tackle the coupling caused by these large sized apertures.

2. Transmission lines in Substrate cavities

In case of chip last embedded actives there are cavities in dielectrics and there will be transmission lines inside the cavities to route the chip interconnections. Fig. 1 shows the

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schematic of the transmission lines investigated in embedded chip cavity design.

The analysis of the results for the models of transmission lines within the cavity shows that the line will behave similar to a surface microstrip provided the substrate height below the trace in both cases is maintained the same. The insertion loss for the line inside the cavity is the same as that with a thin substrate.

This analysis also includes investigation of lines inside the cavities, buried transmission lines, the transition of surface micro strip lines to buried lines, the proximity of the transmission lines to the dielectric cavity wall, and the influence of the cavity sizes. [6] gives detailed explanation of these parametric variations with appropriate simulation and preliminary measurement results.

For a given substrate height when the cavity depth is changed (when a, as shown in fig1, is changed) the substrate height below the trace on the cavity surface will also change (b, as shown in fig1, changes as well) and this will cause all lines to have widths of varying values to maintain standard impedance matching. The behavior of these buried lines is dependent on the height of the substrate above them and when this height keeps changing, the line width will need modification at all the regions where the line crosses the cavity. It is recommended to route the buried traces with a distance of about 0.2mm from the cavity base [6].

All the lines which are laid within a cavity need to be extended out in order to be routed to different layers. These lines become buried micro strips when extended outside the cavity. The transitions need to be properly characterized to avoid impedance mismatch. The effect of cavity width on the transmission lines within the cavity and the dielectric wall proximity also need to be accounted for.

Here test vehicles (layout is shown in fig 3) have been fabricated with transmission lines within cavities and fig 4 shows comparison of simulation and measurement results. The graph shows reasonable agreement (--0.1 dB and -0.3 dB at 3 GHz and -0.72 dB and -0.8 dB at 10 GHz for model and measurement respectively for a 0.9 cm long transmission line) between the two results. These results show the similarity in the behavior of microstrip transmission lines on substrates as thin as that beneath the cavity with those inside the cavity.

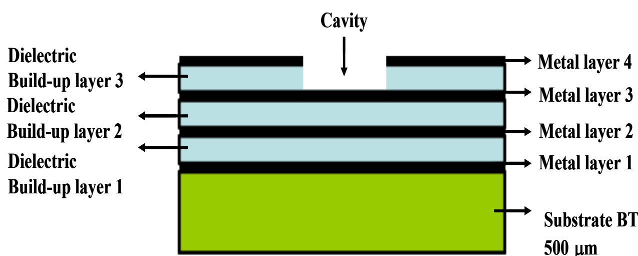

Fig2. Cross-section of the Test Vehicle

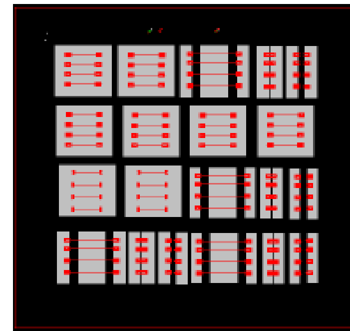

Fig3. Test Vehicle Layout with Transmission Lines in Cavities

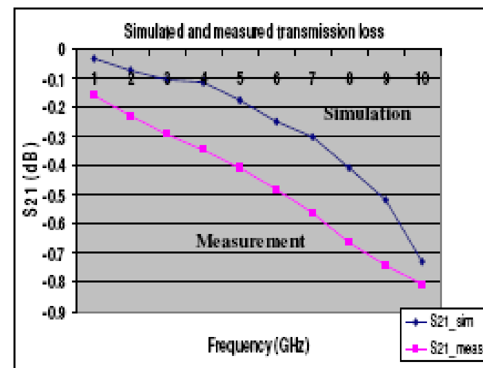

Fig4. Comparison of Measurement and Simulation Results

3.0 Power and Ground Planes in Substrates with Cavities

The Chip-last method of embedded chips involves the presence of cavities in the substrate dielectric material to embed the chips. As shown in figure 5 the presence of these cavities causes large apertures on power/ground planes present in the package. The presence of these apertures results in very significant levels of noise coupling from one power ground cavity to another. This part gives an introduction on how important the analysis of coupling noise is, followed by the resonance phenomenon observed in different power/ground plane stack-up structures, the modeling requirements for analyzing such structures using electromagnetic solver tools, fabrication and measurement procedures involved for the test vehicle and finally discussion of results.

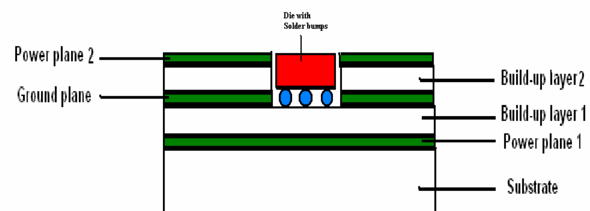

Fig5. Model of a Package with Embedded Die in a Cavity and Power/ground Plane Stack-up

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3.1 Power/Ground Coupling Noise in Substrates with Cavities

As the semiconductor industry progresses through each technology generation node, there is an increase in chip power dissipation and current consumption. With the frequency of operation rising, this increase in switching current increases the Simultaneous Switching Noise (SSN). This power supply simultaneous switching noise causes fluctuations in the voltage that is supplied to the chips and also gets coupled to power ground cavities other than the one in which the noise is generated if there are slits, openings or even vias present in the power/ground planes [7].

Using split power planes in mixed signal systems is an important cause for this coupling phenomenon. Analysis of cutouts and slits on planes to isolate plane sections in multilayer substrates has been reported in literature [8]. But this analysis is for very thin slits and cutouts whose width is much smaller as compared to their lengths. The resonant frequencies where the coupling between adjacent power ground plane cavities is significant are predictable by using the common rectangular waveguide TEM mode resonant frequency formula. But in cases having large sized apertures, strong coupling occurs not only at the regular resonant frequencies but also at other unexpected frequencies. The apertures that are formed in substrates with embedded chips are large enough to accommodate the dies. Such large sized apertures cause significant coupling at frequencies other than the plane resonant frequency in addition to resonant frequency coupling.

Another phenomenon observed is in the case of having apertures on successive metal layers. This case occurs in chip-last embedded actives where depending on the thickness of the die the cavity depth can cut across more than one plane as shown in figure 5. These conditions again result in modification of the coupling phenomenon observed at resonant frequencies. The following section will explore the application of software tools to model and analyze structures having cavities and power/ground planes.

3.2 Design and modeling of structures with dielectric cavities and apertures in metal planes

The analysis of the coupling that arises in the presence of large-sized apertures is performed on different power/ground stack-up structures that exist in packages and this demonstrates the coupling behavior and the need for such an analysis to effectively implement power/ground stack-up in substrates housing embedded chips. The modeling requirements to analyze the cavity effect on power/ground planes are also demanding as a full wave 3D solver is required to accurately model the structure. This section introduces 3 different structures as shown below and we investigate the suitability of tools to validate the coupling analysis of these structures.

Structure 1

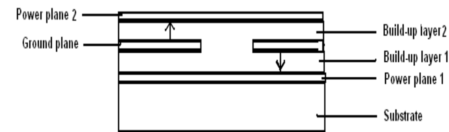

Fig6. An aperture of about the size of the die is present in the center plane

Structure 2

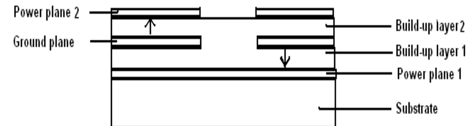

Fig7. Apertures to Accommodate the Die are Present in the Top and Center Planes

Structure 3

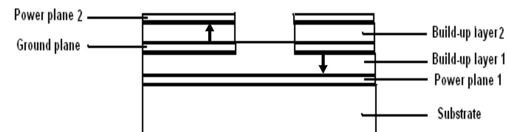

Fig8. Apertures are Formed in the Top and Center Planes and Dielectric Material is Removed to Form the Cavity in which the Chip can be Buried.

The arrows indicate ports which are used to excite the planes.

The 1st structure, Structure 1 involves only a single metal aperture. This structure can be adequately modeled and simulated using a 2.5D or a 3D electromagnetic solver to get coupling noise information. In addition to the commercially available tools we also use an in-house GT tool in the validation process. This structure is primarily to gain confidence in the modeling methodology of the 3D solver.

- 3D EM solver – Ansoft HFSS
- 2.5D planar solver – Sonnet
- MSDT tool – tool developed at Georgia Tech

Structure 2 can again be modeled by both Sonnet and HFSS and this gives an insight into the effect of opening apertures on successive metal layers. Structure 3 which involves a dielectric cavity requires a full wave 3D solver to appropriately model it. So we use HFSS for this.

Material and size specifications for the structures designed -

- Lateral size of the planes used is 10 X 20 mm
- Cavity size (die size) – 7 X 7 mm
- Dielectric material used – Probelec81
- Thickness of the dielectric layers – 50 m
- Dielectric constant – 3.4, Loss tangent – 0.015
- Thickness of the planes – 0.01mm
- Substrate core – BT (thickness – 0.5mm)

In all these structures Port 1 (present in the lower power/ground cavity) is excited and the S-parameter S21 is plotted to observe the noise that is getting coupled to the un-excited port 2 in the upper power/ground cavity. In the ideal

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case, when the planes are fully continuous the S21 values should be very low (negative values), indicating almost zero coupling. But the presence of openings in the planes causes the electric field to couple from one power/ground cavity to another [8]. For the dimension of the planes that is considered here, the (1, 0) mode occurs at 4.06 GHz, (0, 1) mode occurs at 8.12 GHz and (1, 1) mode occurs at 9.1 GHz. From figure 9 we can see that, coupling between adjacent power/ground cavities is significant not only at these resonant frequencies but also at others such as 2.6 and 6.2 GHz. The size of the aperture with respect to the total plane dimensions is the reason for picking up additional coupling at non-resonant frequencies. This also makes simulations of these structures very important because it is hard to predict the non-resonant frequencies at which coupling gets significant.

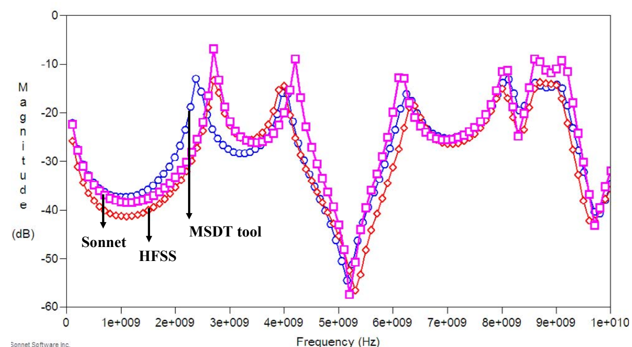

Fig9. S21 (dB) Coupling in Structure 1 – Comparison of HFSS, Sonnet and MSDT Tool Results

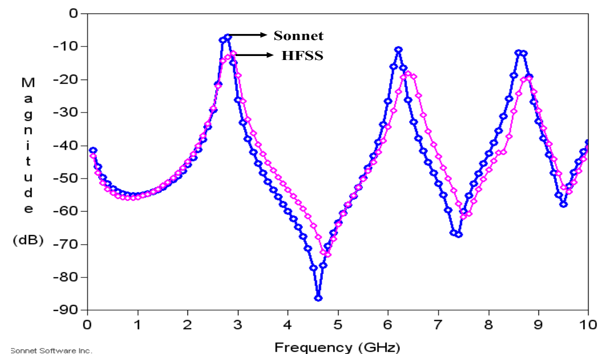

Fig10. S21 (dB) Coupling in Structure 2 – Comparison of HFSS, and Sonnet Results

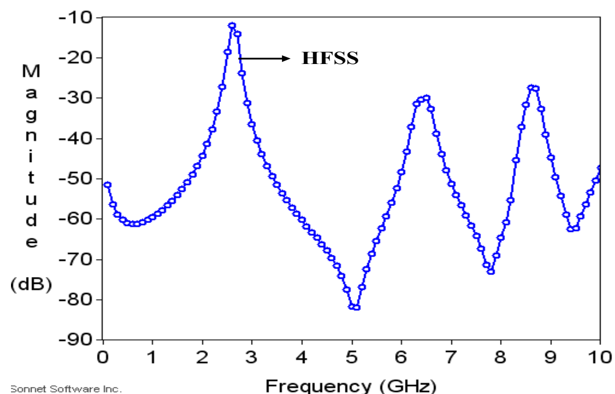

Fig11. S21 (dB) Coupling in Structure 3 – HFSS Result

Figure 9 shows the results for Structure 1 showing the additional resonances that are picked up. Figure 10 shows that when apertures are opened on successive metal layers, the coupling at original resonant frequencies disappears and those at the non-resonant frequencies continue to exist. The resonances shift with increase in the size of the aperture from their original frequencies of occurrence. Figure 11 (from Structure 3 with a dielectric cavity) produces a result very similar to that of Structure 2. Structures 2 and 3 also show about 15-20dB lesser coupling upto 2 GHz as compared to Structure1. The graphs above are results from different EM solver tools and they are used to validate modeling methodologies and to get a first hand idea of the responses of the planes before proceeding for fabrication of test vehicles. These results show that coupling between adjacent power/ground plane cavities can be very significant incase of adapting to Chip-last method of embedded actives.

3.3 Fabrication of Test Vehicle for Power/Ground Plane Stack-up

Cavity formation procedure for Chip-last embedded chip process is adopted from Micro-via formation processes such as photolithography, plasma etching and laser drilling. The merits and drawbacks of each of these processes are well documented in [5]. As advocated by [5], we follow the photo-lithography process as it is of low cost and supports mass cavity generation.

As shown in the figure below the test vehicle consists of 3 metal layers and 2 build-up dielectric layers.

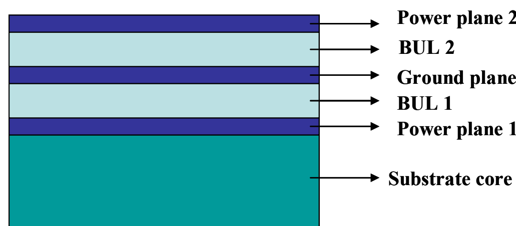

Fig 12.Power/Ground Plane Stack-up used for Fabrication

Photo-imageable dielectric (PID) Probelec-81/7081 (Huntsmann–Vantico Inc.) is used for dielectric build-up layers. For substrates, Cu-clad BT (Bismaleimide Triazine) of 500 μm in thickness is used. The thickness of each of the dielectric layers is 50μm (with a tolerance of +/- 5 μm) and metal layer is 10 μm thick. A detailed description of the stacked build-up process is given in [5]. The primary concern during the fabrication processes was the shorting of adjacent metal planes through the cavity opening during electrolytic plating. The photoresist that covers the electroless copper plated seed layer bends at the cavity edge and forms crinkles at the bends causing the electroplating copper to seep through. This will short adjacent metal planes. So a stepped cavity structure is adopted for Structures 3 involving cavities in dielectric layers. But this is not encountered when there are no dielectric cavities as in Structures 1 and 2. As shown in the figure below a 100 μm clearance is provided on either side to avoid the copper from reaching the next layer.

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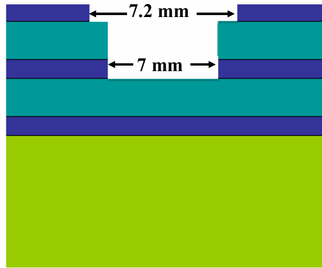

Fig13. Stepped Cavity Structure

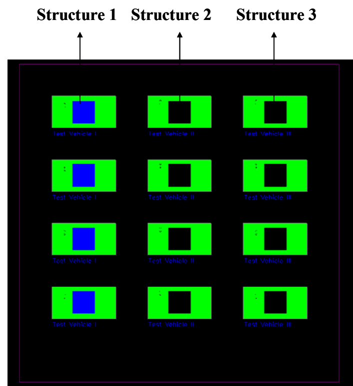

Fig14. Test Vehicle layout with 3 Different Structures for Power/Ground Stack-up

3.4 Comparison of Measurement and Simulation Results

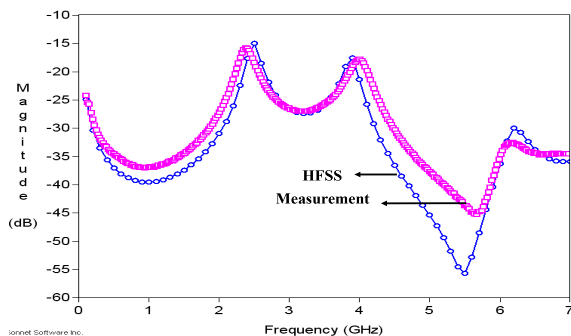

Fig15. Comparison of Simulation and Measurement Results for Structure 1

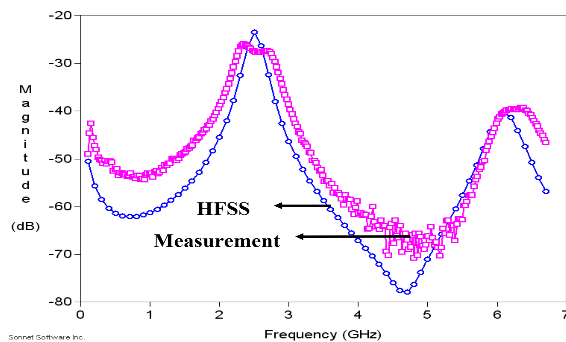

Fig16. Comparison of Simulation and Measurement Results for Structure 2

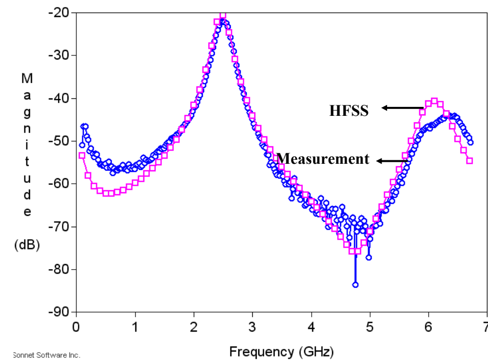

Fig17. Comparison of Simulation and Measurement Results for Structure 3

The measurement and simulation results in figures 15, 16 and 17 show reasonable agreement. The measurements are done upto a frequency range of about 6.5 - 7 GHz. This is because the test vehicles had some metal traces in the regions between the vias and further micro-etching resulted in a situation endangering the probe pads. The metal traces cause some shorting issues at higher frequencies. We show the comparison between HFSS and measurement results as HFSS is the EM tool that can support the modeling of Structure 3 which has the dielectric cavity like in the real chip last embedded active process.

The following section describes the influence of variations in physical parameters in the coupling noise response.

3.5 Parametric Variations Influencing the Coupling between Power/ground Plane Cavities

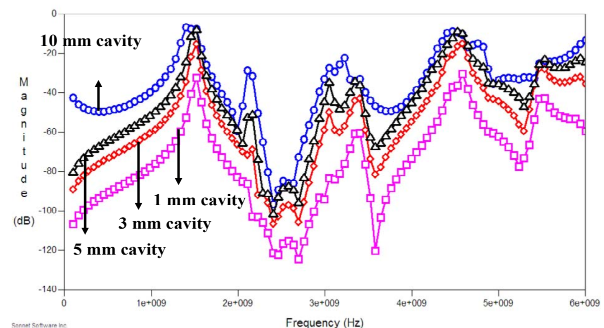

Fig18. S21 (dB) Plots for Cavities of Different Sizes

The presence of large apertures in the metal planes and the removal of dielectric material to form the cavity all influence the power/ground cavity coupling. This dictates the amount of decoupling required and the module size decides the placement of capacitors to counter the noise issue.

The factors that primarily influence the coupling patterns are the sizes of the dielectric cavities and apertures on metal planes, the depth of the cavities and the apertures formed on successive metal layers due to the presence of cavities. As shown in figure 18, increase in the cavity size causes an increase in the magnitude of coupling. So when deciding on the methods to mitigate the coupling the factors of concern

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are the size of the planes in the module, the cavity size, and the coupling noise tolerance for the application.

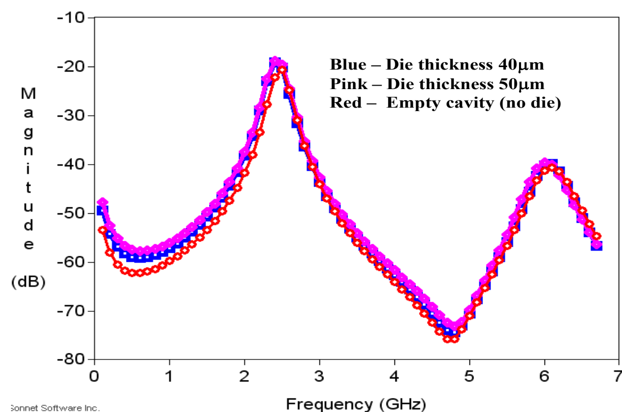

Fig19. S21 (dB) plot for Structure 3 with Silicon Die Embedded in the Cavity

3.6 Models with Silicon Chip

The simulations and measurements so far were without any die embedded in the cavity. They analyzed the influence of the cavity by itself. Here we perform simulations including the silicon die inside the cavity. The Structure 3 was simulated with silicon chip embedded in the dielectric cavity; the results are similar to the case without the silicon chip. The chip was modeled as a silicon tile inside the cavity. The presence of a material inside the cavity doesn't seem to show any considerable variation in the coupling magnitude as shown by the simulations. The presence of the cavity by itself is a predominant factor and this shows that when having dies inside it, the high level of coupling that occurs can cause a lot of issues related to noise. This points to the necessity of having adequate decoupling schemes to control the coupling that occurs.

4. Conclusions

Chip-last method of embedding chips involves cavities in substrates within which active dies are embedded and this paper has presented the validation of measurement and simulation results for transmission line behavior in substrates with cavities and summarized the findings from parametric variations that influence the loss responses of transmission lines in cavities.

Power/Ground cavity noise coupling is another predominant issue in miniaturized modules with embedded actives. This paper has analyzed different power/ground stack-up structures in chip-last embedded actives technology and obtained the coupling noise responses. Test vehicles have been fabricated incorporating the different structures and the simulation results from electromagnetic solver tools have been validated with frequency domain based VNA measurements. This analysis on coupling phenomenon in cavity based substrates has also given insight into the effect of parametric variations such as cavity sizes, apertures on successive metal layers, and presence of dielectric cavities on the noise coupling from one power/ground cavity to another and this paper accounts for these.

This study will be continued to further investigate the resonance pattern behavior and also ways to provide decoupling to suppress the coupling noise.

5. Acknowledgments

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