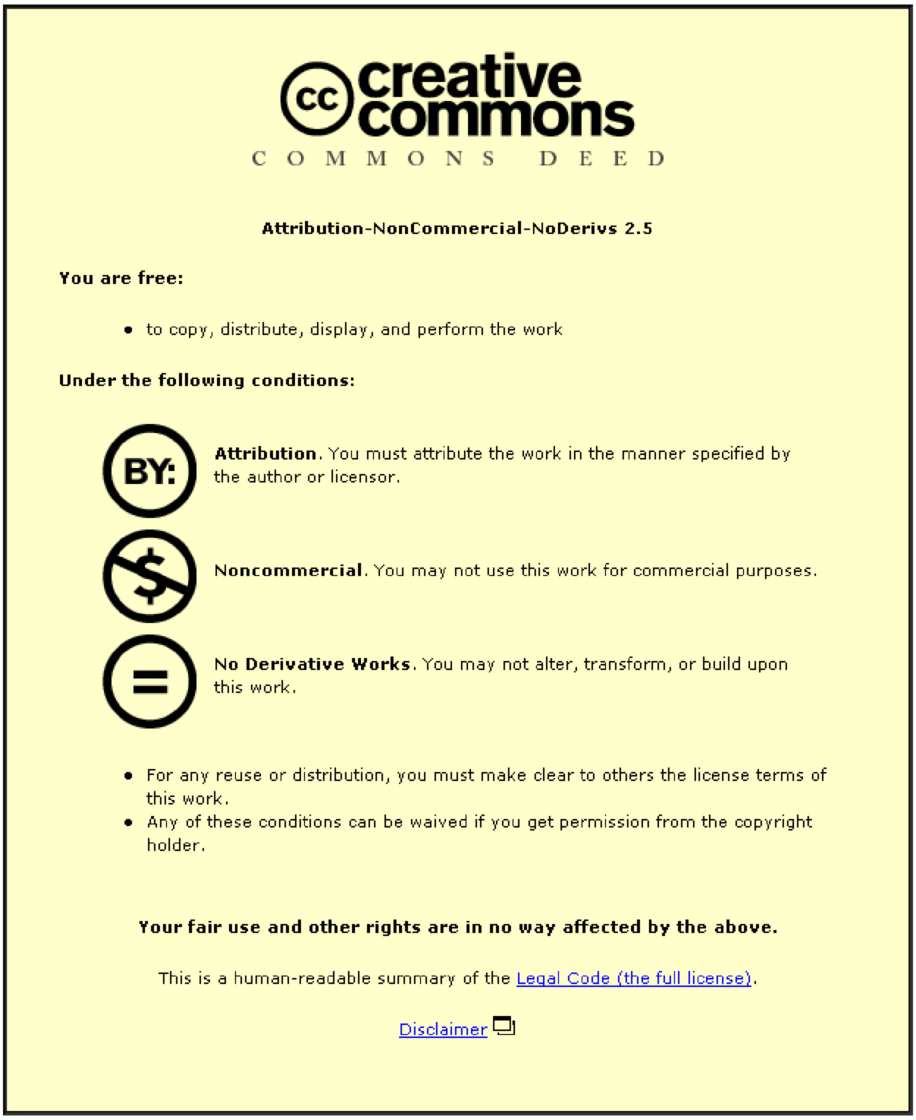
This item was submitted to Loughborough's Institutional Repository (https://dspace.lboro.ac.uk/) by the author and is made available under the following Creative Commons Licence conditions.



creative commons

COMMONS DEED

Attribution-NonCommercial-NoDerivs 2.5

You are free:

- to copy, distribute, display, and perform the work

Under the following conditions:

Attribution. You must attribute the work in the manner specified by the author or licensor.

Noncommercial. You may not use this work for commercial purposes.

No Derivative Works. You may not alter, transform, or build upon this work.

- For any reuse or distribution, you must make clear to others the license terms of this work.
- Any of these conditions can be waived if you get permission from the copyright holder.

Your fair use and other rights are in no way affected by the above.

This is a human-readable summary of the Legal Code (the full license).

Disclaimer

For the full text of this licence, please go to: http://creativecommons.org/licenses/by-nc-nd/2.5/

Creep Analysis of a Lead-free Surface Mount Device

Pradeep Hegde, David Whalley, Vadim. V. Silberschmidt
Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire, LE11 3TU, UK

Abstract

In this paper finite element analysis (FEA) is used to understand the effect of a non-uniform temperature distribution on the creep and fatigue behaviour of lead-free solder joints in an electronic assembly comprising of a chip resistor mounted on printed circuit board (PCB). Solder joints in surface mount devices (SMDs) operate over a temperature range as extreme as -55^{o}C to 125^{o}C, which is high compared to the melting temperature of solder alloys. Exposure of solder joints to these temperatures can result in thermo-mechanical fatigue. Eutectic or near- eutectic tin-lead alloys have previously been used as an interconnection material, but the ban imposed on the use of toxic materials in electronic products demands new lead-free solder materials. This paper presents the experiments carried out using a thermal camera to obtain the real temperature distribution in the electronic assembly. These temperature distributions were used in FEA of the chip resistor under temperature cycling conditions. Unlike accelerated tests for obtaining reliability data, FEA is quick and less expensive.

1. Introduction

The environmental impact of lead in electronic products is relatively low, but due to the size of the industry, is becoming a major concern all around the world. The stimulus for the "green movement" is market trend's and customers' perception. Therefore, manufacturers, suppliers and research institutes around the world are investing their efforts into developing lead-free soldering technologies to substitute for tin-lead solder alloys. In addition, researchers are also pondering the pressing need to find a high-performance solder alloy with improved mechanical properties and similar processing characteristics to tin-lead solders [1].

The reliability of lead-free solder joints is still a major concern due to their widespread application in the electronic industry only very recently and therefore there is not a great deal of material data or practical experience available. In this study a near-eutectic lead-free SnAgCu (SAC) solder alloy, with a melting temperature of 217^{o}C, is considered because it is being widely adopted due to its excellent wetting and mechanical properties [2]. When the solder is subjected to a cyclic stress induced by thermal cycling, the reliability of the solder joint depends on its resistance to fatigue. Along with thermo-mechanical fatigue, solder joints are subjected to creep as they operate at high homologous temperatures (T_g, the ratio of absolute operating and melting temperature). In this study a solder joint is subjected to thermal cycles between -55^{o}C and 125^{o}C. This means that they operate between T_g = 0.44 and T_g = 0.81. It is well documented [3] that creep plays a very important role in deformation behaviour of materials at homologous temperatures close to and above 0.5 if the loading rate is slow enough for creep damage to occur. Since under actual service conditions, the temperature cycle duration is in the order of minutes to days and the homologous temperature is more than 0.5, solder joints formed using SnAgCu alloy are expected to deform primarily due to creep [3]. This is essentially the same as for SnPb solders, but much less is known about the creep fatigue response of Pb free alloys.

Research into the use of finite element analysis (FEA) has been widely carried out to understand the elasto-plastic and creep behaviour of solder joints exposed to uniform (isothermal) temperature cycling conditions [1,3,4,5]. Thermo-mechanical analysis of a chip scale package (CSP) assembled using both lead-free and lead containing solder materials [1] and thermal cycling analysis of flip-chip solder joint reliability [5] are examples. However, experimental studies show that the temperature distribution within an electronic assembly is non-uniform due to different heat dissipation rates in the constituents of the electronic assembly. In addition, the mass distribution within the electronic assembly results in a non-uniform distribution of temperature during rapid changes in ambient temperature or power dissipation. Therefore, this paper focuses on the use of FEA to investigate the effect of a non-uniform temperature distribution on the creep behaviour of SAC solder joints in surface mount devices and a comparison is made with that for an uniform temperature distribution. The finite element analysis is first used to estimate stresses/strains due to cooling from reflow and then three different thermal cycling conditions are applied.

2. Experimental analysis

2.1 Experimental set up

In order to establish an appropriate magnitude for the non-uniform temperature distribution in the electronic assembly, a series of experiments were carried out to acquire the temperature profile in a flip chip assembly under power cycling conditions, using an infrared (IR) camera. Although this flip chip is different to the component (chip resistor) modelled, the general size and interconnection joint distribution makes both flip chip and chip resistor assemblies roughly comparable and means the flip chip experimental results will provide an indication of the temperature gradients to be expected in the chip resistor. The camera measures thermal radiation from the surface, which has a wavelength spectrum and intensity dependent on its temperature, structure and composition. The higher the temperature, the more the radiation emitted. This infrared radiation, not perceptible with the naked eye, is made visible and measurable by the infrared camera. By analysing this infrared radiation it is possible to measure temperature as well as, indirectly, the thermal conductivity, mechanical stresses, material compositions, defects such as pores and delamination, and various other kinds of inhomogeneities in the materials.

The IR camera used (Fig. 1) has an IR detector head with a focal plane array (FPA) detector sensitive in the range 1 µm – 14 µm. An infrared microscopic lens MWIR 2.5X, with a focus distance of 21-22 mm was used. The camera is interfaced with software to control real-time acquisition and analysis of the infrared data.

The specimens used were identical flip chip assemblies attached to either a copper or FR4 substrate. They were mounted vertically and powered at 1.2 W and cooled by free convection.

The flip chip specimens were silicon-on-silicon multi-chip modules (MCMs) the same as those used in a previously reported experiment [6]. Both MCMs consisted of a 3 mm × 3 mm × 0.5 mm “heater” chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The “carrier” chip was larger at 6 mm × 6 mm × 0.5 mm and included larger ball grid array type pads allowing for external connections to be made, as well as the corresponding pads to match those on the heater chip. The heater chip was attached to the carrier chip so that a standoff height of 35 µm was achieved (without underfill). The MCMs were subsequently attached to the corresponding substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Fig. 2.

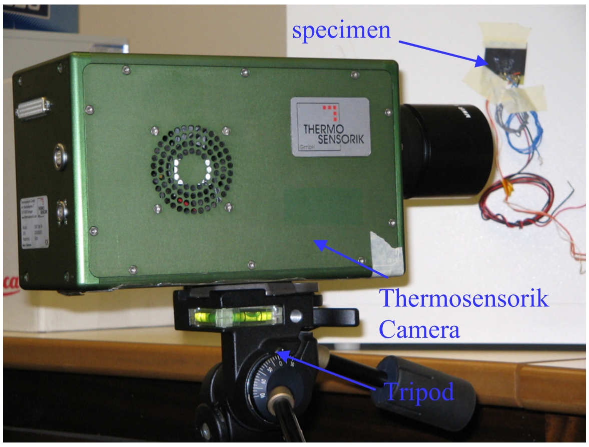


Figure 1 Experimental setup

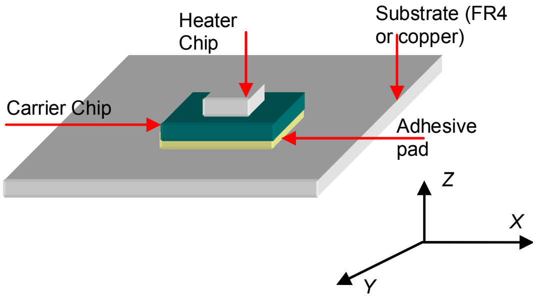


Figure 2 Schematic of flip chip specimens

Figure 1 shows the experimental setup, used for acquiring the temperature data for the flip chip assemblies. The camera, fitted with the micro lens, is mounted on the tripod, the specimen is powered on for few minutes to stabilise the temperature distribution in the specimen, then the lens is focused on the specimen and the temperature profile is captured.

2.2 Experimental results and discussion

The temperature distributions over the chip for a continuous 1.2 W power dissipation are given in Figs. 3 and 4 for free convection. The path used for subsequent temperature distribution analysis, is also shown. These figures demonstrate the effect of the substrate on the chip temperature distribution: the copper substrate results in lower temperatures compared to the FR4 substrate. From comparison of these two temperature profiles, the temperature distribution is symmetric on the chip with a

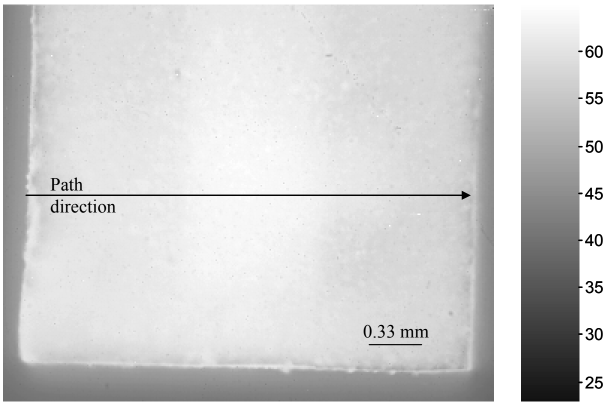


Figure 3 Temperature distributions in a chip mounted on a copper substrate at 1.2W

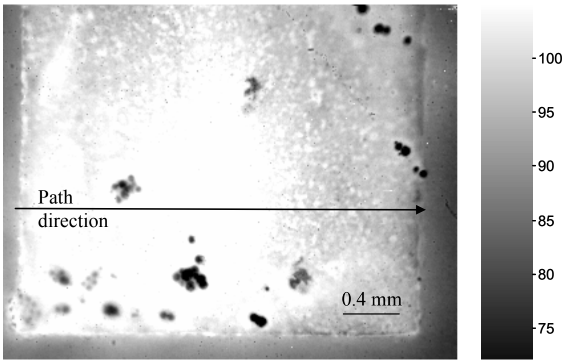


Figure 4 Temperature distributions in a chip mounted on FR4 substrate at 1.2 W

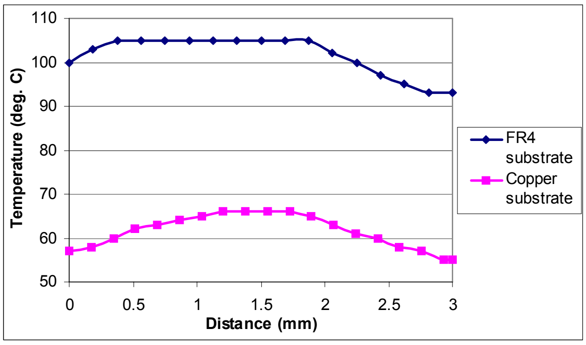


Figure 5 Effect of substrate on temperature distribution in the chip for free convection

copper substrate, while that for the chip with a FR4 substrate is asymmetric. The cool appearing patches may be attributed to non-uniform application of the black paint which is applied to ensure a higher uniform emissivity of the chip surface. Figure 5 shows the temperature distribution across the width of the chip for both types of substrate. It is evident that these temperature distributions are non-uniform: the maximum temperature is observed at the centre of the chip, where the heat is generated, while its boundary is at a lower temperature. Another important observation of this analysis is that the FR4 substrate induces higher thermal gradients in the chip than the copper substrate. This can be explained by the much higher thermal conductivity of copper compared with FR4. The experimental temperature distribution in the chip with a FR4 substrate is used as one of the thermal load cases for creep analysis, as it best represents typical operating conditions of the chip modelled in the finite element analysis.

3. Creep analysis

The geometry of a standard 1206 resistor chip was used for the creep analysis. Figure 6 shows the geometric dimensions of chip resistor modelled for finite element analysis. In the finite element modelling only one half of the geometry was used, due to the symmetry of the structure. The finite element model was created using 2D plane strain elements and a fine mesh pattern is maintained around the interface between component and solder. Figure 7 shows the mesh details.

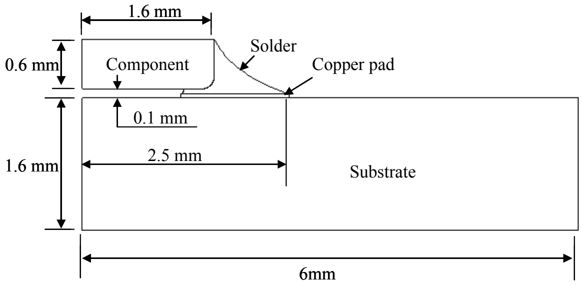


Figure 6 Geometry of 1206 chip resistor

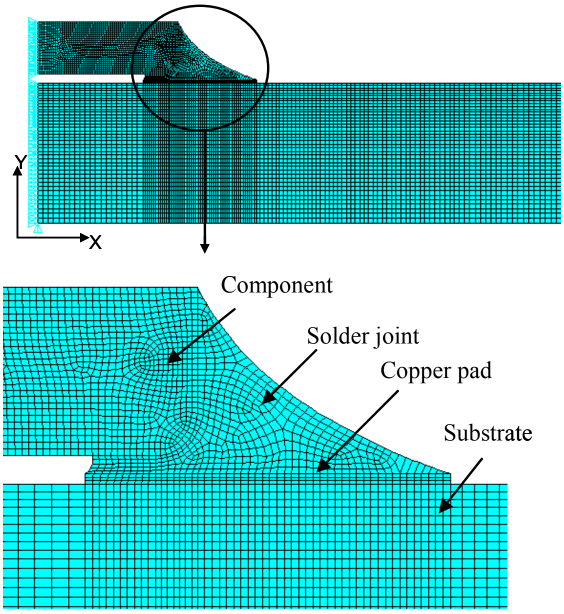


Figure 7 Finite Element Model of 1206 resistor

3.1 Creep constitutive equation

The solder joints of the 1206 resistor were modelled using the temperature-dependent material properties as shown in Table 1. A number of papers have been published [7, 8, 9] on the constitutive equation for creep deformation of SnAgCu alloys and they have identified two mechanisms for steady-state creep deformation. They attributed these to a dislocation climb controlled (low stress) and combined glide/climb (high stress) behaviour and have represented the steady-state creep behaviour using a double power law model. In this paper the creep model determined by Schubert et al. [7] is used for the steady-state creep behaviour. They also identified two regions for stress-strain rate behaviour, but postulated the high stress region as a power law break-down region, and chose the hyperbolic sine function to fit their creep data:

Temperature (°K)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/°K)	Density (gm/cm³)
218	57300	0.4	12.7	7.5
248	55800	0.4	12.7	7.5
298	52600	0.4	21.2	7.5
248	49300	0.4	21.7	7.5
398	45800	0.4	23.0	7.5

Table 1 Elastic material properties for SnAgCu

$$\dot{\varepsilon}_{cr} = A_1[\sinh(\alpha\sigma)]^n \exp\left[\frac{-H_1}{kT}\right] \qquad (1)$$

Where A_1 = 277984 s^{-1}, α = 0.02447 MPa^{-1}, n = 6.41, $\frac{H_1}{k}$ = 6500, $\dot{\varepsilon}_{cr}$ is steady state creep strain rate, σ is stress, T is absolute temperature.

Plasticity is also included along with creep in the finite element analysis. Plasticity is modelled with bilinear kinematic hardening (BKIN), which includes the Bauschinger effect due to thermal cycling. Table 2 gives the plastic material properties used for SnAgCu [10].

The material properties of 96% alumina (Al_2O_3) are used for the component body, whilst high-conductivity copper and FR4 material properties [10, 11] are used for pad and substrate respectively.

Temperature (ºK)	Yield stress (MPa)	Tangent modulus (MPa)
218	45	5700
248	41	5600
298	32	5260
348	21	4900
398	13	4600

Table 2 Plastic material properties of SnAgCu

3.2 Thermal cycling conditions

In the surface mount assembly process, the components are reflowed in an oven to create the solder joint and the assembly is then returned to room temperature. Therefore, creep analysis is carried out in two steps for three different temperature cycling conditions. In the first step, creep analysis is carried out for the reflow soldering process and relaxation for one hour at room temperature (assuming there is a one hour storage period before the resistor assembly is subjected to thermal cycling). The stress levels at the end of the reflow process give the manufacturing-induced stress in the solder joint, and similarly stress level at the end of relaxation gives the amount of stress after relaxation has taken place in the solder joint due to storage at room temperature. Below are the three different thermal cases used.

Case A: Uniform temperature ranging from 398°K (+125 °C) to 218°K (-55°C), where the entire resistor-substrate assembly is subjected to the same temperature.

Case B: Uniform temperature for the component, solder joint and copper pad ranging from 398°K (+125°C) to 218°K (-55°C), while the substrate's temperature (T_{sub}) is also uniform but varies according to the following relation:

$$T_{sub} = 0.18 * T_{comp} + 299.4, \quad (2)$$

Where T_{comp} is the component's temperature. This equation is deduced from the previously described experimental results.

Case C: This case is more representative of real conditions where the temperature gradient from the experimental results is indirectly used in the thermal cycling. A thermal analysis was first carried out using temperature boundary conditions from the experimental results to obtain a continuously varying temperature distribution throughout the surface mount assembly. Figure 8 shows the different thermal zones within the resistor assembly used in the thermal analysis. Temperature boundary conditions were applied on the outer surface of the body at zone 1 and zone 3. In zone 2, a set of nodes was selected for temperature boundary condition application. The temperature boundary conditions in zone 2 (solder joint) and zone 3 (substrate) are based on the zone 1 (component) temperature. The

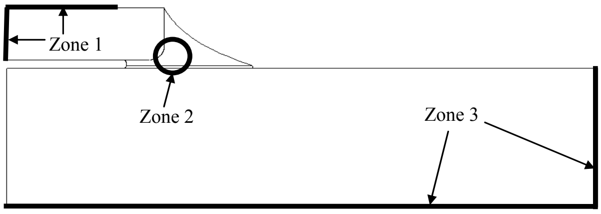


Figure 8 Temperature zones for thermal analysis

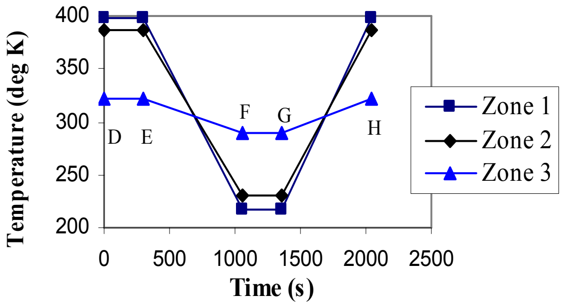


Figure 9 Temperature variations in zone 1, zone 2 and zone 3 in thermal analysis

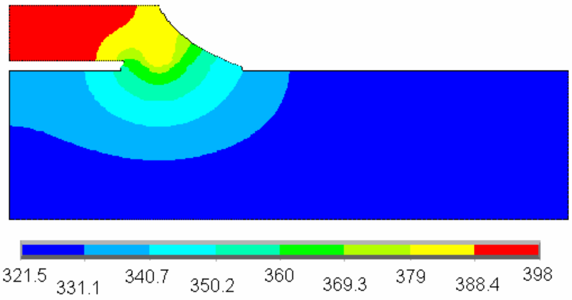


Figure 10 Temperature distribution in resistor assembly when component is at 398°K

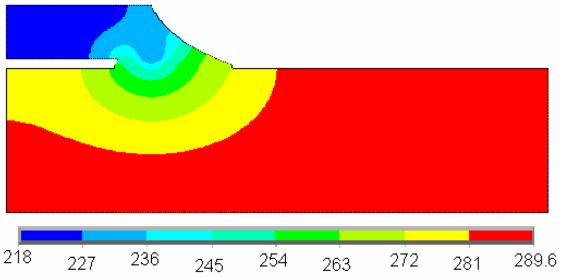


Figure 11 Temperature distribution in resistor assembly when component is at 218°K

relationship between the temperatures in zone1, zone2 and zone3 were deduced from the experimental results. Figure 9 shows the variation of temperature boundary conditions at different zones throughout the thermal cycle. Figures 10 and 11 give the temperature distribution in the 1206 resistor assembly after thermal analysis was carried out when the zone 1 (component) temperatures are 398°K and 218°K respectively. In Case C the resistor assembly is subjected to a thermal cycle between these two extreme temperature profiles.

Figure 12 shows the typical thermal cycle used in creep analysis. Line AB represents the reflow process, where a cooling rate of 4°C/s is used, and line BC represents storage of the resistor at room temperature for an hour. After an hour of storage at room temperature, the component temperature (T_{comp}) is ramped to 398°K (in Case A this is the whole assembly temperature) to start the thermal cycling. A complete thermal cycle starts at D and ends at H. In this thermal cycle there is a ramp of 12 minutes between temperature extremes (398°K and 218°K) and dwells of 5 minutes at the extreme temperatures.

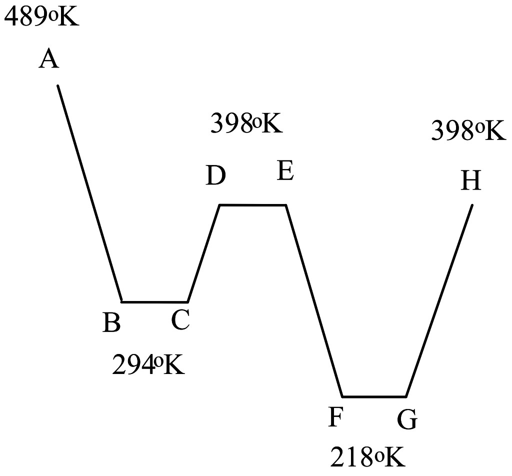


Figure 12 Thermal cycle used for creep analysis based on component temperature

4. Result and discussions

Finite element analysis of the chip resistor assembly was carried out for two thermal cycles and for the three different thermal loading cases described above. Figure 13 shows the shear stress distribution in the solder joint after the reflow process and also the location of maximum shear stress. The maximum shear stress of 25 MPa observed in the solder joint fillet, is mainly due to the mismatch of coefficients of thermal expansion (CTE) between component (made from alumina), solder and substrate (made from FR4). This stress is well above the yield stress of SnAgCu solder alloy at room temperature. When the resistor assembly is stored at room temperature, this stress reduces by the solder joints undergoing creep strain. This process is called stress relaxation. The shear stress after stress relaxation for one hour at room temperature reduces to 12 MPa, as can be seen in Fig. 14, which is below the yield stress at room temperature of SnAgCu alloy. The shear stress evolution for the entire creep analysis is shown in Fig. 14, which includes reflow period, relaxation period and 2 thermal cycles, all for the peak stress location in Fig. 13. It is evident from the figure that the shear stress range is 35MPa for Case A and that for Cases B and C is only about 15 MPa. This shows that there is about a 60% reduction in the shear stress

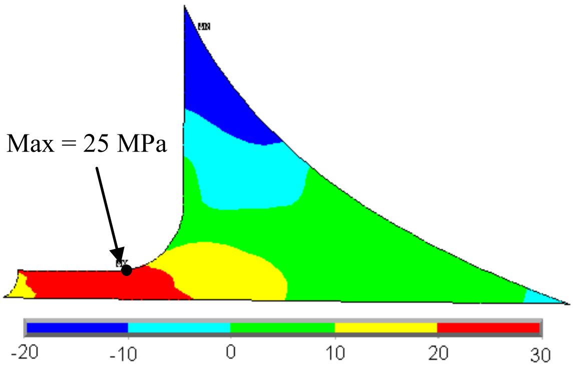


Figure 13 Distribution of shear stress in the solder joint at the end of reflow period (time = 48s)

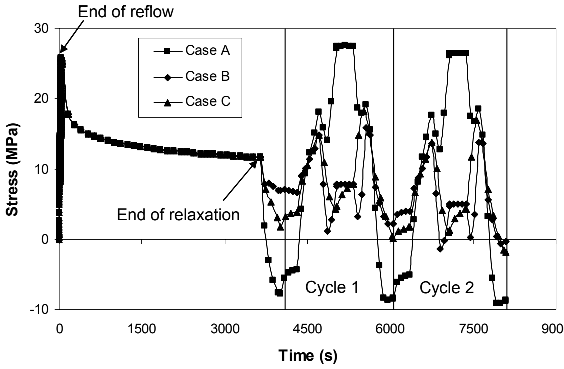


Figure 14 Distribution of shear stress in the solder fillet over time

range for Case B and C.

Accumulated inelastic strain due to thermal cycling is also studied for the solder joint. Figure 15 shows the worst case variation of inelastic strain over time at solder fillet. The total accumulated inelastic strain at the end of two thermal cycles was largest (9.5%) for Case A and smallest for Case C (7.2%). In Case B and Case C the total accumulated creep strain at the end of the thermal cycle is reduced by 13% and 28% respectively compared with case A. It can be observed from Fig. 15 that, even though most of the inelastic strain accumulation has taken place during the reflow and relaxation periods, this depends on parameters such as relaxation time, temperature and number of thermal cycles. In this particular analysis inelastic strain accumulation during the reflow and relaxation period accounts for 50%, 57% and 69% for Case A, Case B and Case C respectively. The amount of inelastic strain accumulation is reduced in thermal cycle 2 compared with that in thermal cycle 1. This reduction is only 3% for Case A compared with Cases B and C where it is 23% and 20% respectively. It is however expected that further reductions for subsequent cycles would be smaller.

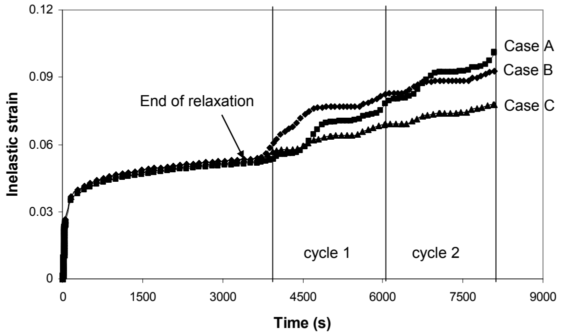


Figure 15 Accumulation of creep strain with time

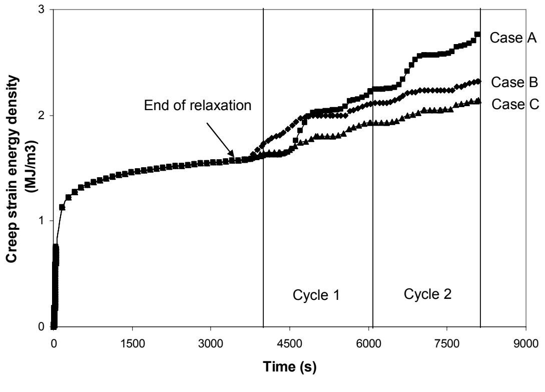


Figure 16 Accumulation of creep strain energy density in solder joint

Figure 16 demonstrates the density of creep strain energy dissipated in the solder joint during the analysis. This variation is quite similar to the variation of accumulated inelastic strain in the solder joint, with Case A having a higher density of creep strain energy dissipation (2.64 MJ/m^3) due to the higher inelastic strain accumulation and Case C having a lower density of creep strain energy dissipation (1.96 MJ/m^3).

The number of cycles to failure, N_f, for the solder joints were predicted based on the following Coffin-Manson based relationship [3]:

$$N_f = (C'\varepsilon_{acc})^{-1} \qquad (3)$$

Where ε_{acc} = Accumulated inelastic strain per cycle and C' = inverse of creep ductility. The accumulated inelastic strain calculated for the 2nd thermal cycle was considered for these life calculations.

Table 3 gives the predicted lives for the three different thermal loading cases. From comparison of predicted lives for the three different thermal cases, there is more than 100% improvement in the life of the solder joint in case B and case C. Case C is predicted to have the longest life for the solder joint (i.e. 2456 cycles) out of the three cases.

Thermal cycling conditions	C' (inverse of creep ductility)	Acc. inelastic strain in 2nd cycle	Predicted lives (cycles)
Case A	0.0468	0.023	929
Case B	0.0468	0.0104	2054
Case C	0.0468	0.0087	2456

Table 3 Predicted life for chip resistor

5. Conclusions

The experimental results demonstrate a typical non-uniform temperature distribution in an electronic assembly. The finite element study carried out based on the experimental results is a preliminary study to understand the effect of a non-uniform temperature distribution on the fatigue behaviour of lead-free solder joints. Out of the three different thermal loading cases considered, Case C (non-uniform temperature distribution) is predicted to result in lower levels of shear stress, creep strain accumulation and creep strain energy density. However, the accumulation of creep strain and creep strain energy density depend on relaxation time, temperature and number of thermal cycles. Therefore, further creep studies are required considering various relaxation times, temperature and a greater number of thermal cycles. The inelastic strain based estimated lives demonstrate the significant impact of non-uniform temperature distribution (case C) on fatigue life of solder joint in the chip resistor, case C predicting highest number of life cycles. However, the accumulated inelastic strain is from 2nd thermal cycle, which needs further creep analysis to establish the stabilised accumulated inelastic strain per cycle. The capture of thermal data for the actual components studied and a more accurate thermal model, taking into account the thermal mass distribution in the assembly, will be used to assess the interaction of power and thermal cycles on fatigue. Future analysis will also establish the relevant contributions of plastic and creep strains to fatigue damage and the life reduction attributable to post reflow stress relaxation.

References

1. Gonzalez, M., Vandevelde, B., Beyne, E., "Thermo-Mechanical Analysis of a Chip Scale Package (CSP) Using Lead Free and Lead Containing Solder Materials", *Proc 3rd European Microelectronics and Packaging Symposium*, Prague, Czech Republic, June. 2004.
2. Wu, C.M.L., Yu, D.Q., Law, C.M.T., Wang, L., "Properties of Lead-free Solder Alloys with Rare Earth Element Additions", Material Science and Engineering R 44 (2004) pp. 1-44.
3. Syed. A., "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints", *Proc 54th Electronic Components and Technology Conf*, Las Vegas, USA, June. 2004, pp. 737-746.
4. Warde, J., Wallach, E.R., "The Prediction of Creep Damage in Surface Mount Components using Finite Element Modelling," NPL Report CMMT(A)218, March. 1999.
5. Pang, J.H.L., Chong, D.Y.R., Low, T.H., "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability," *IEEE Trans* Compn. and Packag. Technol. Vol. 24, No. 4 (2001), pp. 705-712.
6. Ochana, A.R., Hutt, D.A., Whalley, D.C., Sarvar, F., Al-Habaibeh, A., "Modelling of the Power Cycling Performance of a Si on Si Flip Chip Assembly," *Proc 10th Intersociety Conference on Thermal and Thermochanical Phenomena in Electronics Systems, ITHERM 2006*, San Diego, USA, May. 2006, pp. 243-250.
7. Schubert, A., Dudek, R., Auerswald, E., Gollbardt, A., Michel, B., Reichl, H., "Fatigue Life Models of SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulations," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 603-610.
8. Wiese, S., Meusel, E., Wolter, K.-J., "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 197-206.
9. Morris, J.W., Song, H.G., Hua, F., "Creep Properties of Sn-rich Solder Joints," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 54-57.
10. Database for solder properties with emphasis on new lead-free solders http://www.boulder.nist.gov/div853/lead%20free/props01.html
11. Matweb material property database, www.matweb.com.