Critical Inductance in Voltage Regulator Modules

Pit-Leong Wong, *Member, IEEE*, Fred C. Lee, *Fellow, IEEE*, Peng Xu, *Member, IEEE*, and Kaiwei Yao, *Student Member, IEEE*

***Abstract*—Multichannel interleaving makes it possible to use small inductances to improve voltage regulator modules' (VRMs) transient responses. However, smaller inductances reduce efficiency. Analysis shows that the transient responses are not only determined by the inductances but also the control bandwidths. This paper presents the concept of critical inductance in VRM. Critical inductance is the largest inductance that gives the fastest transient responses. Critical inductance is a good reference for optimal VRM design. Critical inductance is a function of the feedback control, the step current magnitude and the steady-state operating point.**

***Index Terms*—Critical inductance, interleaving, voltage regulator module.**

THE voltage regulator module (VRM) and microprocessor system is shown in Fig. 1. The capacitor C shown in the figure represents the VRM output capacitors. During microprocessor load transitions, the current flowing out of the capacitor has a much faster current slew rate than the current flowing into the capacitor. The two currents are i_o and i_L, as shown in the figure.

The difference between the two currents causes unbalanced charges that need to be provided by the VRM output capacitors, as shown in Fig. 2. The VRM output voltage drops that occur during transient responses are caused by this unbalanced charge. It is just a function of capacitor discharging.

For the same VRM output capacitors, if the unbalanced charges can be reduced, the VRM transient voltage drops can also be reduced. The load transient magnitude ΔI_o and the slew rate of i_o are determined by the application. The delay time t_d, shown in Fig. 2, is mainly due to the switching actions of the VRM. For the same switching frequencies and interleaving channels, the worst-case delay times are the same and will not be discussed in this paper. To reduce the unbalanced charges, either the slew rate of i_L must be increased or the rise time t_r must be decreased.

In conventional VRMs, a single synchronous buck is used, as shown in Fig. 3. The current i_L is the inductor current. Due to the steady-state ripple requirements, large inductances must be used. The large inductances limit the speed of VRM transient responses.

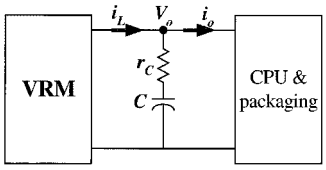

Fig. 1. VRM and microprocessor system.

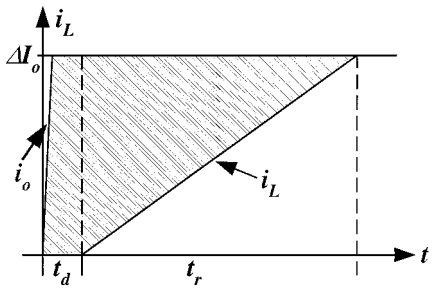

Fig. 2. Unbalanced charges during transient responses.

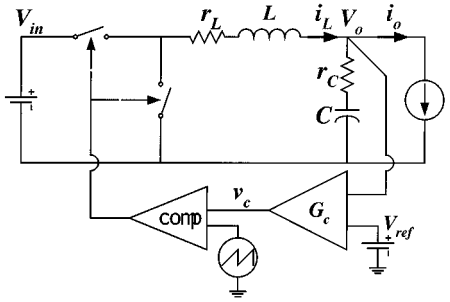

Fig. 3. Single synchronous buck VRM.

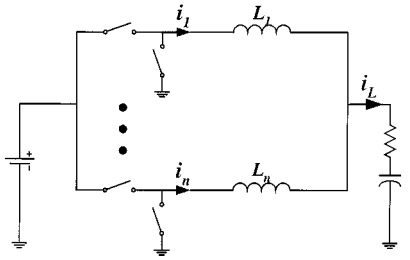

Fig. 4. Multichannel interleaving VRM.

Using the multichannel interleaving synchronous buck topology shown in Fig. 4, the current ripples of i_L can be greatly reduced. This reduction allows the use of very small inductances in the VRM, which improves transient responses. Because of this advantage, multichannel interleaving is a common practice in the VRM industry.

In and interleaving VRM, the channel current ($i_1 \ldots i_n$ in Fig. 4) still has large ripples because of the small inductance in

Manuscript received May 2, 2001; revised January 4, 2002. Recommended by Associate Editor N. Femia.

P.-L. Wong is with the Linear Technology Corporation, Milpitas, CA 95035 USA (e-mail: pwong@linear.com).

F. C. Lee and K. Yao are with the Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (e-mail: fclee@vt.edu; kwyao@vpec.vt.edu).

P. Xu is with Philips Research, Briarcliff Manor, NY 10510 USA (e-mail: peng.xu@philips.com).

Publisher Item Identifier 10.1109/TPEL.2002.800978.

0885-8993/02$17.00 © 2002 IEEE

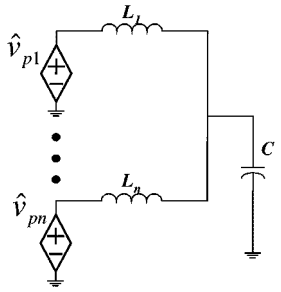

Fig. 5. Small signal circuit model of n-channel interleaving buck.

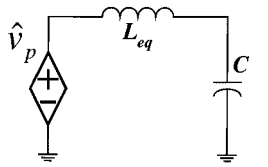

Fig. 6. Simplified small signal model of n-channel interleaving buck.

each channel. The large current ripples cause extra conduction and switching losses, which reduce converter efficiency. Multichannel interleaving of the VRM improves the transient responses, but at the expense of efficiency.

The inductance design in the interleaving VRM is a very important issue. The main purpose of this paper is to discuss the effects of inductance on transient responses and efficiencies. Smaller inductances results in low efficiencies, but do not necessarily always improve transient responses. There exists an inductance tradeoff point, the critical inductance, to give fast transient responses and high efficiencies. The transient response discussions in next section start with the small-signal model analysis.

I. Average Current Transfer Functions

The transient response analysis in this section is based on the average model. Researches show that the small-signal model of parallel/interleaving converters can be simplified as a single converter with corresponding equivalent parameters [1]–[3]. The small-signal model of an n-channel interleaving buck converter is equivalent to a single buck converter with the inductance equal to $1/n$ of the channel inductance in the interleaving buck. The results can be briefly explained as follows:

Small signal perturbations are imposed to the switching nodes of the interleaving VRM as shown in Fig. 5.

For constant input voltages, $\hat{v}_p$ can be simplified as follows:

$$\hat{v}_p = V_{in} \cdot \hat{d}. \tag{1}$$

In voltage feedback control, the interleaving channels share the same compensator. The duty cycle perturbation in different channels can also be considered the same. For constant input voltages, the small-signal perturbations in different channel are the same and can be connected together. This makes the inductors in each channel in parallel. The average model of Fig. 5 can be simplified as Fig. 6, which is exactly the same average model of a single buck converter. Thus, the small signal model of the interleaving buck can be simplified to an equivalent single buck.

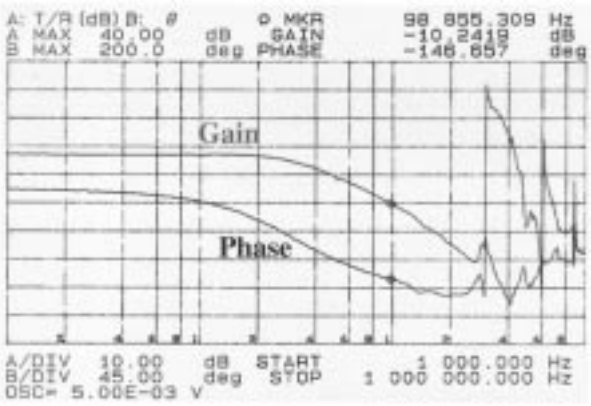

Fig. 7. Experimental measurement of control-to-output-voltage transfer function from a four-channel interleaving buck.

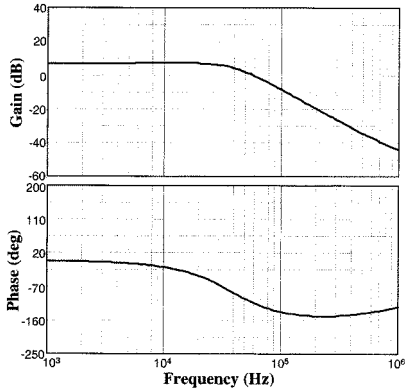

Fig. 8. Control-to-output-voltage transfer function of interleaving buck based on the simplified small signal model.

For symmetric channels, $L_1 = L_2 = \cdots = L_n = L$, the equivalent inductance is as follows:

$$L_{eq} = \frac{L}{n}. \tag{2}$$

In order to verify the validity of the simplified small signal model, the control-to-output-voltage transfer function of a four-channel interleaving buck converter hardware is measured as shown in Fig. 7. The inductance in each channel is 280 nH. Two types of capacitors are paralleled for output. The total output capacitance is 1.28 mF.

The bode plot of the corresponding transfer function based on the simplified circuit model is shown in Fig. 8 for comparison. The equivalent inductance is $280\ \text{nH}/4 = 70$ nH. The good match between the measurements and the model verifies the validity of the simplified small signal model of interleaving buck.

Because the small signal model of interleaving buck can be simplified to a single buck converter, the small-signal analysis in this section is based on a single buck converter. The results are also valid for interleaving buck converters.

For the buck converter shown in Fig. 2, how well the current i_L can follow the changes of i_o determines the extent of the transient unbalanced charges. The current transfer function defined in (3) describes how well i_L follows i_o:

$$G_{ii}(s) = \frac{\tilde{i}_L(s)}{\tilde{i}_o(s)} \tag{3}$$

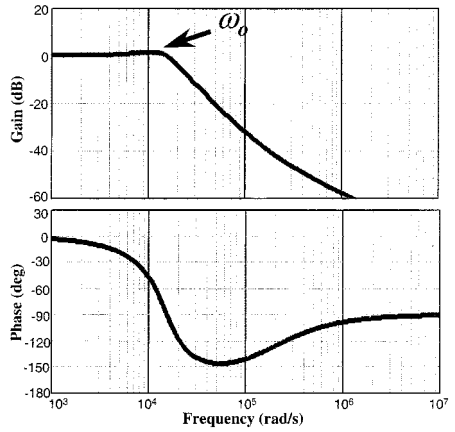

Fig. 9. Open-loop current transfer function $G_{ii}(s)$.

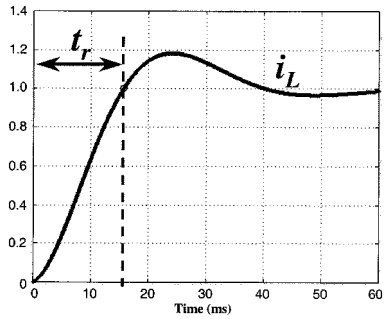

Fig. 10. Step response of open-loop current transfer function $G_{ii}(s)$.

where $\tilde{i}_o(s)$ and $\tilde{i}_L(s)$ are the perturbations added to the currents i_o and i_L, respectively. The parameters for the single synchronous buck VRM are given in Fig. 3. The open-loop transfer function of a buck VRM can be easily derived, as shown

$$G_{ii}(s) = \frac{\tilde{i}_L(s)}{\tilde{i}_o(s)} = \frac{s \cdot r_C \cdot C + 1}{s^2 \cdot L \cdot C + s \cdot (r_C + r_L) \cdot C + 1}. \quad (4)$$

This transfer function is only a function of the passive component parameters: The duty cycle, load current and input voltage do not affect it. If linear parameters are assumed, (4) is also valid for the large-signal perturbations as long as the duty cycle is not saturated. This linearity is only valid for the buck converter; it may not be true for other topologies. For interleaving bucks, the linearity is valid only when none of the channels has duty cycle saturation.

The bode plot of $G_{ii}(s)$ is shown in Fig. 9. The corner frequency in the plot, ω_o, represents the double poles of the power stage.

The slew rate of i_o is much faster than that of i_L. For simplicity, the average current of i_L during transient responses can be approximated as a step response of the transfer function of $G_{ii}(s)$. The normalized step response of $G_{ii}(s)$ in time domain is shown in Fig. 10.

The waveform, which represents the inductor current, is close to the step response of a typical under-damping second-order system. The rise time t_r (defined in Fig. 10) is the mismatch between i_o and i_L. The definition of the rise time t_r is consistent with the definition in Fig. 2. For simplicity, the average inductor

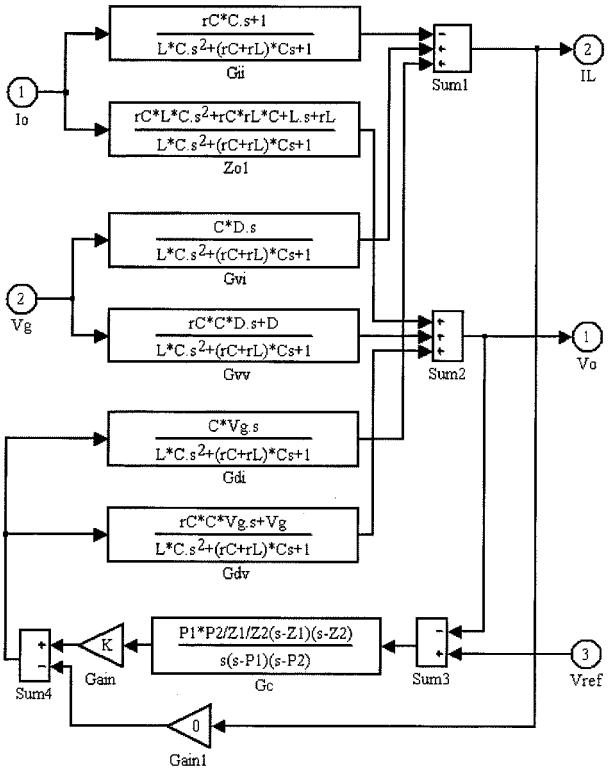

Fig. 11. Block diagram of buck converter.

current slew rate during the transient response can be approximated as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta I_o}{t_r}. \quad (5)$$

The preceding analysis relates only to the open-loop transfer function. In order to analyze the effect of the feedback control on the inductor current responses, a closed-loop current transfer function must be derived. The block diagram of a buck converter with feedback control is shown in Fig. 11. The transfer functions in the blocks are defined as follows.

$G_{ii}(s)$ Load current perturbation to inductor current.
$Z_{o1}(s)$ Load current perturbation to output voltage, also output impedance.
$G_{vi}(s)$ Input voltage perturbation to inductor current.
$G_{vv}(s)$ Input voltage perturbation to output voltage.
$G_{di}(s)$ Control perturbation to inductor current.
$G_{dv}(s)$ Control perturbation to output voltage.
$G_c(s)$ Voltage loop feedback compensator.

The closed-loop current transfer function can be easily derived following the block diagram shown in Fig. 11. This paper considers only the cases in which voltage loop feedback control is used. With voltage feedback control, the closed-loop current transfer function is as follows:

$$G_{iic}(s) = G_{ii}(s) - G_{di}(s) \cdot G_c(s) \cdot \frac{Z_O(s)}{1 + T(s)} \quad (6)$$

where $G_{di}(s)$ is the duty-cycle-to-inductor-current transfer function, $G_c(s)$ is the transfer function of the compensator,

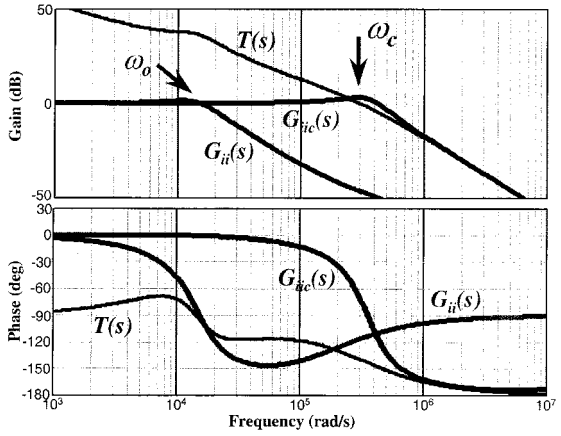

Fig. 12. Transfer functions: $G_{ii}(s)$, $G_{iic}(s)$, and $T(s)$.

$Z_o(s)$ is the converter output impedance and $T(s)$ is the loop gain, as shown in

$$T(s) = K \cdot G_{dv}(s) \cdot G_c(s). \tag{7}$$

$G_{dv}(s)$ is the duty-cycle-to-output-voltage transfer function and K is the gain of the compensator, as shown in Fig. 11.

The transfer functions involved in the closed-loop current transfer function are K, $G_c(s)$, $Z_o(s)$, $G_{ii}(s)$, $G_{di}(s)$, and $G_{dv}(s)$. K and $G_c(s)$ represent the compensator, which is linear. As illustrated in Fig. 11, $Z_o(s)$ and $G_{ii}(s)$ are determined only by the passive component parameters. $G_{di}(s)$ and $G_{dv}(s)$ include the input voltage and the passive parameters. In the cases in which input voltages are fixed, $G_{di}(s)$ and $G_{dv}(s)$ are also linear. During load transient responses, the duty cycle changes. Fortunately, the duty cycle change does not affect the closed-loop current transfer function $G_{iic}(s)$. As long as the duty cycle is not saturated, the small-signal model transfer function is also valid for large signal analysis.

The closed-loop current transfer function is affected by the compensator K and $G_c(s)$. The open-loop and closed-loop current transfer functions, $G_{ii}(s)$ and $G_{iic}(s)$ and the loop gain $T(s)$ are shown in Fig. 12.

The closed-loop current transfer function has the same shape as its open-loop counterpart unless the corner frequency reaches ω_c, which is the feedback control bandwidth. The control bandwidth is much higher than the power stage double poles. Because of this great increase in the corner frequency, the step response of the closed-loop current transfer function becomes much faster than that of the open-loop current transfer function, as shown in Fig. 13. The rise time of the closed-loop step response is much smaller than that of the open-loop step response. The unbalanced charge area is greatly reduced. A much faster transient response can be expected with feedback control.

For a nondamped second-order system, the rise time is one-fourth of its resonant cycle. The relationship between rise time and control bandwidth can be approximated as follows:

$$t_r = \frac{T_c}{4} = \frac{\frac{\pi}{2}}{\omega_c}. \tag{8}$$

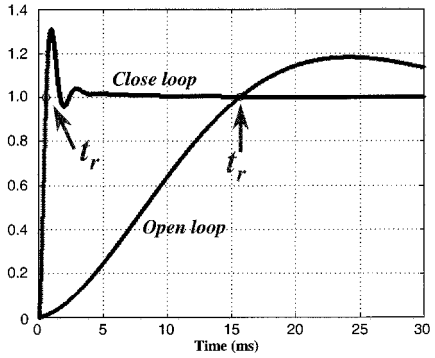

Fig. 13. Step responses of open-loop and closed-loop current transfer functions.

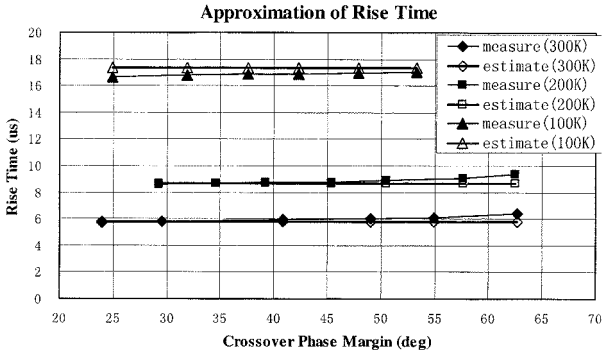

Fig. 14. Rise time of closed-loop current transfer function.

For systems with light damping, the rise time is close to that given in (8). But how close an approximation can the formula give? In order to answer this question, a power stage designed with different feedback crossover frequencies and different phase margins is simulated. The rise times measured from simulations and the rise times estimated from (8) are compared in Fig. 14. For the phase margin in the range of 20°–60°, the errors between the two sets of results are below 5%, which is considered to be a very accurate approximation. The agreement between the two sets of results verifies the validity of (8).

As shown in Fig. 12, with the high bandwidth feedback control, the closed-loop current transfer function is not affected by the power stage double poles. Thus, the rise time discussed in (8) and Fig. 14 should be valid for different power stages. In order to verify this, three power stages with different output filters are designed to compare the transient inductor current rise time. The double pole frequencies of the three power stages are 14.4 K(rad/s), 21.8 K(rad/s), and 31.6 K(rad/s). The rise times measured from simulations and those estimated from (8) are compared in Fig. 15, which illustrates that (8) is an accurate equation for a variety of power stages.

Based on the preceding analysis, the impact of voltage feedback control on inductor current rise time can be ascertained. Within the phase margin range of 20°–60°, the inductor current rise time is inversely proportional to the control bandwidth and is independent of the power stage parameters. The analysis in this section relates the VRM transient responses with the small-signal models.

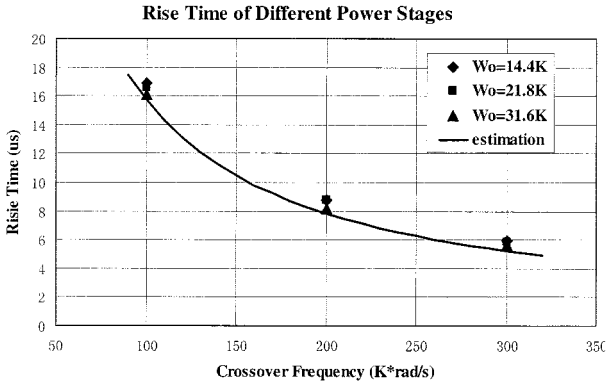

Fig. 15. Closed-loop current rise time for different power stages.

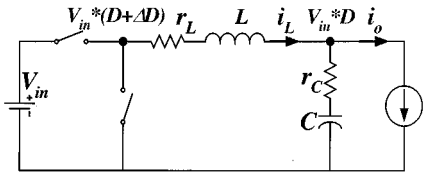

Fig. 16. Explanation of average current slew rate from circuitry.

II. Critical Inductance

From the analysis in Section II, the transient inductor average current slew rate can be derived from (5) and (8)

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta I_o \cdot \omega_c}{\frac{\pi}{2}}. \tag{9}$$

The average current slew rate can also be derived from the average model of a buck VRM, as shown in Fig. 16.

Assume the duty cycle has an increase of ΔD during the transient response; the net voltage applied to the inductor is $(V_{in}{}^{*}\Delta D$. The inductor average current slew rate during the transient response can be derived as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{V_{in} \cdot \Delta D}{L}. \tag{10}$$

If the duty cycle is not saturated, (9) and (10) should be equal. When (9) and (10) are equal, the duty cycle increase during the transient response can be derived as follows:

$$\Delta D = \frac{\Delta I_o \cdot \omega_c}{\frac{\pi}{2} \cdot V_{in}} \cdot L. \tag{11}$$

For certain applications, V_{in} and ΔI_o can be considered constant. From (9), in order to increase the average current slew rate, the control bandwidth needs to be designed as high as possible. For a fixed switching frequency, ω_c can also be considered constant. In these cases, ΔD increases proportionally to the increase in inductance.

This phenomenon can be explained as follows.

Consider two buck converters with the same output capacitor but different inductances. Their open-loop current transfer functions are shown in Fig. 17. The larger inductance has a lower gain at frequencies beyond the corner frequencies. However, the two power stages are designed to have the same control bandwidth. The power stage with larger inductance requires larger high frequency gain in the compensator to achieve the same loop

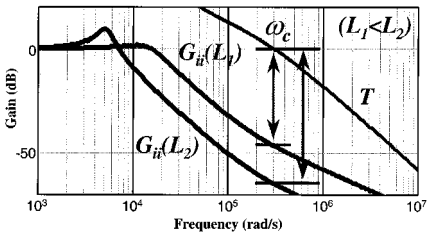

Fig. 17. Compensator gain for different inductances.

gain. Because the transient voltage variations at the output capacitors are the same for both power stages, the one with the larger compensator gain results in larger transient duty cycle increases.

Now, the inductance can be changed, while the control bandwidth is kept constant in order to determine the impact on the transient responses. The design starts with a very small inductance. From (11), ΔD during the transient response is very small. The duty cycle is not saturated. The average model in the previous section is valid. The inductor average current slew rate is determined in (9). As the inductance increases, ΔD also increases. As long as the duty cycle is not saturated, the average model analysis in the previous section is valid. The inductor average current slew rate is still determined in (9). For the same control bandwidth, the transient voltage spikes are maintained. When the inductance reaches a value such that the duty cycle is close to saturation during the transient response, the inductance is defined as the "critical inductance." The critical inductance can be calculated by letting ΔD in (11) equal $\Delta D_{\max}$

$$L_{ct} = \frac{\frac{\pi}{2} \cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot \Delta D_{\max} \tag{12}$$

where $\Delta D_{\max}$ is the maximum duty cycle increase during transient. Therefore

$$\Delta D_{\max} = D_{\max} - D \tag{13}$$

where $D_{\max}$ is the maximum duty cycle. The duty cycle is considered saturated when it reaches $D_{\max}$.

If the inductance increases beyond the critical inductance, the duty cycle becomes saturated at $D_{\max}$. The average model analysis is no longer valid. The inductor average current slew rate cannot be maintained as in (9). The current slew rate is determined by (10). Because ΔD is constant during saturation, the inductor current slew rate decreases as the inductance increases. This results in the increase of the transient voltage spikes. The impacts of the inductance on the VRM transient output voltage spikes are shown in Fig. 18.

For all the data points in the figure, the control bandwidths and the converter output capacitors are kept the same. The compensators for the different inductances are different in order to maintain the same bandwidth.

In conventional continuous conduction mode (CCM) synchronous buck VRM designs, inductor currents usually have 10%–20% of peak-to-peak ripples at full load. Large inductances are needed to achieve small current ripples. For CCM designs, the duty cycle is saturated during transient responses. The inductor current slew rate is limited by the inductance. For the QSW design proposed by CPES in 1997, the inductor peak-to-peak current ripple is designed to be twice of its

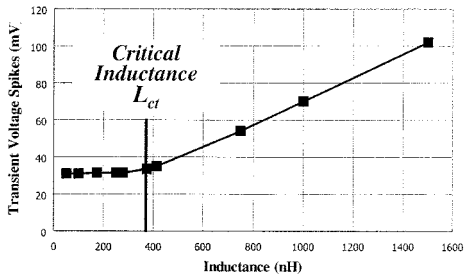

Fig. 18. Inductance effects to step-up transient voltage spikes (constant ω_c).

dc value at full load. Very small inductances are used. The duty cycle is not saturated during the transient response. The transient responses are greatly improved. However, the small inductances result in large current ripples in the MOSFETs, which cause large conduction losses and turn-off losses in the MOSFETs.

From Fig. 18, the critical inductance is the largest inductance that gives the fastest transient responses. Compared with the QSW design, critical inductance gives the same transient responses with smaller current ripples. Compared with conventional design, critical inductance greatly improves the transient responses.

The simulation results of the CCM, QSW and critical inductance designs are compared in Fig. 19. For all the three designs, two-channel interleaving is used. The input and output voltages are 5 V and 2 V, respectively. The switching frequency and control bandwidth are 300 kHz and 100 kHz, respectively. The step-up load transient is 20 A.

The inductances for the three designs are $L_{QSW} = 200$ nH, $L_{ct} = 827$ nH and $L_{CCM} = 2000$ nH. Same output capacitors are used for the three designs. The equivalent total output capacitor in simulation is 1 mF with an ESR of 0.5 mΩ. The peak-to-peak currents in each channel are 20 A for QSW design, 4.8 A for critical inductance design, and 2 A for CCM design. The QSW design has much larger root-mean-square (RMS) current than the other two. The lowest efficiency is expected for the QSW design. The transient voltage spikes at the output capacitors are 33 mV for both the QSW and critical inductance designs and 68 mV for the CCM design. Compared to the QSW design, the critical inductance design is expected to have higher efficiency while maintaining the same transient responses. Compared to the CCM design, the critical inductance design gives much faster transient response. The critical inductance design results in a reasonable tradeoff between the steady-state efficiency and transient responses.

The preceding discussion of the critical inductance is only based on the load step-up transient responses. The step-down transient responses also have a critical inductance defined for the case in which the duty cycle is close to the minimum duty cycle $D_{\min}$. The feedback control bandwidth is the same for both step-up and step-down transient responses. The step down critical inductance can still be obtained using (12). However, $\Delta D_{\max}$ needs to be rewritten as follows:

$$\Delta D_{\max} = D - D_{\min}. \tag{14}$$

Because $\Delta D_{\max}$ may not be the same for step-up and step-down transient responses, the critical inductance for the

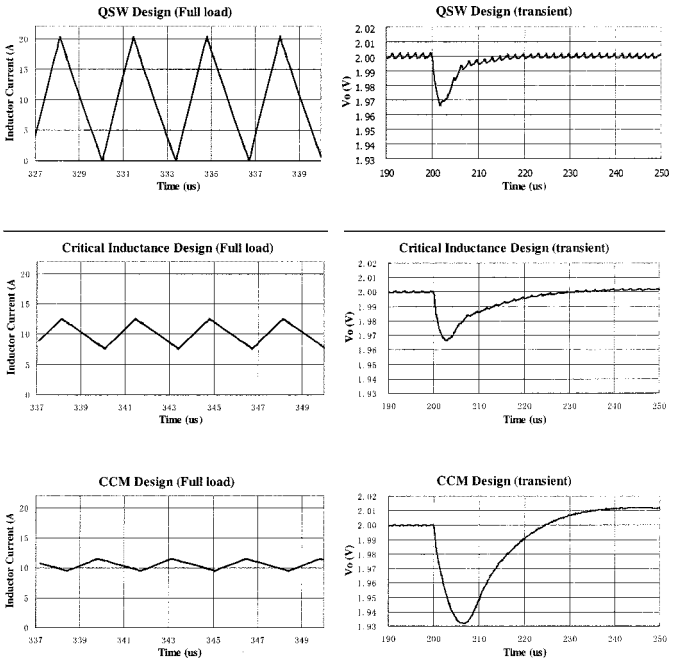

Fig. 19. Steady-state inductor current and transient output voltage waveforms of different inductance designs.

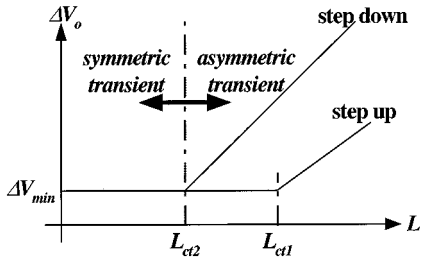

Fig. 20. Inductance effects on transient voltage spikes.

two transient responses can be different. However, the minimum voltage spikes are the same because they are determined by the control bandwidth. Both the step-up and step-down transient voltage curves are shown in Fig. 20. The step-up and step-down critical inductances are marked as L_{ct1} and L_{ct2}, respectively. The smaller of the two critical inductances is defined as L_{ctm}

$$L_{ctm} = \min\left(L_{ct1}, L_{ct2}\right). \tag{15}$$

When the inductance is smaller than L_{ctm}, the duty cycle is not saturated in either step-up or step-down transient response. The transient response is determined by the control bandwidth, which is the same for the two transient responses. The converter has symmetric voltage spikes for both step-up and step-down transient responses. When the inductance is larger than L_{ctm}, the duty cycle is saturated in at least one transient response. The transient responses are no longer symmetric. Both the symmetric or asymmetric transient responses can happen in either 5 V or 12 V VRMs depending on the inductance.

The simulation results in Fig. 21 show that both the 5 V and 12 V VRMs can have symmetric or asymmetric transient responses. Another observation from the waveforms is that when the transient responses are asymmetric, at least one of the transient voltage spikes is larger than the voltage spikes that occur

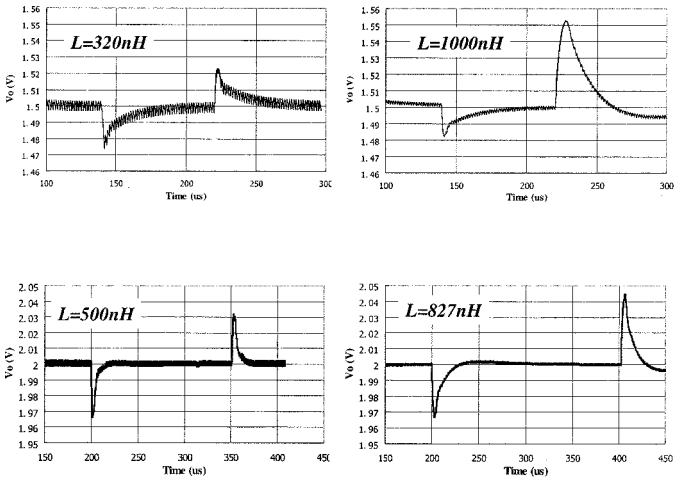

Fig. 21. Symmetric and asymmetric transient responses.

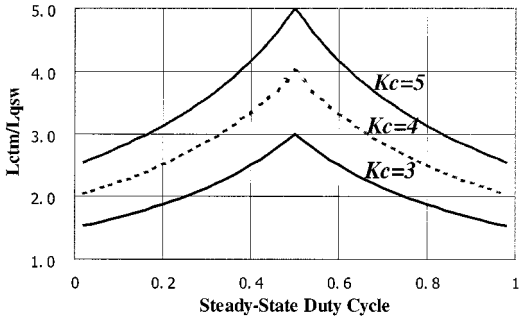

Fig. 22. Comparison of critical inductance and QSW inductance.

with symmetric transient responses. This is clear from Fig. 20. Of course, the asymmetry in 12 V VRMs is much more severe than that occurs in 5 V VRMs.

The critical inductance L_{ctm} is the largest inductance that gives symmetric, fast transient responses. When the adaptive reference voltage is used, the total output voltage variance is the larger of the step-up and step-down transient voltage spikes. Symmetric transient responses give smaller total output voltage variance. In this case, symmetric transient responses are desirable.

The critical inductances L_{ctm} and the QSW inductances are compared in Fig. 22. Because the critical inductance is a function of the control bandwidth, the different ratios between switching frequency and control bandwidth give different curves. The ratio K_c is defined as follows:

$$K_c = \frac{F_s}{F_c} = \frac{2\pi \cdot F_s}{\omega_c}. \tag{16}$$

Theoretically, for voltage feedback control, the average small-signal model of an n-channel interleaving buck converter is accurate up to $n/2$ of the switching frequency, which is n-time higher than the single channel converter [2]. However, due to the noise and current sharing problems, it is not practical to design control bandwidth higher than half the switching frequency. Moreover, if current feedback control is used, the theoretical control bandwidth is reduced to the same as a single converter. Thus, K_c between 3 and 5 is an aggressive design range for feedback control bandwidth.

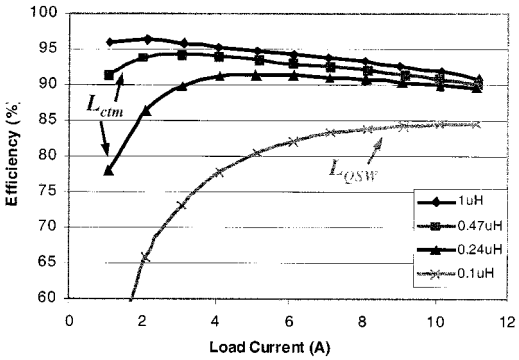

Fig. 23. Efficiency comparison of different inductance designs.

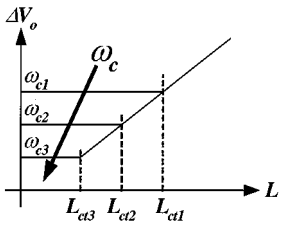

Fig. 24. Control bandwidth effects on transient voltage spikes.

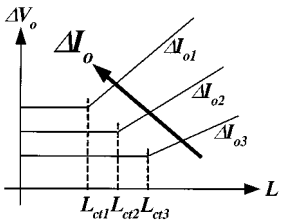

Fig. 25. Load current effects on transient voltage spikes.

Since the critical inductance is larger than the QSW inductance, it would result in better efficiency in the converter. A synchronous buck converter is built for an efficiency comparison of different inductances. The input and output voltage of the circuit are 5 V and 2 V, respectively. The switching frequency is 500 kHz. Full load output current is 11 A. The QSW inductance is 110 nH. The critical inductance is 270 nH for $K_c = 3$ and 460 nH for $K_c = 5$. Inductances of 100 nH, 240 nH, 470 nH, and 1000 nH are selected for the experiments: The first one represents the QSW design; the second and third ones represent the critical inductance designs; and the fourth inductance is to show how much the efficiency can be improved by further increasing the inductance. The MOSFETs used in the circuits are Hitachi's HAT2064Rs and their drivers are HIP6601s from Intersil. The inductors used are IHLP series from Vishay. The experimental results are shown in Fig. 23.

The critical inductance designs have much higher efficiency than the QSW design. Further increase of the inductance does not significantly improve efficiency, but it does slow down the transient responses. In this sense, the critical inductance is a good design tradeoff between the efficiency and transient response for VRMs.

From (12), the critical inductance is a function of both control bandwidth and load current step magnitude. With the increase of control bandwidth, the critical inductance decreases. The min-

imum voltage spike decreases, too. A larger current step magnitude results in smaller critical inductance and larger minimum voltage spikes. The effects of control bandwidth and current step magnitude on transient voltage spikes are shown in Figs. 24 and 25, respectively [4]–[7].

III. Conclusion

This paper presents the concept of critical inductance in VRM design. The critical inductance is defined at the point at which the duty cycle is close to saturation during transient responses. The critical inductance is the largest inductance that gives the fastest transient responses; It is a function of control bandwidth and load current step magnitude.

Both step-up and step-down transient responses have a corresponding critical inductance. Inductances smaller than the lesser of the two critical inductances give symmetric step-up and step-down transient responses. The transient voltage spikes in symmetric transient responses are smaller than those in asymmetric transient responses.

References

[1] R. Ridley, "Small-signal analysis of parallel power converters," Ph.D. dissertation, Virginia Tech, Blacksburg, 1986.

[2] P.-L Wong, "Performance improvements of interleaving voltage regulator modules with coupling inductors," Ph.D. dissertation, Virginia Tech, Blacksburg, 2001.

[3] R. Tymerski and V. Vorperian, "Generation, classification and analysis of switched-mode dc-to-dc converters by the use of converter cells," *INTELEC*, pp. 181–195, 1986.

[4] P.-L. Wong, F. C. Lee, X. Zhou, and J. Chen, "Voltage regulator module (VRM) transient modeling and analysis," *IEEE Ind. Applicat.*, vol. 35, pp. 1669–1676, Oct. 1999.

[5] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, pp. 1172–1182, Nov. 2000.

[6] Y. Panov and M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," in *Proc. IEEE APEC'00 Conf.*, 2000, pp. 39–46.

[7] M. Zhang, M. Jovanovic, and F. C. Lee, "Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits," *IEEE Trans. Power Electron.*, vol. 11, pp. 328–337, Mar. 1996.

Pit-Leong Wong (S'99–M'02) received the B.E. degree in control, B.S. degree in physics, and the M.S. degree in systems engineering from Tsinghua University, Beijing, China, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from the Virginia Polytechnic Institute and State University, Blacksburg, in 2001.

He joined Linear Technology Corporation, Milpitas, CA, in 2001. His research interests include power management IC design, low-voltage dc/dc converters, power factor correction techniques, distributed power system, magnetics and modeling, and control of converters.

Fred C. Lee (S'72–M'74–SM'87–F'90) received the B.S. degree in electrical engineering from the National Cheng Kung University, Taiwan, R.O.C., in 1968 and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1971 and 1974, respectively.

He is a University Distinguished Professor at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, and was the Lewis A. Hester Chair of Engineering at Virginia Tech and the James S. Tucker endowed professor in the Bradley Department of Electrical and Computer Engineering. He directs the Center for Power Electronics Systems (CPES), a National Science Foundation engineering research center whose participants include five universities and over 100 corporations. In addition to Virginia Tech, participating CPES universities are the University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University and the University of Puerto Rico-Mayaguez. He is also the Founder and Director of the Virginia Power Electronics Center (VPEC), one of the largest university-based power electronics research centers in the country. His research interests include high-frequency power conversion, distributed power systems, space power systems, power factor correction techniques, electronics packaging, high-frequency magnetics, device characterization and modeling and control of converters.

Dr. Lee received the Society of Automotive Engineering's Ralph R. Teeter Education Award (1985), Virginia Tech's Alumni Award for Research Excellence (1990) and its College of Engineering Dean's Award for Excellence in Research (1997), the William E. Newell Power Electronics Award, the highest award presented by the IEEE Power Electronics Society for outstanding achievement in the power electronics discipline, in 1989, the Power Conversion and Intelligent Motion Award for Leadership in Power Electronics Education (1990) and the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998). From 1993 to 1994, he served as president of the IEEE Power Electronics Society and, before that, as Program Chair and then Conference Chair of IEEE-sponsored power electronics specialists conferences.

Peng Xu (S'00–M'01) received the B.S. and M. S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1994 and 1997, respectively, and the Ph. D. degree in electrical engineering from Virginia Polytechnic Institute and State University, Blacksburg, in 2002.

He has been a Senior Member of Research Staff at Philips Research—USA, Briarcliff Manor, NY, since January 2002. His research interests include low voltage high current power conversion, distributed power systems, power factor correction techniques, high-frequency magnetics, and device characterization.

Kaiwei Yao (S'99) received the B.S. degree from Xi'an Jiaotong University, China, in 1992 the M.S. degree from Zhejiang University, China, in 1995, both in electrical engineering, and is pursuing the Ph.D. degree in power electronics at the Virginia Polytechnic Institute and State University, Blacksburg.

From 1995 to 1998, he was an Engineer for UPS Design, Hwa Da Electronics, Shenzhen, China. He is now a Research Assistant at the Center for Power Electronics Systems (CPES). His research interests include low-voltage power management, high-frequency high-density power supplies, modeling and control for converters, design for distribute-power systems, and power-factor-correction techniques.