Critical Parameters of Gate Control in NC-FinFET on GaAs

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Critical Parameters of Gate Control in NC-FinFET on GaAs

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Abstract: Gate control ability is expected to keep constant, guaranteeing accurate MOSFET adjustment of drive strength by changing its size. In NCFET, the non-uniform distribution of ferroelectric polarization and capacitance match are sensitive to the size and tend to enhance the fluctuation of gate control. In the current work, a detailed simulation was made on NC-FinFET to clarify the effect of structural factors on its gate control. These factors include the Fin structure (length, width, and height), the doping concentration in the GaAs channel, and ferroelectric film thickness. Simulation results indicate that the SS of NC-FinFET with BTFM-CTO film is more insensitive to the variation of structural factors than that with HfO_2 or PZT film. Thus, the fluctuation of gate control can be significantly weakened with a suitable set of structure factors and ferroelectric parameters. The current work generates new insights into the fluctuation of gate control with varying structure factors and adjustment of NC-FinFET drive strength, which are essential for NC-FinFET to applicate in an analog circuit.

Keywords: NC-FinFET, GaAs, steep SS, GVA, NDR, multi-channel, ferroelectric polarization.

Advanced technologies such as the Internet of Things (IoT)[1], mobile smart devices[2], and wearable devices[3] have put forward higher requests for ultralow-power and high-performance electronic devices. However, deep submicron devices suffer from troublesome short channel effects (SCE)[4], such as increasing leakage current (I_{OFF}) and drain-induced barrier lowering (DIBL)[5], which poses a limit on the development of transistors. One common inducement for these problems is that as the channel shortens, the effect of drain voltage (V_d) cannot be neglected, and the control ability of gate voltage (V_g) over the channel is weakened. This ability is usually described by subthreshold swing (SS)[6]. A fin field-effect transistor (FinFET) enhances gate control over the channel by controlling the channel three-dimensionally[7-9]. Under the restriction of the Boltzmann distribution, the SS of conventional transistors has the limit value of 60 mV/dec. The negative capacitance (NC)[10, 11] effect existing in the ferroelectric film offers a unique solution to the thermionic limit termed Boltzmann's Tyranny through gate voltage amplification (GVA)[12, 13] effect. As a result, NC-FinFET[14-16] incorporating

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ferroelectrics film has low SS and superior gate control, becoming a competitive candidate to keep Moore's law. Gate control ability is expected to keep constant, guaranteeing accurate adjustment of transistors' drive strength by changing its size. Thus clarifying the effects of structural factors on gate control of NC-FinFET related to its transfer performance and reducing the fluctuation of gate control are of a great significance to further circuit application of NC-FinFET.

The vertical channel existing in FinFET is termed Fin, which is an excellent asset to control the carrier transport in the channel well. Thus, FinFET has a significant advantage over conventional planar Metal oxide semiconductor field-effect transistor (MOSFET), especially in SCEs[17, 18]. Drive strength of the FinFET structure is usually insufficient and adjusted by changing its size. Increasing the height or width of the fin channel (C_H, C_W) can enhance the drive strength of FinFET. However, for stability purposes, C_H is an important parameter that should be small. Moreover, the electric field intensity in the channel is bound to change when C_W or C_H varies, resulting in fluctuation of gate control and thus other parameters such as threshold voltage (V_{th}) [19, 20]. Large C_W or C_H weakens the gate control over the Fin and makes the FinFET behave like a quasi-planar structure, leading to terrible performance. As a result, accurate adjustment of the FinFET drive strength is not convenient.

GVA effect endows NC-FinFET with steep SS and superior performance. However, it is also tricky for the NC-FinFET to adjust the drive strength accurately by changing size. According to related theory, the key to activating the performance of NCFET is to polish up the match between the negative and positive capacitance[21, 22]. There is much research focusing on the ferroelectric parameters, such as coercive electric field intensity (E_C), remanent polarization (P_r), the thickness of the ferroelectric film (T_{FE}), etc.[23, 24]. Previous research has established that ferroelectrics films with large E_C, small P_r, and large T_{FE} tend to endow NC-FinFET with a splendid performance. Researchers have not detailed the structure factors of NC-FinFET, such as C_W, C_H, channel length (C_L), substrate doping concentration (N_D), and the capacitance matching, which further enhances the fluctuation of gate control. Moreover, NC-FinFET without an internal gate is more prone to drain bias, and the distribution of ferroelectric polarization (P), is non-uniform[25] due to the multi-domain structure of ferroelectric material[26]. The non-uniform distribution of P depends on structural factors and has the potential to strengthen the fluctuation of gate control. Thus, P and channel surface potential (V_{int}) distribution are investigated with varying structure factors that guide the analyses of simulation results. The V_{int} with and without V_g bias reflects the GVA and negative differential resistance (NDR)[27] effect, respectively.

In this work, detailed simulations and analyses are made on dual-channel NC-FinFET to clarify the effect of structural factors on its transfer performance related to gate control. Firstly, we introduce the inducement of gate control fluctuation and the adverse effect. Secondly, we state the basic theory of NC-FinFET and device simulation parameters used in the current work. Then we describe the simulation results of transfer performance with varying structure factors. The transfer performance assessment comprises four parameters: SS, ON-current (I_{ON}), OFF-current (I_{OFF}), and I_{ON} / I_{OFF}. P and V_{int} are also investigated, which provide a reference for the analyses on simulation results. Finally, we give comprehensive analyses and discussions. Simulation results indicate that the fluctuation of gate control can be significantly weakened if a suitable set of structure factors and ferroelectric parameters is obtained. Thus, the drive strength of NC-FinFET is hopeful to be adjusted by changing its size, and a multi-channel structure is not necessary.

THEORY AND MODEL OF NC-FINFET

Fig. 1(a) is a schematic description of NC-FinFET. Fig. 1(b) is an equivalent circuit for NC-FinFET[28]. V_{int} is dominant in the electrical characteristic of FinFET.V_{int} is defined by equation (1) which can be further simplified into equation (2) with amplification factor (A_g) and drain couple factor (A_d) defined by equations (3) and (4), respectively. C_{int} is composed of C_{gdo}, $C_{s,}$ and C_{gso}. These equations indicate that V_g and V_d determine V_{int}. Considering that the capacitance of ferroelectric film (C_{fe}) is negative, the A_g exceeds unity, termed the GVA effect. GVA effect endows the NC-FinFET with reinforced I_{ON} and sub-60 mV/dec SS. A_d turns negative when $|C_{fe}|$ is larger than C_{int}. According to equation (2), a negative A_d leads to a decrease in V_{int}. As a result, both I_{ON} and I_{OFF} have the potential to decrease with increasing V_d, which is termed the NDR effect. The NDR effect can hold back SCE effects such as the DIBL effect and channel length modulation effect (CLME)[29], making for scaling down of MOSFET. In addition, the NDR effect favors certain applications such as high-frequency oscillators, reflection amplifiers, memory, and logic switch[30]. Large A_g and small A_d are expected to reinforce gate control capability.

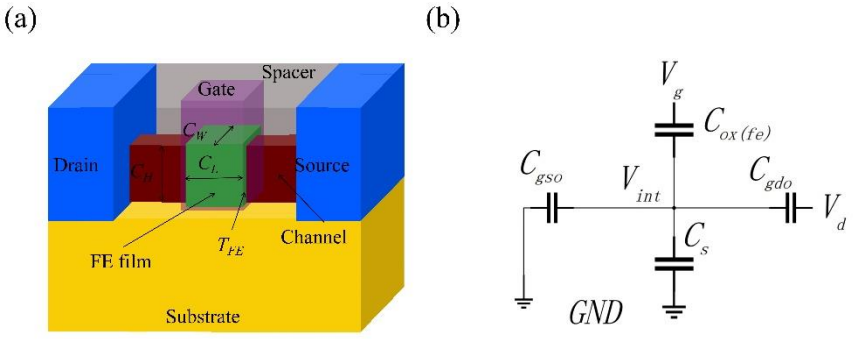

Fig. 1. (a) Schematic description of NC-FinFET, with *FE*, T_{FE}, C_L, C_H, and C_W representing the ferroelectric material, thickness of ferroelectric film, channel length, channel height, and channel width, respectively. (b) Equivalent circuit representation of the NC-FinFET with C_{fe} the negative capacitance of ferroelectric film, V_{int} the internal voltage across substrate capacitance (C_s), C_{gso} the parasitic capacitance between gate and source, C_{gdo} the parasitic capacitance between gate and drain.

$$V_{int} = \frac{C_{fe}V_g + C_{gdo}V_d}{C_{gdo}+C_{gso}+C_{fe}+C_s} \quad (1)$$

$$V_{int} = A_g V_g + A_d V_d \quad (2)$$

$$A_g = \frac{\partial V_{int}}{\partial V_g} = \frac{C_{fe}}{C_{fe}+C_{int}} = 1 + \frac{C_{int}}{|C_{fe}|-C_{int}} \quad (3)$$

$$A_d = \frac{\partial V_{int}}{\partial V_d} = \frac{C_{gdo}}{C_{fe}+C_{int}} = -\frac{C_{gdo}}{|C_{fe}|-C_{int}} \quad (4)$$

SS is given by equation (5) and is further simplified into equations (6) and (7)[31]. *K* refers to the Boltzmann constant, *m* refers to the gate control coefficient, and n refers to the transportation coefficient. *n* is determined by how the charge carrier transports and is limited by the Boltzmann statistical distribution. For the NC-FinFET structure, as shown in Fig. 1(b), the C_{ox} is replaced by negative C_{fe}. If $|C_{fe}|$ is greater than the C_{int}, the SS may be less than 60 mV/dec. To achieve steep SS, the C_{int} of MOSFET should be as small as possible, while it is converse regarding NCFET for negative C_{fe}.

$$SS = \frac{\partial V_g}{\partial\, lg\, I_d} = \frac{\partial V_g}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial\, lg\, I_d} \quad (5)$$

$$SS = ln\,10 \times \frac{KT}{q} \times (1 + \frac{C_{int}}{C_{ox}}) \quad (6)$$

$$SS = ln\,10 \times m \times n \quad (7)$$

Based on the conventional FinFET structure, NC-FinFET can be fabricated by replacing the gate oxide with ferroelectric film. Its Schematic is shown in Fig. 1 (a). Landau–Khalatnikov (L–K) equations describe NC by relating the derivative of *P* to time (*t*) and the derivative of free energy density to *P*[32-34]. The electrical characteristic of NC-FinFET is determined by coupling of three-dimensional TCAD simulation along with the L–K equation of electric field across ferroelectric film (E_{FE}) as a function of *P*. L-K equation is shown as equation (8):

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\frac{dP}{dt} \quad (8)$$

Here α, β and γ are anisotropy constants, and ρ is the viscosity coefficient that accounts for the dissipative process during polarization switching. These parameters are extracted by fitting the L-K equation to the experimental *P-V* hysteresis curves. E_c refers to the minimum E_{FE} needed to switch all the P_r. They are characteristic parameters of NC measured from experimental *P-V* hysteresis curves and used to describe the value of C_{fe}. Considering that the distribution of *P* and V_{int} may depend on the properties of ferroelectrics film, FinFET is simulated with $PbZr_{0.1}Ti_{0.9}O_3$ (PZT)[35], BTFM-CTO[36, 37], and HfO_2[38] film, respectively. PZT film is famous for its superior ferroelectric properties but is limited by its bad compatibility with current integrated fabrication technology. BTFM-CTO film has been successfully fabricated in our previous work, and its ferroelectric properties are weaker than that of PZT film, but it is based on GaAs substrate. HfO_2 film is widely used as a high-K gate dielectric and does not show ferroelectric properties. The α, β, E_c, and P_r of PZT film are -6×10^{10} cm/F, 5×10^{18} $cm^5/(FC^2)$, 73 $\mu C/cm^2$, and 3 MV/cm, respectively. The α, β, E_c, and P_r of BTFM-CTO film is -5×10^9 cm/F, 2×10^{17} $cm^5/(FC^2)$, 96 $\mu C/cm^2$ and 0.341 MV/cm, respectively. In our simulation, C_{fe} is not a fixed value, and it is calculated by solving self-consistently the Landau-Khalatnikov equation, which

guarantees the accuracy of the simulation results. $|C_{fe}|$ is estimated by equation (9) when P is considered independent of its size[39, 40]. In equation (9), the A_{fe} refers to the capacitance area.

$$\left|C_{fe}\right| = A_{fe}\frac{2P_r}{3\sqrt{3}E_cT_{fe}} \tag{9}$$

Parameters g in equation (8) is domain interaction constant. Compared with the metal-ferroelectrics-metal-insulator-semiconductor (MFMIS) structure, the NCFET without an internal gate shows steeper SS and larger ON-current[41, 42] when drain bias is high. MFMIS ensures uniform P in a ferroelectric film. Thus, it shows excellent performance with a short channel. However, when the channel is short, it is difficult for the internal metal gate to occupy the gate trench and support charge injection and accumulation. Therefore, the MFMIS structure is not adopted in the current simulation, and the non-uniform distribution of P still exists, which cannot be neglected. What is more, structural factors affect the electric field intensity in the channel. Moreover, C_{int} is also related to structural factors. Equations (3-4) and (7) demonstrate that gate control and drive strength significantly depend on C_{int}. The drive strength of transistors cannot be adjusted by changing its size if current density in channel is not resistant to structural factors and fall to keep constant. As a result, drive strength and gate control of NC-FinFET tend to be more sensitive to structural factors than FinFET. Thus, P and V_{int} are also investigated, which provide a reference for the analyses on transfer performance simulation results and reflect the variation of gate control.

Technology computer-aided design (TCAD) Sentaurus has been widely used to simulate the development and optimization of semiconductor technology and devices. Sentaurus tools acquire simulation results by solving partial differential equations such as diffusion and transport equations. This underlying physical approach guarantees that sentaurus can produce results with predictive value, and the accuracy can be approximately equal to that of the experiment. Therefore, when developing new semiconductor devices or processes, Sentaurus is widely adopted by the semiconductor industry to replace expensive and time-consuming wafer tests. As technology becomes sophisticated, the semiconductor industry is more dependent on Sentaurus to reduce costs and accelerate research and development. In addition, Sentaurus is also used to analyze, monitor, measure, and optimize the process's integrated circuit process flow and fluctuation.

The simulation results achieved in the current work are based on TCAD Sentaurus semiconductor simulation software. The movement of carriers induces the current. Therefore, Poisson equation, carrier continuity equation, and L-K equations are solved using the self-consistent method to figure out the distribution and movement of carriers. The L-K equation, which describes NC effect, is only activated in a ferroelectric film. NC-FinFET device is heavily doped in current work, which introduces the doped impurity level into the energy band structure of the semiconductor material. Therefore, band gap reduction models are added to the simulation to quantify the band gap narrowing effect. Since the scattering of ionic impurities induced by dopants affects the migration of carriers and results in limited mobility, a mobility model which is dependent on impurity concentration is adopted in simulation. In addition, mobility is also related to the electric field. The mobility increases with electric field intensity but reaches saturation at a high electric field. Therefore, a high electric field mobility model is also added to the simulation. Because heavy doping introduces deep energy levels of impurities and defects, leading to indirect recombination, affecting carrier life and device performance. Thus, the SRH recombination model is adopted. The generation rate of electrons and holes depends on location and electric field

intensity. Due to the non-local generation of electrons and holes in the tunneling path, the non-local band tunnel model is used in the simulation. Other nonideal factors such as interface states, temperature, and radiation are ignored in current work. In our following paper, we plan to investigate the effects of interface states and temperature on NC-FinFET.

Benefiting from the GVA and NDR effects, the NCFET tends to have relatively steep SS, large $I_{ON,}$ and small I_{OFF}. However, limited by the relatively small carrier mobility and energy gap of conventional silicon conductors, NCFET based on silicon still suffers from the saturation of carrier mobility (SCM) and tunneling current, which obstructs further enhancement of the NCFET performance. Devices based on GaAs substrates are extensively used for their high electron mobility and wide-bandgap. GaAs is superior when it comes to high electron mobility transistors (HEMT)[43] and low power consumption application[44]. Thus, GaAs substrate is adopted in the NC-FinFET simulation model.

Parameters of the basic NC-FinFET remain unchanged except as otherwise noted. Key parameters include C_W, C_L, C_H, $T_{FE,}$ and N_D. Their values are shown as follow: C_W = 20 nm, C_L = 40 nm, C_H = 45 nm, T_{FE} = 12 nm, and $N_D = 1\times10^{18}/cm^3$. For accurate observation of the SS and gate control of NC-FinFET, the supply voltage is 0.4 V which guarantees that the NC-FinFET is biased to operate in a weak inversion region. In this paper, I_{ON} refers to the I_D when V_g equals supply voltage, I_{OFF} refers to the I_D when V_g is zero. Multi-channel structure[45, 46] may resolve this problem at a high cost, and the drive strength is adjusted by changing the number of fins. The current simulation model adopted a representative multi-channel structure, namely dual-channel structure.

SIMULATION RESULTS OF TRANSFER PERFORMACE

Fig. 2 shows that the transfer performance of dual-channel FinFET with N_D varied from 2×10^{17} / cm^3 to 1×10^{18} / cm^3. Fig. 2(a) shows the variation tendency of SS and I_{ON}/I_{OFF}, and Fig. 2(b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively. Fig. 2 shows that SS of FinFET decreases with increasing N_D. This decreasing tendency is outstandingly enhanced when it comes to NC-FinFETs. It is evident that the I_{ON} of FinFET with HfO_2, BTFM-CTO and PZT film remarkably decreases, decreases, and increases with increasing N_D, respectively. Moreover, the I_{OFF} of FinFET with HfO_2 or BTFM-CTO film decreases with increasing N_D. In contrast, I_{OFF} of NC-FinFET with PZT film increases with increasing N_D. Variation tendency of I_{ON}/I_{OFF} with increasing N_D is almost in contrast with that of I_{OFF}.

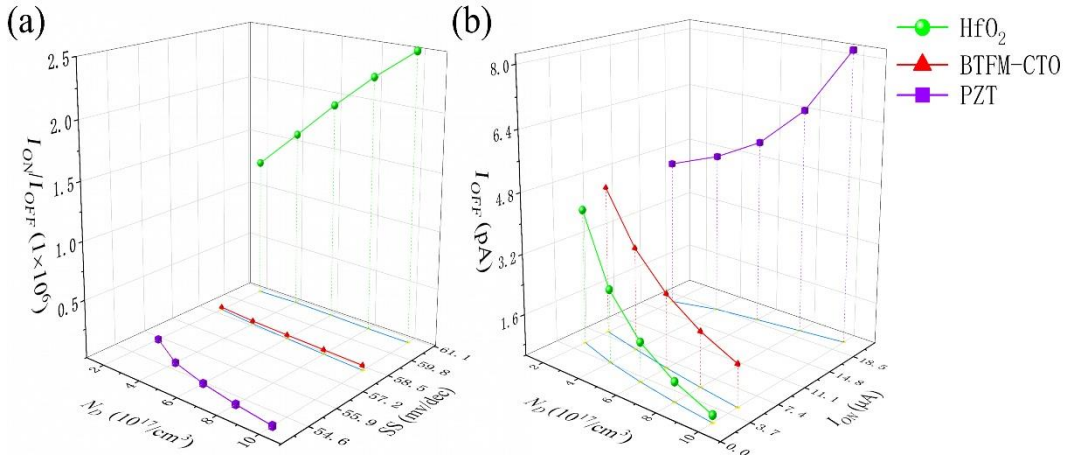

Fig. 2. Transfer performance of dual-channel FinFET with substrate doping concentration (N_D) varied from 2×10^{17} / cm^3 to 1×10^{18} / cm^3: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively.

Fig. 3 shows that the transfer performance of dual-channel FinFET with T_{FE} varied from 6 nm to 16 nm. Fig. 3(a) shows the variation tendency of SS and I_{ON}/I_{OFF}, and Fig. 3(b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are BTFM-CTO and PZT, respectively. Benefiting from the GVA effect, large T_{FE} leads to small SS and large I_{ON}, especially when the ferroelectric film is PZT, as shown in Fig. 3. This variation tendency is consistent with the conclusion deduced from equations (3) and (6). I_{OFF} of NC-FinFET with BTFM-CTO film presents a clear decrease tendency with increasing T_{FE}. However, PZT film achieves a minimum value at 10 nm T_{FE}. When T_{FE} equals 16 nm, I_{OFF} and I_{ON}/I_{OFF} are unexpectedly large and small, respectively. The I_{ON}/I_{OFF} variation tendency of NC-FinFET with PZT film is nearly consistent with the corresponding variation tendency of I_{ON}. That with BTFM-CTO film contrasts with the corresponding variation tendency of I_{OFF}.

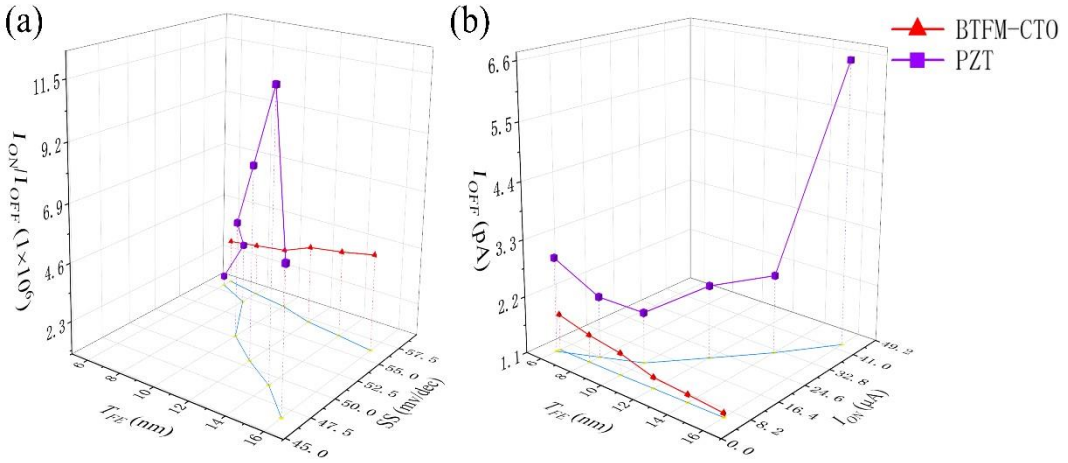

Fig. 3. Transfer performance of dual-channel NC-FinFET with with ferroelectric layer thickness (T_{FE}) varied from 6 nm to 16 nm: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are BTFM-CTO and PZT, respectively.

Fig. 4 shows that the transfer performance of dual-channel FinFET with C_L varied from 35 nm to 60. Fig. 4(a) shows the variation tendency of SS and I_{ON}/I_{OFF}, and Fig. 4(b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively. It is detected in Fig. 4 that SS of FinFET decreases with increasing C_L. While the SS of NC-FinFET increases with increasing C_L, especially when the ferroelectric film is PZT. I_{ON} decreases with increasing C_L. Another noteworthy finding is that the I_{ON} of FinFET with HfO_2 film decreases more dramatically than that with BTMF-CTO or PZT film. I_{OFF} of FinFET with HfO_2, BTFM-CTO, and PZT film decreases, increases, and markedly increases with increasing C_L, respectively. The variation tendency of I_{ON}/I_{OFF} with increasing C_L contrasts with that of I_{OFF}.

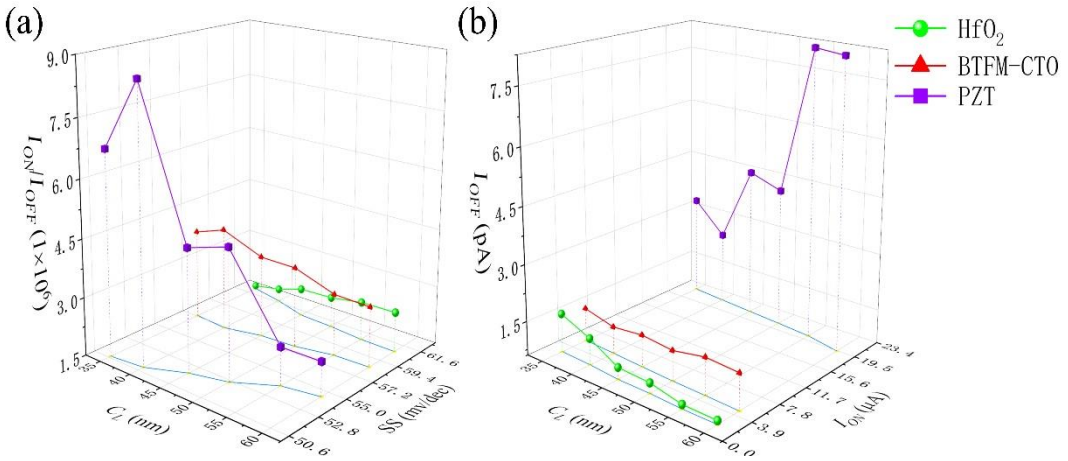

Fig. 4. Transfer performance of dual-channel FinFET with channel length (C_L) varied from 35 nm to 60 nm: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively.

Fig. 5 shows that the transfer performance of dual-channel FinFET with C_W varied from 15 nm to 40 nm. Fig. 5(a) shows the variation tendency of SS and I_{ON}/I_{OFF}, and Fig. 5(b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively. From Fig. 5, we can learn that SS of FinFET with HfO_2, BTFM-CTO, and PZT film increases, almost remains unchanged, and decreases with increasing C_W, respectively. I_{ON} of FinFET with HfO_2 or BTFM-CTO film decreases with increasing C_W. While that with PZT film dramatically increases with increasing C_W. It is noticeable that the I_{OFF} of FinFET with HfO_2, BTFM-CTO, and PZT film slightly increases, decreases, and

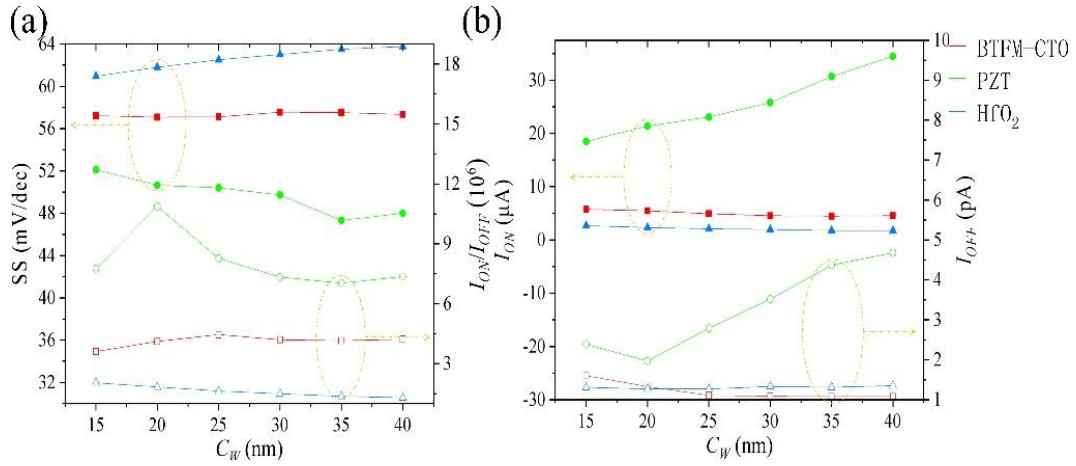

Fig. 5. Transfer performance of dual-channel FinFET with channel width (C_W) varied from 15 nm to 40 nm: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively.

outstandingly increases with increasing C_W, respectively. Moreover, I_{OFF} of NC-FinFET with PZT film achieves a minimum value at 20 nm C_W. The effect of C_W on the variation tendency of I_{ON}/I_{OFF} is in contrast with that of I_{OFF}.

Fig. 6 shows the transfer performance of single-channel FinFET whose gate dielectric materials are HfO2, BTFM-CTO, and PZT. Its C_W varies from 30 nm to 80 nm to keep the same channel volume as dual-channel FinFET. Overall transfer performance variation tendency of single-channel NC-FinFET with increasing C_W is similar to that of double-channel FinFET. A careful comparison between Fig. 5 and 6 reveals that double-channel NC-FinFET tends to have relatively large SS but large I_{ON} and small I_{OFF} compared with single-channel NC-FinFET. Moreover, drain current (I_d) decreases if the C_W is too large (larger than 70 nm).

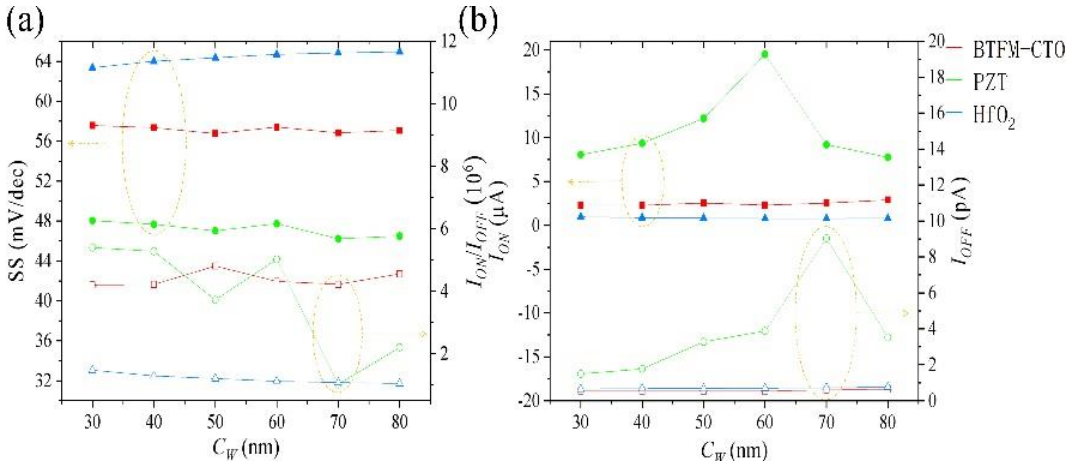

Fig. 6. Transfer performance of single channel FinFET with channel width (C_W) varied from 30 nm to 80 nm: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively.

Fig. 7 shows that the transfer performance of dual-channel FinFET with C_H varied from 30 nm to 80 nm. Fig. 7(a) shows the variation tendency of SS and I_{ON}/I_{OFF}, and Fig. 7(b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively. As shown in Fig. 7, SS of FinFET with HfO_2, BTFM-CTO, and PZT film increases, remains unchanged, and decreases with increasing C_H, respectively. Moreover, when C_H equals 50 nm SS of NC-FinFET with PZT film achieves maximum value. I_{ON} increases with increasing C_H. Another remarkable finding is that the I_{ON} increase tendency of NC-FinFET with PZT film is steeper than that with BTFM-CTO or HfO_2 film. However, it is not monotonous. I_{OFF} of FinFET with HfO_2 or BTFM-CTO film increases with increasing C_H. I_{OFF} and I_{ON}/I_{OFF} variation tendency of NC-FinFET with PZT film is confusing and requires further research. I_{ON}/I_{OFF} of NC-FinFET with HfO_2 and BTFM-CTO film decreases and increases with increasing C_H, respectively.

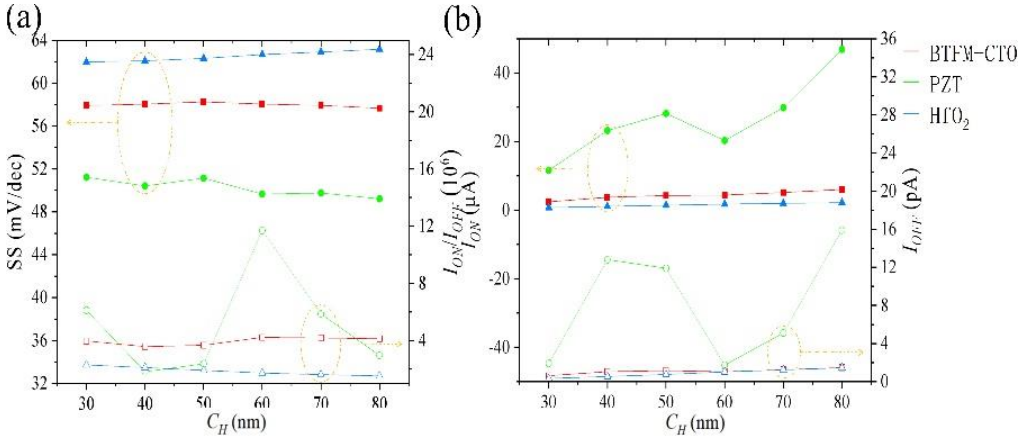

Fig. 7. Transfer performance of dual-channel FinFET with channel width (C_H) varied from 30 nm to 80 nm: (a) shows the variation tendency of SS and I_{ON}/I_{OFF}, (b) shows the variation tendency of I_{ON} and I_{OFF}. Gate dielectric materials are HfO_2, BTFM-CTO, and PZT, respectively.

SIMULATION RESULTS OF POLARIZATION AND POTENTIAL

To precisely give analyses on the effect of structural factors on the performance of dual- NC-FinFET and its gate control, the variation tendency of V_{int} and P with varying structure factors have been investigated. This variation tendency reflects the fluctuation of gate control and non-uniform distribution of P. Moreover, the variation tendency of V_{int} with and without 0.4 V V_g bias reflects the GVA and NDR effect change, respectively. Moreover, P and V_{int} are related to each other. FinFET has three gates, namely the top, front and back gate. Front gate and back gate form symmetry with each other. In current work, they are classified into side gates. Side P and top P are defined to better describe the structure, which refers to the P located in the center of the side and top gate ferroelectric film. Similarly, side V_{int} and top V_{int} are defined, referring to the V_{int} near the side and top gate. The value located in the center of the top and side represents the overall value.

The Variation tendency of side and top P with varying C_W, C_L, C_H, and N_D is shown in Fig. 8, indicating the overall variation tendency of P when structure factors are changed. Overall variation tendency of P increases when C_W, C_L, C_H, and N_D increase. Fig.8(a) shows that as C_W increases, the increase of top P is more outstanding than that of side P when the ferroelectric film is PZT. Fig. 8(b) reveals that the increased tendency of side P is more remarkable than that of top P when N_D increases. Fig. 8(c) indicates that top P achieves maximum value at 40 nm C_L and side P is relatively large when dielectric gate film is PZT. What is more, P is relatively not sensitive to C_L. The variation tendency of P with C_H from 30 nm to 80 nm shown in Fig. 8(d) is not monotonous. Top P and side P achieve minimum values at 50 and 60 nm C_H, respectively. When C_H equals 80 nm, the P in the side PZT film is relatively large. Due to the lack of an internal metal gate, ferroelectric polarization is not uniform. Increasing P distributes mainly in the bottom of the side film and the center of the top film. Possible cause is that the horizontal and vertical electric fields across the channel and ferroelectric film affect each other.

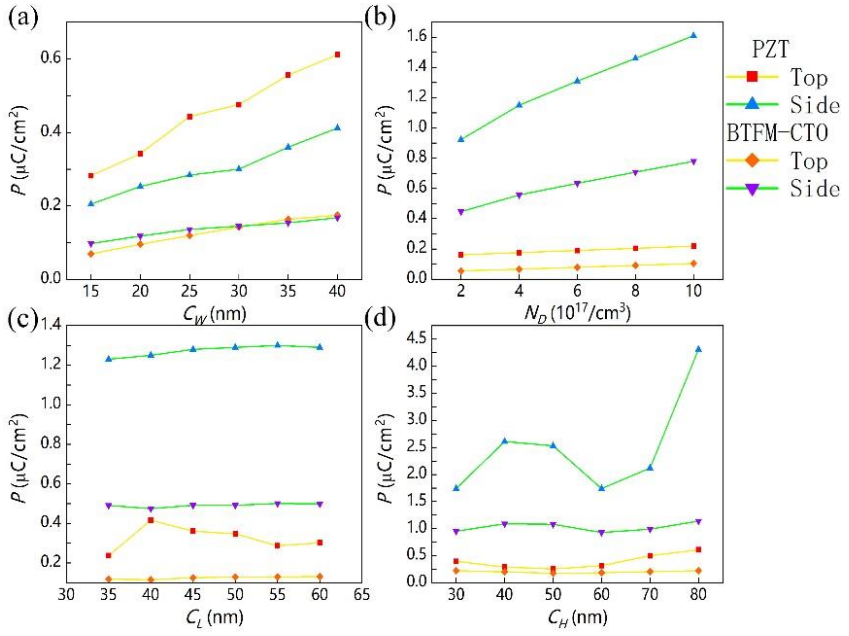

Fig. 8. Ferroelectric polarization (P) in the center of the top and side ferroelectric film. (a) Channel width (C_W) varied from 15 nm to 40 nm. (b) Substrate doping concentration (N_D) varied from 2×10^{17} / cm^3 to 1×10^{18} / cm^3. (c) Channel length (C_L) varied from 30 nm to 65 nm. (d) Channel height (C_H) varied from 30 nm to 80

To simultaneously achieve superior performance and low power consumption, I_{ON} transistors are supposed to be large and I_{OFF} transistors should be as small as possible. Thus, V_{int} should be high when

V_g equals V_{DD} while it should be low when V_g is zero. To make it, a splendid gate control is needed. Fig. 9 shows the variation tendency of side and top V_{int} with (a, c) and without (b, d) 0.4 V V_g, respectively. (a-b): C_W is varied from 15 nm to 40 nm. (c-d): N_D is varied from 2×10^{17} / cm^3 to 1×10^{18} / cm^3. It is distinct in Fig. 9(a) that the top V_{int} decreases with increasing C_W, which indicates that gate control over the center of the top channel is weakened as C_W increases. In contrast, the side V_{int} increases with increasing C_W, especially when the ferroelectric film is PZT. Fig. 9(b) shows that when V_g equals zero, top V_{int} decreases with increasing C_W.

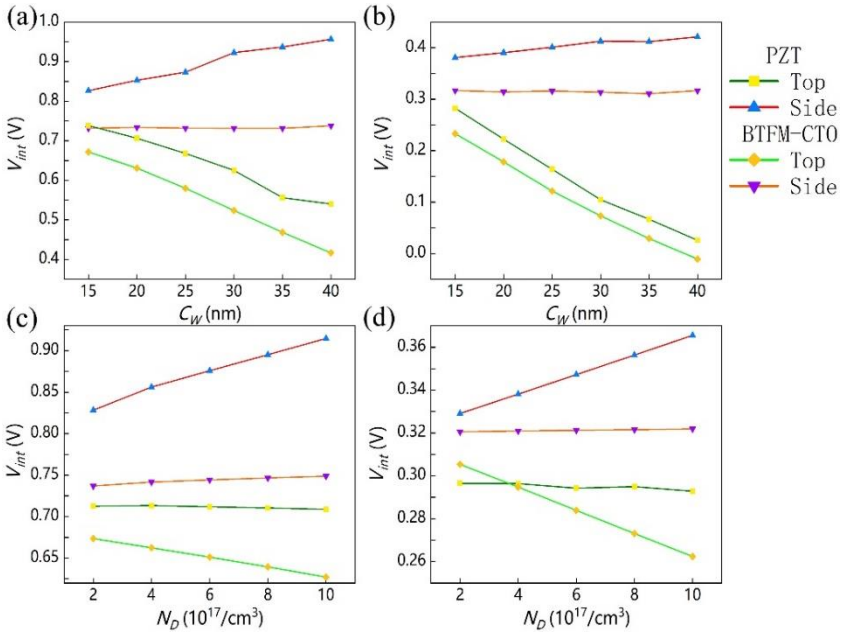

Fig. 9. Electronic potential in the center of the top and side channel (V_{int}). (a-b) Channel width (C_W) varied from 15 nm to 40 nm. (c-d) Substrate doping concentration (N_D) varied from 2×10^{17} / cm^3 to 1×10^{18} / cm^3. (a-c) 0.4 V gate voltage (V_g) and 0.05 V drain voltage (V_d). (d) 0 V V_g and 0.05 V$_d$.

What is more, side V_{int} of NC-FinFET with PZT film increases with increasing C_W while that with BTFM-CTO film decreases with increasing C_W. Thus, the overall NDR effect and gate control are strengthened, leaving I_{OFF} decrease with increasing C_W when the ferroelectric film is BTFM-CTO film. While that with PZT film is contrast, as shown in Fig. 5(b). Fig. 9(c-d) shows that the side and top V_{int} of NC-FinFET with PZT film increase and decrease with increasing N_D, respectively. Regarding BTFM-CTO film, the increase of side V_{int} fades and the decrease of top V_{int} boosts. Therefore, when N_D increases, the overall GVA and NDR effect of NC-FinFET with PZT film are enhanced and weakened with increasing N_D, respectively. Thus, when V_g equals V_{DD}, the gate control is reinforced, but when V_g is zero, the gate control is weakened. Correspondingly, SS is steep, and I_{ON}, together with I_{OFF}, becomes significant with increasing N_D. The variation tendency is almost converse when the ferroelectric film is BTFM- CTO, as shown in Fig. 2.

Fig. 10(a) shows that overall V_{int} is slightly increased with increasing C_L which signifies that the GVA effect is enhanced and the NDR effect is weakened with increasing C_L. The variation tendency of V_{int} with increasing C_H is shown in Fig.10(b), which is consistent with that of P, I_{ON}, and I_{OFF}. This variation tendency is overall increasing but not monotonous. Fig. 10(c) shows that when V_g equals zero, both top and side V_{int} of NC-FinFET with PZT film increases with increasing T_{FE}. Thus, the NDR effect and gate control are weakened when V_g is zero, and I_{OFF} increases with increasing T_{FE}. The variation tendency is converse if the ferroelectric film is BTFM-CTO, as shown in Fig. 3(b) and Fig. 10(c).

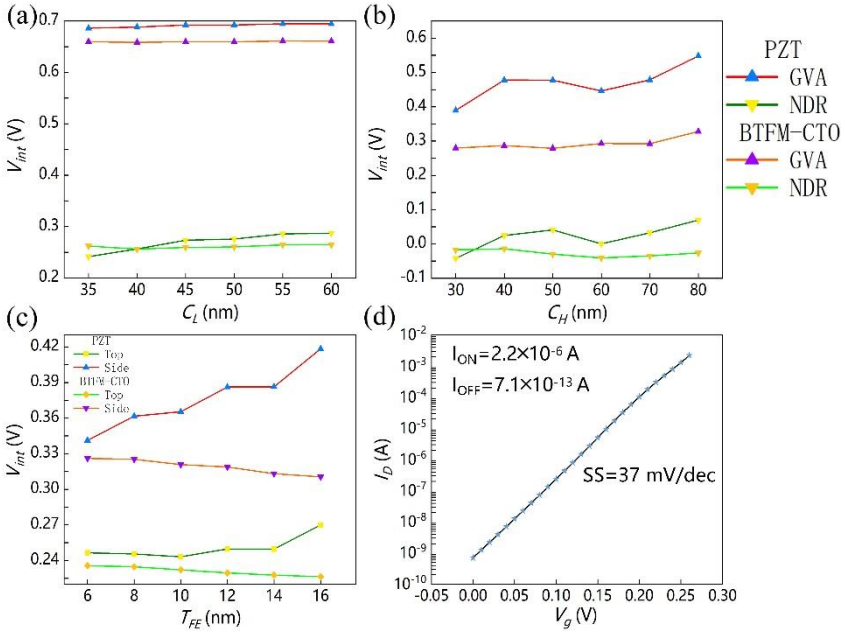

Fig. 10. Electronic potential in the center of the channel (V_{int}) with (GVA) and without (NDR) 0.4 V gate voltage (V_g). (a) Channel length (C_L) varied from 35 nm to 60 nm. (b) Channel Height (C_H) varied from 30 nm to 80 nm. (c) Electronic potential in the center of the top and side channel with T_{FE} varied from 6 nm to 16 nm and 0 V V_g. (d) Transfer curve of optimized single channel NC-FinFET with 0.25 V V_g.

ANALYSES AND DISCUSSION

When V_g equals V_{DD} increasing V_{int} distributes mainly in the side surface channel, and top V_{int} decreases with increasing C_W or N_D, which indicates that the top gate control and side gate control are weakened and enhanced, respectively. However, the overall GVA effect and gate control are enhanced when V_g equals V_{DD}, which results in steep SS and large I_{ON}. This enhancement is weak when the ferroelectric film is BTFM-CTO. In comparison, the transfer performance of FinFET with HfO_2 film deteriorates with increasing C_W or N_D, which is ascribed to inadequate gate control induced by large C_W or N_D. When V_g is zero, overall V_{int}, especially side V_{int}, increases with increasing N_D or C_W if the ferroelectric film is PZT. As a result, overall gate control is weakened, and I_{OFF} increases. Regarding BTFM-CTO film, the increase of side V_{int} is not outstanding, while the decrease of top V_{int} is significant, which is in favor of reinforced gate control. Correspondingly, I_{OFF} of NC-FinFTE with PZT film is relatively large, as shown in Fig. 2, 5 and 9.

The increasing tendency of V_{int} with increasing C_L is not significant and that of C_H is not monotonous. Consequently, gate control is weakened when V_g equals zero and gate control is reinforced when V_g equals V_{DD} with increasing C_H or C_L. Theoretically, I_d decreases as C_L increases for the weak electric field between drain and source. However, profiting from the reinforced gate control when V_g equals V_{DD}, I_{ON} drop of NC-FinFET with increasing C_L is not significant compared with that of FinFET. Moreover, I_{OFF} of NC-FinFET with PZT film increases with increasing C_L, which is attributed to the weak DNR effect and bad gate control when V_g is zero.

Similarly, NC-FinFET has steeper SS, large I_{ON} and I_{OFF} with large C_H when compared with FinFET especially if ferroelectric film is PZT, as shown in Fig. 4(b), Fig. 7 and Fig. 10(a-b). Fig. 10(c) shows that when V_g equals zero, the V_{int} of NC-FinFET with PZT film increases, and gate control is weakened with increasing T_{FE}. The variation tendency is converse when it comes to BTFM-CTO film. Fig. 2-7 shows that superior ferroelectric properties of PZT film endow NC-FinFET with steep SS, large I_{ON}.

However I_{OFF} of NC-FinFET with PZT film is relatively large and increases with increasing C_W, C_H, T_{FE}, and N_D (less than 20 pA). This phenomenon is outstandingly weakened when the ferroelectric film is BTFM-CTO, as shown in Fig. 2, 3 and 5. However, the transfer performance of NC-FinFET with PZT film is sensitive to the variation of structure factors. In general, ferroelectric properties play an essential role in the performance of NC-FinFET. Variation tendency of transfer performance may even be converse if the ferroelectric properties are changed. Fig. 4 shows that when C_L decreases, SS and I_{OFF} of NC-FinFET decrease, which is converse to conventional FinFET and to the benefit of scaling down. Moreover, the I_{ON} of NC-FinFET slightly decreases with increasing C_L compared with that of FinFET. Therefore, large C_L is terrible for the transfer performance of NC-FinFET, and gate control is significantly changed with varying C_L. To achieve steep SS, C_W, N_d, C_H, and T_{FE} should be significant, and C_L should be small.

Fig. 8 shows that the overall variation tendency of P at 0.4 V V_g increases when C_W, C_L, C_H, and N_D increase. The increased tendency of P with increasing C_W or N_D is relatively outstanding. Increasing P distributes mainly in the bottom of the side ferroelectric film and the center of the top ferroelectric film. The increase of side P is usually sharper than that of top P when C_W or N_D increases. Moreover, P is relatively not sensitive to the variation tendency of C_H or C_L. As a result, V_{int} increases, and gate control is enhanced. Thus, NC-FinFET has a significant advantage over FinFET regarding SS and I_{ON}, especially when the ferroelectric film is PZT. This advantage is reinforced by increasing C_W, C_H, and N_D, which indicates that the overall gate control is enhanced by increasing N_D, C_H, and C_W when V_g is 0.4 V, as shown in Fig. 2, 5, and 7.

Drive strength of MOSFET is adjusted by changing its width (W) and length (L). Regarding FinFET, the equivalent W is defined by two C_H and C_W. However, this law fails to precisely apply in FinFET for the inflation of gate control induced by variation of structure factors. According to L-K equations, P is theoretically determined by V_{FE}. However, due to the lack of an internal gate and multi-domain structure of ferroelectric material, the distribution of P and V_{int} is not uniform. Thus, gate control of NC-FinFET is more sensitive to the variation of structure factors than FinFET. As stated, gate control is mainly reflected by transfer performance, especially the SS. Fig. 2, 4, 5, and 7(a) show that SS of NC-FinFET with BTFM-CTO film is more resistant to the variation of structure factors.

As demonstrated above, the effect of structural factors on gate control depends on the ferroelectric film. Large C_H or C_W makes the gate control weak, while NC can enhance the gate control. Supposing that a suitable set of structure factors and ferroelectric parameters is obtained. In that case, the balance between these two effects can be achieved, which means that the fluctuation of gate control with increasing C_H or C_W is significantly diminished. Similarly, large C_L reinforces the gate control while NC weak the gate control. Similarly, the fluctuation of gate control with increasing C_L can also be significantly diminished. Therefore, it is practicable that the drive strength of NC-FinFET can be adjusted by changing its size without significant fluctuation of gate control if a suitable set of structure factors and ferroelectric parameters is obtained. Compared with other structure factors, increasing T_{FE} and C_H can significantly increase the I_{ON} of NC-FinFET with PZT film. However, this adjustment is inaccurate, as shown in Fig. 3 and 7. The multi-channel structure is a promising alternative to adjust the drive strength of NC-FinFET, but further research is needed to reduce its cost and complexity. Fig. 5 and Fig. 6 reveal that if given the same channel volume, dual-channel NC-FinFET shows relatively large SS but large I_{ON} and small I_{OFF} compared with single-channel NC-FinFET.

Fig. 10(d) shows the transfer performance of optimized single-channel NC-FinFET with PZT film. Its C_W, C_L, C_H, $T_{FE,}$ and N_D are 60 nm, 40 nm, 45 nm, 18 nm, and 1×10^{18}/cm^3, respectively. To better illustrate its superior performance, we compare this NC-FinFET and other NCFETs reported in a review that is just published[47], as shown in Fig. 11. In Fig. 11, V_{DD} refers to the V_g or $V_{d,}$ and some missing data is not given. The NC-FinFET designed by us has a relatively steep SS (37 mV), small V_{DD} (0.24 V), T_{FE} (18 nm), and gate length (L_G) (40 nm), which is beneficial for the high performance of NCFET. Moreover, profiting from high electron mobility and wide bandgap, the NC-FinFET reported in the current work has a high I_{ON}/I_{OFF} value of 3.1×10^6. Results achieved in the current work demonstrate that GaAs-NC-FinFET is a promising candidate for NCFET. The GaAs NCFET designed by us applies to the optimization of GaAs-based devices in memory or low power applications.

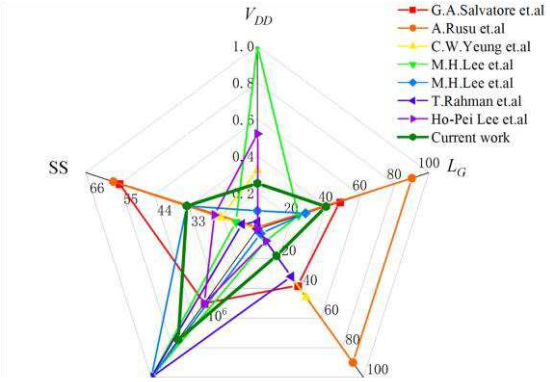

Fig. 11. Radar chart of the different figures of merit (FOMs) for different NCFETs.

CONCLUSION

In this work, a detailed simulation was made on NC-FinFET to clarify the effect of crucial structural factors on the performance of NC-FinFET, which is related to gate control. Simulation results show that the overall variation tendency of P and V_{int} increases when C_W, C_L, $C_{H,}$ and N_D increase. Increasing P and V_{int} distribute mainly in the bottom of the side and the center of the top. Correspondingly, gate control is enhanced, which leads to steep SS and large I_{ON} but large I_{OFF} (less than 20 pA), especially when the ferroelectric film is PZT. In general, ferroelectric properties play an essential role in the performance of NC-FinFET. The effect of structural factors on gate control is usually converse to that of NC on gate control. Supposing that a suitable set of structure factors and ferroelectric parameters is obtained, the balance between these two effects can be achieved, which means that the fluctuation of gate control can be significantly weakened. Thus, the drive strength of NC-FinFET is hopeful to be adjusted by changing its size, and a multi-channel structure is not necessary. If given the same channel volume, dual-channel NC-FinFET shows relatively large SS but large I_{ON} and small I_{OFF} compared with single-channel NC-FinFET. Large C_W, T_{FE}, $C_{H,}$ and small C_L are suggested to endow NC-FinFET with steep SS and high I_{ON}/I_{OFF}. The current work generates new insights into the fluctuation of gate control with varying structure factors and adjustment of NC-FinFET drive strength, which are essential for NC-FinFET to applicate in analog circuits.

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