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Cryocooled wideband digital channelizing radio-frequency receiver based on low-pass ADC

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Abstract
We have demonstrated a digital receiver performing direct digitization of radio-frequency signals over a wide frequency range from kilohertz to gigahertz. The complete system, consisting of a cryopackaged superconductor all-digital receiver (ADR) chip followed by room-temperature interface electronics and a field programmable gate array (FPGA) based post-processing module, has been developed. The ADR chip comprises a low-pass analog-to-digital converter (ADC) delta modulator with phase modulation–demodulation architecture together with digital in-phase and quadrature mixer and a pair of digital decimation filters. The chip is fabricated using a 4.5 kA cm^{-2} process and is cryopackaged using a commercial-off-the-shelf cryocooler. Experimental results in HF, VHF, UHF and L bands and their analysis, proving consistent operation of the cryopackaged ADR chip up to 24.32 GHz clock frequency, are presented and discussed.

1. Introduction

The conventional analog radio-frequency (RF) technology fails to meet the demand for optimal spectrum utilization of future military and commercial radio-frequency applications, i.e. wider input bandwidth, higher frequencies and better flexibility in accommodation of a variety of input and output devices. Extension of digital processing to this traditionally analog RF domain is one of the most promising applications for superconductor electronics. This approach, known as software-defined radio [1], presents an opportunity for superconductor rapid single flux quantum (RSFQ) mixed-signal technology that enables direct conversion between analog and digital domains at multi-gigahertz radio frequencies. This concept of digitizing at RF and conducting all subsequent processing in the digital domain not only replaces the RF analog components, but also enables the true software radio architecture, and brings the power of digital processing to the RF domain.

HYPRES is developing a class of digital receivers with direct digitization at radio frequency (RF) for military and commercial applications. In what follows, we describe our progress in building such a digital receiver for HF, VHF, UHF and L bands as a complete turnkey system.

2. System description

This complete system, fitting into a standard 19 in. rack shown in figure 1, consists of an all-digital receiver (ADR) chip cryopackaged on a commercial-off-the-shelf (COTS) cryocooler, a computer-controlled multi-channel current source to bias the ADR chip, room-temperature interface amplifiers and a PCI FPGA-based post processing module. Details of the ADR chip architecture and design are described elsewhere [2]. The single-bit oversampled data from a low-pass phase modulation–demodulation (LP PMD) delta ADC modulator are applied to a digital channelizer comprising a single-bit digital in-phase and quadrature (I&Q) mixer and a pair of digital decimation filters. The complete 1 cm × 1 cm ADR chip contains about 10 500 Josephson junctions and was fabricated with the 4.5 kA cm^{-2} HYPRES fabrication process [3]. The ADR chip is packaged on a Sumitomo SRDK-101D-A11 two-stage cryocooler.

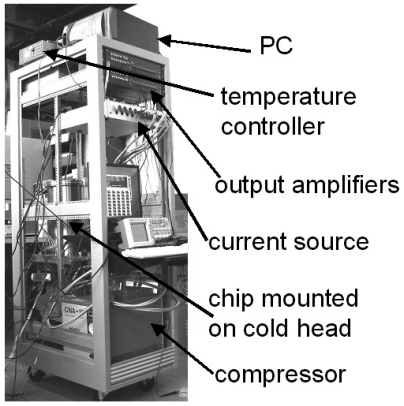

Figure 1. The complete 19 in. rack with all components of the digital receiver packaged on a Sumitomo cryocooler.

This cryocooler was selected due to its relative compactness, adequate heat lift and air-cooled compressor. It includes a helium damper to reduce temperature oscillations in order to avoid their potential effect on circuit operational bias margins. For this work, we used a second-generation cryopackage with a completely redesigned 4 K stage for better grounding and magnetic shielding. This new cryopackage enabled us to provide significantly reduced flux trapping and high thermal and electrical reliability. Figure 2 shows a cryocooler cold head both without (see figure 2(a)) and with chip assembly (figure 2(b)). These improvements allowed the system to operate with high reproducibility at clock frequencies up to 24.32 GHz with identical bias settings at temperatures from 4.03 to 4.38 K measured in close proximity to the chip.

The current version of the superconducting ADR chip has many independent dc bias currents, typically in the range of 1 to 100 mA per bias line. For this purpose, custom current-control hardware and software modules were designed and fabricated. The current source hardware module is shown in figure 3(a) and is a box mounted in a standard 19 in. rack. This box operates using less than 300 W of standard AC power. It consists of 48 independently controlled sources, which are connected to the cryocooler in 4 bundles of 12 lines each, shown on the right side of the front panel in figure 3(a). This current source is controlled by a computer using a standard USB-bus line located in the middle of the front panel. The current sources are under complete digital software control, but are additionally equipped with 4 multi-turn control knobs in the left portion of the front panel for those who prefer a more traditional rotary knob for adjusting currents. Each knob can be assigned to any of the 48 bias lines under software command from the graphical user interface (GUI). The current source box is equipped with a hardware 'mute' function. This mode is used whenever the system is turned ON or OFF to prevent fast transients from being coupled to the superconducting chip. This feature turned out to be quite practical in the real test environment.

The ADR digital output signals are generated and pre-amplified by the superconducting chip up to about 1–2 mV in amplitude. This is not sufficient to be accepted by the PCI FPGA-based post-processing module. We developed a custom amplifier bank consisting of two sets of 16 broadband amplifiers, mounted in the system 19 in. rack as shown in

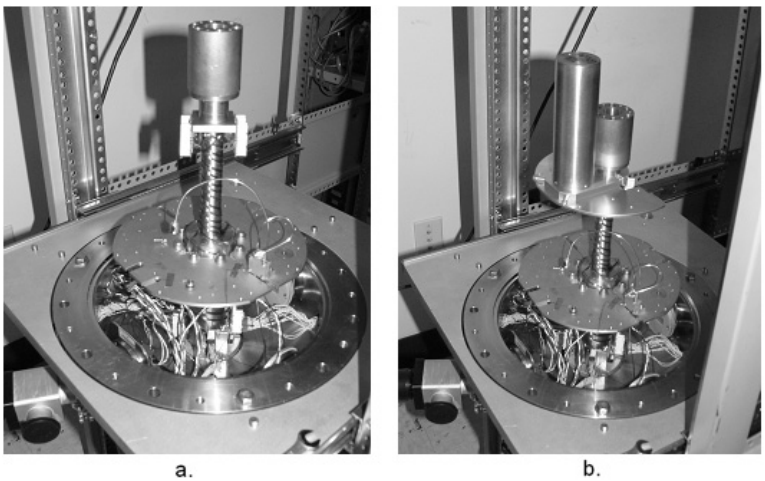

Figure 2. Coldhead of Sumitomo SRDK-101D-A11 cryocooler (a) without and (b) with chip assembly.

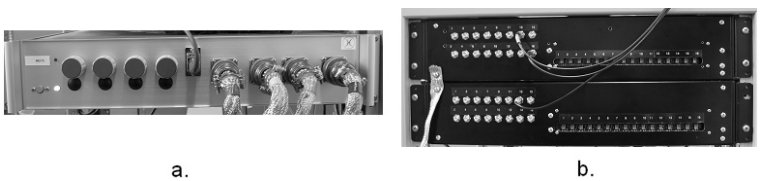

Figure 3. Custom-developed (a) multi-channel current source and (b) bank of output amplifiers.

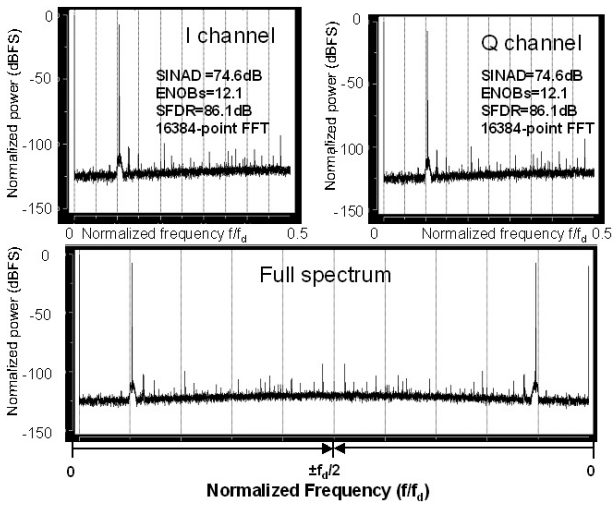

Figure 4. Spectrum of digital I and Q data and complex I + jQ FFT for a single 10 MHz input tone sampled at 24.32 GHz clock, digitally filtered, and acquired to FPGA at 95 MS s^{-1}.

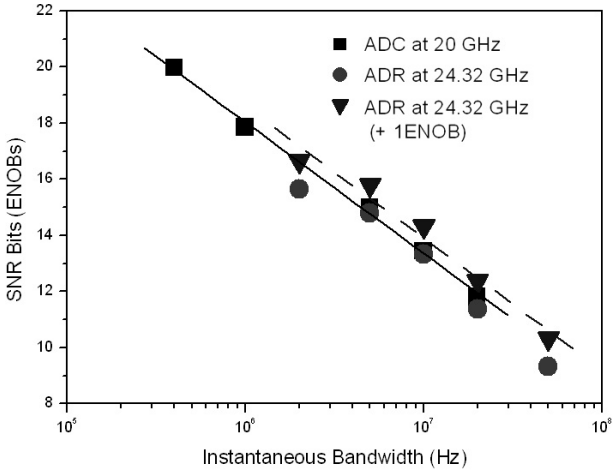

Figure 5. Experimentally measured (circles and squares) and projected (triangles) ENOB versus instantaneous bandwidth for ADR and ADC (please see text for details).

figure 3(b). For the ADR system described in this paper, only 27 of the 32 channels are being used—13 for each of the I and Q output signals and the output decimated clock. Each amplifier module consists of a linear stage with an amplitude gain of about 1000 to positive ECL level, followed by a pulse shaping stage that produces standard-level digital signals that are sent to a commercial FPGA data processing board housed in the internal PCI slot of the computer.

3. Experimental results

The ADR chip design [2] with special attention to magnetic shielding and uniformity of the bias current distribution together with improved cryopackage and custom-developed room-temperature electronics made reliable and reproducible chip operation possible. The chip operated with identical performance at $f_{\rm clk} = 24.32$ GHz with identical bias settings between 4.03 and 4.38 K. Turning the ADR system on from a quiescent state ($T < 4.38$ K) involved simply loading a file with preset bias values using our GUI and applying an external clock sinewave at 24.32 GHz.

We performed complete evaluation of the system both with and without applying a local oscillator (LO) input. Digital outputs were acquired and displayed with the help of room-temperature interface amplifiers, and a PCI FPGA data acquisition and processing board run by our GUI. Figure 4 shows the fast Fourier transform (FFT) for each I and Q channel and complex (I + jQ) FFT (16 384 points) from the acquired I and Q data with a single 10 MHz input tone. The full spectrum represents a bandwidth of $f_d = f_{\rm clk}/256 = 95$ MHz. To reduce the effects of harmonic distortion and noise from an available test signal generator, a 10 MHz bandpass filter with ∼1 MHz bandwidth was used. This is evident from the characteristic noise cusp in the vicinity of the tone (figure 4). The measurement was taken close to the slew rate limit of the ADC. The measured SINAD of 74.6 dB over a bandwidth of 47.5 MHz compares well with 75.7 dB over a bandwidth of 39 MHz produced by our low-pass (LP) ADC [4] with two-channel synchronizer.

The single-tone measurements with 2, 5, 20 and 50 MHz tones were performed with a variety of appropriate band-pass or low-pass filters, depending on their availability. To take full advantage of oversampling in our ADR, additional filtering in software was performed. In calculating the signal-to-noise ratio (SNR), only noise in the band from zero to the tone frequency has been integrated. As an example, for a 10 MHz tone at $f_{\rm clk} = 24.32$ GHz with $f_d = 95$ MHz, this additional filtering produced an additional 7.15 dB of SNR as compared to the result shown in figure 4. This improvement was achieved due to the band reduction ($10 \times \log(f_d/(2 \times 10\ \text{MHz})) = 6.77$ dB) and also due to the elimination of out-of-band harmonics. Figure 5 shows these data, together with our earlier data for an ADC chip clocked at 20 GHz clock [4]. The curves (solid for the ADC [4] and dashed for the ADR measured here) closely follow the effective number of bits (ENOB) versus bandwidth trade-off curve at a rate of 1.5-bit/octave characteristic for ideal delta modulators. The difference in the ENOB performance for two ADC circuits, the first with an N-channel synchronizer and the second with an M-channel synchronizer ($N > M$), but otherwise identical, is expected to be $\log_2 N - \log_2 M$ [5]. The phase modulation–demodulation ADC modulator circuit on both ADC and ADR chips are identical and has a two-channel synchronizer. However, the single-bit mixer on the ADR chip permits only one channel of the two-channel synchronizer to be used, resulting in the loss of 1 bit of resolution compared to the previous 20 GHz ADC chip [4]. For fair comparison, we have plotted another set of points by adding 1 ENOB to the ADR results.

In order to improve ADC linearity, a dither sinewave signal was applied to the input at the decimated clock frequency of 95 MHz. Indeed, data recorded with the dither applied shows the spur-free dynamic range (SFDR) improvement up to 10 dB, especially for small signal amplitudes. Since the dither signal does reduce the signal-to-noise ratio somewhat, its power was kept at a minimum. The positive effect of the dither was maximized by tuning

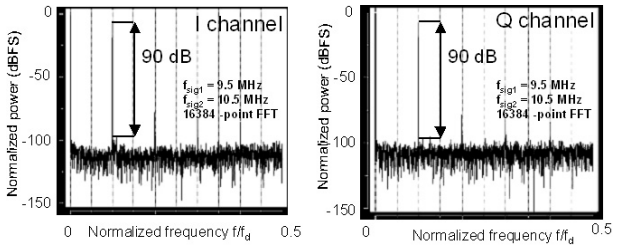

Figure 6. The two-tone 'big–little' 16 384-point spectra of the I-channel output (left) and the Q-channel output (right) acquired at 24.32 GHz. The 9.5 MHz tone has an amplitude of −5 dBm, while the 10.5 MHz tone has an amplitude of −95 dBm. A top section of the narrow tone on the spectra is further obscured by a grid line. The full spectrum (I + jQ) is not shown.

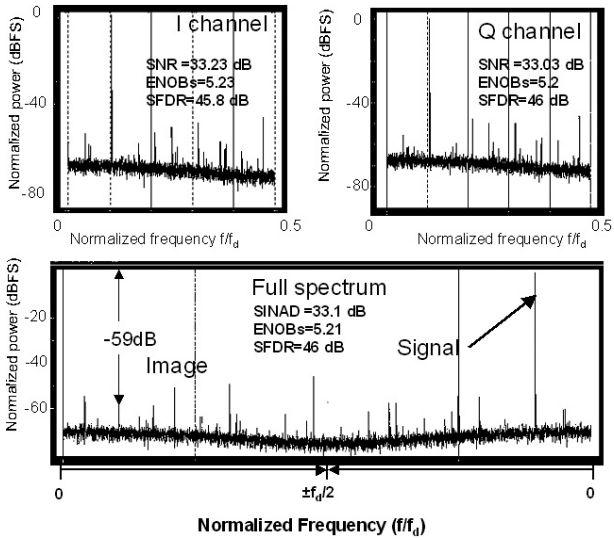

Figure 7. The 16 384-point spectra of the I-channel output (top left) and the Q-channel output (top right) along with the full spectrum (I + jQ, bottom) acquired at 24.32 GHz. The input tone frequency is 950 MHz and the LO is 940 MHz. The output bandwidth ($f_d = f_{clk}/256$) is 95 MHz.

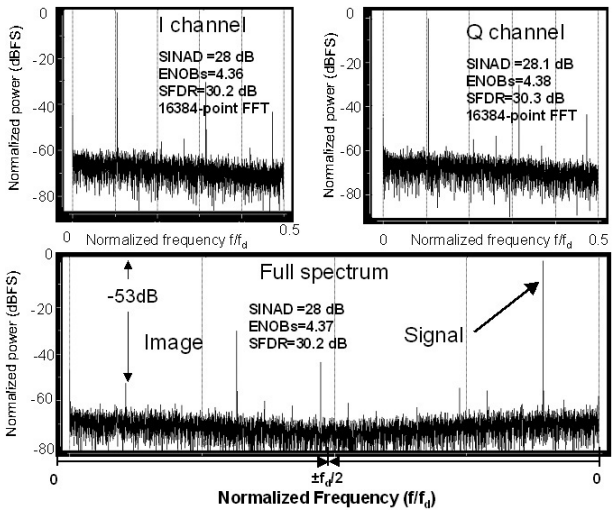

Figure 8. The 16 384-point spectra of the I-channel output (top left) and the Q-channel output (top right) along with the full spectrum (I + jQ, bottom) acquired at 24.32 GHz. The input tone frequency is 1.5 GHz and the LO is 1.49 GHz. The output bandwidth ($f_d = f_{clk}/256$) is 95 MHz.

dither power and observing smoothed-out quantization steps on signal reconstruction for a low amplitude, low frequency input signal [4]. To make this process easier by making quantization steps more pronounced, a triangular input signal was applied. The dither was particularly useful in detection of single-tone small amplitude signals.

Detection of small signals in the presence of large interferers is important for many signals intelligence, communication, and radar applications. As an example, figure 6 shows the FFT of I- and Q-channels (complex spectra are not shown for simplicity) when a −95 dBm 10.5 MHz signal was applied to the ADR chip in the presence of a 9.5 MHz signal with −5 dBm amplitude. In this so-called 'big–little' test, the 10.5 MHz tone is clearly recognizable on the spectra.

A collection of FFT spectra were acquired with the input RF signals in HF, VHF, UHF and L bands while the LO frequency was chosen to obtain a 10 MHz intermediate frequency (IF) response. In our single-bit mixer, we use a single-bit square-wave LO signal derived from an external sinewave generator signal [2]. Figure 7 shows the FFT for I- and Q-channels and the complex (I + jQ) FFT (16 384 points) with a 950 MHz sinewave input. A local oscillator at 940 MHz was applied. The IF at 10 MHz is clearly visible for both I- and Q-channels. The image rejection was measured from the complex FFT to be 59 dB. Similarly, figure 8 shows the FFT for I- and Q-channels and the complex (I + jQ) FFT (16 384 points) with a 1.5 GHz sinewave input. A local oscillator at 1.49 GHz was applied. The IF at 10 MHz is clearly visible for both I- and Q-channels. The image rejection was measured from the complex FFT to be 53 dB. The signal-to-noise ratio for the 950 MHz (figure 7) and the 1.5 GHz input (figure 8) is expectedly lower than for 10 MHz input (figure 4). This is due to the lower input RF amplitude necessary to stay within the LP delta ADC slew-rate limit—the maximum signal, for example, at 1.5 GHz is about 43.5 dB less than that at 10 MHz. Additionally, the SNR is reduced by the mixing of out-of-band quantization noise with the harmonics of the single-bit square-wave LO. With this type of LO, only odd harmonics are present. Under the assumption that their power decreases as $1/f^2$ and the quantization noise power increases approximately as f^2 (since the mixing occurs right after the delta modulator) the harmonic excess noise is approximately 4.8 dB. This corresponds to three odd harmonics of the local oscillator that fall within the unfiltered quantization noise band $0 - f_{clk}/2$. At lower input frequencies, the excess noise contribution due to mixing by the LO harmonics is greater since more of them contribute. Figure 9 shows the collection of measured data with the input RF signals in VHF, UHF and L bands. The corresponding LO signals were applied in order to obtain a 10 MHz IF response. When tests were performed with certain input signals, e.g. 450 MHz, 800 MHz, 925 MHz, 1.1 GHz and 1.35 GHz, the FFT spectra showed much richer harmonic content than at neighboring frequencies. This significantly reduced the SINAD for those input signals

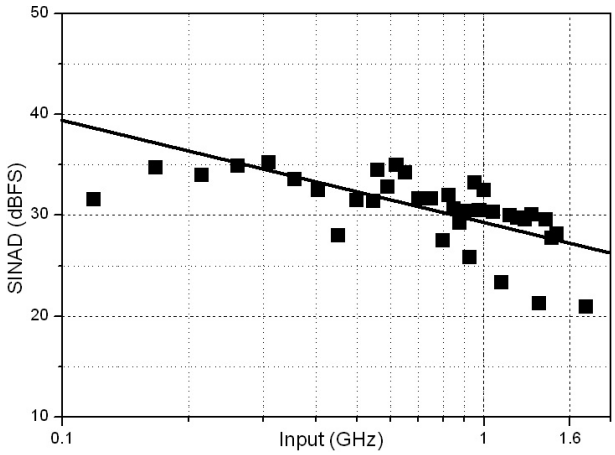

Figure 9. SINAD versus input signal frequency. See text for details. A line with the slope of 3 dB/octave is also shown for reference.

and reflected by outliers on SINAD versus input dependence (figure 9). The reason for this SINAD reduction is not yet fully understood and requires further investigation currently underway. The line with the slope of 3 dB/octave to account for the 6 dB/octave loss due to the slew-rate limit and gain of 3 dB/octave due to the decrease in the number of LO harmonics within $0 - f_{\mathrm{clk}}/2$ band is shown in figure 9.

4. Conclusions

In conclusion, we have developed a digital receiver for HF, VHF, UHF and L bands as a complete turnkey demonstrator system. The system fits in a standard 19 in. rack and consists of a superconducting chip packaged on a COTS cryocooler and accompanied by all necessary custom-built room-temperature hardware and software such as a computer-controlled multi-channel current source, interface amplifiers, FPGA-based post-processing PCI module and PC with GUI. The system reliably operated at 24.32 GHz clock frequency with consistent performance both inside and outside of our lab run by both HYPRES and customer personnel. To our knowledge this is the fastest digital receiver demonstrated to date.

Acknowledgments

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