

Cryogenic Control Architecture for Large-Scale Quantum Computing

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Solid-state qubits have recently advanced to the level that enables them, in principle, to be scaled-up into fault-tolerant quantum computers. As these physical qubits continue to advance, meeting the challenge of realising a quantum machine will also require the engineering of new classical hardware and control architectures with complexity far beyond the systems used in today's few-qubit experiments. Here, we report a micro-architecture for controlling and reading out qubits during the execution of a quantum algorithm such as an error correcting code. We demonstrate the basic principles of this architecture in a configuration that distributes components of the control system across different temperature stages of a dilution refrigerator, as determined by the available cooling power. The combined setup includes a cryogenic field-programmable gate array (FPGA) controlling a switching matrix at 20 millikelvin which, in turn, manipulates a semiconductor qubit.

Realising the classical control system of a quantum computer is a formidable scientific and engineering challenge in its own right^{1,2}. The hardware that comprises the control interface must be fast relative to the timescales of qubit decoherence, low-noise so as not to further disturb the fragile operation of qubits, and scalable with respect to physical resources, ensuring that the footprint for routing signal lines or the operating power does not grow rapidly as the number of qubits increases^{3,4}. As solid-state quantum processors will likely operate below 1 kelvin⁵⁻⁸, components of the control system will also need to function in a cryogenic environment, adding further constraints.

Similar challenges have long been addressed in the satellite and space exploration community⁹, where the need for high-frequency electronic systems operating reliably in extreme environments has driven the development of new circuits and devices¹⁰. Quantum computing systems, on the other hand, have to date largely relied on brute-force approaches, controlling a few qubits directly via room temperature electronics that is hardwired to the quantum device at cryogenic temperatures.

Here we present a control architecture for operating a cryogenic quantum processor autonomously and demonstrate its basic building blocks using a semiconductor qubit. This architecture addresses many aspects related to scalability of the control interface by embedding multiplexing sub-systems at cryogenic temperatures and separating the high-bandwidth analog control waveforms from the digital addressing needed to select qubits for manipulation. Our demonstration comprises a commercial field-programmable gate array (FPGA) operating at 4 kelvin and controlling a microwave signal switching matrix at 20 mK, which then interfaces with a quantum dot device. Bringing these sub-systems together in the con-

text of our control architecture suggests a path for scale-up of control hardware needed to manipulate the large numbers of qubits in a useful quantum machine.

I. CONTROL MICRO-ARCHITECTURE

Our control micro-architecture takes advantage of the universality of quantum gates, which allows for arbitrary logic operations to be realised using a small set of repeated single- and two-qubit unitaries applied in sequence. At the level of physical qubits in the solid-state, whether they are spins¹¹, transmons⁶, or quasiparticles¹², these elemental gate operations amount to applying calibrated electrical waveforms to a particular qubit or pair of qubits each clock cycle as determined by a quantum algorithm.

A key aspect of our control architecture is the separation of these analog 'prime waveforms', which are typically pulses at microwave frequencies, from the digital qubit addressing information that determines which waveform is directed to which qubit, at a particular point in the code. In comparison to brute-force approaches, this scheme lifts the need of having a separate waveform generator and transmission line for each qubit, taking advantage of a small universal gate set that uses the same analog waveforms over-and-over throughout the algorithm. As realistic qubits will inevitably include variations in their physical parameters, the control architecture must also incorporate means of calibrating and adjusting the response of the qubit to the control waveforms, as described below.

Our 'prime-line / address-line' (PL/AL) architecture is shown schematically in Fig. 1, where we have drawn part of a circuit for implementing a quantum error cor-

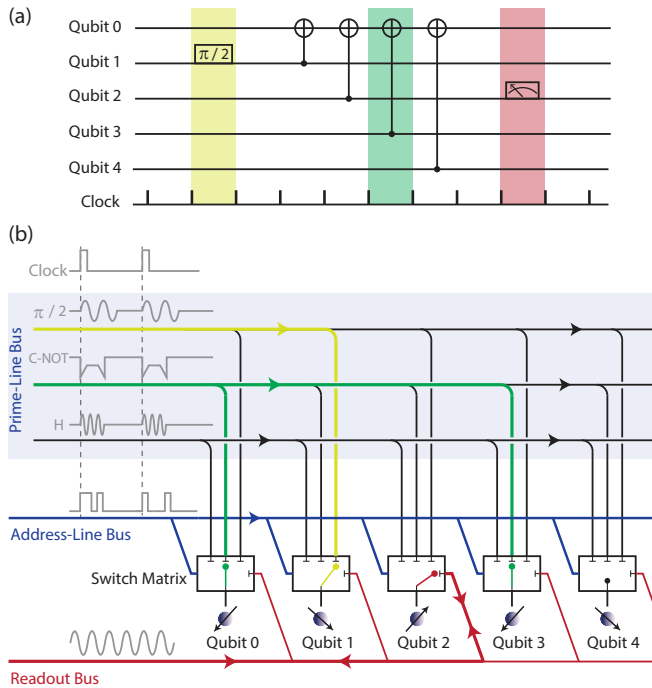


FIG. 1. ‘Prime-line / Address-line’ (PL/AL) architecture that separates prime analog waveforms, used to manipulate qubits, from the addressing data used to select qubits. (a) An example quantum algorithm shown using quantum circuit notation. The highlighted clock cycles include a single-qubit rotation (yellow), a two-qubit gate (green) and readout operation (red). (b) Prime-lines corresponding to a universal gate set are routed to qubits via a switching matrix controlled by the address-lines. Coloured paths correspond to the highlighted clock cycles in (a).

recting surface code^{13,14}. Precisely timed analog prime waveforms, generated at cryogenic or room temperature, propagate cyclicly on a high-bandwidth prime-line bus that is terminated with a matched impedance at a location in the system where heat can be dissipated. The quantum algorithm is then executed exclusively via the digital address-line bus, selecting qubits and qubit pairs to receive the appropriate prime waveform at the correct clock cycle in the circuit. Readout proceeds in a similar way, with the digital address bus selecting a particular qubit (or readout device) for interfacing with analog readout circuitry such as a chain of amplifiers and data converters.

II. IMPLEMENTATION OF THE CONTROL ARCHITECTURE

Realising our PL/AL architecture requires integrating multi-component control and readout hardware with the quantum system of qubits fabricated on a chip. Owing to the large number of qubits that are likely to be needed for quantum computation and the timescales involved in their control, there are advantages to locat-

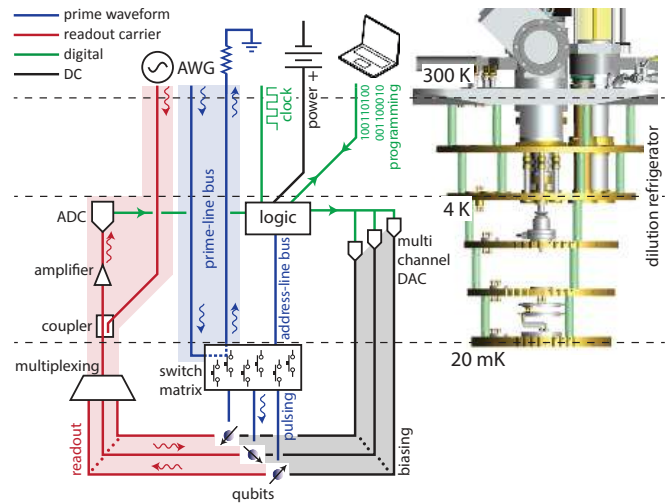


FIG. 2. Schematic of a control micro-architecture that distributes sub-systems across the various temperature stages of a dilution refrigerator, depending on the available cooling power (image is of a Leiden Cryogenics CF450). A millikelvin switching matrix, on the same chip as the qubit device or close to it, steers a small number of control pulses to qubits using addressing information from cryogenic logic at 4 K. The cryogenic logic also interfaces with multiplexed readout and digital-to-analog converters. The 4 K stage typically has a cooling power ~ 1 W, with the 20 mK stage having less than 1 mW.

ing sub-systems of the control architecture at cryogenic temperatures, either on-chip with the physical qubits, or in close proximity and connected via integrated multi-chip modules¹⁵ and compact transmission lines. Aspects of the control system will however, generate significant heat or fail to function at the millikelvin temperatures needed for qubit operation. The competing constraints of interconnect density, heat generation, signal latency, footprint, and noise performance suggest a control architecture that is distributed across a cryostat, taking advantage of the significantly different thermal budgets available at each temperature stage. This distributed architecture is illustrated in Fig. 2, where control sub-systems are positioned at different temperature stages of a cryogen-free dilution refrigerator. Below we describe and provide a basic demonstration of these sub-systems.

III. SWITCHING MATRIX

The key sub-system underpinning the control micro-architecture is a switching matrix, or routing technology that steers the prime waveforms to particular qubits based on a digital address. This technology is ideally located in close proximity to the qubits to avoid latency and synchronization challenges that arise when signals propagate over length-scales comparable to the electromagnetic wavelength (typically centimetres for quantum control waveforms). Physically integrating the switching

matrix and qubit system has the further advantage of significantly reducing the wiring and interconnect density by making use of lithography (or multi-chip module packaging) to provide connection fan-out. In this way we envisage a switching matrix that receives multiplexed data on a small number of transmission lines and decodes this address data to operate large numbers of parallel switches (see Fig. 2). Multiplexing of this kind will likely be essential for operation in cryogenic environments where large numbers of parallel transmission lines add a sizeable heat load when carrying signals between stages that are at different temperatures. The use of superconducting materials is key as these can dramatically reduce the cross-section and thereby thermal load of transmission lines without degrading electrical performance¹⁵.

A switching matrix with elements that act as variable impedances can also be configured to enable the amplitude and phase of the prime waveforms to be individually adjusted before arriving at each qubit. By incorporating a calibration routine or feedback scheme, this approach can be used to account for the variation in physical parameters that will inevitably occur with systems comprising large numbers of qubits.

Various technologies appear suitable for constructing such a switching matrix, including semiconducting devices^{16–18}, mechanical systems^{19,20}, and superconducting logic²¹. For qubit technologies built from semiconductors^{8,22}, field-effect based devices are ideally suited owing to their sub-nanosecond switching-speed, gigahertz transmission bandwidth, low dissipation, small footprint, cryogenic compatibility, and opportunity for integration with qubits. Below we demonstrate the operation of such devices using GaAs high electron mobility transistor (HEMT) circuits, configured as a switching matrix with variable amplitude and phase response.

A. HEMT Switching Elements

A prototype HEMT-style microwave switch based on a GaAs/AlGaAs heterostructure is shown in Fig. 3(a,b). In the on-state, the switch is configured to have a characteristic impedance of $\sim 50 \Omega$, owing to its coplanar waveguide (CPW) geometry. Prime waveforms are fed to and from the HEMT two-dimensional electron gas (2DEG) via eutectic ohmic contacts and TiAu planar transmission lines. In the off-state a negative voltage applied to the TiAu top gate pinches-off the electron gas channel, reflecting the prime waveform signal due to the large impedance of the HEMT relative to the characteristic impedance of the $\sim 50 \Omega$ feedline. The transmission response of the switch is shown in Fig. 3(c), with an on/off ratio (OOR) above 40 dB in the frequency range 0 - 2.5 GHz, suitable for control of spin qubits²³. For these prototype devices a large insertion loss of 10-20 dB is observed, owing mostly to the resistance of the ohmic contacts, which deviates from 50Ω . Precise control of the contact resistance and capacitance using ion-

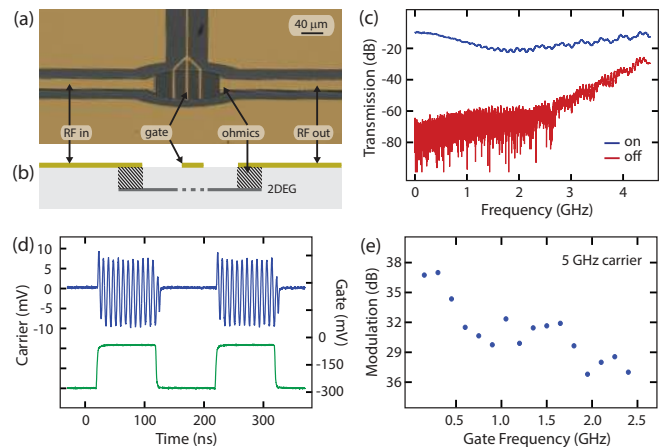


FIG. 3. **Characterisation of a HEMT switch as a building block for the PL/AL architecture.** (a) Microscope photograph of the device fabricated on GaAs/Al_{0.3}Ga_{0.7}As heterostructure. (b) Schematic cross-section showing the coplanar line diverted through the 2DEG. A negative voltage (-300 mV) on the top gate increases the impedance of the switch, reflecting the input signal. (c) Transmission as a function of frequency for the on (blue) and off (red) state. (d) Example of time-domain response. When the gate voltage (green) is zero, the 120 MHz sine wave provided at the switch input is propagated to the output (blue), and not otherwise. (e) Modulating a carrier signal through the 2DEG with a sinusoidal gate voltage creates sidebands. The amplitude of the sidebands as a function of frequency indicates a 1 - 2 ns switching time.

implantation can overcome this limitation and also dramatically shrink the footprint of these devices^{24,25}.

The time-domain response of the switch is demonstrated by amplitude modulating an applied 120 MHz constant wave tone, as shown in Fig. 3(d). To determine the maximum switching time of the HEMT we modulate a 5 GHz carrier tone with a sinusoidal waveform applied to the gate and measure the depth of modulation as a function of gate frequency, as indicated in Fig. 3(e). For these prototype devices the switching time is of order 1 ns.

B. Capacitive Switching Elements

Microwave switching devices based on the depletion of an electron gas also enable a new capacitive mode of operation. In this configuration the CPW feedline transitions to a microstrip geometry by contacting the electron gas to the planar ground planes using ohmic contacts, as illustrated in Fig. 4(a,b). The two conductors in the microstrip transmission line are thus constructed using the top gate and electron gas as ground. This device can act as a reflective switch by depleting the effective ground plane using a negative bias on the gate. Depletion reduces the capacitance between the conductors of the microstrip and modulates the device impedance.

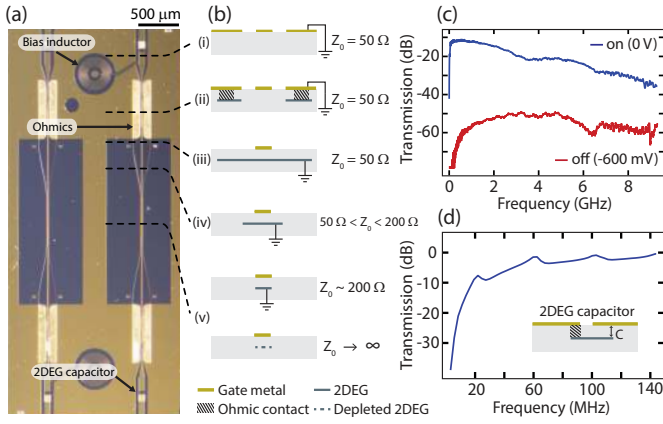


FIG. 4. **A switch design that produces an impedance mismatch by depleting the transmission line ground plane.** Shown is an image (a) and cross-sections (b) of the device. The input is a coplanar line (i) which transitions to a microstrip using the 2DEG as the ground plane (ii,iii). The ground plane is tapered so that it lies beneath the signal track (iv,v). When a negative voltage is applied to the signal track, the ground plane is depleted (v) and the impedance mismatch reflects the input signal. (c) Transmission through the switch in the on (blue) and off (red) states. (d) Frequency response of capacitors formed using surface gates and 2DEG as a parallel plate (inset).

Transmission through the switch is shown in Fig. 4(c) in the on (blue) and off (red) state, with an OOR greater than 25 dB for 0 - 8 GHz. To the best of our knowledge, a switching device based on a depleted ground plane has not been reported previously.

The switch is capacitively coupled to the input and output ports, with a planar spiral inductor at one port forming a bias tee to provide the dc gate voltage needed to deplete the electron gas. In place of a planar interdigitated capacitor, we make use of the GaAs heterostructure to provide a low footprint parallel plate capacitor, formed between the CPW central track and the electron gas, as shown in the inset to Fig. 4(d). The frequency response of this capacitor is shown in Fig. 4(d).

The capacitance-based switch has improved performance at higher frequency than the HEMT-based switch, although it has a larger footprint due to both the length of line needed for adiabatic tapering from 50 to 200 Ω and for the coplanar-to-microstrip transition. This improvement stems from the absence of a gate structure, which in the HEMT switch capacitively couples the source and drain contacts, even in the off state. The required footprint is reduced significantly in an all-microstrip circuit that is designed to operate at a characteristic impedance close to 200 Ω .

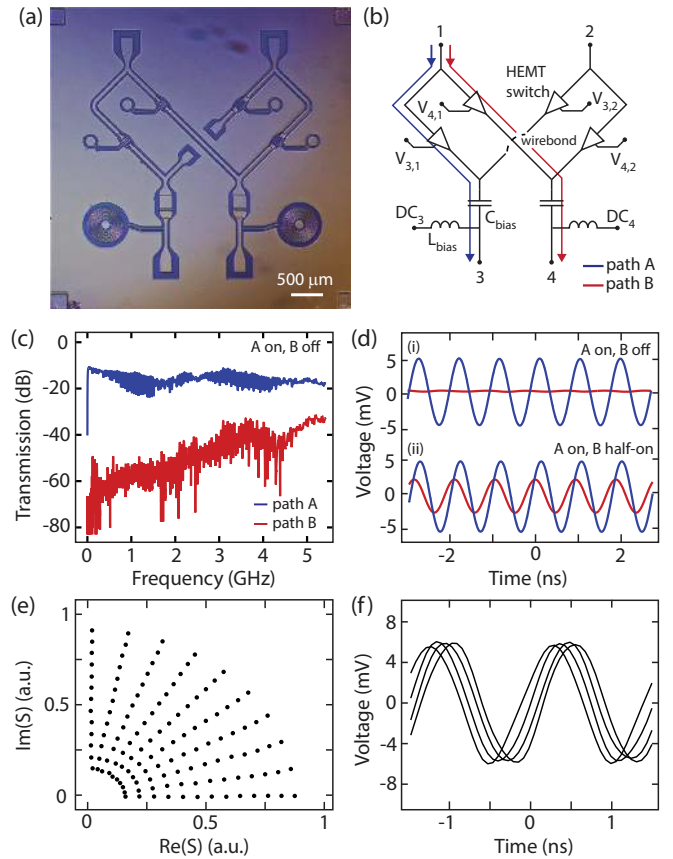


FIG. 5. **Small scale 2-input, 2-output switching matrix based on HEMT switches, with on-chip bias tees for quantum dot operation.** Device image is shown in (a) with associated circuit diagram in (b). (c) Transmission measurement with path A (blue) in the on-state and path B (red) in the off-state. (d) Voltage output with a 1 GHz input tone where path A is in the on-state and path B is (i) off, and (ii) half-on. (e) An example of IQ modulation, implemented by feeding the input ports of the 2:2 matrix with signals that have a 90° phase offset. Arbitrary amplitude and phase is produced at the output (data shown in figure) by selecting the appropriate $V_{i,j}$ (see main text). (f) Example voltage output for one of the constant amplitude quarter circles in (e).

C. 2:2 Switch Matrix

We demonstrate cryogenic operation of a prototype routing matrix based on HEMT switches with two input and two output ports. A magnified image of the device is shown in Fig. 5(a) with associated schematic in (b). Each input port is split and connected to each output port via a switch so that the transmission parameters S_{ij} of the device are controlled by the respective gate voltages $V_{i,j}$. The output ports include bias tees, which are needed for use with qubits based on semiconductor quantum dots. Bias tees are constructed using planar spiral inductors and 2DEG-based capacitors as illustrated in the inset of Fig. 4(d).

Operation of this switching matrix is demonstrated by comparing the transmission of signals as a function of frequency for path A (blue) and path B (red), as indicated in Fig. 5(b). The response through both paths when path A is on ($V_{3,1}=0$) and path B is off ($V_{4,1} = -500$ mV) is shown in Fig. 5(c). The corresponding time-domain response for a 1 GHz tone is shown in Fig. 5(d)(i). We observe a negligible (< 0.05 dB) change in the response of one path when the other is path is switched from the on state to the off state. An advantage of semiconductor-based switching elements is their ability to be configured as variable impedances, producing arbitrary amplitude output, as shown in Fig. 5(d)(ii).

We also demonstrate basic IQ modulation using our switching matrix by applying rf tones at both inputs with a 90° phase offset between them. The 90° shift can be produced by a length of transmission line (with narrowband response) or as a separate quadrature prime waveform. The output waveform at angular frequency ω is $A \sin \omega t + B \cos \omega t = R \sin(\omega t + \phi)$, where the magnitude R and phase ϕ are determined by the amplitudes A and B , controlled by the gate voltages $V_{i,j}$. After the calibration function $R, \phi = \mathcal{F}(V_{i,j})$ is generated once, we can select the appropriate $V_{i,j}$ to produce a tone with arbitrary phase and amplitude in the first quadrant of the complex plane, as shown in Fig. 5(e). The corresponding voltage output along a quarter circle of constant amplitude is shown in Fig. 5(f). By controlling the amplitude and phase shift using the integrated switching matrix, the connection between each qubit and the prime line bus can be specifically adjusted to compensate for the inevitable variation in parameters between physical qubits²⁶.

IV. CRYOGENIC LOGIC

For controlling and programming the switching matrix via the address bus, we envisage a layer of fast, classical logic that serves as an interface between the physical qubits and compiled quantum algorithm (comprising mostly an error correcting code). This layer of classical logic is also needed for executing various automatic sequences associated with fast feedback for qubit stabilisation, readout signal conditioning, or open-loop error suppression^{27,28}. For controlling a large-scale quantum computer there are many advantages to locating this classical logic and associated data converters close to the qubits, inside a dilution refrigerator. In comparison to room temperature based control systems, cryogenic operation results in an enhanced clock speed, improved noise performance, reduced signal latency, and larger bandwidth. Some of these aspects stem from the ability to make use of compact superconducting transmission lines and interconnects at cryogenic temperatures.

The choice of technology for constructing this layer of classical control is largely dictated by the qubit coherence times, control signal bandwidth, and the number of simultaneous qubits under control. With a convergence

of solid-state qubit coherence times now approaching 1 millisecond^{29–31}, present day CMOS-based FPGAs or application specific integrated circuits (ASICs) operating at 4 kelvin are a viable control platform. Higher performance control systems that are likely to be realised in the longer term include technologies based on InP devices³², SiGe BiCMOS^{33,34}, and superconducting flux logic²¹.

For the basic demonstration of the PL/AL scheme considered here the classical logic is implemented using a commercial FPGA (Xilinx Spartan-3A) that we have made operational at the 4 K stage of a dilution refrigerator. To achieve cryogenic operation the FPGA chip was mounted on a custom, cryogenic printed circuit board that includes components which vary little in their parameters at cryogenic temperatures^{35,36}. Power and clock signals to the FPGA are adjusted for cryogenic operation using room temperature sources and a semi-rigid coax line is configured for sending serial commands, with reprogramming of the low temperature array occurring via a dedicated ribbon cable. With the FPGA mounted at the 4 K stage we measure an idle power dissipation of ~ 30 mW, with negligible increase during dynamic logic operations for the simple code executed here. We estimate a dynamic power dissipation of ~ 100 mW for computational operations that use most of the gates in the Spartan-3 array (further details of cryogenic operation of FPGAs are given elsewhere³⁷). The FPGA is programmed to interpret serial communication and output a 3.3 V signal on selected pins to activate prime waveform routing in the switching matrix. These outputs are combined with a negative voltage provided from room temperature via a cold resistive adder so that the switching matrix gates receive -50 mV for the on-state and -380 mV for the off-state voltage.

V. SEMICONDUCTOR QUBIT CONTROL

We combine the building-blocks of our micro-architecture described above, to demonstrate that a semiconductor qubit can feasibly be controlled autonomously without introducing additional noise or heating to the quantum system. The qubit is a GaAs double quantum dot configured as a charge or spin qubit in the few-electron regime. These qubits are commonly controlled using dc-pulse waveforms on the gates to rapidly manipulate the energy levels of the quantum dots³⁸. A typical setup connects a waveform generator to each gate using a separate high bandwidth coaxial cable and bias tee.

For this demonstration we connect a single coaxial cable from a waveform generator at room temperature to the input of the 2:2 switching matrix, with the two matrix output ports connected to the two plunger gates LP and RP of the double dot, as shown schematically in Fig. 6(a). The waveform generator produces a prime waveform consisting of a 100 kHz square wave (shown in Fig. 6(b)) which is then steered by the 4 kelvin FPGA by opening and closing switches in the matrix depending

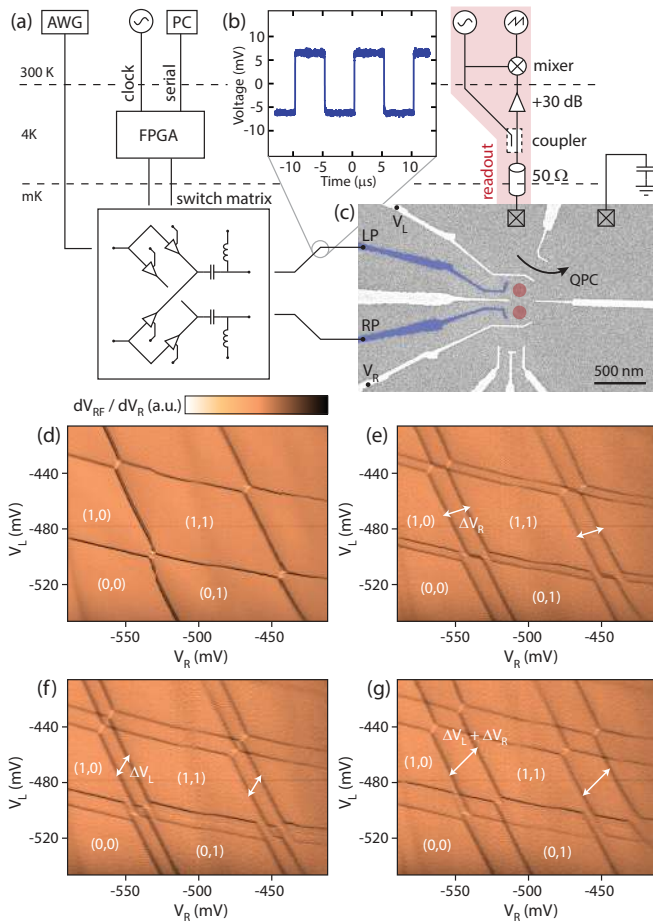


FIG. 6. **Simple implementation of the micro-architecture introduced in Fig. 2.** (a) Experimental setup for measuring a double quantum dot, using a cryogenic FPGA to steer pulses via a millikelvin switching matrix. Charge-state readout is performed using an rf-QPC. (b) Switching matrix output showing a 100 kHz square wave directed to plunger gates of the quantum dot. (c) Micrograph of the quantum dot device. The shaded gates, labelled LP and RP, are connected to the switching matrix output. (d-g) Charge sensing of the double quantum dot in the few-electron regime, with electron occupancy indicated by the labels (m, n). The colour axis is the derivative of the sensing signal V_{rf} with respect to V_R . When the FPGA-controlled switching matrix blocks waveforms (d), a standard double dot stability diagram is detected. When the square wave is directed to either LP (e), RP (f) or both (g), copies of the stability diagram appear (see text). These measurements demonstrate that the double dot potential can be controlled autonomously by the switching matrix and cold FPGA.

on commands sent from room temperature.

The charge state of the double dot is sensed using an rf quantum point contact^{39,40}, which provides a readout signal V_{rf} as a function of the gate voltages V_L and V_R indicated in (c). With both switches of the matrix set to the off state, a standard charge stability diagram is detected indicating that the off state provides sufficiently high isolation between input and output ports, as shown

in Fig. 6(d)⁴¹.

Sending a command to the cold FPGA allows the prime waveform to be directed to the left, right, or both plunger gates, producing two copies of the charge stability diagram. These copies appear because, on the timescale of the readout, a square wave with 50% duty-cycle configures the double dot in two distinct charge states that are offset from one another by the voltage ΔV_R or ΔV_L , as shown in Fig. 6(e-g)⁴². In comparison to data taken on the bare quantum dot, we are unable to detect any additional noise or an increase in the electron temperature (which is of order 100 mK) when configuring the charge-state using the cryogenic FPGA and switching matrix.

VI. DISCUSSION

Our simple demonstration of a multi-component control architecture provides a path for scaling up the classical support system needed for operating a large-scale quantum computer. Aspects of this demonstration will also likely find immediate use in improving the performance of few-qubit experiments using electron spins in quantum dots. For example, in using the switching matrix to produce multiple out-of-phase copies of control waveforms, crosstalk can be suppressed by cancelling the voltage that is capacitively coupled to neighbouring surface gates⁴³. Using the switching matrix as a high frequency cryogenic multiplexer will also enable the automated testing and characterisation of many devices in a given cool-down experiment. In the longer term, our micro-architecture can be extending to allow additional functionality of the switching matrix, providing qubit control frequency correction by using the HEMTs as mixers, or as cryogenic adder circuits that reduce the complexity or resolution needed for biasing surface gates that define quantum dots.

At the layer of classical logic, our demonstration shows that commercial FPGA devices can be configured to work at cryogenic temperatures and are compatible with controlling qubits in close proximity. Beyond the control architecture presented here, the use of cold, low-latency classical logic will likely improve the performance of feedback systems generally needed for adaptive measurement, quantum state distillation, and error correction protocols. Given the power dissipation inherent to such control systems however, improvements in cryogenic refrigeration technology, similar to what has been achieved in rare-event physics⁴⁴, will likely be needed to enable large-scale quantum information processing.

VII. CONCLUSION

We have proposed a micro-architecture for the control of a large-scale quantum processor at cryogenic temperatures. The separation of analog control prime waveforms

from the digital addressing needed to select qubits offers a means of scaling this approach to the numbers of qubits needed for a computation. To demonstrate the feasibility of our scheme we have shown that a semiconductor qubit can be controlled using a cryogenic FPGA system and custom switching matrix for steering analog waveforms at low temperature. We anticipate that integrated, autonomous control systems of this kind will be increasingly important in the development and demonstration of fault tolerant quantum machines.

VIII. METHODS AND MATERIALS

The fabrication of GaAs switching elements follows similar procedure to quantum dot devices (allowing easy integration). The mesa is wet etched using sulphuric acid, before Au/Ge/Ni ohmic contacts are thermally evaporated and annealed at 470 degrees for 100 seconds. The final metal layer is thermally evaporated TiAu (10 nm / 100 nm). The device (Fig. 6(c)) is an electrostatically defined double quantum dot on GaAs/Al_{0.3}Ga_{0.7}As heterostructure (carrier density $2.4 \times 10^{-15} \text{ m}^{-2}$, mobility $44 \text{ m}^2 / \text{Vs}$ at 20 K).

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X. AUTHOR CONTRIBUTIONS

D.J.R. devised the micro-architecture, J.M.H. fabricated the switches and switching matrix, M.J.M., J.D.W., G.G., and S.F. grew the heterostructure for the switches. J.M.H. and S.J.P. performed the experiment on the switches, J.M.H., J.I.C., I.D.CL., and S.J.P. performed the experiment on the quantum dot with FPGA control. H.L. and A.C.G. grew the heterostructure for the quantum dot. J.M.H. and D.J.R. wrote the manuscript.

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