Crystalline silicon solar cells with thin poly-SiO x carrier-selective passivating contacts for perovskite/c-Si tandem applications

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Abstract

Single junction crystalline silicon (c-Si) solar cells are reaching their practical efficiency limit while perovskite/c-Si tandem solar cells have achieved efficiencies above the theoretical limit of single junction c-Si solar cells. Next to low-thermal budget silicon heterojunction architecture, high-thermal budget carrier-selective passivating contacts (CSPCs) based on polycrystalline-SiO $_x$ (poly-SiO $_x$) also constitute a promising architecture for high efficiency perovskite/c-Si tandem solar cells. In this work, we present the development of c-Si bottom cells based on high-temperature poly-SiO $_x$ CSPCs and demonstrate novel high-efficiency four-terminal (4T) and two-terminal (2T) perovskite/c-Si tandem solar cells. First, we tuned the ultra-thin, thermally grown SiO $_x$. Then we optimized the passivation properties of p-type and n-type doped poly-SiO $_x$ CSPCs. Here, we have optimized the p-type doped poly-SiO $_x$ CSPC on textured interfaces via a two-step annealing process. Finally, we integrated such bottom solar cells in both 4T and 2T tandems, achieving 28.1% and 23.2% conversion efficiency, respectively.

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Abstract

Single junction crystalline silicon (c-Si) solar cells are reaching their practical efficiency limit while perovskite/c-Si tandem solar cells have achieved efficiencies above the theoretical limit of single junction c-Si solar cells. Next to low-thermal budget silicon heterojunction architecture, high-thermal budget carrier-selective passivating contacts (CSPCs) based on polycrystalline-SiO_x (poly-SiO_x) also constitute a promising architecture for high efficiency perovskite/c-Si tandem solar cells. In this work, we present the development of c-Si bottom cells based on high-temperature poly-SiO_x CSPCs and demonstrate novel high-efficiency four-terminal (4T) and two-terminal (2T) perovskite/c-Si tandem solar cells. First, we tuned the ultra-thin, thermally grown SiO_x. Then we optimized the passivation properties of p-type and n-type doped poly-SiO_x CSPCs. Here, we have optimized the p-type doped poly-SiO_x CSPC on textured interfaces via a two-step annealing process. Finally, we integrated such bottom solar cells in both 4T and 2T tandems, achieving 28.1% and 23.2% conversion efficiency, respectively.

Introduction

Single junction c-Si solar cells are reaching their practical efficiency limit [1],[2]. One way to further increase the efficiency of solar cells based on c-Si is to deploy them as bottom device in tandem structures with a wide bandgap top device. Perovskite/c-Si tandem solar cells attract considerable attention in this regard [3]-[31] with certified conversion efficiencies so far up to 32.5% [32]. The two common tandem architectures are a monolithically integrated two-terminal (2T) tandem configuration, where the two devices are electrically connected via a tunnel recombination junction (TRJ), and a mechanically stacked four-terminal (4T) tandem configuration where the two devices are optically connected but electrically decoupled. The 2T tandem solar cell design has simple electrical connections but requires current matching between the two devices to reach optimal efficiency. It is thus sensitive to the daily variations of solar spectrum. The 4T tandem configuration does not require current matching between its component devices and so has fewer restrictions on the device optimizations. However, due to the devices being electrically decoupled, each of them has its own transport layers and additional encapsulation layers for optical coupling, which increases the overall parasitic absorption. The advantages and disadvantages of 2T and 4T tandem configurations have been explored before [33]-[36]. As bottom device, besides silicon heterojunction (SHJ) cells [3]-[7],[24]-[27], silicon solar cells based on high-thermal budget carrier-selective passivating contacts (CSPCs) have rarely been reported [8], [28]-[30]. Such CSPCs are so-called since they require high temperature fabrication steps, which can be up to 1100 °C. Poly-crystalline silicon (poly-Si) is an example of these high-thermal budget CSPCs and has enabled high efficiency single junction c-Si solar cells [37]-[41], concurrently yielding high quality surface passivation and charges transport. However, doped poly-Si exhibits a high free carrier absorption, which has turned the attention of researchers towards wide bandgap materials, such as polycrystalline-SiC_x [42],[43] and polycrystalline-SiO_x (poly-SiO_x), which can be more transparent while ensuring similar conductivity with respect to poly-Si [44],[45]. Such CSPCs consist of doped poly-Si, alloyed with carbon or oxygen, which are deposited on an ultra-thin SiO_x layer, prepared by a wet-chemical process (nitric acid oxidation of silicon, NAOS) [45], thermal oxidation [46], UV/O_3 process [47], or low-temperature plasma oxidation [48]. The opto-electronic properties of poly-SiO_x depend on the oxygen content [45],[49]. Poly-SiO_x is a novel material which has been successfully employed in c-Si single junction solar cells [45],[49],[50] and, to the best of our knowledge, its long-wavelength optical potential in tandems has not been explored so far. As these CSPCs are compatible with high temperature production processes, they are appealing to the mainstream c-Si PV industry. In view of potential tandem efficiencies well above 30%, perovskite/c-Si tandem solar cells with bottom cells fabricated with high-thermal budget CSPCs can significantly reduce the levelized cost of electricity compared to single junction silicon photovoltaics [51].

Solar cells fabricated with poly-SiO_x CSPCs on an ultra-thin tunnelling SiO_x layer grown via NAOS process have exhibited active area efficiency of around 21% in a front/back contacted (FBC) architecture [50]. However, these cells were 2-cm^2 wide and deployed thermally evaporated metal contacts. In this work, next to adopting screen printing for metallization and developing larger area devices (from 2 cm^2 to 4 cm^2), an ultra-thin SiO_x layer prepared by thermal oxidation of the c-Si surface is used as tunnelling SiO_x. As compared to tunnelling oxide grown via NAOS, thermal oxides are denser and less prone to blistering, have lesser bulk defects, provide better wafer chemical passivation [52] and is more stoichiometric resulting in higher thermal stability [53]. Other advantages of using a thermal oxide are (i) the controllability over the oxide thickness and its microstructures by changing the oxygen flow rate, temperature, and time, and (ii) the industrial applicability in state-of-the-art furnaces.

We optimized the passivation of both n-type and p-type doped poly-SiO_x on the ultra-thin thermally grown SiO_x especially because p-type poly-SiO_xon textured surfaces has been a limiting factor in terms of passivation [43],[52],[54]. To this end, a two-step annealing process was used to improve the passivation quality of p-type poly-SiO_x CSPCs on textured interfaces. Finally, we studied the integration of c-Si solar cells endowed with these optimized high-thermal budget CSPCs in perovskite/c-Si 4T and 2T tandem devices, achieving conversion efficiency of 28.07% and 23.18%, respectively.

Experimental details

Crystalline silicon (c-Si) solar cells

We used 4-inch n-type float zone (FZ) double-side polished (DSP) Topsil wafers (orientation: <100>, resistivity: 1 ~ 5 cm, thickness: 280 +- 20 μm). For double-side textured (DST) solar cells, both sides of the wafers were textured in a tetramethylammonium hydroxide (TMAH) solution containing ALKA-TEX (GP-Solar-GmbH) as additive. For single-side textured (SST) solar cells, the front side was protected by a thick silicon dioxide (SiO_2) layer deposited using plasma-enhanced chemical vapour deposition (PECVD). After partially texturing the wafer, the SiO_2 layer was etched using a Buffered Hydrogen Fluoride (BHF (1:7)) solution. Subsequently, the samples were cleaned by dipping them in HNO_3 (99%), to remove eventual organic contaminations, and then in HNO_3 (69.5%, at 110 °C) to remove inorganic contaminations. The samples are then dipped in 0.55% HF solution to remove any native oxide layer before thermal oxidation to grow a thin tunnelling oxide layer. Here, after preliminarily investigating an optimal growth temperature (ultimately fixed at 675 °C), the time of the thermal oxidation process is optimized. Then, both the n-type and the p-type poly-SiO_x passivating contacts are deposited on the thermal oxide with a dual-stack layer of 10-nm thick intrinsic a-Si layer using low-pressure chemical vapour deposition (LPCVD) process and 20-nm thick doped a-SiO_x:H layer from PECVD process. Thus, the total thickness of the passivating contact hereby described will not overcome 30 nm. Because of that thickness, an additional TCO layer is needed for lateral transport of carriers. Also here, after an initial study on the optimal annealing temperature seeking for an eventual co-annealing temperature between the n-type and p-type doped layers, these samples were annealed at 950 °C between 5 and 15 minutes to crystallize the abovementioned films into poly-SiO_x layers and drive in the dopants for both DST and SST cells. In this high temperature process, hydrogen effuses from the whole layer stack. Therefore, these cell precursors were hydrogenated by forming gas annealing (FGA) at 400 °C for 1 hour after being preliminarily capped with a 100-nm thick PECVD SiN_x layer [55]. Upon the removal of the SiN_x capping layer, indium tin oxide (ITO) layers were sputtered to ensure efficient (i) lateral carrier transport of charge carriers and (ii) optical performance at the front side as an anti-reflective coating (75 nm) and at the rear side as an optical buffer for the rear reflector (150 nm) [56]. As this step deteriorates the passivation quality [50],[57],[58], an additional annealing was executed in hydrogen for one hour at 400 °C. Finally, screen printing and curing for 30 minutes at 170 °C was used to realize low-temperature front and rear Ag-based metallic contacts. We have also fabricated a front side flat (rear side textured) c-Si solar cell that is deployed in 2T tandem devices (see Figure 1). The fabrication of such an architecture is described in more detail in Section 2.2. The current-voltage measurements of c-Si solar cells were performed using an AAA class Wacom WXS-90S-L2 solar simulator. The best SST and DST devices were certified at the CalTeC of the Institute for Solar Energy Research Hamelin (ISFH), Germany, which provided also

the related external quantum efficiency (EQE) spectra (illumination in-between the front metal fingers). For passivation tests, symmetrical samples were fabricated with n-type or p-type doped poly-SiO_x CSPCs on flat and textured c-Si wafers. A lifetime tester (Sinton WCT-120) was used to perform passivation measurements, such as implied open-circuit voltage (iV_{oc}), on precursors in quasi-steady-state photoconductance (QSSPC) or transient photoconductance decay (transient PCD) mode [59],[60].

Perovskite/c-Si tandem solar cells

For 2T perovskite/ c-Si tandem solar cells, SST solar cells were fabricated with front side flat n-type poly-SiO_x and rear side textured p-type poly-SiO_x. This configuration of the bottom sub- cell is chosen to meet the requirements for depositing the perovskite top device in a p-i-n configuration. After high temperature annealing (900 °C for 15 minutes) and the abovementioned hydrogenation step, the SiN_x capping layer was removed. This was followed by sputtering 30-nm (150-nm) thick ITO layer on the front (rear) side of the cell. Finally, a 500-nm thick Ag layer was deposited on the rear side of the cell using thermal evaporation. Atomic layer deposition (ALD), in combination with solution-processing, thermal evaporation, and sputtering were used to fabricate the perovskite top device. On the front, flat ITO layer of the bottom device, the perovskite top device comprised in a bottom-up sequence NiO_x / 2-(9*H* -carbazol-9-yl)ethyl]phosphonic acid (2PACz) / perovskite (1.67 eV) / C_{60} / SnO_x / ITO / MgF_2. The front electrical contact was made of evaporated silver. The 8-nm thick NiO_x layer was deposited on the ITO layer using thermal ALD [61],[62]. The deposition was done at a base pressure of 5×10^{-6}mbar in a home-built reactor using nickel bis(*N* ,*N* '-di-tert-butylacetamidinate) (Ni(^{t}Bu-MeAMD)$_2$) as nickel precursor and water as the co-reactant. The precursor bubbler was maintained at 90 degC and an Ar flow was used for bubbling. The substrate temperature approached 150 degC during the deposition. Subsequent solution-processed and evaporated layers were processed in an inert atmosphere. 2PACz (TCI, 98%, dissolved 0.3 mg/ml in ethanol) was deposited by spin-coating at 3000 rpm for 30 s followed by annealing the substrate at 100 degC for 10 minutes [63]. The perovskite precursor solution was prepared by mixing 936 µl PbI_2 (TCI, >99.99%, 691.5 mg/ml in DMF:DMSO 4:1) with formamidinium iodide (FAI, Greatcell Solar Materials) (199.9 mg)and 936 µl $PbBr_2$ (TCI, > 99%, 550.5 mg/ml in DMF:DMSO 4:1) with methylammonium bromide (MABr, Greatcell Solar Materials) (133.1 mg), followed by mixing the $FAPbI_3$ and $MAPbBr_3$ solutions in a 79:21 (v/v) ratio and adding 5 vol.% CsI (Sigma Aldrich, 99.999%, dissolved 389.7 mg/ml in DMSO) and 5 vol.% KI (Alfa Aesar, 99.998%, dissolved 249.0 mg/ml in DMF:DMSO 4:1). The precursor was spin-coated at 4000 rpm (5 s to reach 4000 rpm) for 35 s; at 25 s from the start of spin-coating, 300 µl anisole was cast onto the substrate leading to perovskite crystallization. The substrate was then placed on a hot-plate and the film was annealed at 100 °C for 30 minutes. Following the substrate cooling down, choline chloride (Sigma Aldrich, >99%, 1 mg/mL in 2-propanol) was dynamically spin-coated at 4000 rpm for 35 s followed by thermal annealing at 100 °C for 30 minutes. Then, C_{60} (10 nm) was deposited by thermal evaporation at a rate of 0.5 /s. Following that, spatial atomic layer deposition (s-ALD) was used to deposit a SnO_2 (20 nm) buffer layer [64]. Tetrakis(dimethylamino)tin(IV) was used as tin precursor and water as the co-reactant. A nitrogen curtain was used to isolate the two half-reaction steps. A 180-nm thick ITO layer was deposited using RF sputtering process at a rate of 0.3 /s. Finally, a 100-nm thick Ag perimeter contact, and a 120-nm thick MgF_2 anti-reflective coating were thermally evaporated to complete the tandem device. More information about this solar cell stack can be found in [65]. Schematic sketches of single junction solar cells combined with perovskite solar cells in 4T and 2T tandem devices are reported in Figure 1.

Current density – voltage (J–V) scans of the 2T perovskite/c-Si tandem solar cells were done using a tungsten-halogen illumination source filtered by a UV filter (Schott GG385) and a daylight filter (Hoya LB120) with intensity adjusted to 100 mW/cm^2. A 1 cm^2 shadow mask was used. The solar cells were operated under reverse or forward sweeps (between + 2.0 V and – 0.5 V for tandem solar cells) at a rate of 0.25 V/s using a Keithley 2400 source meter. The EQE measurements of the 2T perovskite/c-Si tandem solar cells were performed using a modulated monochromatic probe light (Philips focusline, 50 W) through a 1 mm radius aperture. The response was recorded and converted to the EQE using a calibrated silicon reference cell. Light- and voltage-biasing was used to isolate the EQE of the individual devices; 530 nm (perovskite) or 940 nm (silicon) bias light and a forward bias close to the open-circuit voltage of the single-junction solar cell

was used.

The single junction c-Si solar cells, described in Section 2.1, were combined with earlier processed and certified semi-transparent perovskite solar cells [66]-[69] to fabricate the 4T tandem devices. The efficiency of 4T tandem cells was determined by following the procedure described by Werner et al. [70]. Next to the conversion efficiency of our 4T tandem devices, another outcome of this procedure was the filtered EQE of the deployed bottom devices.

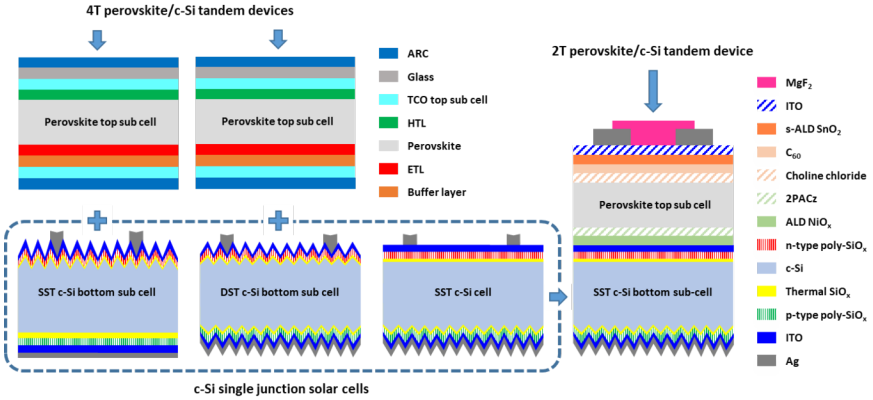

Figure 1 : Sketches of the various solar cells reported in this work. The c-Si single junction solar cells endowed with p-type and n-type poly-SiO_x CSPCs are shown in the dashed box at the bottom left. The single-side textured (SST) with front textured and the double-side textured (DST) solar cells are then combined with 4T perovskite/c-Si tandem devices. The SST with rear textured solar cell is used for the 2T perovskite/c-Si tandem device.

Results and discussion

3.1. Passivation properties of poly-SiO_x CSPCs

Here, we optimized the passivation quality of n-type and p-type doped poly-SiO_x CSPCs. Since, SST poly-SiO_xpassivated c-Si solar cell has n-type doped poly-SiO_xCSPC applied on front textured interface and p-type doped poly-SiO_x applied on rear side flat interface, we optimized n-type doped poly-SiO_x CSPC on DST symmetric samples and p-type doped poly-SiO_x on DSP symmetric samples (see Figure 2(a)). On the other hand, for DST poly-SiO_x passivated c-Si solar cell, we optimize both n-type and p-type doped poly-SiO_x CSPC applied on DST symmetric samples (see Figure 2(b)). As mentioned earlier in Section 2.1, these CSPCs are prepared stacking doped poly-SiO_xlayers on a tunnelling oxide grown by thermal oxidation on a c-Si FZ wafer, followed by a high temperature annealing step. The passivation results in Figure 3 were obtained after the high temperature annealing step. We use two parameters to optimize the passivation of these CSPCs: (1) the thermal oxidation time for the growth of tunnelling oxide and (2) the annealing time. Figure 3(a) and (b) show the passivation (in terms of iV_{oc}) of p-type doped poly-SiO_xCSPC applied on DSP symmetrical sample and n-type doped poly-SiO_x applied on DST symmetrical sample, respectively, for different thermal oxidation time at 675 °C (shown with different colours). Three annealing times (5, 10 and 15 minutes at 950 °C) were considered for each thermal oxidation time. For both p-type doped CSPC on DSP wafers and n-type doped poly-SiO_x CSPC on DST wafers, we found the same optimal thermal conditions for the tunnelling SiO_x and the high temperature annealing: 6 minutes at 675 °C and 10 minutes at 950 °C, respectively (see Figure 3(a) for p-type case and Figure 3(b) for n-type case).

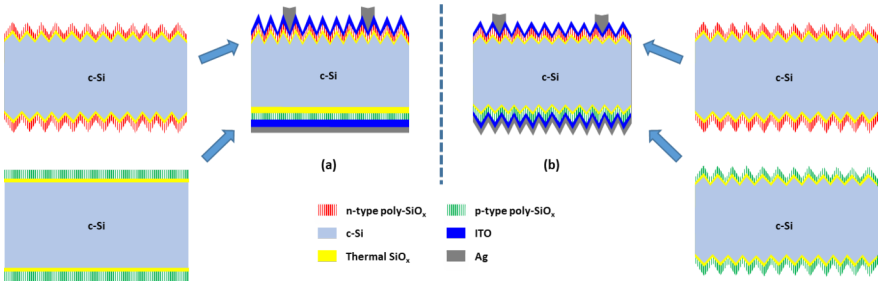

Figure 2 : (a) SST poly-SiO_x passivated c-Si solar cell with (top) symmetric n-type doped poly-SiO_xon DST substrate and (bottom) symmetric p-type doped poly-SiO_x DSP substrate; (b) DST poly-SiO_x passivated c-Si solar cell with symmetric (top) n-type doped poly-SiO_x and (bottom) p-type doped poly-SiO_x on DST substrates.

On the other hand, for the symmetric p-type doped poly-SiO_x on DST wafer, notwithstanding the optimum found again at 10 minutes of thermal annealing in Figure 3(c), thermally grown tunnelling SiO_x prepared at 675 °C for 3 minutes was found to yield better results (iV_{oc}˜ 640 mV) than the rest of the samples. The underwhelming passivation performance of these DST samples can be ascribed to a strong Auger recombination due to the excessive diffusion of dopants in the c-Si bulk. To quench such a diffusion, a 2-step annealing was used [71],[72]. The first annealing step, done after the intrinsic a-Si layer deposition, was performed at 950 °C for 1 minute. This was meant to render this intrinsic silicon denser [73] and therefore harder for dopants to be crossed. The second annealing step, done after the deposition of the doped a-SiO_x:H layer, was performed at 950 °C between 5 and 15 minutes like in previous cases so far discussed. For this new series of samples, thermally grown tunnelling SiO_x was prepared at

675 °C for 3 minutes. The passivation results for the symmetric p-type doped poly-SiO_x on DST wafers are reported in Figure 3(d), showing more than 20 mV improvement with respect to the best passivation achieved with the single-step annealing.

Figure 3: Implied V_{oc} of symmetric (a) p-type doped poly-SiO_x on DSP wafer, (b) n-type doped poly-SiO_x on DST wafer,

As described in Section 2.1, hydrogenation by FGA after SiN_x layer capping is performed on p-type and n-type doped CSPCs to reintroduce the hydrogen that effused after high temperature annealing. Figure 4 shows the comparison in passivation of p-type and n-type doped poly-SiO_x symmetric samples after thermal annealing and after hydrogenation. The optimum thermal oxidation and annealing conditions, as described in Figure 3, have been chosen for each type of CSPC. We observe that p-type and n-type doped poly-SiO_x CSPCs applied on DSP and DST symmetric samples, respectively, gave the same iV_{oc} of 690 mV after high-temperature annealing which improved to 710 mV after hydrogenation. Using the 2-step annealing technique, the symmetric p-type doped poly-SiO_x applied on DST wafer exhibited an iV_{oc} of 687 mV after hydrogenation. Applying the same 2-step annealing technique to symmetric n-type doped poly-SiO_x on DST wafer (including the thermally grown tunnelling SiO_x prepared at 675 °C for 3 minutes as in the p-type case), an iV_{oc} of 690 mV was found after hydrogenation, resulting in lower passivation quality than the single step annealing case. Here, as the intrinsic poly-Si layer resulting from the first annealing got denser [73], we speculate that the phosphorus doping atoms do not easily reach the tunnelling SiO_x/c-Si bulk interface to establish an effective electric field. In addition, as shown in Figure 3(b), the tunnelling SiO_x prepared at 675 °C for 3 minutes is not the best condition for the n-type doped poly-SiO_x on a textured surface. Still, this case is investigated (and later put forward in solar cell fabrication) to realize a neat flow chart in which both n-type and p-type doped poly-SiO_x layers essentially undergo the same thermal processes at the same time.

Figure 4: Implied V_{oc} for different types of CSPCs after high temperature annealing and after hydrogenation processes.

3.2. Solar cell results

In this Section, we report on the performance of single junction c-Si solar cells with based on n-type and p-type poly-SiO_x as CSPCs. The sketches of SST and DST poly-SiO_x passivated c-Si solar cell were shown in Figure 2. The evolution of surface passivation quality after annealing, hydrogenation, TCO deposition and hydrogen annealing for SST solar cell precursors is shown in Figure 5(a). As expected, the iV_{oc} increases by 20 mV after hydrogenation. Then, the TCO deposition results in a considerable loss in iV_{OC} from 714 mV to 690 mV due to sputtering-related damages [50],[58]. This loss in passivation is recovered by annealing the cell precursor at 400 °C in hydrogen environment for 1 hour [57]. The best SST solar cell exhibited a certified designated area power conversion efficiency (PCE) of 20.47% (V_{oc} = 695 mV, J_{sc} = 36.68 mA/cm^2, FF = 80.33%, metallization faction ˜3%, designated area = 3.915 cm^2, see Figure 5(c)). Moving from the previous 2-cm^2 wide area device, SiO_x layer grown via wet-chemical NAOS and evaporated metallic contacts [50], as well as applying the further optimized doped poly-SiO_x layers, we could keep the V_{oc}relatively high (from 691 mV to 695 mV) and sensibly improve the FF (from 76.4% to 80.3%) of the solar cells based on poly-SiO_x CSPCs.

Figure 5: (a-b) The evolution in passivation quality (iV_{oc}) after specific steps of single side textured (SST) and double sid

As mentioned in Section 3.1, the p-type and n-type doped poly-SiO_x CSPCs with 2-step annealing technique are used as the hole and electron contacts in DST solar cells, respectively. The change in passivation after different fabrication steps for the DST solar cell precursor is shown in Figure 5(b). The increase in passivation after hydrogenation and its decrease after ITO deposition are as expected. However, unlike the SST case, the loss in passivation after TCO deposition is not fully recovered after hydrogen annealing at 400 °C for 1 hour. This is because the DST solar cell precursor has p-type doped CSPC applied to the textured side, which is the limiting factor in terms of passivation and does not recover its passivation even after such a hydrogen annealing. The best DST solar cell gave a certified designated area PCE of 19.44% (V_{oc} = 655 mV, J_{sc} = 37.85 mA/cm^2, FF = 78.42%, metallization faction ˜3%, designated area = 3.903 cm^2, see Figure 5(d)). Compared to the SST solar cell, despite suffering from poorer surface passivation as witnessed by the lower V_{oc} and FF, the DST cell exhibits higher J_{sc}. This gain can be ascribed to the textured rear side of the DST solar cell which promotes a more efficient light scattering at the rear side and thus higher absorption in the c-Si bulk. Figure 6(a) shows the EQE of the SST and DST devices. As expected, the EQE of the DST cell outperforms that of the SST cell at wavelengths above 800 nm.

Figure 6: (a) EQE spectra of the SST and DST single junction c-Si solar cells endowed with n-type and p-type poly-SiO_x

3.3. Application in four terminal (4T) perovskite/c-Si tandem solar cells

The SST and DST poly-SiO_x solar cells were deployed as bottom devices in high efficiency 4T tandem devices together with a previously processed and certified perovskite top device (bandgap 1.60 eV) [66]-[69]. The schematic sketches of the two 4T tandem devices alongside their constituting layers are presented in Figure 1. Following the method of measurement reported in [70] and with the certified measurements of both semi-transparent perovskite top and c-Si bottom devices, the combined results are summarized in Table 1.

The 4T tandem devices based on SST and DST poly-SiO_x bottom devices provide a PCE of 27.97% and 28.07%, respectively. Both SST and DST cells, after being illuminated with the transmitted light through the perovskite top device, experienced similar J_{sc}losses. Looking at the filtered EQE (see Figure 6(b)), the DST cell keeps the optical edge over the SST cell for every wavelength above 800 nm. The SST cell loses however more in V_{oc} and FF than the DST cell. In fact, due to stronger Auger recombination at the p-type poly-SiO_x / tunnelling SiO_x / c-Si wafer side, the DST cell had poorer V_{oc}, which is less sensitive to light-induced carriers' injection, and FF more dominated by the low contact resistivity of the doped stack rather than an efficient extraction of light-induced majority carriers.

Table 1: External parameters of the semi-transparent perovskite top device (certified at ESTI, code XF812), the SST poly-SiO_x bottom cell (certified at ISFH CalTeC, code 0019018) and DST poly-SiO_x bottom cell (certified at ISFH CalTeC, code 002603), and their 4T perovskite/c-Si tandem device combinations.

Solar cell	**Description**	**V_{oc} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**PCE (%)**
Perovskite top device	Single junction	1139	22.00	78.60	19.70
SST poly-SiO_x based bottom device	Single junction	695	36.68	80.33	20.47
	Filtered	666	16.00	77.60	8.27
	4T Tandem				**27.97**
DST poly-SiO_x based bottom device	Single junction	655	37.85	78.42	19.44
	Filtered	637	16.80	78.20	8.37
	4T Tandem				**28.07**

3.4. Application in two terminal (2T) perovskite/c-Si tandem solar cells

As sketched in Figure 1, we also fabricated SST solar cells with flat front side coated with n-type poly-SiO_x and textured rear side coated with p-type poly-SiO_x. This solar cell architecture was deployed to form a 2T perovskite/c-Si tandem device with a p-i-n perovskite top device. Due to the textured p-type poly-SiO_x CSPC limiting the passivation quality, these solar cells suffered large passivation loss after the ITO deposition. Again, some of the passivation loss was recovered after annealing in hydrogen at 400 °C for 1 hour. The best single junction solar cell achieved a designated area PCE of 16.67% (V_{oc} = 649 mV, J_{sc} = 34.28 mA/cm^2, FF = 74.93%, metallization faction 3.15%, designated area = 3.92 cm^2). The current density-voltage characteristic and the EQE spectrum of the single junction solar cell are reported in Figure 7(a) and (b), respectively. From the EQE and reflectance spectra in Figure 7(b), we note large parasitic absorption at short wavelengths (300 - 400 nm) and at very long wavelengths (1000 - 1200 nm). This light is absorbed in the front/rear ITO and in the front/rear poly-SiO_x CSPCs. Between 600 and 1000 nm, other than the reflection losses, most of the light is absorbed in c-Si solar cell.

Figure 7: (a) Current density-voltage characteristic and (b) EQE and 1-Reflectance (1-R) spectra of the single junction c-S

The abovementioned poly-SiO_x passivated c-Si solar cell was integrated with the perovskite top device into a 2T perovskite/c-Si tandem device yielding an active area PCE of 23.18% (V_{oc} = 1.76 V J_{sc} = 17.8 mA/cm^2, FF = 74%, active area: 1 cm^2, see Figure 8(a)). The 2T tandem efficiency is higher than the efficiency of its top device by $5\%_{abs}$(with respect to an opaque analogous single junction perovskite solar cell efficiency

[65],[74]) and the efficiency of its bottom device by 6.5%$_{abs}$. This efficiency is higher than that of the earlier reported value of 21.3% for a monolithic 2T perovskite/PERC-POLO tandem device [29]. On the other hand, it is lower than that of the earlier reported value of 25.1% for monolithic 2T perovskite/c-Si tandem device where the bottom device is endowed with poly-SiC_x CSPCs [43]. These three types of high-thermal budget devices exhibit similar V_{oc}s (1.74 to 1.8 V) and FFs (74%) in 2T tandem devices while only the one with poly-SiC_x CSPCs could achieve better current matching between the devices (19.5 mA/cm^2). The EQE of the 2T tandem device (Figure 8(b)) shows that our bottom device can deliver 19.2 mA/cm^2, but that the top device limits the short-circuit current density of the stack to 17.8 mA/cm^2. By further optimizing the layer thickness and perovskite bandgap, the current generation of the two devices can be better matched and consequently the efficiency of the 2T tandem devices can be further increased.

Figure 8: (a) JV curve and (b) EQE curve of 2T perovskite/c-Si tandem solar cell with poly-SiO_x passivated c-Si bottom

Conclusions

In this study, we optimized n-type and p-type poly-SiO_xCSPCs on an ultra-thin thermally grown tunnelling SiO_xlayer. We incorporated these into single junction c-Si solar cells which were eventually used as bottom devices in 4T and 2T tandem devices. Good passivation quality was achieved for textured n-type poly-SiO_x (iV_{oc} = 710 mV). Using a two-step annealing process, the passivation quality of the textured p-type doped poly-SiO_x could be improved too (iV_{oc} = 687 mV). With the developed n-type and p-type poly-SiO_x CSPCs, we fabricated ˜4-cm^2 wide, screen-printed, a SST single junction c-Si solar cell with certified efficiency of 20.47% and FF > 80%. Likewise, a certified efficiency of 19.44% was obtained for a DST cell endowed poly-SiO_x CSPCs. This DST solar cell architecture is presented here for the first time and exhibits, without any dual anti-reflective coating, an active area J_{sc} = 37.85 mA/cm^2. This is in line with state-of-the-art FBC silicon heterojunction solar cells and other architectures based on high-thermal budget CSPCs.

We tested our c-Si solar cells in combination with a previously processed and certified semi-transparent 19.70% perovskite solar cell. The internally measured efficiencies of the 4T perovskite/c-Si tandem devices featuring SST and DST poly-SiO_x passivated c-Si bottom devices are 27.97% and 28.07%, respectively.

Based on the improved passivation quality of the textured p-type poly-SiO_x, we fabricated SST solar cell with flat n-type poly-SiO_x at the front side and textured p-type poly-SiO_x at the rear side with an efficiency of 16.79%. Integrating such a poly-SiO_x solar cell as bottom device with a p-i-n perovskite solar cell on top, resulted in a 2T tandem device with an efficiency of 23.18%.

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