Hindawi Publishing Corporation
ISRN Electronics
Volume 2013, Article ID 968749, 11 pages
http://dx.doi.org/10.1155/2013/968749

Research Article

Current Controlled Differential Difference Current Conveyor Transconductance Amplifier and Its Application as Wave Active Filter

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Received 17 November 2012; Accepted 10 December 2012

Academic Editors: H. A. Alzaher and H.-C. Chien

This paper proposes current controlled differential difference current conveyor transconductance amplifier (CCDDCCTA), a new active building block for analog signal processing. The functionality of the proposed block is verified via SPICE simulations using 0.25 μm TSMC CMOS technology parameters. The usefulness of the proposed element is demonstrated through an application, namely, wave filter. The CCDDCCTA-based wave equivalents are developed which use grounded capacitors and do not employ any resistors. The flexibility of terminal characteristics is utilized to suggest an alternate wave equivalents realization scheme which results in compact realization of wave filter. The feasibility of CCDDCCTA-based wave active filter is confirmed through simulation of a third-order Butterworth filter. The filter cutoff frequency can be tuned electronically via bias current.

1. Introduction

The current mode approach for analog signal processing circuits and systems has received considerable attention and emerged as an alternate method besides the traditional voltage mode circuits [1] due to its potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption, and high operating speed. The current mode active elements are appropriate to operate with signals in current, voltage, or mixed mode and are gaining acceptance as building blocks in high performance circuit designs which is clear from the availability of wide variety of current mode active elements [2–10]. Recently some analog building blocks [11–16] based on current conveyor variants and transconductance amplifier (TA) cascades in monolithic chip are proposed in open literature which gives compact implementation of signal processing circuits and systems. The examples of such blocks are current conveyor transconductance amplifier (CCTA) [11, 12], current controlled current conveyor transconductance amplifier (CCCCTA) [13], differential voltage current conveyor transconductance amplifier (DVCCTA) [14], differential voltage current controlled conveyor transconductance amplifier DVCCCTA [15], and differential difference current conveyor transconductance amplifier (DDCCTA) [16].

A new active building block, namely, current controlled differential difference current conveyor transconductance amplifier (CCDDCCTA) which has current controlled differential difference current conveyor (CCDDCC) [10] as input block followed by a TA. The CCDDCCTA possesses all the good properties of CCCCTA and DVCCCTA including the possibility of inbuilt tuning of the parameters of the signal processing circuits to be implemented and also all the versatile and special properties of DDCC such as easy implementation of differential and floating input circuits [9, 17, 18]. The CCDDCCTA can be implemented using separate CCDDCC and OTA analog building blocks, but it will be more convenient and useful if CCDDCCTA is implemented in monolithic chip which will result in compact implementation of signal processing circuits and systems. The analytical formulations for port relationship of the proposed

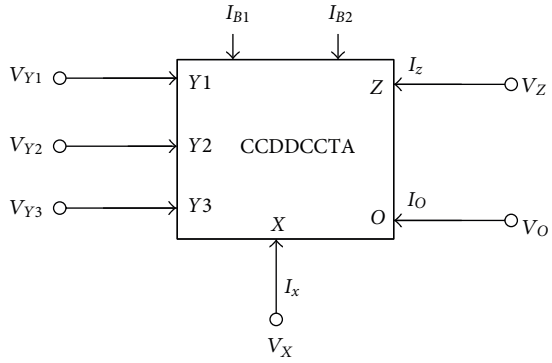


Figure 1: Schematic symbol of CCDDCCTA.

CCDDCCTA circuit are presented in Section 2. Section 3 elaborates the concept of wave filter followed by derivation of CCDDCCTA-based wave equivalent of series inductor. The methodology for obtaining wave equivalent of other passive elements is outlined. An alternate scheme for wave equivalents of shunt capacitor and inductor is also presented. A third order Butterworth filter has been designed using the outlined approach and is presented in Section 4 followed by conclusion. The functionality has been verified through SPICE simulation using 0.25 μm TSMC CMOS technology parameters.

2. Proposed CCDDCCTA

The CCDDCCCTA is an extension of CCDDCC [10] and consists of differential amplifier, translinear loop, and transconductance amplifier. The port relationships of the CCDDCCTA as shown in Figure 1 can be characterized by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & R_x & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \\ V_O \end{bmatrix}, \tag{1}$$

where R_x is the intrinsic resistance at X terminal, and g_m is the transconductance from Z terminal to O terminal of the CCDDCCTA.

The CMOS-based internal circuit of CCDDCCTA in CMOS is depicted in Figure 2. The transistors M_1 to M_{10} present differential difference voltage ($V_{Y1} - V_{Y2} + V_{Y3}$) at gate terminal of M_6, and transistors M_{11} to M_{23} form translinear loop and transistors M_{24} to M_{31} are connected as transconductance amplifier. The analytical expressions for port relationships are obtained in the following sub sections.

2.1. Relationship between Voltages of X Port and Y1, Y2, and Y3 Ports. The analysis of the differential difference part and translinear loop (comprising of transistors from M_1 to M_{21}) of the circuit of Figure 2 gives the voltage at X port as

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3} + \varepsilon_V + I_X R_X, \tag{2}$$

where $R_X = 1/(g_{m16} + g_{m18})$

$$\begin{aligned} \beta_1 &= \frac{1}{P_1}\left(g_{m5}g_{m8} + \frac{g_{m5}\left(g_{m6}g_{m7} - g_{m5}g_{m8}\right)}{g_{m5} + g_{m6}}\right), \\ \beta_2 &= \frac{1}{P_1}\left(g_{m2}g_{m7} + \frac{g_{m2}\left(g_{m2}g_{m7} - g_{m3}g_{m8}\right)}{g_{m2} + g_{m3}}\right), \\ \beta_3 &= \frac{1}{P_1}\left(g_{m3}g_{m8} + \frac{g_{m3}\left(g_{m2}g_{m7} - g_{m3}g_{m8}\right)}{g_{m2} + g_{m3}}\right), \\ \varepsilon_V &= \frac{I_B}{P_1}\left(\frac{g_{m2}g_{m7} - g_{m3}g_{m8}}{g_{m2} + g_{m3}} + \frac{g_{m6}g_{m7} - g_{m5}g_{m8}}{g_{m5} + g_{m6}}\right) \\ &\quad + \frac{I_{B1}}{g_{m16} + g_{m18}}\left(\frac{g_{m20}g_{m12}g_{m18}}{g_{m11}g_{m17}g_{m19}} - \frac{g_{m13}g_{m16}}{g_{m11}g_{m15}}\right), \\ P_1 &= g_{m6}g_{m7} - \frac{g_{m6}\left(g_{m6}g_{m7} - g_{m5}g_{m8}\right)}{g_{m5} + g_{m6}}, \end{aligned} \tag{3}$$

where I_B represents the current flowing through transistor M_1, M_4, and M_9. With matched transconductances $g_{m2} = g_{m3} = g_{m5} = g_{m6}$ and $g_{m7} = g_{m8}$, V_X is obtained as

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} + I_X R_X. \tag{4}$$

2.2. Relationship between Currents at Z and X Ports. The analysis of the portion of the circuit comprising of transistors from M_{11} to M_{23} of the circuit of Figure 2 gives

$$I_Z = \alpha I_X + \varepsilon_1, \tag{5}$$

where

$$\begin{aligned} \alpha &= \frac{1}{g_{m16} + g_{m18}}\left(\frac{g_{m18}g_{m22}}{g_{m21}} + \frac{g_{m23}g_{m16}}{g_{m14}}\right), \\ \varepsilon_1 &= \left(\frac{g_{m12}g_{m20}g_{m18}g_{m22}}{g_{m11}g_{m17}g_{m19}g_{m21}} - \frac{g_{m13}g_{m16}g_{m23}}{g_{m11}g_{m14}g_{m15}}\right) \\ &\quad + \frac{1}{g_{m16} + g_{m18}}\left(\frac{g_{m18}g_{m22}}{g_{m21}} + \frac{g_{m23}g_{m16}}{g_{m14}}\right) \\ &\quad \times \left(\frac{-g_{m12}g_{m18}g_{m20}}{g_{m11}g_{m17}g_{m19}} + \frac{g_{m13}g_{m16}}{g_{m11}g_{m15}}\right) I_{B1}. \end{aligned} \tag{6}$$

For matched transistors, (6) reduced to

$$I_Z = I_X. \tag{7}$$

2.3. Relation for Currents at O Port. The transistor comprising from M_{24} to M_{31} forms transconductance amplifier (TA). Assuming gate voltages of transistors M_{24} and M_{25} as V_{T1} and V_{T2}, respectively, the output currents I_O may be found as

$$I_O = \gamma_1 V_{T1} - \gamma_2 V_{T2} + \varepsilon_2, \tag{8}$$

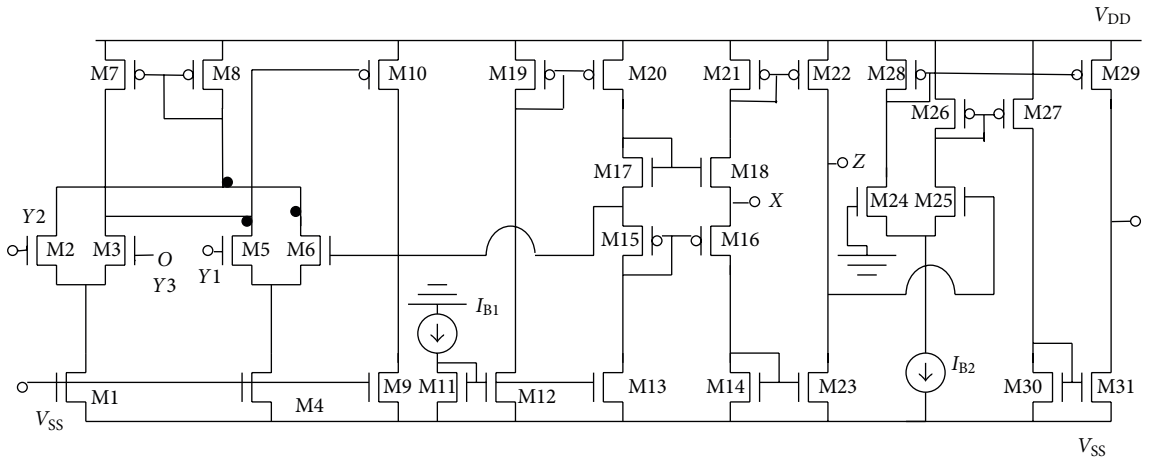


Figure 2: CMOS implementation of CCDDCCTA.

where

$$\gamma_1 = \frac{-1}{g_{m24}+g_{m25}}\left(\frac{g_{m24}g_{m25}g_{m29}}{g_{m28}}+\frac{g_{m24}g_{m25}g_{m27}g_{m31}}{g_{m26}g_{m30}}\right),$$

$$\gamma_2 = \frac{-1}{g_{m24}+g_{m25}}\left(\frac{g_{m24}g_{m25}g_{m29}}{g_{m28}}+\frac{g_{m24}g_{m25}g_{m27}g_{m31}}{g_{m26}g_{m30}}\right),$$

$$\varepsilon_2 = \frac{I_{B2}}{g_{m24}+g_{m25}}\left(\frac{-g_{m24}g_{m29}}{g_{m28}}+\frac{g_{m25}g_{m27}g_{m31}}{g_{m26}g_{m30}}\right). \quad (9)$$

With $g_{m24} = g_{m25} = g_m$, $g_{m26} = g_{m27}$, $g_{m28} = g_{m29}$, and $g_{m30} = g_{m31}$, (8) reduced to

$$I_O = g_m V_{T1} - g_m V_{T2}, \quad (10)$$

as $V_{T1} = 0$ and $V_{T2} = V_Z$

$$I_O = -g_m V_Z, \quad (11)$$

where

$$g_m = \sqrt{2\mu C_{OX}\left(\frac{W}{L}\right)_{24,25} I_{B2}}. \quad (12)$$

2.4. Simulation. To verify the port relationship of proposed CCDDCCTA, PSPICE simulations have been carried out using TSMC 0.25 μm CMOS process model parameters. The aspect ratio of various transistors for CCDDCCTA is given in Table 1. The supply voltages of VDD = −VSS = 1.25 V and VBB = −0.8 V are used. The DC transfer characteristics of the proposed CCDDCCTA from $Y1$, $Y2$, and $Y3$ terminals to X terminal are shown in Figure 3. The variation of current at Z terminal with X terminal current is shown in Figure 4. Figures 3 and 4 verify the port relationships. The variation of resistance, R_X with respect to bias current I_{B1}, is shown in Figure 5. The transconductance of CCDDCCTA is bias current controllable which is depicted in Figure 6 by varying I_{B2} from 0 to 800 μA. There is decrease in transconductance for bias currents larger than 400 μA. This is due to transistors M_{24}, M_{25} entering in linear region of operation from saturation region.

Table 1: Aspect ratio of various transistors.

Transistors	W (μm)/L (μm) ratio
M_1, M_4, M_9, M_{11}–M_{14}, M_{23}, and M_{30}-M_{31}	3.0/0.25
M_2-M_3, M_5-M_6	1.0/0.25
M_7-M_8	5.0/0.25
M_{10}	12.5/0.25
M_{15}	8.0/0.25
M_{16}	9.0/0.25
M_{18}	4.5/0.25
M_{27}	4.35/0.25
M_{17}, M_{19}–M_{22}, M_{24}-M_{25}, M_{26}, and M_{28}-M_{29}	5.0/0.25

3. CCDDCCTA's Application as Wave Active Filter

In this section the proposed CCDDCCTA has been used to develop higher-order filter. There are many schemes for simulating higher order filters using doubly terminated lossless ladders available in the literature. The element replacement, operational simulation, and impedance scaling schemes employ mostly lossless integrator which is not easy to implement in integrated circuits due to active and passive element imperfections. Recently, wave approach based ladder filter realization has received attention which relies on modelling incident and reflected voltage waves. It utilizes only lossy integrators for passive component representation and results in a very modular structure. Considering this, some wave active filters have been reported in the literature [19–22]. The wave active filter realization using proposed CCDDCCTA is presented in this section which has the following advantageous features.

(i) It does not use any resistor in contrast to those proposed in [19–21].

(ii) It uses only active elements and capacitors similar to [22].

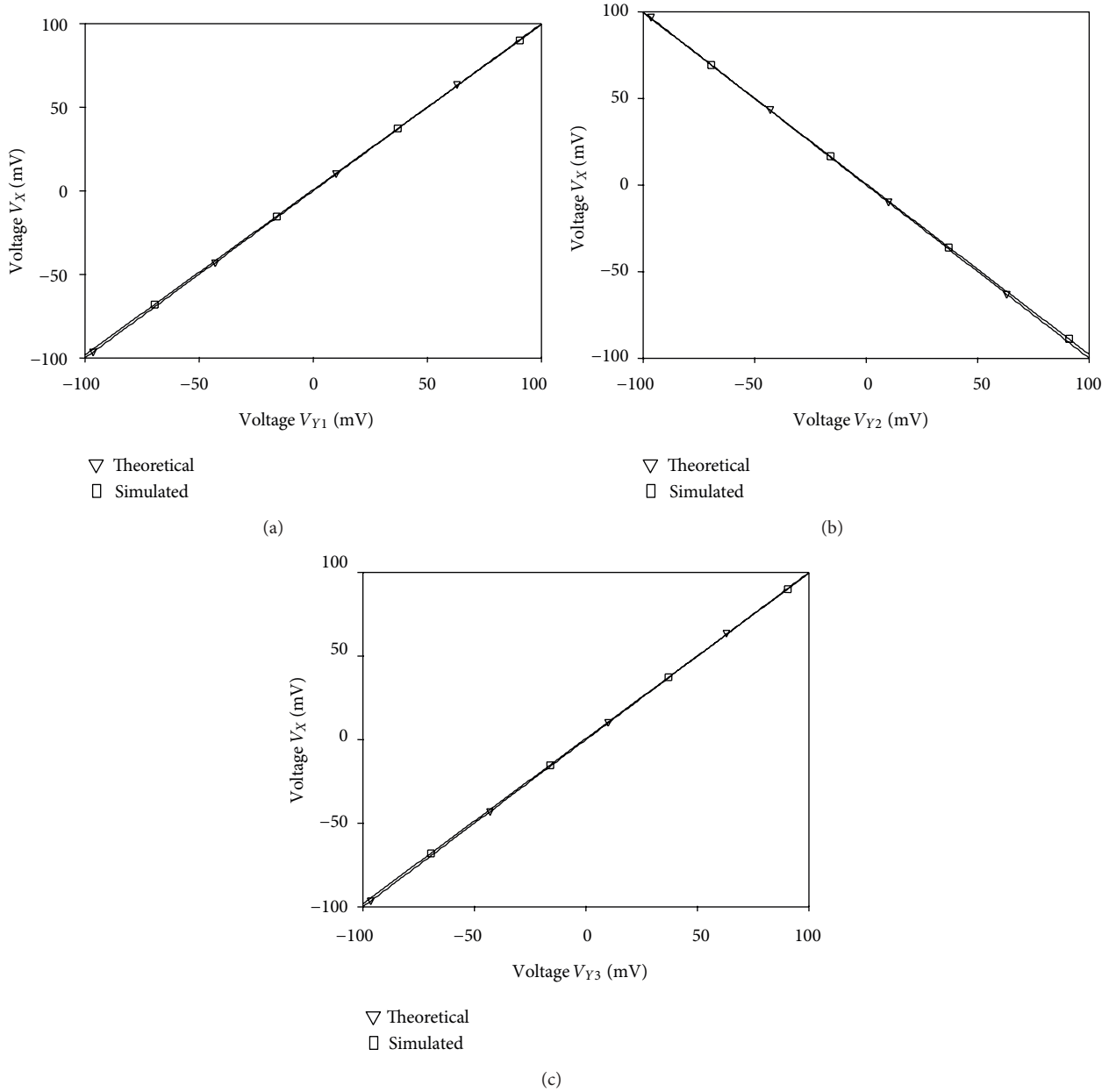


Figure 3: DC transfer characteristic for voltage transfer from (a) $Y1$ port to X port, (b) $Y2$ port to X port, and (c) $Y3$ port to X port.

(iii) It possesses an attractive feature of electronic tunability via bias currents of CCDDCCTA similar to the reported in [22].

(iv) The availability of an additional voltage input terminal in CCDDCCTA as compared to DVCCCTA, the active elements required for wave equivalent can be reduced. Thus, the proposed element gives a compact resistorless realization of wave filter than the one reported in [22].

3.1. Derived Basic Wave Equivalent. According to wave method, the corresponding LC ladder filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and signal inversion. Then each element of the passive prototype filter is substituted by its wave equivalent.

The development of the filter using wave method is based on modeling incident and reflected voltage waves. For a two-port network of Figure 7, the voltage wave is defined as

$$A_j = V_j + I_j R_j, \qquad B_j = V_j - I_j R_j, \tag{13}$$

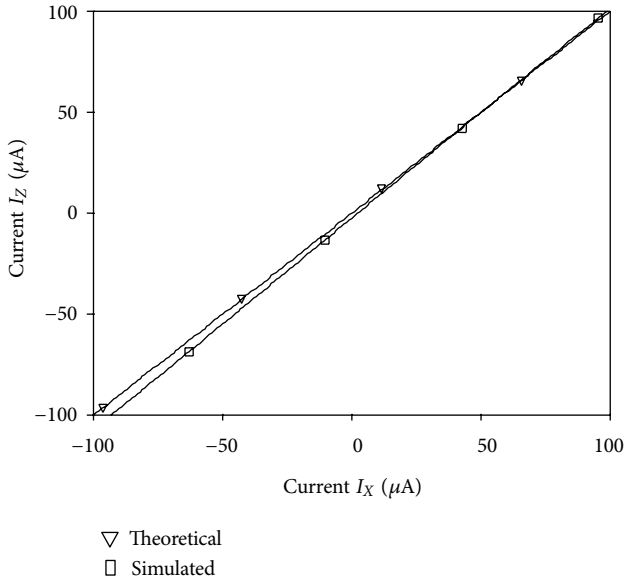


FIGURE 4: DC transfer characteristic for current transfer from X port to Z port.

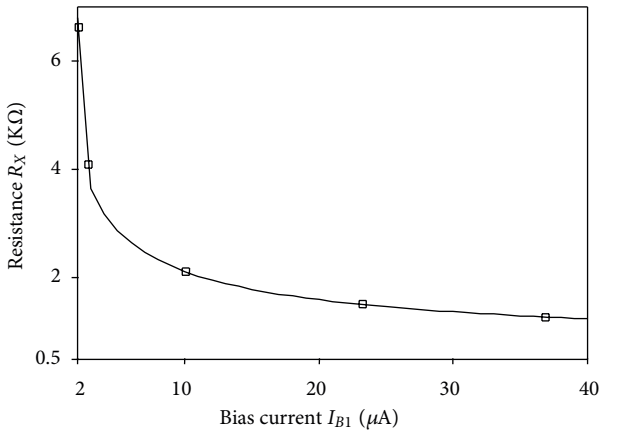


FIGURE 5: Variation of resistance with bias current I_{B1}.

where A_j, B_j, and R_j ($j = 1, 2$) represent incident and reflected voltage waves and port normalization resistance of port j, respectively.

Equation (13) can be expressed in terms of scattering matrix S as

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}. \tag{14}$$

The ladder network may be viewed in terms of its constituent series-arm impedance elements and shunt-arm admittance elements [19, 20], and the scattering matrices

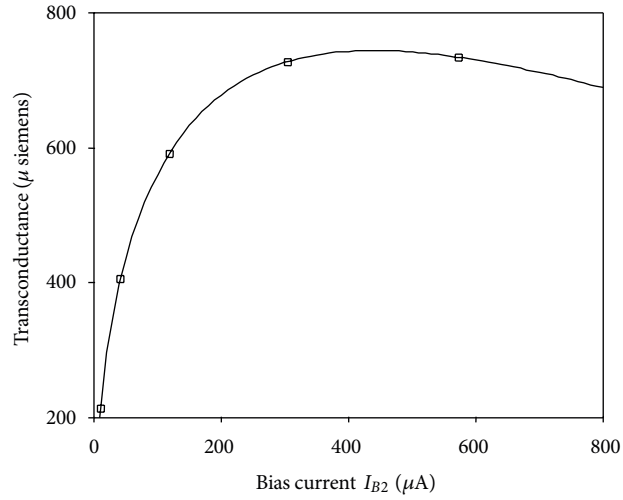


FIGURE 6: Variation of transconductance with bias current I_{B2}.

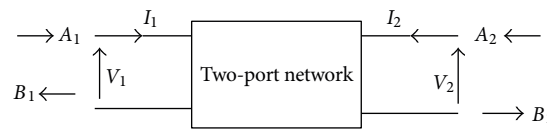


FIGURE 7: Two-port network with wave variables.

(S_Z and S_Y) [20] for series-arm impedance (Z) and shunt-arm admittance (Y) are represented as

$$S_Z = \begin{bmatrix} \dfrac{Z}{2R+Z} & \dfrac{2R}{2R+Z} \\ \dfrac{2R}{2R+Z} & \dfrac{Z}{2R+Z} \end{bmatrix}, \tag{15}$$

$$S_Y = \begin{bmatrix} \dfrac{-Y}{2G+Y} & \dfrac{2G}{2G+Y} \\ \dfrac{2G}{2G+Z} & \dfrac{-Y}{2G+Y} \end{bmatrix}, \tag{16}$$

where R is port normalization resistance, and G is its reciprocal.

The series inductor L is considered as a basic element for the wave active filter realization. Its scattering matrix (S_{Z_L}) may be obtained from

$$S_{Z\_L} = \frac{1}{1+s\tau} \begin{bmatrix} s\tau & 1 \\ 1 & s\tau \end{bmatrix}, \tag{17}$$

where $\tau = L/2R$ represents time constant.

Using (14) and (17), the reflected wave (B_j, $j = 1, 2$) for a series inductor can be expressed in terms of its incident wave (A_j, $j = 1, 2$) as

$$B_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2), \tag{18}$$

$$B_2 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2). \tag{19}$$

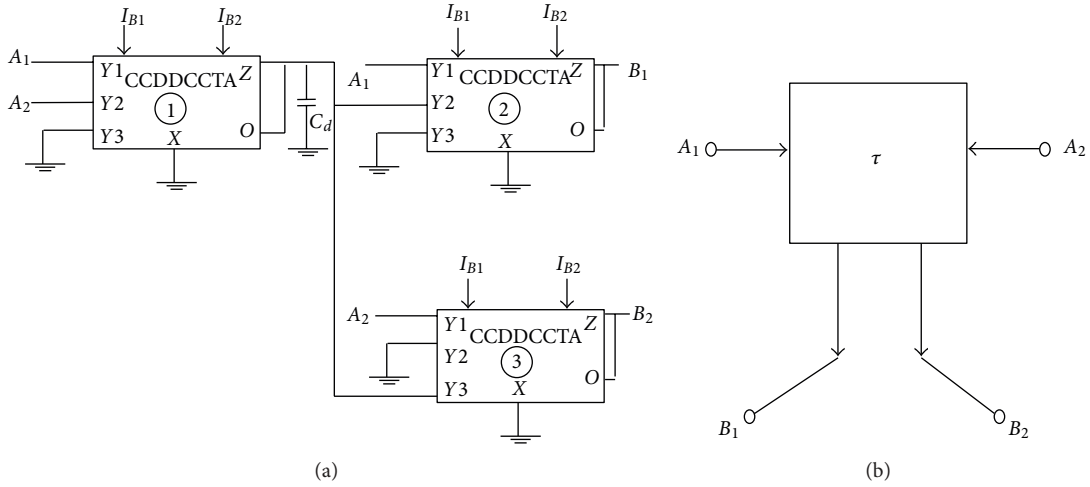


Figure 8: (a) Complete schematic of CCDDCCTA-based wave equivalent of series inductor and (b) its symbolic representation.

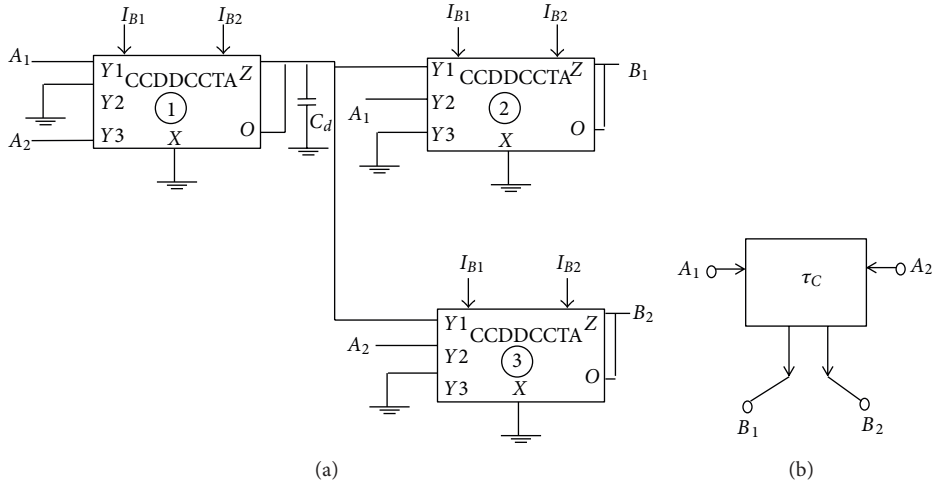


Figure 9: (a) Complete schematic of CCDDCCTA-based wave equivalent of shunt capacitor and (b) its symbolic representation.

The circuit implementation of (18) is derived by cascading lossy integration subtraction with subtraction, whereas (19) requires a lossy integration subtraction followed by an adder. The complete realization is depicted in Figure 8. The CCDDCCTA marked as "1" in Figure 8(a) performs lossy integration subtraction and provides output voltages V_1 as

$$V_1 = (A_1 - A_2)\frac{1}{1+s\tau}, \tag{20}$$

where $\tau = R_X C_d$ is time constant and $g_m R_X = 1$. Using (18), (19), and (20), the value of C_d may be computed as

$$R_X C_d = \frac{L}{2R}. \tag{21}$$

With $R = R_X$, the value of capacitor C_d may be expressed as

$$C_d = \frac{L}{2R^2}. \tag{22}$$

The CCDDCCTAs marked as "2" and "3" in Figure 8(a) perform subtraction and addition operations and provide the output voltages as

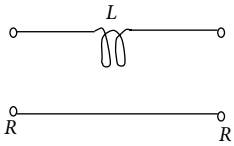
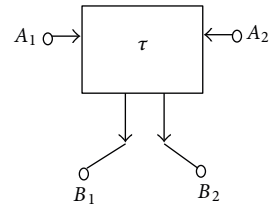
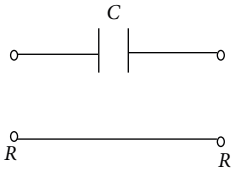
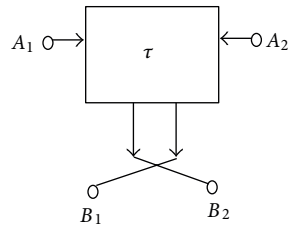
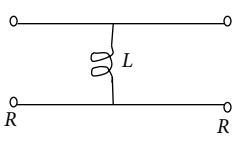
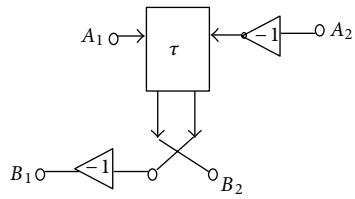
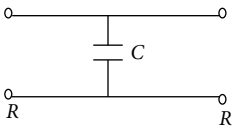
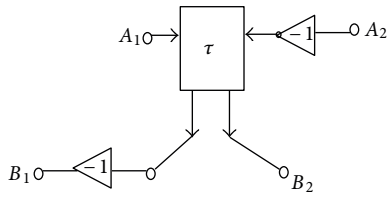
$$B_1 = A_1 - V_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2) \text{ with } g_m R_X = 1,$$
$$B_2 = A_2 + V_1 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2) \text{ with } g_m R_X = 1. \tag{23}$$

The symbolic representation of the wave element is shown in Figure 8(b) [19–22].

The wave equivalent of other reactive elements can be obtained using the basic wave equivalent of Figure 8. The wave equivalent for inductor and capacitor in series and shunt branches is given in Table 2 which can be obtained by swapping outputs and signal inversion.

3.2. Alternate Scheme for Shunt Impedance Realization. An alternate scheme for wave equivalent realization of shunt

Table 2: Wave equivalent of elementary two-port network consisting of single element in series and shunt branch.

Elementary two-port network	Port connection	Realized time constant; capacitor value for CCDDCCTA-based wave equivalent
		$\tau = L/2R$ $C_d = L/2R^2$
		$\tau = 2RC$ $C_d = 2C$
		$\tau = 2L/R$ $C_d = 2L/R^2$
		$\tau = RC/2$ $C_d = C/2$

impedances is suggested in this section. This scheme is based on direct realization of port relation of shunt capacitor wave equivalent. It may be noted from Table 2 that shunt capacitor requires two inverters with a basic wave equivalent of Figure 8 amounting to a total of five CCDDCCTAs. Using (16), the incident (A_j, $j = 1, 2$) and the reflected wave (B_j, $j = 1, 2$) for a shunt capacitor are related through the following scattering matrix:

$$S_{Y\_C} = \frac{1}{1 + s\tau_C} \begin{bmatrix} -s\tau_C & 1 \\ 1 & -s\tau_C \end{bmatrix}, \tag{24}$$

where $\tau_C = RC/2$ is time constant. The expressions for reflected waves B_1 and B_2 become

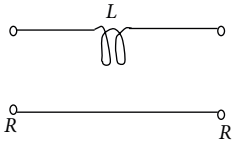
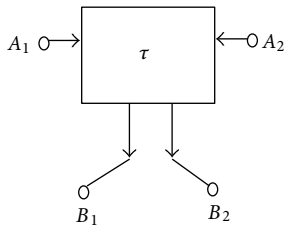
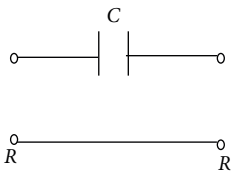
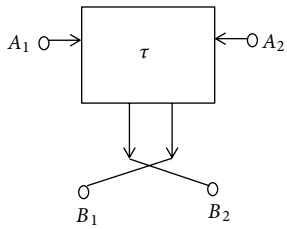
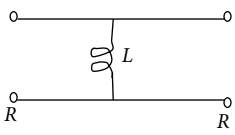
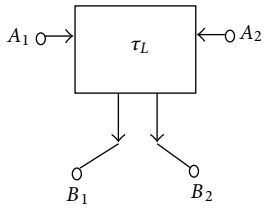
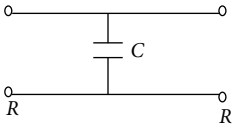
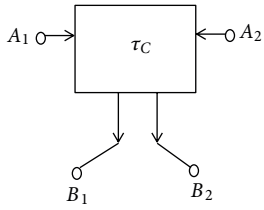
$$B_1 = -A_1 + \frac{1}{1 + s\tau_C}(A_1 + A_2), \qquad B_2 = -A_2 + \frac{1}{1 + s\tau_C}(A_1 + A_2). \tag{25}$$

The implementation of (25) and (33) requires two operations-lossy integration addition and subtraction. The high impedance input terminal $Y3$ of CCDDCCTA can be used for lossy integration addition, and proper outputs are obtained by feeding A_1 and A_2 to $Y2$ terminals of second and third CCDDCCTAs as shown in Figure 9(a). This realization may be represented by a symbol of Figure 9(b) for clarity. This slight modification in implementation method results in the saving of two CCDDCCTAs. Similar reduction of active element may be achieved for a shunt inductor as shown in Figure 10. The complete set of wave equivalents is summarized in Table 3. It may be noted that all the wave equivalents in Table 3 use only three active blocks. Thus, this method leads to a compact realization of wave active filter as compared to the one proposed in [22].

The design of wave active filter [19–22] starts with the selection of prototype filter based on specifications. The individual inductors or capacitors are replaced by their wave equivalents resulting in a modular realization. The complete filter schematic is then implemented by cascading the wave equivalents of the passive elements of prototype ladder.

3.3. Simulation of Third-Order Butterworth Filter. The theoretical proposition is verified using SPICE simulations using 0.25 μm TSMC CMOS technology parameters and power supply of ±1.25 V. The usefulness of the proposed CCDDCCTA is shown by implementing wave active filter based on

Table 3: Elementary two-port network consisting of single element in series and shunt branch using alternate scheme.

Elementary two-port network	Port connection	Realized time constant; capacitor value for CCDDCCTA-based wave equivalent
		$\tau = L/2R$ $C_d = L/2R^2$
		$\tau = 2RC$ $C_d = 2C$
		$\tau = 2L/R$ $C_d = 2L/R^2$
		$\tau = RC/2$ $C_d = C/2$

the method outlined in Sections 3.1 and 3.2. A third-order low-pass filter of Figure 11 has been taken as prototype. The normalized component values are $R_S = 1$, $L_1 = 1$, $L_2 = 1$, $C_1 = 2$, and $R_L = 1$ for maximally flat response.

The wave equivalent topology of Figure 11 may be constructed by replacing series inductor and shunt capacitor by wave equivalent of Table 3 and is shown in Figure 12. For cutoff frequency $f_o = 10$ MHz, the bias currents I_{B1} and I_{B2} are taken as 25 μA and 200 μA, respectively. The capacitor values for wave equivalent of series inductors (L_1, L_2) and shunt capacitors (C_1) are 5.4 pF, 5.4 pF, and 10.8 pF, respectively. The topology of Figure 12 has been simulated using CCDDCCTA-based wave equivalent discussed in Section 3. Figures 13 and 14 show the simulated low pass responses (V_{out}) and its complementary high-pass response ($V_{\text{out},c}$), respectively. The tunability of the filter response by varying bias current I_{B1} from 10 μA to 50 μA and I_{B2} from 50 μA to 400 μA ($I_{B2} = 8I_{B1}$ for $g_m R_x = 1$) is also studied through simulations, and the results are shown in Figure 15. The power dissipation of the CCDDCCTA-based filter is simulated to be 13.7 mW, whereas TA-based wave filter power dissipation is found to be 25.6 mW.

To study the time domain behavior, input signal comprised of two frequencies of 5 MHz and 20 MHz is applied. Signal amplitude was 50 mV each. The transient response with its spectrum for input and output is shown in Figure 16, which clearly shows that the 20 MHz signal is significantly attenuated. The proposed circuit is also tested to judge the level of harmonic distortion at the output of the signal. The %THD result is shown in Figure 17 which shows that the output distortion is low and within acceptable limit of 6% up to about 300 mV.

4. Conclusion

In this paper current controlled differential difference current conveyor transconductance amplifier (CCDDCCTA), a new active building block for analog signal processing, is presented. The expressions for port characteristics are derived and verified through SPICE. The wave filter based on CCDDCCTA is included to show the usefulness of the element. The CCDDCCTA-based wave equivalent of series inductor is introduced which is applied for other passive element realization by making suitable connections. The

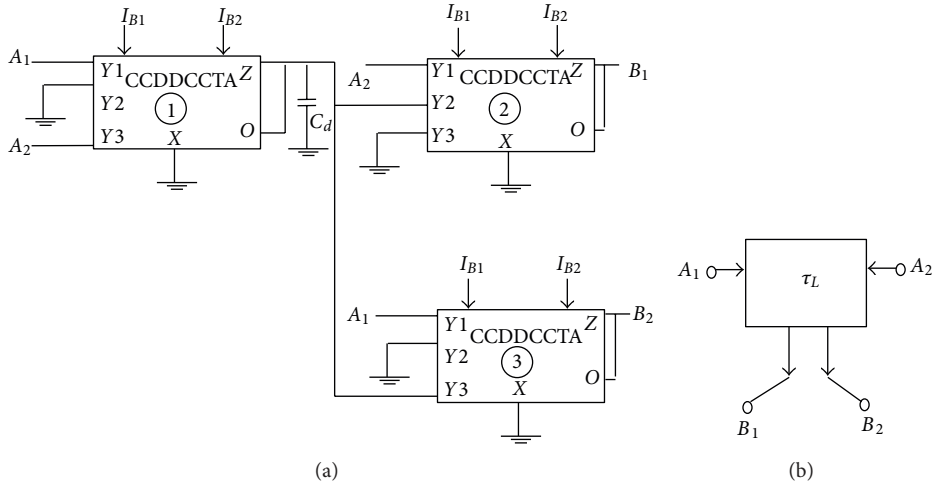


Figure 10: (a) Complete schematic of CCDDCCTA-based wave equivalent of shunt inductor and (b) its symbolic representation.

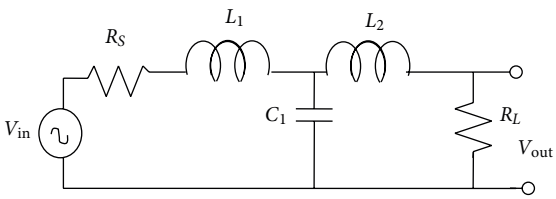


Figure 11: Third order low-pass Butterworth Filter.

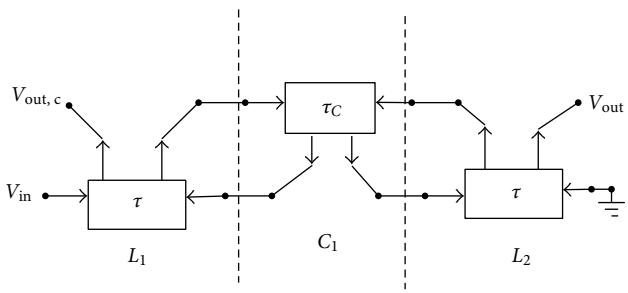


Figure 12: Wave equivalent of prototype filter.

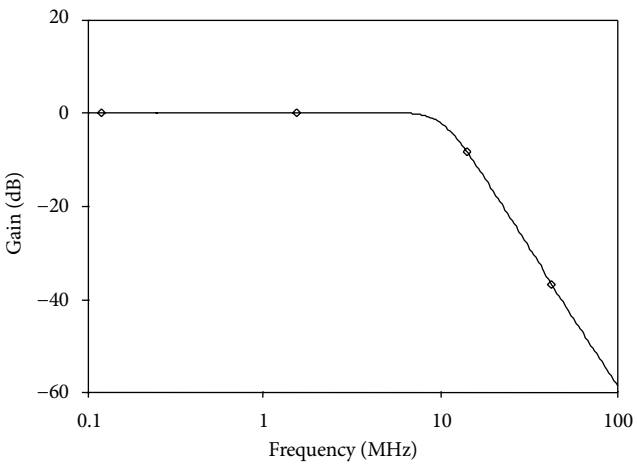


Figure 13: Frequency response of third order low-pass filter.

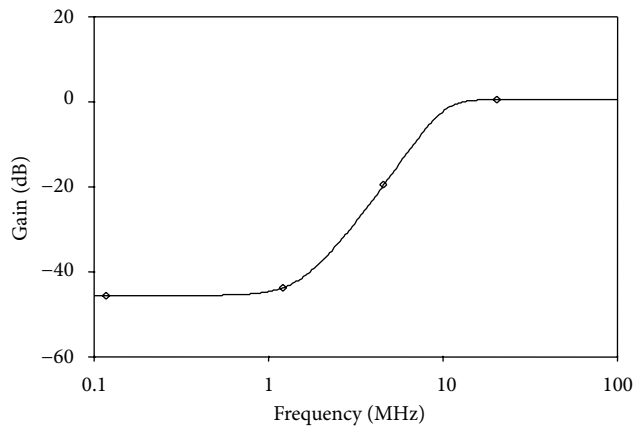


Figure 14: Frequency response of complementary high-pass filter.

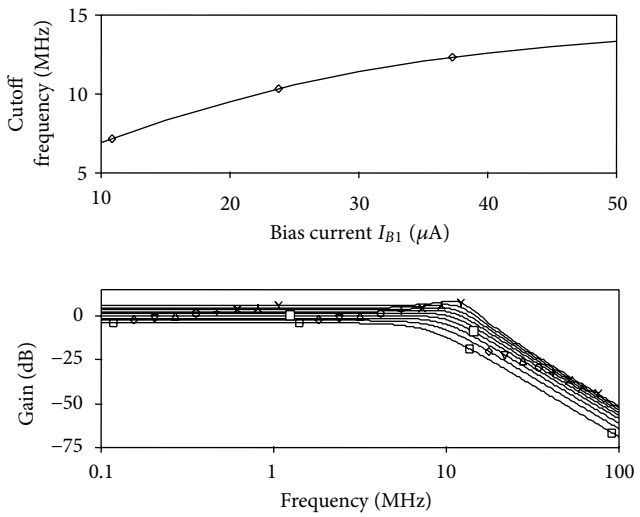


Figure 15: Demonstration of electronic tunability.

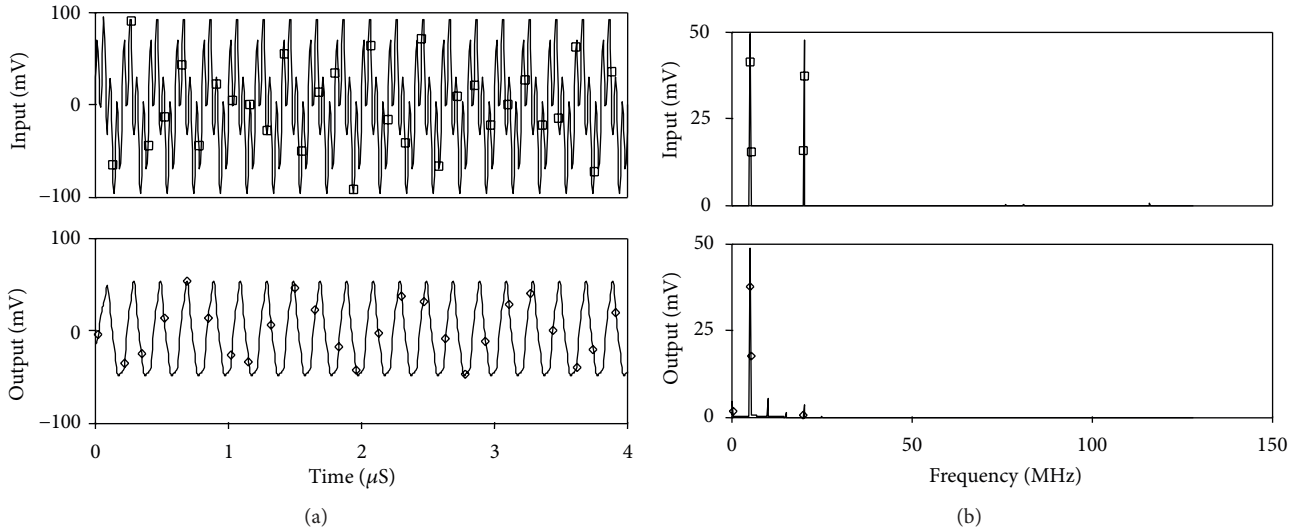


Figure 16: Transient response with (a) input and output signals and (b) spectrum of input and output signals.

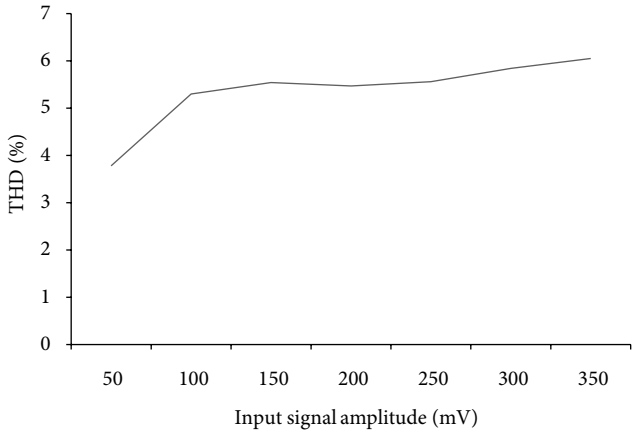


Figure 17: Variation of %THD with input signal amplitude.

availability of additional input terminals in CCDDCCTA is gainfully used for obtaining a compact realization of shunt impedance wave equivalents. The structure is resistorless, employs grounded capacitors, possesses electronic tunability of cutoff frequency, and is modular.

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