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Current Crowding Effect on Copper Dual Damascene Via Bottom Failure for ULSI Applications

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***Abstract*—Reliability of interconnect via is increasing an important issue in submicron technology. Electromigration experiments are performed on line/via structures in two level Cu dual damascene interconnection system and it is found that wide line/via fails earlier than the narrow line/via. Atomic flux divergence based finite element analyses is performed and stress-migration is found to be important in the failure rate behavior observed. Semi-classical width dependence Black's equation together with the finite element analysis revealed that the difference in the time to failure is due to the much larger average current density along the interface between the line and via for the wide line/via structure, and good agreement is obtained between the simulation and experimental results.**

***Index Terms*—Atomic flux divergence, copper, current crowding, via electromigration.**

I. Introduction

ELECTROMIGRATION (EM) induced failure continues to be a major reliability issue as the feature size of ULSI technology is reducing. The ever increasing complexity of interconnect system requires more demanding reliability on the various components in the system. Today, the limiting factor in interconnect reliability is increasingly dominated by the EM performance of vias with the performance of lines playing a substantially lesser role in submicron technology [1]–[3]. The transition from Al to Cu interconnects leads to new via structure fabricated by dual damascene process, and the EM reliability of Cu interconnects has not been found to be as good as anticipated over Al interconnects [4]. A recent critical review can be found in [5] in this aspect.

In a via structure, current density, temperature, and stress distributions are not uniform as in an interconnect line. The peak current density appears at the inner corners of via-top and via-bottom, resulting in high local current density at the corners. This high local current density produces strong electron wind driving force and hence affects the median time to failure (MTF) as MTF is directly related to the current density by the semi-classical Black's formula. Furthermore, the atomic flux divergences due to nonuniform distributions of temperature and stress could be comparable to that due to electron-wind force.

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Moreover, Cu EM performance is strongly depends on the interface/surface available for mass transport [6], [7]. Unfortunately, chemical–mechanical polishing (CMP), an integral part of the Cu interconnect fabrication process, does not allow the top surface of metallization line to be covered by the barrier layer unlike its side walls and bottom surface. Therefore, at the inner corner of the via-bottom, two kinds of diffusion interface paths are available: one with Cu and barrier layer at the cylindrical via bottom; and the other with Cu and cap layer at the top surface of metallization near the cylindrical via. These are the locations at which the current is crowded. Hence, current crowding in via should be a dominant factor for via EM performance. Though the effect of current crowding has been reported for Al based interconnects, similar work has not been explored for Cu based interconnects. In this work, the effect of such current crowding on Cu via EM performance will be investigated.

In this work, we will focus on the via bottom failure of a two-level Cu dual damascene line/via structures with line widths of 0.28 and 0.7 μm, respectively. They will be termed as narrow and wide line/via, respectively, in the subsequent discussion. Both structures have the same cylindrical via diameter of 0.26 μm and line thickness of 0.35 μm. EM experiments and three-dimensional (3-D) static finite element analysis (FEA) will be employed to explain the various physical failure mechanisms at the EM test condition.

II. Experimental Details

EM test structures with line widths of 0.28 and 0.7 μm have been fabricated using 0.18 μm Cu/oxide dual damascene technology. The first inter-metal dielectric (IMD) stack consisted of plasma enhanced chemical vapor deposited (PECVD) layer of 50 nm SiN and 800 nm undoped silicate glass (USG) on top of p-Si substrate using Novellus concept two Sequel Express PECVD system. M1 trench was patterned using 248 nm lithography, and the USG layer was etched using a fluorine-based dry-etch chemistry in TFL 85 DRM oxide etcher. Photoresist stripping and wet clean were performed to ensure polymer residue-free trenches.

Formation of Cu metallization in these trenches involved depositing a stack of 25 nm Ta barrier and 150 nm Cu seed by physical vapor deposition (PVD) in Applied materials PVD/CVD Endura HP 5500 followed by 0.6 μm electrochemically plated (ECP) Cu layer using Novellus SABRE system. A 50 nm thick SiN layer was deposited after CMP process to serve as Cu cap layer. Then layers of 800 nm USG, 50 nm SiN and 500 nm USG were deposited as IMD-2 in which 50 nm SiN serve as trench-2 stop layer. Via and M2 trench were then formed by a via-first dual damascene process. In the M1 test structures, M2 (lines

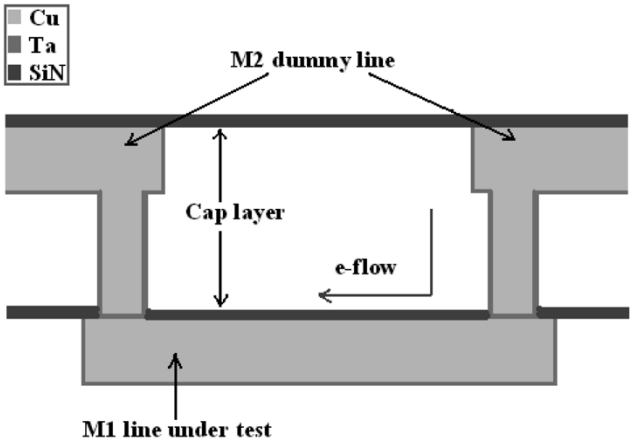

Fig. 1. Cross sectional schematic diagram of the test structure.

connected to pads) were short so that voids would be expected to form in M1 and is *vice versa* for the M2 test structures. The lines are 0.35 μm thick and the via diameter is 0.26 μm for all the test structures. Both the M1 and M2 test structures were fabricated on the same wafers while only EM characterization of M1 test structure will be discussed for the present work. Schematic diagram of the test structure employed in this study is shown in Fig. 1.

EM test was performed using *Qualitau* package level electromigration test system. Resistance increase with time was monitored until failure. Failure criterion of 10% increase in resistance was used in this study. Both the narrow and wide line/via M1 test structures were tested with 0.8 MA/cm^2 current density at three different temperatures of 300 °C, 325 °C, and 350 °C, with their MTFs computed. The cumulative failure distributions for the narrow and wide line/via structure are shown in Figs. 2 and 3, respectively. The EM results are summarized in Table I. The narrow and wide line/via M2 test structures are also tested with the same EM test conditions as that of M1 test structures but their results will not be discussed in this work. The physical failure analysis has been performed using focused ion beam (FIB), and Fig. 4 shows a FIB image of a failed line/via structure.

III. Simulation

In order to understand the various physical mechanisms in the via EM failure in this work, 3-D FEA was performed where the atomic flux divergences (AFD) due to various driving forces were computed. In contrast to a pure diffusion process in which the concentration gradient of the moving species is the only driving force, EM phenomenon is a completed diffusion process controlled by multiple physical mechanisms, including electron-wind force induced migration (EWM), stress induced migration (SM) as well as thermal induced migration or thermo-migration (TM). The mathematical implementation for the atomic flux divergences due to theses physical mechanisms has been described by Dalleau *et al.* [8] with common activation energy for the three migration processes. However, this is not true from microscope point of view. A detail discussion on this fact can be found in a line EM work presented by Zhang *et al.*

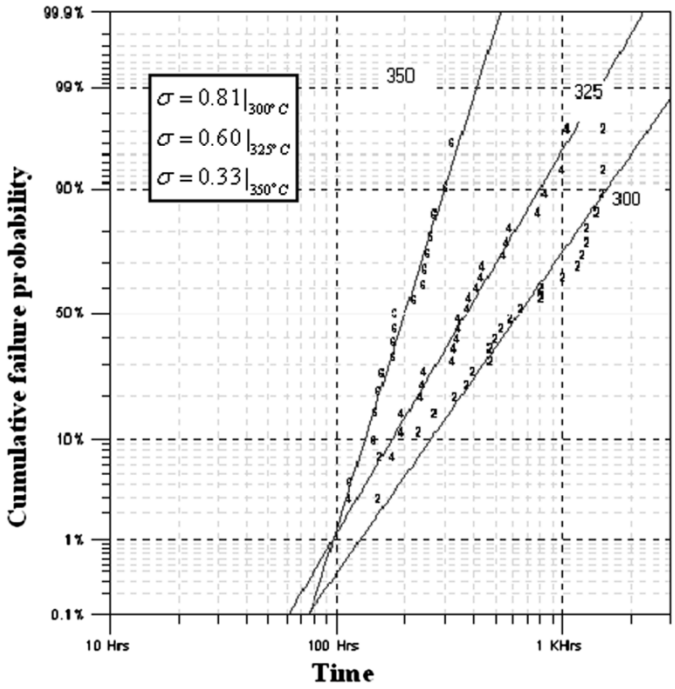

Fig. 2. Cumulative failure distribution for the narrow line/via.

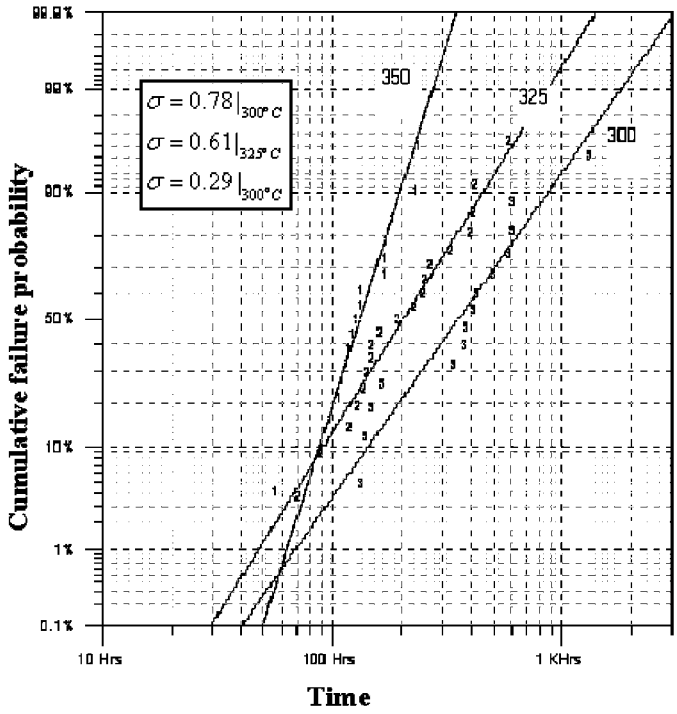

Fig. 3. Cumulative failure distribution for the wide line/via.

[9] and Tan *et al.* [10]. In this work, we follow the later work and applied to a via/line structure.

The basic structure after discritization for FEA is shown in Fig. 5. The length, width, and thickness of the structure are taken along the X, Y, and Z (vertical direction) axes, respectively. The location of the global origin of the coordinate system is shown in Fig. 5, and all the computational results are calculated with

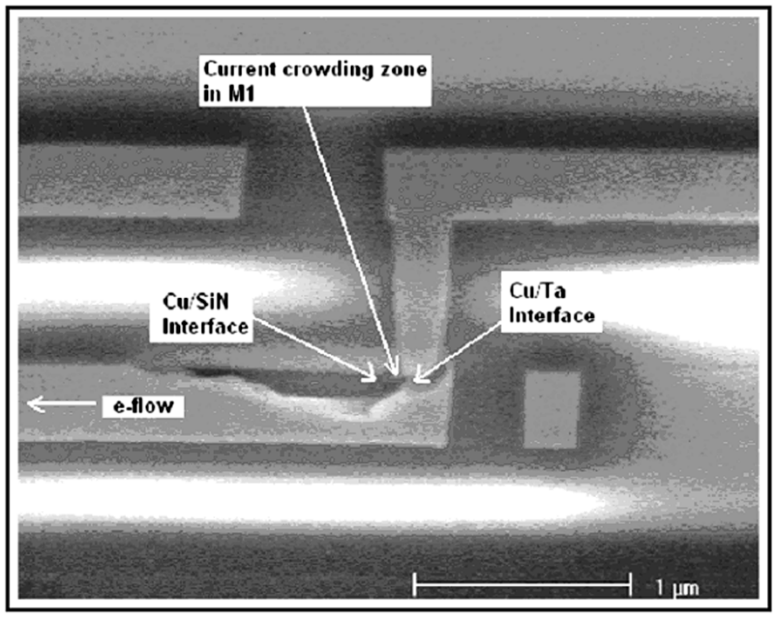

Fig. 4. FIB image of a via bottom failure.

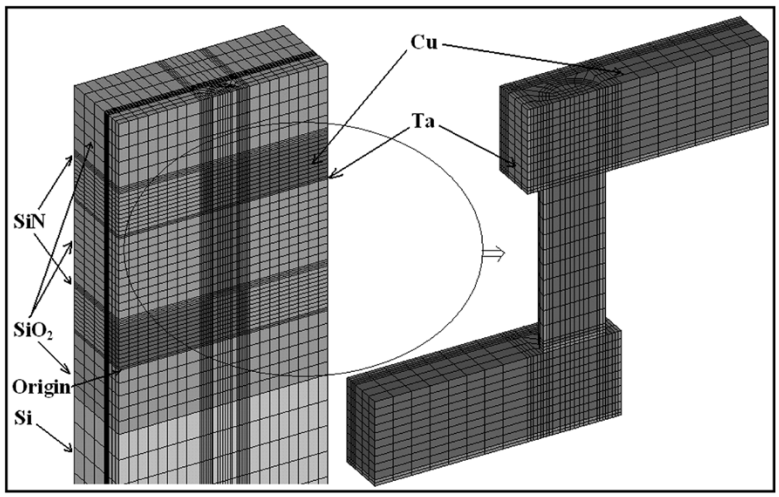

Fig. 5. Typical meshing of the line/via structure for FEA.

TABLE I
EM TEST DATA

Stressing Temp. (in °C)	t_{50}^{narrow} (in hrs) for narrow line/via	t_{50}^{wide} (in hrs) for wide line/via	Ratio of $\frac{t_{50}^{narrow}}{t_{50}^{wide}}$ from experiment	Ratio of $\frac{t_{50}^{narrow}}{t_{50}^{wide}}$ using equation (2) with n=1.9
300	418.8	315.4	1.33	1.33
325	280.2	203.3	1.38	1.38
350	189.4	132.9	1.43	1.42

respect to this origin. For realistic, the full substrate thickness of 300 μm is considered in the model.

The multiphysics finite element analysis software ANSYS is used here. As the element aspect ratio is limited to 20 in the software, it is difficult to discritize all the sub-domains in the structure by using the "Mesh Tool" or "Map Mesh" to mesh the entire structure. Therefore, direct generation technique is used for discritization [11].

In addition, complexity arises due to the fact that the circular via-end surfaces are connected to the rectangular metallization surfaces. Such connection requires both the cylindrical and rectangular coordinate systems to be considered in the model, and proper connection between the two coordinate systems is necessary. Hence, every node in the meshing is created by defining its coordinates and "brick" element is formed that connect the adjacent 8 nodes with defined material properties. With this way of building the FE model, though it is tedious, the user can have a full control and flexibility on the model.

It is a common practice to take the stress-free temperature (SFT) of the damascene interconnects in between 350 °C to

TABLE II
EM PARAMETERS FOR FE SIMULATION

Parameter	Material	Value	Reference
Electronic charge (e)	-	1.6021×10^{-19} Coulomb	-
Boltzmann's constant (k_B)	-	1.3867×10^{-23} Joule/°K	-
Atom concentration	Cu	8.44×10^{-28} /m^3	-
Activation energy for EWM	Cu	0.6 eV	-
Activation energy SM	Cu	0.74 eV	[14]
Effective charge number (Z^*)	Cu	4	[10]
Diffusion constant (D_0)	Cu	7.8×10^{-5} m^2/s	[16]
Atomic volume (Ω)	Cu	1.18×10^{-29} m^3	-
Resistivity @ 20°C (ρ_0)	Cu	1.69×10^{-8} Ω-m	[17]
Temperature coefficient of resistivity (α)	Cu	4.3×10^{-3} Ω-m/°K	[18]
Resistivity @ 300 °C (ρ)	Ta	70×10^{-8} Ω-m	[19]

400 °C [12]–[14], depending on annealing temperature of the sample. In this work, 300 °C is taken as SFT in the simulation.

The FEA model developed here consists of two steady state analyses, namely a direct coupled analysis with the current and temperature fields, and an analysis with indirect coupling between temperature and stress fields. In the first stage of analysis, the substrate bottom surface is kept at constant EM test temperature, and a constant line current density of 0.8 MA/cm^2 is applied as boundary conditions. The nodal temperatures are then retrieved from this stage for use in the second stage of simulation. In the second stage of simulation, structural analysis is performed with the following three boundary conditions: 1) nodal temperatures obtained in the first stage of analysis are used as the body force temperature; 2) the substrate bottom surface is kept fixed i.e., no displacement is allowed to the bottom surface of Si substrate; and 3) the vertical symmetric plane is constrained to remain vertical as arise from the mirror symmetrical nature of the structure under consideration.

With this model, the atomic flux divergences due to EWM, SM, and TM are computed for the wide line/via test structure considering the three different test temperatures of 300 °C, 325 °C, and 350 °C with the same line current density of 0.8 MA/cm^2 at time zero of EM test for all the cases. All the dimensional parameters in the simulation are exactly same as the experimental test structure. The EM parameters and materials properties used in the simulation are listed in Tables II and III.

IV. RESULTS AND DISCUSSION

A. EM Test Data Analysis

From the CDF plots in Fig. 2 and 3, one can see that there is significant variation of the *log-normal* σ with stressing temperature. As significant difference in σ implies different failure mechanisms, one should expect the activation energy (E_a) of EM is different at different test temperatures.

TABLE III
MATERIAL PROPERTIES FOR FE SIMULATION

Material	Young's Modulus (GPa)	Poisson ratio	Thermal conductivity (W/mK)	Coefficient of thermal expansion (/°K)	Reference
Cu	129.8	0.339	379	16.5×10^{-6}	[17], [19]
Ta	186.2	0.35	53.65	6.48×10^{-6}	[20]-[21]
SiN	265	0.27	0.8	1.5×10^{-6}	[22]-[25]
SiO_2	71.4	0.16	1.75	0.68×10^{-6}	[12], [17]
Si	130	0.28	61.9	4.4×10^{-6}	[12], [17]

However, it is interesting to note that, the σ's are very close for the two line widths at a given test temperature. Since it is reported that E_a vary with line width [26], and with the close σ values observed between the two line widths, we should expect that their E_a difference should be small.

In order to determine the difference in E_a, we estimated the E_a using the data from the two test temperatures of 300 and 325 °C. This E_a can be viewed as the mean E_a in the temperature range of 300–325 °C. The E_a values obtained are 0.48 and 0.52 eV for the narrow and wide line/via structures, respectively. Hence, the difference in E_a is only 0.04 eV, which is indeed small as expected. From the E_a values calculated, one can see that the failure is interfacial diffusion dominated [4], [5].

Note here that the test data from 350 °C is not used for the above-mentioned calculation of E_a because its σ value is too much difference from that at 300 °C. Hence, its inclusion in the average E_a computation could render a large error.

The E_a of around 0.5 eV might indicate poor copper process. However, for the M2 test structures fabricated together with the M 1 test structures studied in this work, the EM failure data of the M2 test structures show an activation energy of 0.85 and 0.88 eV for the narrow and wide line/via, respectively. Thus the activation energy in this case is within 0.8–1.0 eV, characteristic of a robust copper processes [4], [5]. Hence the low value of E_a in the M1 test failure should not be taken as an indication of the poor copper process, instead it represents a different physical mechanism underlying the electromigration processes.

B. Atomic Flux Divergence (AFD) Distribution

As AFD is the basic element for void mechanic in EM, we studied the AFD distribution in detail. To study the AFDs due to various driving forces under consideration, we compute the distribution of the AFD over the portion of the structure from the via zone to M1 line 0.5 μm away from the via zone. The AFD will be expected to be maximum around the via zone, and minimum along the M1 line far away from the zone. It is found that the distribution is the same if it is beyond 0.5 μm from the via zone in M1 line.

From the simulation, the contribution of AFD due to TM was found to be negligible (5 order less) as compared to the AFD contributions due to EWM and SM. This is consistent with the report made recently by Nguyen *et al.* [27].

As an example, the AFD distribution due to EWM and SM at test temperature of 325 °C for the case of wide line/via are shown in Figs. 6 and 7, respectively. One can note that the maximum (positive) AFD zones for both the EWM and SM are the

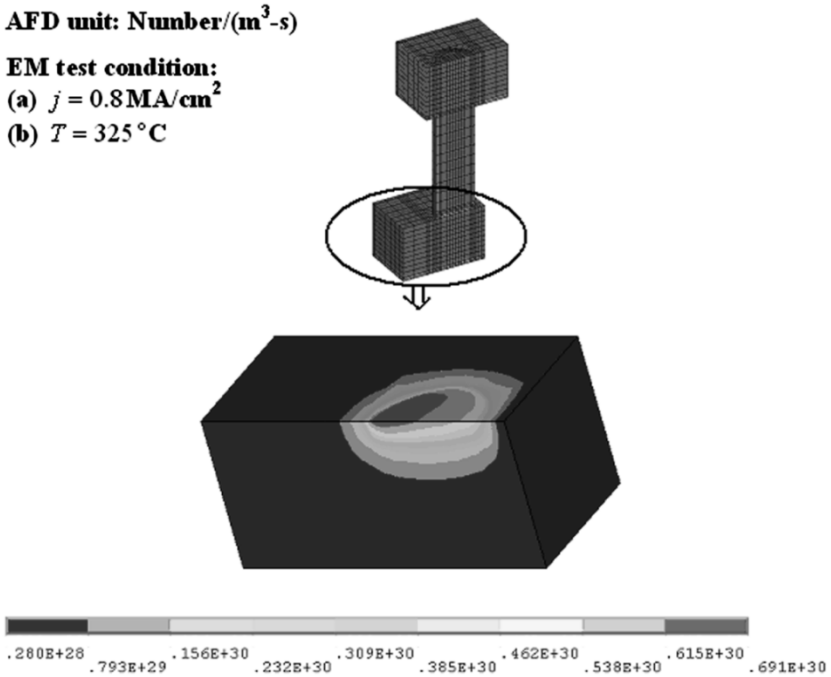

Fig. 6. AFD distribution due to the EWM.

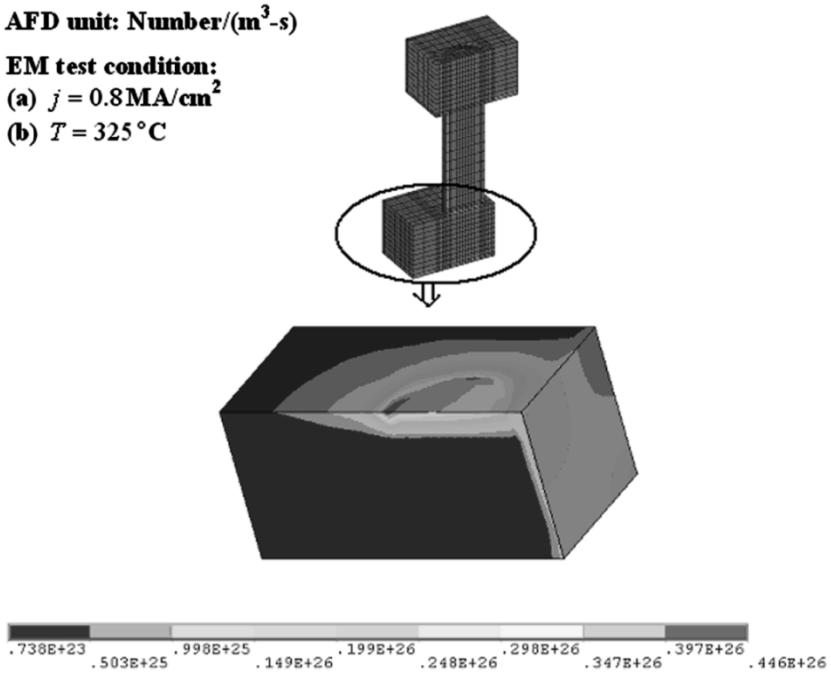

Fig. 7. AFD distribution due to the SM.

same, and they coincide with the failure zone as found in the experiments. The AFD distributions due to EWM and SM are shown in Fig. 8. From this figure, it is clear that the contribution due to SM increases with increasing test temperature. This probably explain the difference in the *log-normal* σ observed at different test temperatures.

It can also be noted that the SM contribution to the total AFD is much higher in case of wide line/via compared to that in the narrow line/via. This is because at the same current density, more heat will be generated which will increase the temperature in the case of wide line/via compared to narrow line/via, causing larger degree of nonuniformity in the stress distribution in the structure in the case of wide line/via.

It is also to be noted here that only qualitative information can be drawn from this static AFD calculation [28]. In reality, during the void growth, AFD will vary, and hence quantitative conclusion can be made only with dynamic model, and this is beyond the scope of the present work.

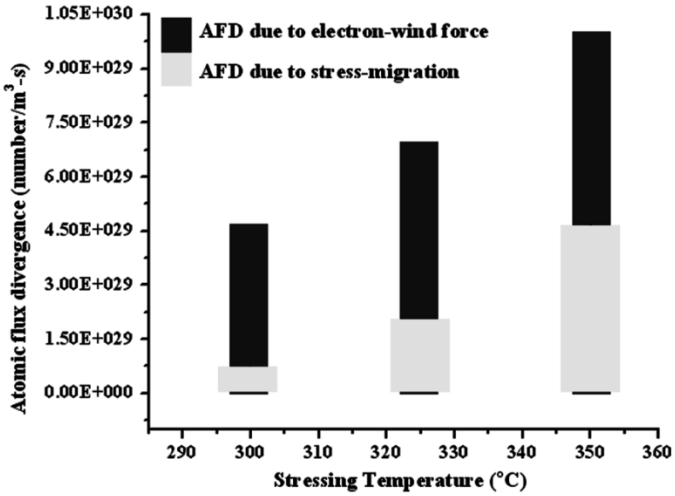

Fig. 8. AFD distributions at three EM test temperatures.

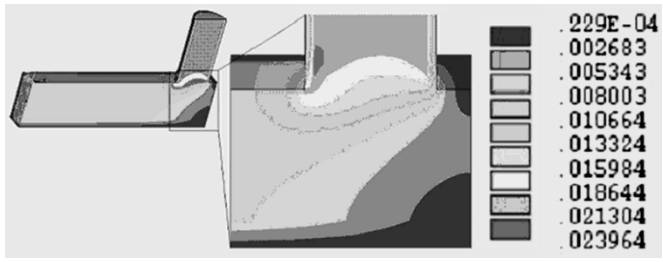

Fig. 9. Current density contour plots for the narrow line/via.

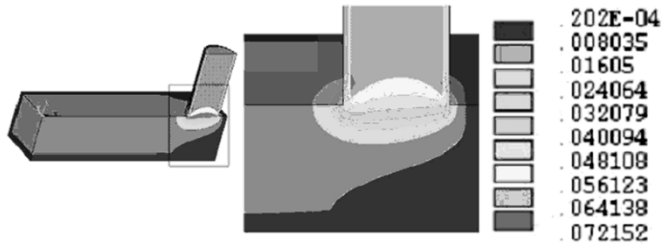

Fig. 10. Current density contour plots for the wide line/via.

C. Via Bottom Current Density Dependency

From the above discussion, one concludes that the EM process was mainly governed by EWM up to the test temperature of 325 °C for the EM test structures under investigation. Therefore, the "current crowing effect" in the line/via structure must be taken into account to understand the MTF behavior of the structures since MTF is inversely proportional to AFD [8], [29].

To ensure the same electron-wind driving force, which is proportional to applied current density rather than the current, both the structures were tested with the same line current density, though the total current in the wide line/via will be 2.5 times of that in the narrow line/via at the same current density level. The EM reliability of the two interconnect structures at service condition with same current can be estimated by extrapolating the EM test data using reliability statistics [30]. Such extrapolation is however beyond the scope of this work.

The via bottom has been identified experimentally as the failure location for both narrow and wide line/via structures at the Cu/Ta or Cu/SiN interfaces in the M1 line. As can be seen in Figs. 9 and 10, the magnitudes of the average current densities along the interfaces of Cu/Ta and Cu/SiN near the via bottom for both structures depend on the line width. It can be computed that the average current density for the narrow line/via (Fig. 9) is 1.7 times the current density in the M1 line, and it is 4.9 times the M1 current density in case of wide line/via (Fig. 10).

The higher ratio of the average current density along the interfaces mentioned above for the wide line/via structure can be understood as follows. As the line current density is the same for both cases, the total current is higher in the wide line/via structure. However, the via diameter is the same for all the test structures, and thus the current is much crowded in the wide line/via structure. This renders the average current density having a higher ratio over the current density in M1 line, and making the current crowed zone more vulnerable to failure.

Under such a high current density, it is reasonable to assume that Cu/Ta or Cu/SiN interfaces are the dominant diffusion path. The average activation energies found earlier do suggest that the Cu interface/surface is indeed the dominant diffusion path.

On the other hand, since the thickness of Ta barrier is 25 nm in our experiments, it is adequate to act as a perfect blocking boundary to the Cu atom flow [31]. Thus, the interface diffusion can only occur at the interface between M1 line and the cap layer near the via zone or at the interface between M1 line and Ta via bottom barrier, and the failure is in essence a line electromigration failure.

The t_{50} of line EM is given by the width dependence Black's equation [32] as follows:

$$t_{50} = BWj^{-n}\exp\left(\frac{E_a}{kT}\right) \tag{1}$$

where B is a constant depending on the material, failure criteria etc., W is the line width, j is the current density, E_a is the activation energy and n is the current density exponent. It is generally agreed that electromigration failure that is controlled by the nucleation of void should yield $n = 2$ [33], and for the case of "downstream" stressing (i.e., the direction of electron flow is same with the present case) in Cu damascene line/via structure, it was reported that the value of n is between 1.87 to 2.01 [26].

Therefore, the ratio of t_{50} for narrow to wide line/via structure is given by

$$\frac{t_{50}^{\text{narrow}}}{t_{50}^{\text{wide}}} = \left(\frac{W^{\text{narrow}}}{W^{\text{wide}}}\right)\left(\frac{j_{\text{int}}^{\text{narrow}}}{j_{\text{int}}^{\text{wide}}}\right)^{-n}\exp\left(\frac{\Delta E_a}{kT}\right) \tag{2}$$

where the superscripts *narrow* and *wide* correspond to the narrow and wide line/via, respectively. The subscript *int* refers to the interface current density at the line/via bottom interface, and ΔE_a is the difference in activation energies of the narrow and wide line/via structures which is found to be -0.04 eV as computed previously.

In order to estimate n, (2) was evaluated using the simulated current density at test temperature at 300 °C with n varying from 1.8 to 2.0. It is found that $n = 1.9$ for the t_{50} ratio in (2) to agrees well with our experimental data, and this value of n is well within the reported value [26]. With this value of n, we computed the t_{50} ratio at other test temperatures, and the results

are summarized in Table I. One can see an excellent agreement between the simulation and experimental results.

On the other hand, if the t_{50} ratio using (2) is computed without considering the current crowding, we will have the factor $(j_{\rm int}^{\rm narrow}/j_{\rm int}^{\rm wide})^{-n}$ equal to 1 as line current densities are the same for both the structures. For the case where the test temperature is 325 °C, the MTF ratio will be 0.18 which is far from the experimental observation. Hence, this study implies that the uniform line current density cannot be used to estimate the MTF of via EM, and indeed the current crowding effect affect the MTF significantly. The average current density along the interface at line/via bottom should be used to compute the MTF of the via bottom EM failure for the line/via structure.

V. Conclusion

Current crowding is found to be a dominant factor in via bottom failure for deep submicron Cu interconnects via structure. The failure time for wide line/via has been found to be shorter as compared to narrow line/via at identical EM test condition due to the effect of current crowding. From our 3-D finite element analyses, it is shown that the stress induced migration cannot be ignored at high test temperature, which is 350 °C in this work. The increasing contribution of stress induced migration in the EM process probably explains the decrease in *log-normal* σ with increasing test temperature.

The uniform line current density is found to be inappropriate for the estimation of MTF of EM in the line/via structure, but the width dependence Black's equation with average current density along the line/via interface provides an excellent approximation for the MTF.

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