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Current-driven magnetic domain-wall logic

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Spin-based logic architectures provide nonvolatile data retention, near-zero leakage, and scalability, extending the technology roadmap beyond complementary metal–oxide–semiconductor (CMOS) logic[1-13]. Architectures based on magnetic domain-walls take advantage of fast domain-wall motion, high density, non-volatility, and flexible design in order to process and store information[1,3,14-16]. Such schemes, however, rely on domain-wall manipulation and clocking using an external magnetic field, which limits their implementation in dense, large scale chips. Here we demonstrate a concept to perform all-electric logic operations and cascading in domain-wall racetracks. We exploit the chiral coupling between neighbouring magnetic domains induced by the interfacial Dzyaloshinskii–Moriya interaction[17-20] to realize a domain-wall inverter, the essential basic building block in all implementations of Boolean logic. We then fabricate reconfigurable NAND and NOR logic gates, and perform operations with current-induced domain-wall motion. Finally, we cascade several NAND gates to build XOR and full adder gates, demonstrating electrical control of magnetic data and device interconnection in logic circuits. Our work provides a viable platform for scalable all-electric magnetic logic, paving the way for memory-in-logic applications.

Our concept for chiral magnetic domain-wall (DW) logic takes advantage of the efficiency and speed of magnetic DW motion induced by spin-orbit torques (SOTs)[16,21-27] and exploits the chiral coupling between adjacent magnets with competing magnetic anisotropy and interfacial Dzyaloshinskii–Moriya interaction (DMI)[17-20] (Fig. 1a). Based on this coupling, we demonstrate that it is possible to invert a DW using an electric current, namely to transform an up/down (⊙|⊗) DW into a down/up (⊗|⊙) DW or vice versa. Here, the magnetization directions of ⊗ and ⊙ in the racetrack represent the Boolean logic "1" and "0", respectively. In Fig. 1b, we illustrate the design of a DW inverter, which consists of an in-plane (IP) magnetized region embedded in a racetrack with out-of-plane (OOP) magnetization. As the two OOP regions on either side of the IP region are coupled by the DMI, the reversal of one OOP region induces the reversal of the other, leading to the inversion of a DW travelling along the racetrack, which is equivalent to a NOT gate.

In order to demonstrate the operation of the DW inverter, we fabricated a set of OOP magnetic nanowires of Pt/Co/AlO_x with 50 nm-wide V-shaped IP regions patterned using a selective oxidation process (Fig. 2a and Extended Data Fig. 1). The DW motion is driven by an electric current (Fig. 2b) and tracked with polar magneto-optic Kerr effect (MOKE) microscopy. Starting from the initial down-right-up magnetization configuration of the OOP-IP-OOP structure (⊗→⊙), an ⊙|⊗ DW is injected from the left OOP region (Fig. 2c). By applying a sequence of current pulses, the ⊙|⊗ DW moves in the direction of the current towards the IP region, as expected for a left-handed chiral Néel DW[22-24]. When the ⊙|⊗ DW encounters the IP region, the IP magnetization switches from → to ←, accompanied by the annihilation of the DW to the left of the IP region and nucleation of a new DW with opposite polarity to the right of the IP region. Insight into the microscopic mechanism of the DW inversion is provided by the combination of scanning transmission x-ray microscopy (STXM) and micromagnetic simulations (Fig. 2d and Supplementary Fig. 1 and 2). As the incident ⊙|⊗ DW approaches the IP region, it is compressed against the IP region by the SOTs and this in turn increases both the magnetostatic and exchange energies. The resulting compact, high-energy spin texture[28] can only be unwound by annihilating the incident DW and switching the IP magnetization with the help of SOTs. Upon switching of the IP magnetization from → to ←, an ⊙ domain nucleates on the right side of the IP region due to the

chiral coupling. This process is promoted at the tip of the V-shaped inverter due to the additive contribution of chiral coupling from both sides of the V-shaped region. Therefore, the optimized design of the narrow V-shaped IP region facilitates the switching of the IP magnetization and the nucleation of a new domain (Extended Data Fig. 2). As a result, the ⊙|⊗ DW is effectively transmitted through the IP region and transformed into a ⊗|⊙ DW. An analogous inversion process occurs for an incident ⊗|⊙ DW (see Extended Data Fig. 3), so that the inverter effectively reverses the magnetization of domains travelling across the IP region, as shown in Fig. 2e. Not only is it possible to invert a single DW with an electric current, but also a sequence of DWs and, consequently, a sequence of domains that propagate along a racetrack. This is a unique feature of chirally coupled nanomagnetic structures.

Building on the principles used to construct the NOT gate, we now demonstrate how to realize a reconfigurable NAND/NOR gate. This gate makes our concept for current-driven DW logic functionally complete, as any Boolean function can be implemented using a combination of NAND or NOR gates. The core structure of this gate (Fig. 3a) is composed of four OOP regions (in red) that form two logic inputs, one bias and one logic output connected via IP regions (in blue). To illustrate the functionality of the NAND gate, we fabricated four devices with the same core structure and different logic input configurations. For each device, two DW reservoirs are connected to the inputs via racetracks. The four logic input configurations of "11", "10", "01" and "00" are achieved by placing inverters after some of the DW reservoirs. The two DW reservoirs and the bias are set to logic "0" by applying an OOP magnetic field of 1 kOe. Applying current pulses, ⊗ (⊙) magnetic domains propagate from the DW reservoirs with (without) inverters, defining the logic inputs to be "1" ("0"). As a result of the chiral coupling[20], the output magnetization depends on the relative alignments of the inputs and the bias (Fig. 3b and 3c), which is analogous to a majority gate[4,8,9]. Therefore, for an ⊙ bias, the output magnetization switches to ⊙ only when both of the input magnetizations are ⊗. Otherwise, the output magnetization is ⊗. As shown in the magnetic force microscopy (MFM) images (Fig. 3d), the magnetization direction of the logic output is ⊙ ("0") for logic inputs of "11", and ⊗ ("1") for logic inputs of "10", "01" and "00". This relationship between the logic inputs and the output corresponds to the required logic operations for a NAND

gate (Fig. 3c). By changing the orientation of the bias to ⊗, as shown in Fig. 3e, we can reconfigure the NAND gate into a NOR gate. In the latter case, the output magnetization is ⊗ only when both of the input magnetizations are ⊙. Hence, our logic gate can be reconfigured between NAND and NOR by switching the bias terminal, allowing for rapid logic reconfiguration during run time[2,10].

We now demonstrate the operation of a single NAND gate using current-driven DW motion to provide a series of different logic inputs to the same gate over time (Fig. 3f). In this device, we place three DW inverters in the left-hand racetrack and two DW inverters in the right-hand racetrack. This means that a sequence of current pulses will generate a sequence of logic inputs going from "00" to "11" to "01" to "11" to "10". The corresponding logic outputs will then change from "1" to "0" to "1" to "0" to "1", respectively, over time. For each operation, the DWs that give the two inputs may not arrive at the gate at the same time. We can mitigate this by introducing a sufficient propagation delay time (see Methods). In a real device, this can be achieved by clocking the electric current. Furthermore, it would be possible to control the logic inputs and bias terminals with magnetic tunnel junctions (MTJs) fabricated on the magnetic racetracks, which can also be used for electrical read out of the outputs[29] (see Methods).

In addition to forming a complete logic set, chiral DW racetracks fulfil three additional requirements for practical implementation in logic circuits, namely input selectivity, data cross-over, and cascading of different logic gates. With current-driven DW propagation through the Y-shape structure in Fig. 4a, it is possible to electrically select the logic input. A simple cross structure allows DWs to propagate in orthogonal racetracks (Fig. 4b and Extended Data Fig. 4), which simplifies the design of cross-overs, avoiding the complexity of metal bridges used in conventional charge-based circuits. Moreover, since our logic inputs and outputs are based on the same physical phenomena, several logic gates can be directly cascaded without the need for additional transducers between magnetic and electric signals (Extended Data Fig. 5). As examples, we present in Fig. 4c a binary half adder created by cascading four NAND gates to form an XOR gate and further show the full adder operation by cascading 15 NAND gates in Fig. 4d. This circuit also demonstrates the possibility for fan-out of a single output that can be used to drive the input of the next logic gates. A remaining challenge is to create magnetic logic circuits with feedback loops. This could be

realized either using an external electrical circuit to read the output and write this back to the input with MTJs or using an additional racetrack with inverted current direction to drive DWs from the output back to the input.

For device applications, the scalability and efficiency of magnetic DW logic circuits should also be addressed. Because the chiral coupling induced by the DMI is effective at the scale of the magnetic moments, it should be possible to scale the size of the logic gates down to a few nm using advanced lithography techniques. The speed of the logic operations is related to the DW velocity, which can reach several hundreds of m/s for chiral DWs driven by SOTs[21-24]. The operation time can be estimated from the time required for a DW to transfer across the gate that, for an inverter scaled down to 10×10 nm^2, can be as fast as a few tens of ps (see Methods). The energy consumption of a single NOT operation in our 0.8×1 μm^2 racetracks is about 20 pJ, which would scale down to sub-20 aJ in structures with a 10×10 nm^2 footprint (see Methods). The nonvolatility of the magnetic inputs and outputs gives further energy savings since magnetic DW logic circuits do not consume power when idle and do not need reloading of data after power-off. These features make all-electric magnetic DW logic attractive for use in low power, "instant-on" microelectronic processors that are ubiquitous in modern-day electronics.

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Figure legends:

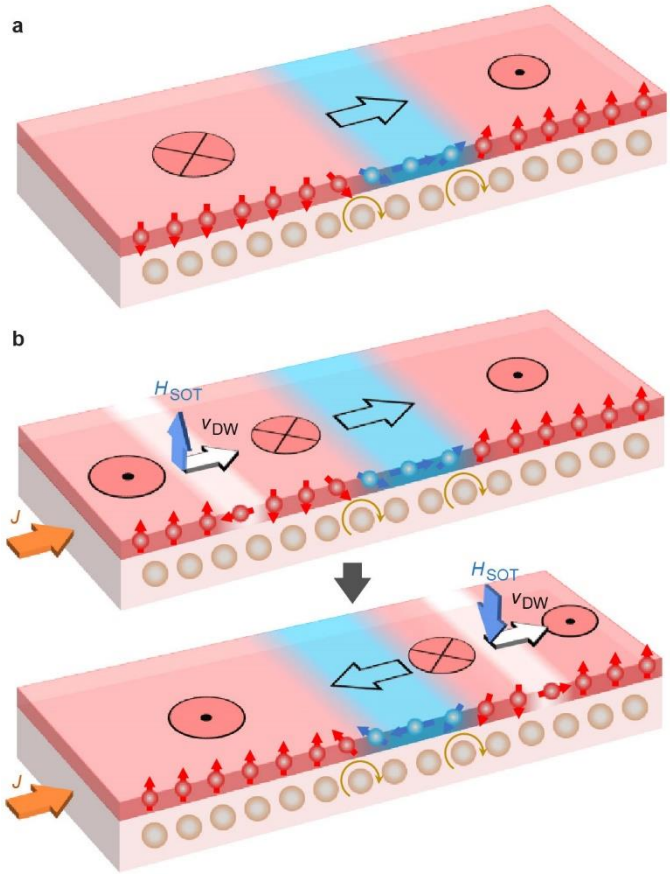


Figure 1 | Chiral coupling between adjacent nanomagnets and current-driven DW inversion. **a**, Schematic of magnetic chiral coupling induced by DMI. After selective oxidization, the magnetization of neighbouring OOP (oxidized, red shaded) and IP (unoxidized, blue shaded) regions are aligned with a left-handed chirality in Pt/Co/AlO_x. **b**, Schematic showing current-driven DW inversion, which occurs as the DW transfers across the IP region. The white shaded region is the DW, and the direction of the effective field induced by the SOTs, H_{SOT}, and the DW velocity, v_{DW}, are indicated with arrows. In Pt/Co/AlO_x, both ⊙|⊗ and ⊗|⊙ DWs move in the same direction as the electric current J.

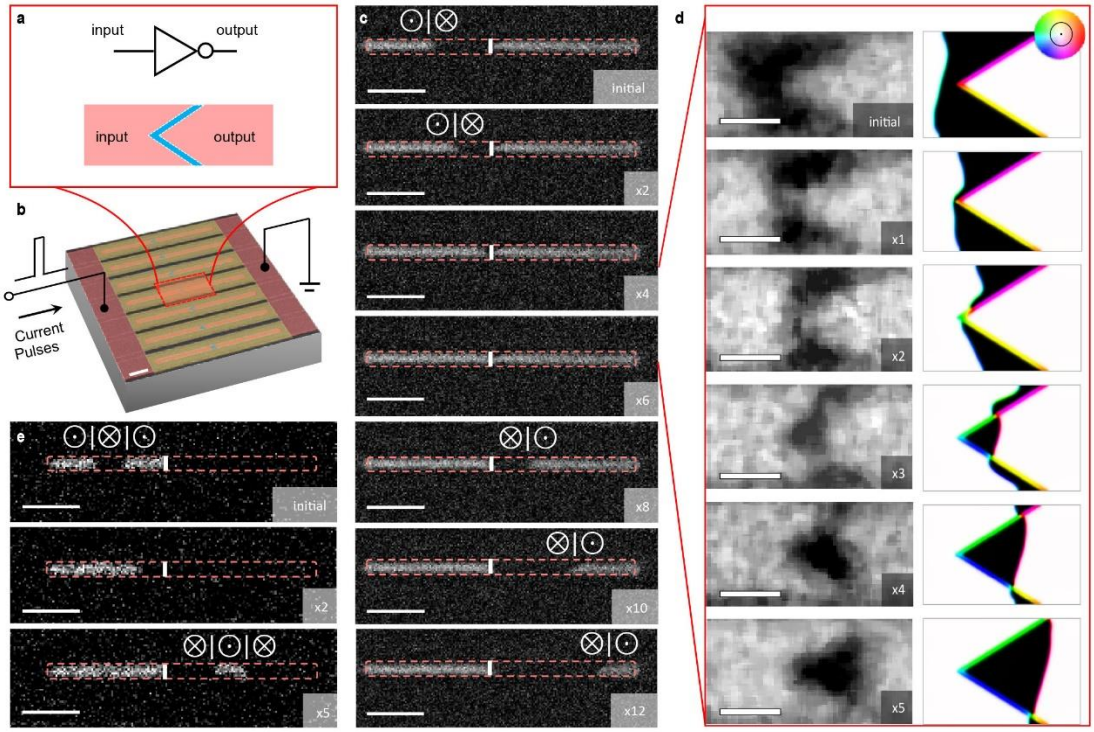


Figure 2 | Current-driven DW inverter. a, Schematics of a NOT gate and current-driven DW inverter. Red and blue shaded regions indicate regions with OOP and IP anisotropies, respectively. **b,** Coloured SEM image of seven parallel DW inverters in a 3D rendering of the DW measurement setup. The direction of the current pulses is indicated. **c**, MOKE image sequence of DW inversion for a DW incident from the left with an ⊙|⊗ configuration. The edges of the magnetic racetracks are indicated by red dashed lines and the positions of the inverters are indicated by white lines. The bright and dark contrasts in the racetracks in the MOKE images correspond to ⊙ and ⊗ magnetization, respectively. The entire image sequence for seven inverters is shown in Supplementary Video 1. **d,** XMCD image sequence of DW inversion for an incident DW with an ⊙|⊗ configuration measured by STXM. Each image is captured after the application of one current pulse. The bright and dark contrasts in the XMCD images correspond to ⊙ and ⊗ magnetization, respectively. Micromagnetic simulations of the inversion process are shown to the right of each image, with the directions of the magnetization indicated by the colour wheel. The entire image sequence is shown in Supplementary Video 2. **e**, MOKE images showing the inversion of a ⊗ domain driven across the IP region with current pulses. The entire image sequence is shown in Supplementary Video 3. The current density and duration of the pulses applied in **c** and **e** are 7.5×10^{11} A/m^2 and 50 ns, while for **d** they are 1.1×10^{12} A/m^2 and 1 ns. The scale bars are 3 µm in the MOKE images and 500 nm for the XMCD and simulation images.

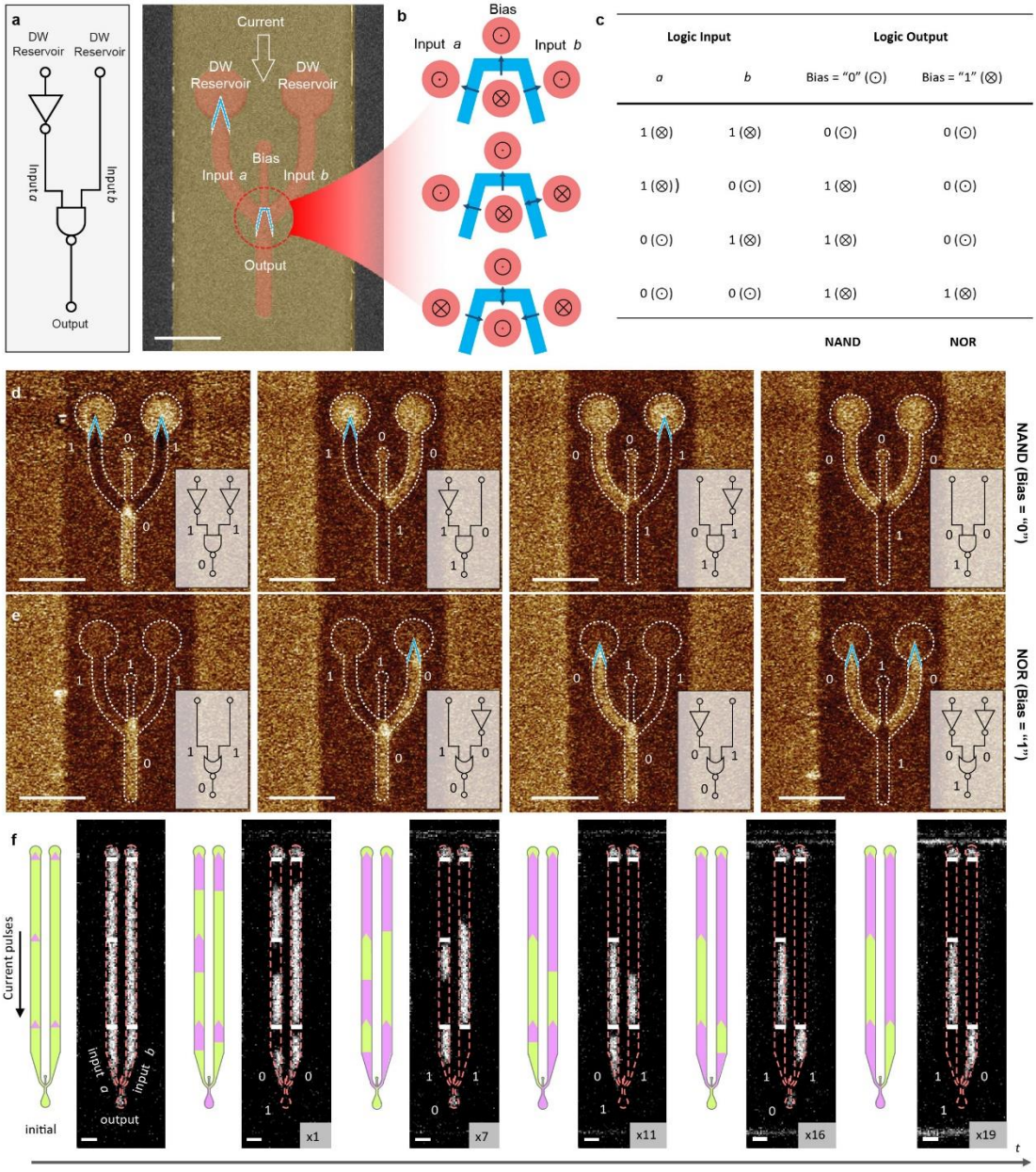


Figure 3 | Reconfigurable NAND/NOR logic gates. a, Coloured SEM image of a reconfigurable NAND/NOR logic gate and corresponding logic circuit symbol. Red, blue, and yellow colours indicate regions in the logic gate with OOP and IP magnetic anisotropies, and the Pt strip, respectively. **b,** Schematics of the relationship between the magnetization in the two logic inputs, the bias, and the logic output for the NAND gate. **c**, Truth table for the reconfigurable NAND and NOR logic operations. **d** and **e**, MFM images of different logic operations for inputs of "11", "10", "01" and "00" with a bias of "0" (**d**) and "1" (**e**), and their corresponding logic circuit symbol. The DW reservoirs (circular pads at the top of each image) and the bias are set to logic "0" by applying an OOP magnetic field of 1 kOe. **f,** MOKE image sequence and corresponding schematics showing the operation of a single NAND gate with a sequence of logic inputs driven by the electric current. The initial magnetization is set to be ⊙ by applying an OOP magnetic field of 1 kOe. Green and purple in the schematic correspond to ⊙ and ⊗ magnetization, respectively. The boundaries of the logic gate are indicated by red dashed lines and the positions of the inverters are indicated by white

lines. The direction and the number of current pulses applied before each MOKE image are indicated (current density 7.5×10^{11} A/m^2 and pulse length 30 ns). The entire image sequence is shown in the Supplementary Video 5. The bright and dark contrast in the device regions in the MFM and MOKE images corresponds to ⊙ and ⊗ magnetization, respectively. All the scale bars are 1 μm.

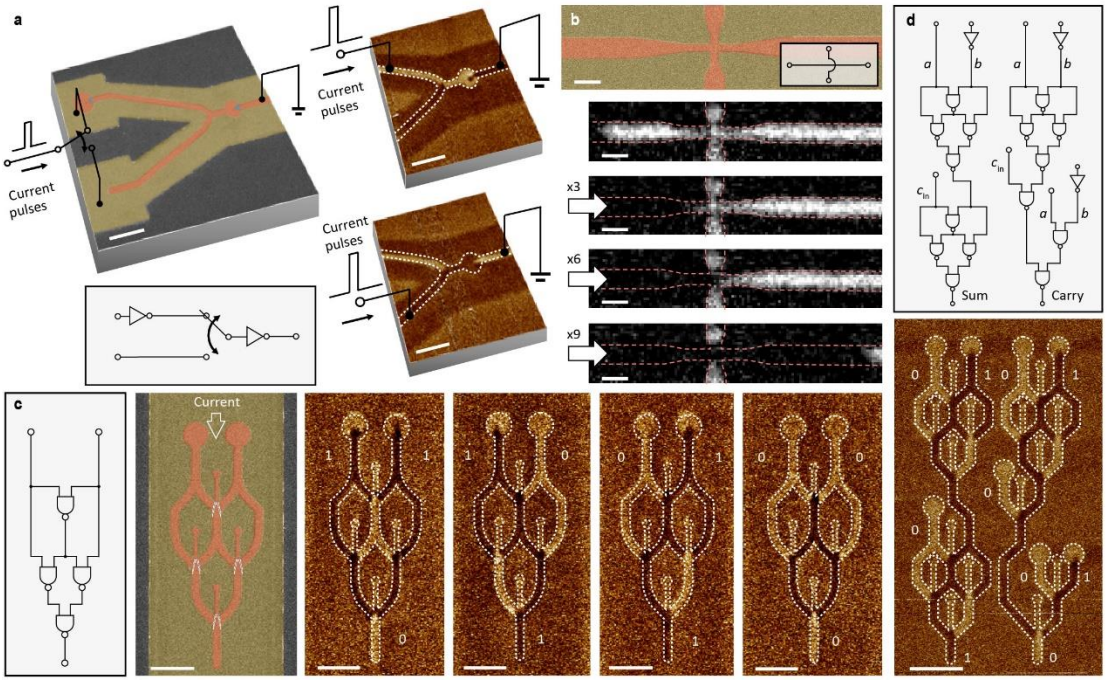


Figure 4 | Electrical control of data flow and cascaded DW logic circuits. a, Data flow switch through a Y-shaped structure. Left: Coloured SEM image of the device and corresponding logic circuit symbol. Right: MFM images of the magnetic configuration when current flows through the upper racetrack (top) and lower racetrack (bottom). **b,** Sequence of MOKE images illustrating electrical control of data flow through a cross structure. The direction and number of current pulses are indicated (current density 9×10^{11} A/m^2 and pulse length 30 ns). A coloured SEM image of the cross structure and the corresponding logic circuit symbol are shown at the top. The entire image sequence is shown in Supplementary Video 6. **c**, XOR gate fabricated by cascading four NAND gates. Left: coloured SEM image of the XOR logic gate and corresponding logic circuit symbol. Right: MFM images of the XOR logic gate with different logic inputs of "11", "10", "01" and "00". The DW reservoirs and the bias are set to logic "0" by applying an OOP magnetic field of 1 kOe. Red, blue, and yellow colours in the SEM images represent the regions with OOP and IP magnetization, and the Pt strips, respectively. **d,** Full adder gate. Top: logic circuit symbol of the full adder with input operands of "a =0", "b =1", and a carry bit of "c_{in} =1". Bottom: MFM image of the full adder magnetic circuit. The bright and dark contrast in the device regions in the MOKE and MFM images correspond to ⊙ and ⊗ magnetization, respectively. All the scale bars are 1 μm.

Methods

Device fabrication

The magnetic films were deposited on a 200 nm-thick SiN_x layer on a silicon substrate using dc magnetron sputtering at a base pressure < 2×10^{-8} Torr and a deposition Ar pressure of 3 mTorr, and patterning was carried out by electron-beam lithography. Continuous films of Pt (5 nm)/Co (1.6 nm)/Al (2 nm) were milled into strips with Ar ions through a negative resist (ma-N2401) mask. In these magnetic strips, the upper Co/Al bilayer was milled through a high-resolution positive resist (PMMA) mask to create the DW racetracks and logic devices. In order to define the IP region in these magnetic structures, a second PMMA mask was patterned by electron-beam lithography on top of the Al layer. Using a low power (30 W) oxygen plasma at an oxygen pressure of 10 mTorr, the unprotected Al layer was oxidized to induce perpendicular magnetic anisotropy in the Co layer. Finally, electrodes of Cr (5 nm)/Au (50 nm) were fabricated using electron-beam lithography combining electron-beam evaporation with a lift-off process. The main steps of the device fabrication are shown in Extended Data Fig. 1a.

The different anisotropies, with OOP regions (exposed to oxygen plasma) and IP regions (protected with the PMMA mask), were confirmed with polar MOKE measurements (Extended Data Fig. 1b). The effective OOP magnetic anisotropy field is 3.94 kOe obtained from anomalous Hall effect measurements with an applied IP magnetic field (Extended Data Fig. 1c). The interfacial DMI constant D was estimated to be -0.9±0.1 mJ/m^2 by measuring the DMI-induced chiral coupling[20].

Electrical measurement configuration

The magnetic DW motion and logic operation are driven by the current pulses generated with a HP Agilent 8114A high voltage pulse generator and AVTECH ultra-high speed pulse generator. The pulse generators can provide pulses of variable voltage and pulse width. The current densities are calculated by dividing the nominal voltage by the device resistance and cross sectional area, and are indicated for each operation. The directions of the current pulses are depicted for each device and summarized in Extended Data Fig. 6.

MFM measurements

The MFM measurements were performed using a Bruker Dimension Icon Scanning Station mounted on a vibration and sound isolation table using tips coated with CoCr. In order to minimize the influence of the stray field from the MFM tip during the measurements, a thin PMMA layer (~20 nm) was spin coated on the samples to increase the distance between the tip and the magnetic film.

MOKE microscopy measurements

The MOKE images were recorded using a custom-built wide-field MOKE microscope. The background image was captured after the application of a large positive OOP magnetic field of 1 kOe. The background image was subtracted from the subsequent images to achieve differential images with magnetic contrast. To prepare the initial state of the DWs shown in Fig. 2c, the racetrack was first saturated with an OOP magnetic field. The magnetic field was removed leaving the racetrack magnetized OOP, with a small reversed region at the V-shaped IP region resulting from the chiral coupling[20]. Then current pulses were applied in the opposite direction to that shown in Fig. 2b in order to create a single DW on the left side of the DW inverter (Fig. 2c).

STXM measurements

The magnetic configuration of the DW inverter was imaged using scanning transmission x-ray microscopy at the PolLux beamline of the Swiss Light Source. The magnetization state was probed exploiting x-ray magnetic circular dichroism (XMCD) at the Co L_3 absorption edge at normal incidence. The devices measured using STXM were fabricated on x-ray transparent SiN_x membranes.

Micromagnetic simulations

In order to understand the mechanism of the DW inversion, micromagnetic simulations were carried out with the MuMax^3 code[30] using a computation box containing 2048×1024×1 cells with a

2×2×1.6 nm^3 discretization using the following magnetic parameters: saturation magnetization M_S = 0.9 MA/m, effective OOP anisotropy field H_{eff} = 150 mT, exchange constant A = 16 pJ/m, spin Hall angle of Pt θ_{sh} = 0.1, and interfacial DMI constant D = -1.5 mJ/m^2.

Mechanism for DW inversion

In order to elucidate the basic mechanism behind DW inversion in an OOP-IP-OOP structure, we consider a simple model. The DW inversion process can be explained in terms of the effective DMI field generated in non-collinear magnets where the DMI vector lies in the plane of the magnetic thin film. This effective DMI field is given by:

$$\vec{H}_{\mathrm{DMI}} = \frac{2D}{\mu_0 M_{\mathrm{S}}}\left(\frac{\partial m_z}{\partial x}, 0, -\frac{\partial m_x}{\partial x}\right), \tag{1}$$

We can then consider a situation where an ⊙|⊗ DW is driven by SOTs towards the IP magnetized region (see Supplementary Fig. 1a). At equilibrium, the IP magnetized region together with the surrounding domains forms a ⊗→⊙ configuration, which is stabilized by the DMI fields (pointing along +x) indicated by H_{DMI}(IP). On applying an electric current, the magnetization is subject to an effective field $\boldsymbol{H}_{\mathrm{SOT}}$ induced by the SOTs, which is given by:

$$\vec{H}_{\mathrm{SOT}} = \frac{\hbar \theta_{\mathrm{SH}} J}{2\mu_0 e M_{\mathrm{S}} t}\vec{m}\times\vec{\sigma}, \tag{2}$$

where $\hbar$, θ_{SH}, J, e, M_s, t, $\boldsymbol{m}$ and $\boldsymbol{\sigma}$ are the Planck constant, spin Hall angle, electric current density, electron charge, saturation magnetization, thickness of magnetic layer, direction of magnetization and direction of spin polarization at the Pt/Co interface. Due to the chiral coupling, the magnetization in the middle of ⊙|⊗ DW points along -x (in blue). As shown in Supplementary Fig. 1b, the $\boldsymbol{H}_{\mathrm{SOT}}$(DW) points along +$z$ so that the ⊙|⊗ DW will propagate along the current direction. As soon as the ⊙|⊗ DW approaches the IP region, the magnetization in the IP region experiences a dipolar field $\boldsymbol{H}_{\mathrm{dip}}$(IP) generated by the IP magnetization of the ⊙|⊗ DW that points along -x. The SOTs also compress the incident DW against the IP region and this in turn increases the DW energy. This results in a compact, high-energy spin texture containing two closely spaced regions with tail-to-tail IP magnetization as shown with the associated magnetic charges in

Supplementary Fig. 1b: one IP magnetization region is in the middle of the ⊙|⊗ DW with magnetization pointing along –x (in blue), and the other IP magnetization region is in the inverter and has magnetization pointing along +*x* (in red). At a certain point in time, the dipolar field becomes strong enough to switch the magnetization in the IP region from +*x* to -*x* with the help of SOTs (Supplementary Fig. 1b and 1c). Simultaneously, the high-energy spin texture on the left side of the IP region collapses, bringing about the annihilation of the ⊗ domain on the left hand side of the IP region shown in grey in Supplementary Fig. 1b. After the reversal of the magnetization in the IP region, a reverse ⊗ domain is nucleated on the right side of the IP region (shown in grey in Supplementary Fig. 1c) as a consequence of the $\boldsymbol{H}_{\mathrm{DMI}}$(OOP) pointing along –*z*. The magnetization points along +*x* in the middle of the resulting ⊗|⊙ DW and the $\boldsymbol{H}_{\mathrm{SOT}}$(DW) points along –*z* so that this new DW is then transported by the electric current towards +*x* (Supplementary Fig. 1c).

While this simple model provides insight into the mechanism for DW inversion, the detailed magnetization dynamics is more complex. We have therefore performed micromagnetic simulations. Here, an ⊙|⊗ DW is driven by an electric current with current density 3×10^{12} A/m^2 in a narrow wire containing a straight, 30 nm - wide IP region (Supplementary Fig. 2a). The OOP anisotropy field was set to H_{k}= 1.5 kOe in the OOP region and set to zero in the IP region. All three components of the magnetization were recorded at three different positions along the wire: in the center of the IP region, and 30 nm away from the center on each side (see the dots in Supplementary Fig. 2a). We show in Fig. S2b to d how the magnetization responds to the approaching DW. As the ⊙|⊗ DW approaches the left side of the IP region, the magnetization on the left side of the IP region reverses from -*z* to +*z* (see Supplementary Fig. 2b). The magnetization in the IP region reverses from +*x* to -*x* along the path shown in Supplementary Fig. 2c to reduce the energy associated with the accumulated magnetostatic charges (shown schematically in Supplementary Fig. 2c). The magnetization on the right side of the IP region is then forced to switch from +*z* to -*z* by the chiral coupling (see Supplementary Fig. 2d).

The DMI is critical in the realisation of current-driven DW inversion, not only to achieve current-driven DW motion, but also due to its role in the nucleation of the reverse domain. The role of DMI in current-driven DW motion has been studied elsewhere[22-24]. Here, we determine the role

of DMI in the DW inversion process with micromagnetic simulations by varying the DMI value and the OOP anisotropy in the IP region. The DMI-OOP anisotropy phase diagram for current-driven DW inversion is shown in Supplementary Fig. 3 for a current density of 3×10^{12} A/m^2 in a narrow wire containing a straight, 30 nm - wide IP region. For zero OOP anisotropy in the IP region, the DW can be inverted when D < -1 mJ/m^2. If the DMI is reduced, it does not provide sufficient chiral coupling to nucleate the reverse domain, so that the incident DW cannot be inverted. By introducing OOP anisotropy into the IP region, which is expected from a Pt/Co interface, the energy for the DW inversion is reduced and the DMI operational window increases.

In order to verify the impact of the IP width on the DW inversion process, we have performed additional micromagnetic simulations of the magnetization dynamics in the inverter for various widths of the IP region. The outcomes of the simulations for a current density of 3×10^{12} A/m^2 and D= -1.5 mJ/m^2 are given in Supplementary Table 1. Here a tick indicates that an inverted DW propagates from the IP region into the OOP region as required. If the IP region is too narrow (<25 nm), the OOP regions on either side of the inverter are strongly antiparallel coupled[20] and the SOTs induced by the current are not strong enough to overcome the chiral coupling. If the width of the IP region is too large (>35 nm), the chiral coupling becomes too weak to give an antiparallel coupling of the OOP magnetizations on the left and right sides of the IP magnetization[20]. The DW is then simply annihilated in the IP region without any further magnetization dynamics occurring on the other side of the inverter. The results of the micromagnetic simulations were confirmed by experiment: for a straight DW inverter in an 800 nm-wide racetrack, the DW was successfully transferred across a 50 nm-wide DW inverter but not across a 100 nm-wide inverter. As shown in Supplementary Table 1, it is possible to increase the operational window of the IP region by including a small OOP anisotropy in the IP region.

Influence of the shape of the IP region of the DW inverter

Here we compare experimentally the performance of straight and V-shaped DW inverters where the width of the IP region is 50 nm, beginning with the measurements of the straight IP inverter. As shown in the STXM images in Extended Data Fig. 2a, when the ⊗|⊙ DW encounters

the IP region, the DW will annihilate to the left of the IP region and a new DW with opposite polarity will be nucleated to the right of the IP region. We performed several inversion operations in the same inverter with a straight IP region and found that the reverse magnetic domains nucleate at different locations (Extended Data Fig. 2b). This implies that the nucleation of the reverse magnetic domain is assisted by the random thermal fluctuations or local inhomogeneities.

To improve the reliability of the DW inverter, we implemented a V-shaped IP region, which has two main advantages: Firstly, the tip of the V-shape offers an easy nucleation site for the reversed magnetic domain. This is because, at the tip of the V shape, the output OOP region is surrounded by the input OOP region, and experiences the strongest antiparallel chiral coupling. In the STXM measurements, we found that the nucleation of the reversed magnetic domain is located at the tip of the V-shape for five out of five operations. Secondly, the V-shape of the IP region leads to lower magnetostatic energy, so lowering the energy barrier for DW inversion. As shown in Extended Data Fig. 2c, we compared the effective DW velocity measured in DW inverters with a V-shaped and straight IP regions (see the method outlined in estimation of the speed of logic operation in Methods). The velocity of the DW transferring across the IP region in the V-shaped IP inverter is higher than that of the DW in straight IP inverter and the standard deviation of the velocity is smaller in the V-shaped IP inverter compared to that of the straight IP inverter. This demonstrates the higher efficiency and reliability of the V-shaped IP region as a DW inverter.

Estimation of the speed of logic operation

Here we estimate the speed of a logic operation in the NOT gates. First, the DW velocity, v_{DW}, in the uniform OOP region of the racetracks is measured. Then we determine the DW displacement, L_{DW}, from S_1 to S_2 across the NOT gate following N current pulses (see schematic in Extended Data Fig. 7). From this, we can obtain the time taken by the DW to transfer across the NOT gate, t_{NOT}, and therefore the effective velocity of the DW, v_{NOT}, as it transfers across the NOT gate and is inverted:

$$t_{NOT} = Nt_{pulse} - \frac{L_{DW} - L_{NOT}}{v_{DW}};\ v_{NOT} = \frac{L_{NOT}}{t_{NOT}}, \quad (3)$$

where t_{pulse} and L_{NOT} are the length of current pulse and length of the NOT gate, respectively. With this method, we can determine v_{DW} and v_{NOT} as a function of current density (Extended Data Fig. 7). The pulse length was decreased to 2 ns for high current densities to reduce heating, with the data given in the inset in Extended Data Fig. 7. We find that the velocity of the DW in the NOT gate can reach 160±17 m/s for a current density of 1.65×10^{12} A/m^2. This value of the DW velocity is used to estimate the energy consumption in the main manuscript.

Here, we estimate the time for the DW to transfer across the DW inverter with the dimensions indicated in Extended Data Fig. 6 scaled down to 10×10 nm^2. Taking the effective inverter DW velocity determined from the experiment of 160 m/s, the time for a DW to transfer across the downscaled inverter is ≈60 ps. For a more accurate estimation, we performed micromagnetic simulations for the downscaled inverter with dimensions 10×10 nm^2. At such a small scale, the device design is limited by the feature size that can be nanofabricated. Therefore, a straight IP region is considered instead of a V-shaped one, with a width of 10 nm. Taking the simulated effective inverter DW velocity of 118 m/s, the time for a DW to transfer across the inverter is 85 ps, which is similar to the rough estimation above. The speed of operation can be further improved by the optimization of the material to increase the DW velocity, e.g., by using an amorphous magnetic material such as CoFeB instead of Co, and device design.

Using a similar method for the DW inverter, we then estimate the speed of a logic operation in the NAND gate from experiment. For this, the operation of the NAND gate with two DW inverters in the input reservoirs was captured using MOKE imaging. Following the application of current pulses, DWs propagate through the NAND gate and perform logic operations (see MOKE images and corresponding schematics in Extended Data Fig. 8). From these images, we determine the time for the DW to transfer across the NAND gate to be t_{NAND} = 74.1 ns with an effective DW velocity of v_{NAND} = 10.8 m/s at a current density of 7.5×10^{11} A/m^2.

Synchronization and propagation delay times in the DW circuits

Due to the presence of defects that lead to pinning of the DWs and the intrinsic stochastic nature of current-driven DW motion, the arrival time of DWs at the logic gates can be different. In

electronic logic circuits, this is commonly addressed by introducing a propagation delay time for each operation, i.e., the circuits are cycled at a rate that is slower than the longest internal propagation delay times. The same concept of propagation delay time can be applied to our magnetic DW logic gates so that a stable output can be obtained that is independent of the arrival time of the input domains. In other words, with sufficient propagation delay time, all the DWs will arrive at the logic gate, which will result in the correct output for a given logic operation.

To demonstrate how the introduction of a propagation delay time can improve the gate operational reliability, we consider the simplest case of a NAND gate with the logic inputs changing from "00" to "11" over time. As schematically shown in Extended Data Fig. 9a, the arrival times of $\otimes|\odot$ DWs for logic inputs *a* and *b* are different. In this case, the change from "0" to "1" of input *a* is slower than that for input *b*, i.e., $t_a > t_b$, where t_i ($i = a, b$) is the time at which the inputs change. Once both DWs arrive at the gate, it will take some time for the nucleation of the reverse magnetic domain, which depends on the effective DW velocity in the NAND gate. The time after the correct magnetic domain propagates into the output racetrack is defined as the required propagation delay time t_{delay}. We fabricated NAND gates with "11" logic inputs with different input racetrack lengths to give different arrival times of the two logic inputs. On application of current pulses, a $\otimes|\odot$ DW propagates in both the left and the right input racetracks. This is the most critical configuration to test for the propagation delay time reliability of the logic gate. As shown in Extended Data Fig. 9b, all devices give the correct output "0", demonstrating that the output of the magnetic DW logic gate is independent of the difference in the arrival time of the input DWs.

For all logic operations in the NAND gate, in general, the operation includes (i) DW propagation in the input racetracks, (ii) DWs transfer across the logic gate and (iii) DW propagation in the output racetrack. The total operation time, and therefore the required propagation delay time, can then be expressed as:

$$t_{delay} = \frac{L_{input} + L_{output}}{v_{DW}} + \frac{L_{NAND}}{v_{NAND}}, \quad (4)$$

where L_{input}, L_{out}, and L_{NAND} are the length of input racetrack, output racetrack and NAND gate, respectively. v_{DW} and v_{NAND} are the DW velocities in the magnetic racetrack and NAND gate,

respectively. Assuming that the DW velocities in the magnetic racetrack and NAND gate have a normal distribution:

$$\begin{aligned} v_{\mathrm{DW}} &\sim N(\overline{v}_{\mathrm{DW}}, {\sigma_{\mathrm{DW}}}^2) \\ v_{\mathrm{NAND}} &\sim N(\overline{v}_{\mathrm{NAND}}, {\sigma_{\mathrm{NAND}}}^2) \end{aligned}, \tag{5}$$

where $\overline{v}_{\mathrm{DW}}$ ($\overline{v}_{\mathrm{NAND}}$) and σ_{DW} (σ_{NAND}) represent the average and standard deviation of the velocity distribution of DW motion in a magnetic racetrack (NAND gate). To obtain a 97.5% probability that the logic operation is successful (see Extended Data Fig. 9c), the required propagation delay time can be estimated to be

$$t_{\mathrm{delay},97.5\%} = \frac{L_{\mathrm{input}} + L_{\mathrm{output}}}{\overline{v}_{\mathrm{DW}} - 2\sigma_{\mathrm{DW}}} + \frac{L_{\mathrm{NAND}}}{\overline{v}_{\mathrm{NAND}} - 2\sigma_{\mathrm{NAND}}}. \tag{6}$$

To demonstrate that a sufficient propagation delay time can improve the reliability for a statistically significant number of operations in a NAND gate, we placed the output of a NAND gate on a Hall cross (Extended Data Fig. 10a) and performed 1172 measurements. For each measurement, the NAND gate is saturated with an OOP magnetic field to set the initial magnetization direction to $\odot$ in all of the reservoirs and a series of current pulses are applied. The output is measured via the anomalous Hall effect on application of a DC current. The pulse source and DC source are separated by a bias tee. As indicated by the change of the Hall resistance in Extended Data Fig. 10b, the output changes from “0” to “1” and back to the state of “0”. The electrical measurements are verified with MOKE measurements performed on the NAND gate (see MOKE images in Extended Data Fig. 10b). By using 14 current pulses (equivalent to a propagation delay time of 14 × 30 ns), the reliability of the NAND gate increases to >95% (Extended Data Fig. 10c).

For a cascaded logic circuit, the propagation delay time is determined by the longest DW propagation route in the circuit. In order to decrease the propagation delay time, several possible approaches, e.g., scaling of the dimensions of the circuit, increase of the DW velocity and decrease of pinning, can be employed.

Reliability of the logic gates

In order to realize large-scale implementation of the logic gates, reliable operation is essential. Here, we evaluate the reliability of the two basic NOT and NAND gates in terms of device-to-device reliability and operational reliability (Supplementary Table 2).

To demonstrate the high device-to-device reliability of the NOT gate, we fabricated 35 NOT gates and 34 of them (97%) showed successful operation. We also performed the NOT operations with various current densities in the range 4×10^{11} A/m^2 to 1.65×10^{12} A/m^2 in a single device with 100 % operational reliability.

To test the device-to-device reliability of the NAND gate, we fabricated 56 NAND gates with different logic inputs and the average success rate was found to be 42/56 (75%). The failure of some of the devices may be related to pinning of the DWs by defects in the material or irregular features resulting from the nanofabrication. The width of the magnetic racetracks in the NAND gate is 200 nm compared to 800 nm for the NOT gate, which means that the edge roughness can induce more pinning. For four selected devices, we performed 20 operations for each device (Supplementary Fig. 4) and they all gave correct outputs, showing high operational reliability.

We now consider the distribution of the device-to-device reliability for different logic inputs. For the 56 NAND gates, we fabricated 14 of each type with logic inputs “00”, “11”, “01” and “10”. The number of NAND gates that give correct outputs/the total number of NAND gates are 13/14, 11/14, 10/14 and 8/14 for logic inputs of “00”, “11”, “01” and “10”, respectively. The device-to-device reliabilities for “00” and “11” inputs are slightly higher than those of “01” and “10” inputs. This can be understood by considering the energy difference between the “1” and “0” outputs for “00”, “11”, “01” and “10” inputs given by:

$$\begin{aligned} E_{1/0}^{\ 00} &= (2E_{\text{input}} + E_{\text{bias}}) \\ E_{1/0}^{\ 11} &= 2E_{\text{input}} \quad E_{\text{bias}} \\ E_{1/0}^{\ 01} &= E_{\text{bias}} \\ E_{1/0}^{\ 10} &= E_{\text{bias}} \end{aligned} \quad , \qquad (7)$$

where $\Delta E_{1/0}^{\ ij}$ is the energy difference between the “1” and “0” outputs for input “*ij*” (“*ij*”= “11”, “00”, “01” or “10”), E_{input} is the coupling strength between output and input, and E_{bias} is the coupling strength between the output and the bias, respectively. From this set of equations, it follows that the

stable output for the "11" input is "0" ($\Delta E_{1/0}>0$) and the stable outputs for the other inputs of "00", "01" and "10" are "1" ($\Delta E_{1/0}<0$), which satisfies the truth table of the NAND operation. For the NAND gate used in the experiment, the size of bias is a bit smaller than that of the inputs. Since the energy of coupling between two OOP magnetizations separated by the IP region is proportional to the length of their boundary, the coupling energy between the output and input magnetization is larger than the coupling energy between the output and bias magnetization, i.e., $E_{input}> E_{bias}$. Hence, $|\Delta E^{00}|> |\Delta E^{11}|> |\Delta E^{01}|= |\Delta E^{10}|$ for the NAND operation. This trend in the energy difference between the correct and erroneous outputs for different logic inputs correlates well with the trend in the device-to-device reliability for different logic inputs.

We also tested the operational reliability of the cascaded logic circuit (full adder) shown in Fig. 4d in the main manuscript. The number of successful operations/the total number of operations performed was found to be 28/30.

Therefore, in our proof-of-concept experiments, we have demonstrated a high reliability of the magnetic gates. We further emphasize that there is plenty of room to improve the device-to-device reliability in terms of optimization of the fabrication process, device design, and material properties.

Electrical control of logic inputs and detection of logic output

For the proof-of-concept experiment shown in Fig. 3f in the main manuscript, we ensured that specific DWs reached the inputs by placing inverters on the input racetracks. After saturation with an OOP magnetic field, the magnetization direction in the racetrack was set to $\odot$. On application of a current, the magnetization of the propagating DWs was reversed as they were transferred across each inverter. By placing different numbers of inverters at different positions in the input racetracks, we could generate a sequence of logic inputs in order to obtain different inputs at the same gate over time and, in this way, demonstrated its real-time operation. We also showed that electrical switching of DW propagation in a Y-shape structure could be used to inject DWs and define specific logic inputs (Fig. 4a in the main manuscript).

For downscaled logic circuits, magnetic tunneling junctions (MTJs) fabricated on the logic input racetracks would provide a more compact method to control the logic inputs (Supplementary

Fig. 5). Indeed, it has been shown that an MTJ on a magnetic racetrack can be used to write magnetic domains via spin transfer torque (STT)[29]. Therefore, MTJs fabricated on magnetic racetracks can be used to electrically control the logic inputs. For the detection of the logic outputs, we used MFM, MOKE microscopy and Hall measurements in our proof-of-concept experiment. For the downscaled logic circuits, MTJs fabricated on the output racetracks could be used to electrically detect the logic outputs.

Moreover, it is practical to not only be able to read the output of a gate and but also to transfer this to the input of another gate using MTJ devices in order to realize information feedback. The feedback is critical for sequential logic operations such as those performed in a flip-flop gate. Therefore, the MTJ/racetrack hybrid structure can provide a compact method to perform complex logic.

Energy consumption of downscaled logic devices

For the estimation of energy consumption of the inverter used in the experiments, we consider the area containing the V-shaped IP region where the DW is reversed. The energy consumption per operation of the inverter is calculated from the power-delay product in the bottom Pt layer:

$$E = I^2 Rt = \frac{J^2 \rho W L^2 h}{v_{\mathrm{NOT}}}, \tag{8}$$

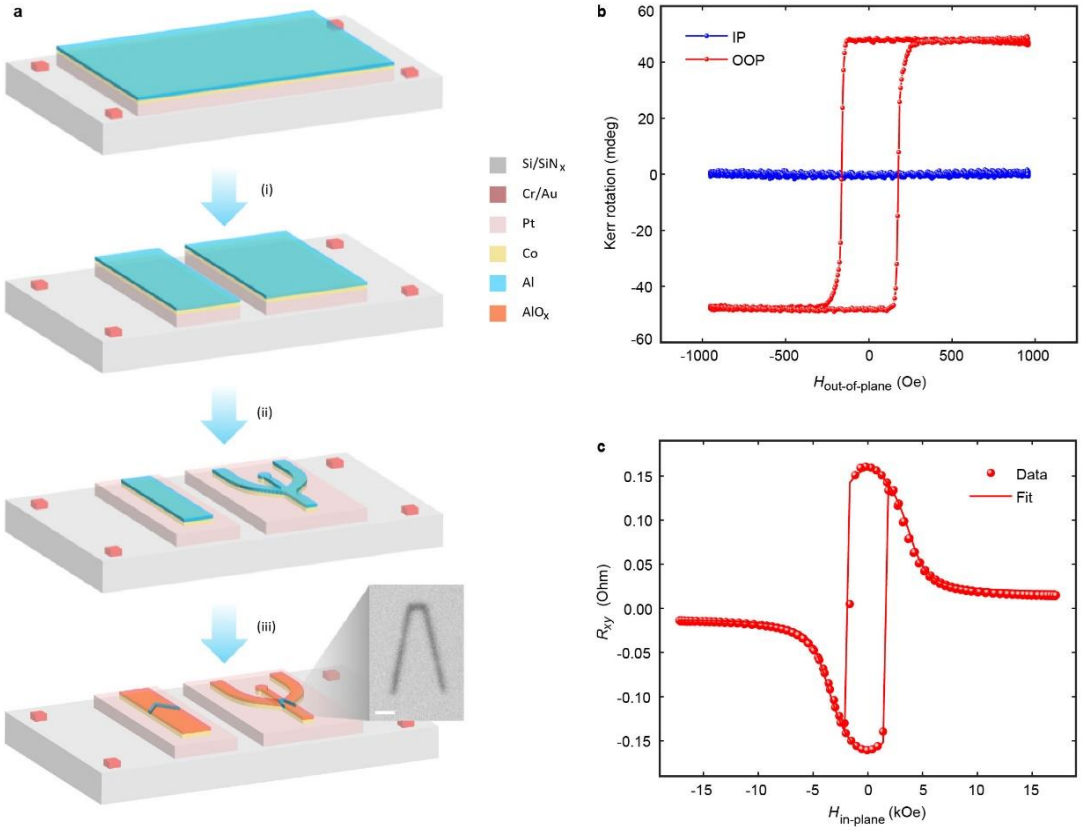
where J, ρ, W, L, h, and v_{NOT} represent the current density, resistivity of Pt, inverter width, inverter length, thickness of Pt layer (5 nm) and effective DW velocity in the inverter, respectively. Taking the inverter dimensions of $W \times L$ =0.8×1.0 μm^2, Pt resistivity in a thin film of ρ =30.0 μΩ·cm, and the current density and effective inverter DW velocity measured experimentally of J =1.65×10^{12} A/m^2 and v_{NOT} =160 m/s, the energy consumption per operation of the inverter is calculated from Eq. 8 to be 20.4 pJ.

For a rough estimation of the energy consumption of a downscaled inverter, we scale down the dimensions of the inverter while keeping the value of the Pt layer thickness, the Pt resistivity, the current density and the effective DW velocity across the inverter the same as those measured in the experiment. The energy consumption per operation for an inverter with the dimensions indicated in

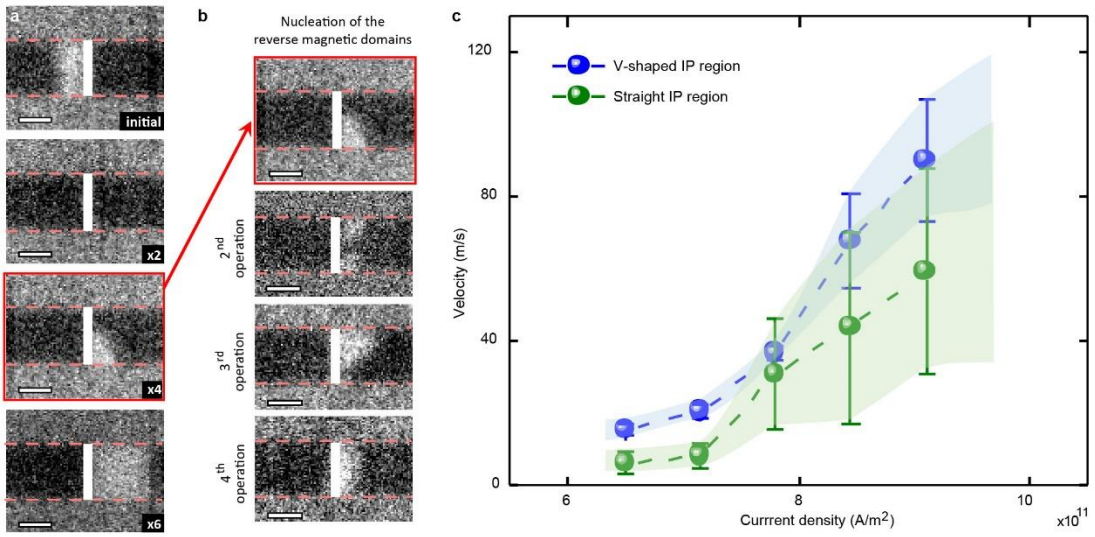
Extended Data Fig. 2 scaled down to 10×10 nm^2 is 25.5 aJ. For a more accurate estimation, we performed micromagnetic simulations for a downscaled inverter with lateral dimensions of 10×10 nm^2. At such a small scale, the device design is limited by the feature size that can be nanofabricated. Therefore, a straight IP region is considered instead of a V-shaped one, with a width of 10 nm. Using a simulated current density of 1.2×10^{12} A/m^2 and effective inverter DW velocity of 118 m/s in Eq. 8, we find that the energy consumption per operation is 18.4 aJ, which is similar to the rough estimation above. This energy consumption for the downscaled inverter is comparable to the switching energy of ≈30 aJ found in advanced CMOS devices[13]. Further improvement of the energy consumption can be achieved by optimizing the material and device design in order to decrease the required current density and increase the DW velocity.

The above estimation concerns only the energy consumed in the logic gate, i.e. the energy consumed for the inversion of a DW. There is additional energy required to nucleate the DWs in the racetrack for the logic inputs, to detect the logic outputs and to move DWs along the interconnections. The total energy consumption therefore depends on the detailed design of the logic circuit.

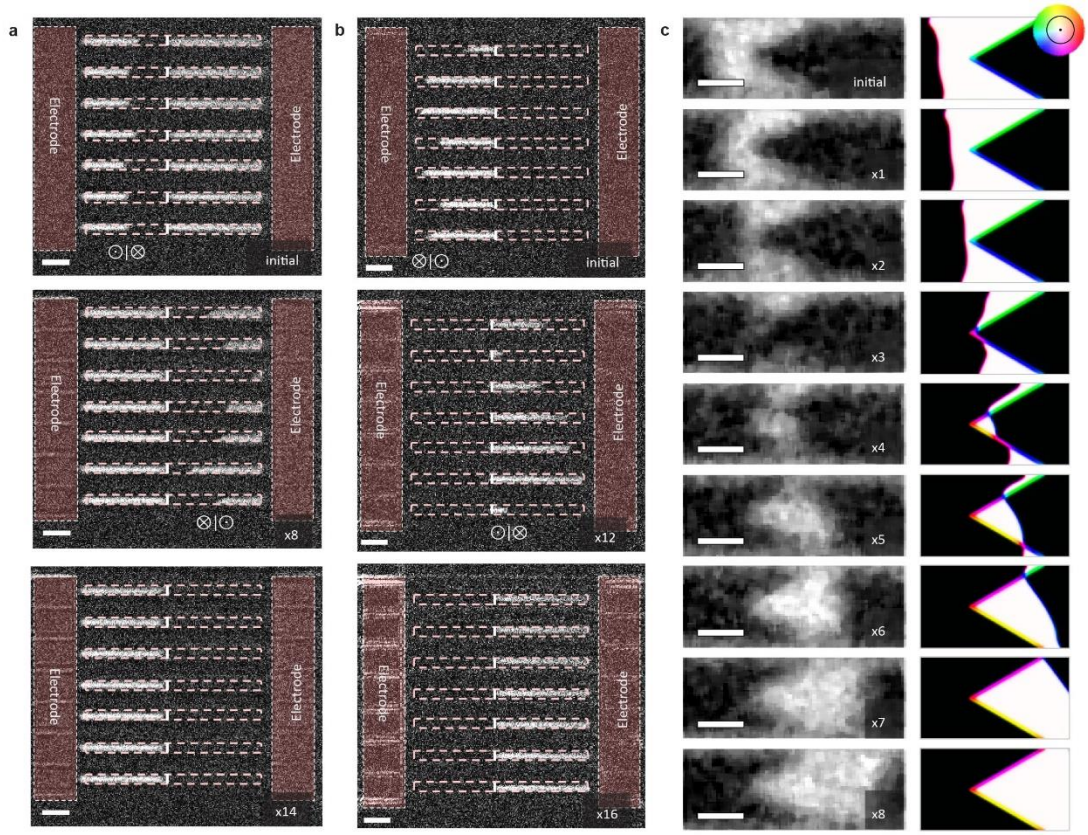
Extended data figure legends



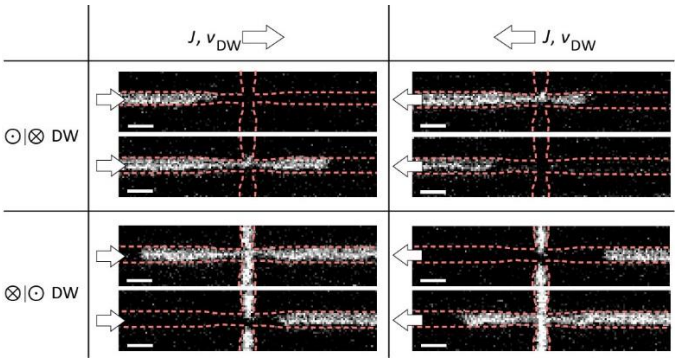
Extended Data Figure 1 | Device fabrication and magnetic characterization. a, Schematics of main nanofabrication processes for magnetic DW logic circuits. (i) Ion milling of magnetic Pt/Co/Al multilayer to create magnetic strips, (ii) ion milling to produce magnetic racetracks and logic gates, and (iii) oxidization of the Al layer in the OOP regions. In the inset, an SEM image is shown of the 50-nm wide PMMA mask used to protect the IP region of the NAND gate shown in Fig. 3a in the main manuscript during oxygen plasma treatment. The scale bar in the SEM image is 100 nm. **b,** Polar MOKE measurement of IP and OOP regions on application of an OOP magnetic field. **c,** Anomalous Hall measurement of OOP region on application of an IP magnetic field.



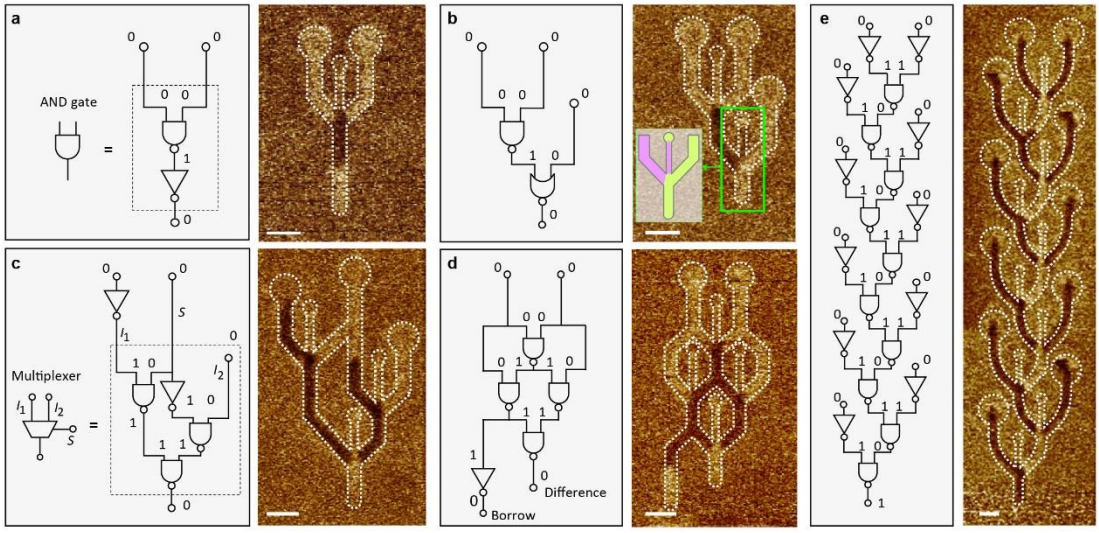
Extended Data Figure 2 | DW inversion in the DW inverter with a straight IP region. a, STXM image sequence of DW inversion for an incident ⊗|⊙ DW performed in the DW inverter with a straight IP region. Each XMCD image is captured after the application of two current pulses. The edges of the magnetic racetracks are indicated with red dashed lines and the positions of the inverters are indicated with solid white lines. The bright and dark contrast in the XMCD images correspond to ⊙ and ⊗ magnetization, respectively. The current density and duration of the pulses are 1.1×10^{12} A/m^2 and 1 ns. **b,** STXM images of the nucleation of reverse magnetic domains in the same DW inverter with a straight IP region for four different operations. **c,** DW velocity in the DW inverters with a V-shaped and straight IP regions as a function of current density determined from the experimental MOKE measurements. Error bars for each point and colored shading represent the standard deviation of the DW velocity for 5 measurements. All the scale bars are 500 nm.



Extended Data Figure 3 | Further experimental demonstration of the DW inverter. a and **b,** MOKE image sequences of DW inversion for incident (**a**) ⊙|⊗ and (**b**) ⊗|⊙ DWs performed in the same device used for Fig. 2c in the main manuscript. The edges of the magnetic racetracks are indicated by red dashed lines and the positions of the inverters are indicated by white lines. The bright and dark contrasts in the magnetic racetracks in the MOKE images correspond to ⊙ and ⊗ magnetization, respectively. The current density and pulse length of the applied current pulses are 7.5×10^{11} A/m^2 and 50 ns, respectively. The number of applied current pulses are indicated. The entire image sequences in **a** and **b** are shown in Supplementary Video 1 and 4. **c,** STXM image sequence of DW inversion for an incident ⊗|⊙ DW and corresponding micromagnetic simulation. Each XMCD image is captured after the application of one current pulse with a current density of 1.1×10^{12} A/m^2 and pulse length of 1 ns. The bright and dark contrasts in the XMCD images correspond to ⊙ and ⊗ magnetization, respectively. For the simulated images, the IP directions of the magnetizations are given by the colour wheel, and the black and white contrast correspond to ⊙ and ⊗ magnetization. The scale bars in the MOKE images are 3 µm and the scale bars for the XMCD and simulation images are 500 nm.

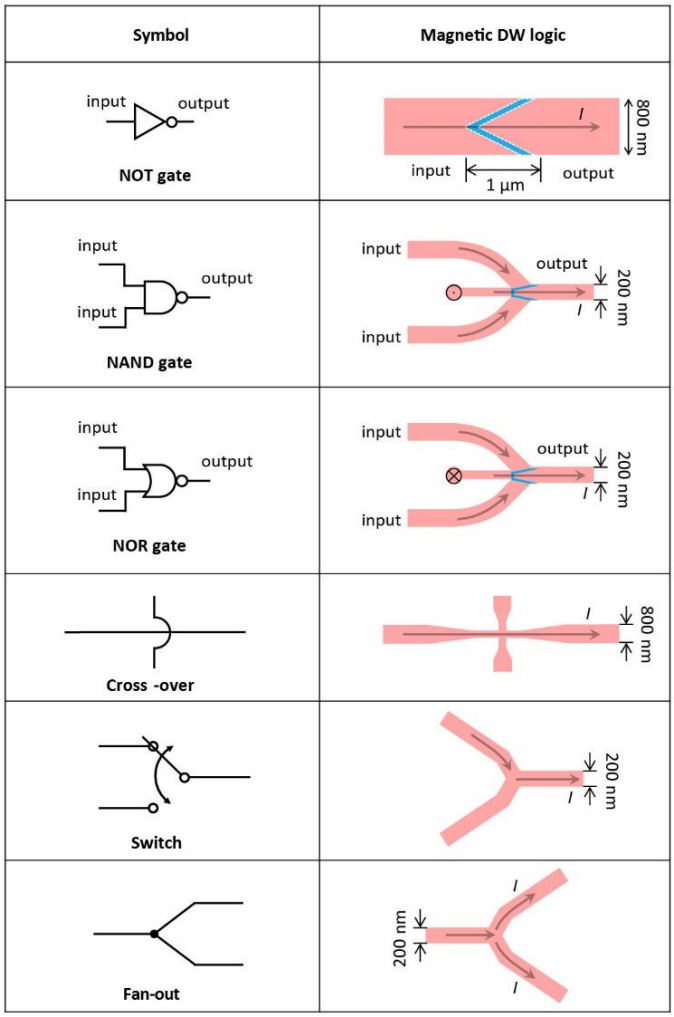


Extended Data Figure 4 | Electrical control of DW motion through a cross structure. The directions of the current *J* and DW motion are the same and indicated for each image (current density 9×10^{11} A/m^2 and pulse length 30 ns). The edges of the cross structures are indicated with red dashed lines. The bright and dark contrast in the cross structure in the MOKE images correspond to ⊙ and ⊗ magnetization, respectively. All the scale bars are 1 μm.

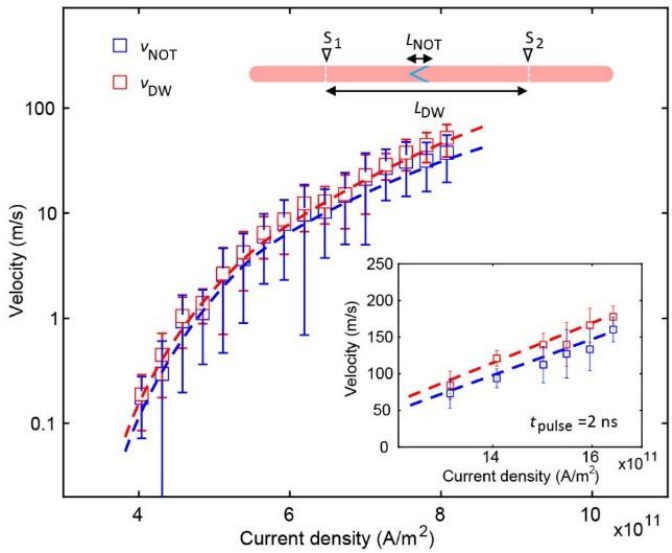


Extended Data Figure 5 | Various cascaded DW logic circuits. a, AND gate fabricated by cascading one NAND gate and one NOT gate. **b,** Cascaded DW logic circuit with NAND gate and NOR gate. Green and purple in the schematic correspond to ⊙ and ⊗ magnetization, respectively. Note that there is an inverter placed in the bias reservoir for the NOR gate highlighted with the green box giving a bias of "1" as shown in inset, while the bias for the NAND gate is "0". **c,** Two-bit multiplexer fabricated by cascading three NAND gates and one NOT gate. **d,** Half subtractor fabricated by cascading four NAND gates and one NOT gate. **e,** Long cascaded DW logic circuits including 10 NAND gates and 11 NOT gates. The bright and dark contrasts in the device regions in

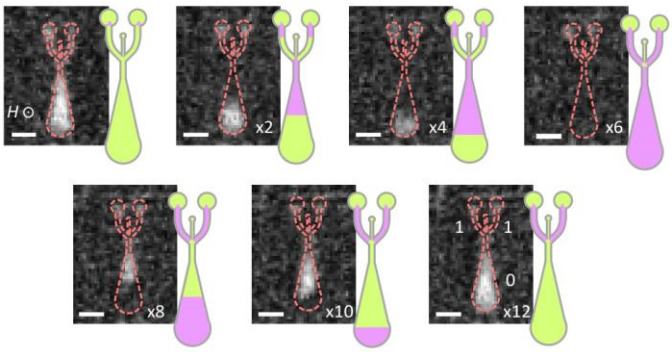
the MFM images correspond to ⊙ and ⊗ magnetization, respectively. The MFM images are captured after saturation with an OOP magnetic field to set the initial magnetization direction to ⊙ in all of the reservoirs followed by applied current pulses to get the final states. All the scale bars are 500 nm.



Extended Data Figure 6 | Magnetic DW logic elements. Red and blue shaded regions indicate regions with OOP and IP anisotropy, respectively. The direction of current flow is indicated by black arrows. The dimensions of the magnetic DW logic elements used in the experiments are indicated.

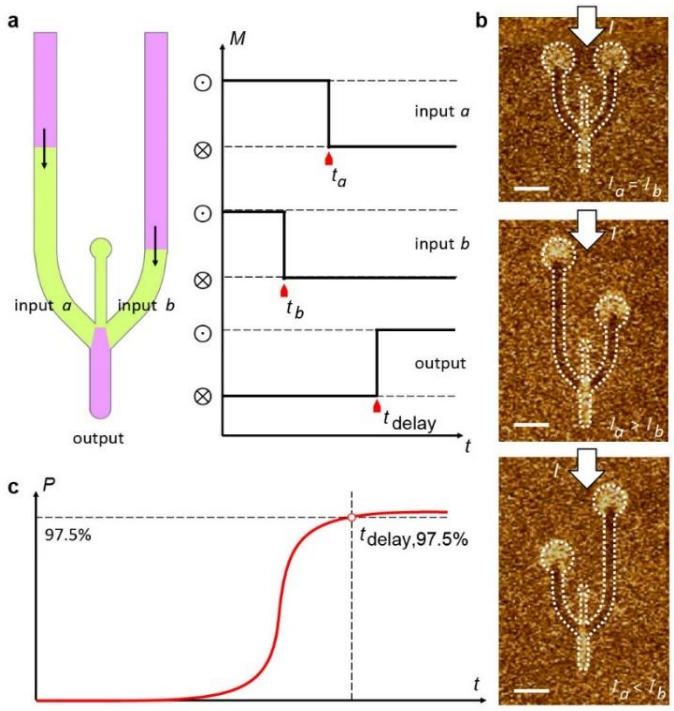


Extended Data Figure 7 | DW velocity in a uniform OOP region of a racetrack and effective DW velocity in a NOT gate as a function of current density. Error bars represent the standard deviation of the DW velocity measured in 5 different devices.

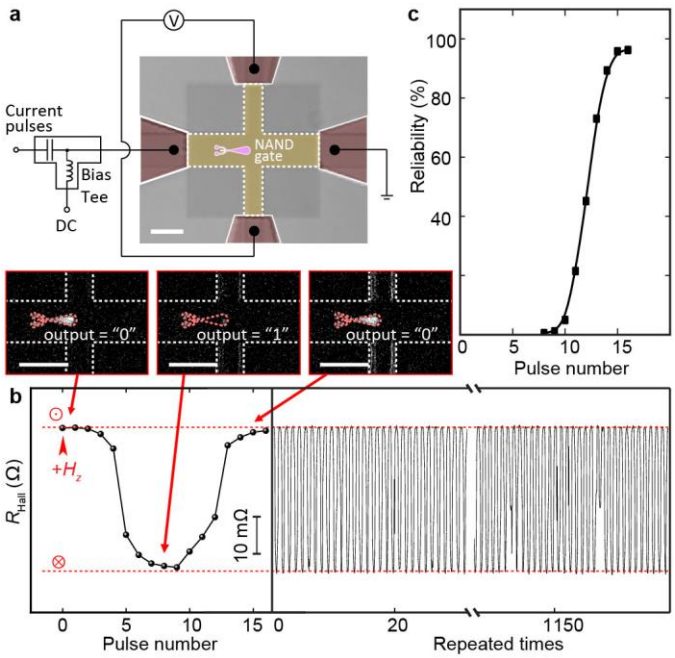


Extended Data Figure 8 | MOKE images of the time sequence of the NAND gate during operation and corresponding schematics. The NAND gate contains two inverters in the DW reservoirs and a bias set to "0", and the boundaries of the NAND gate are indicated by red dashed lines. The two V-shaped inverters in the DW reservoirs are associated with small reverse domains in the initial state (indicated as purple triangles) resulting from the chiral coupling. A sequence of MOKE images is captured where each image is taken following two current pulses with a current density of 7.5×10^{11} A/m^2 and a pulse length of 30 ns. The bright and dark contrasts in the gate structure in the MOKE images correspond to ⊙ and ⊗ magnetization, respectively. In the schematics, green and purple correspond to ⊙ and ⊗ magnetization, respectively. The two DW reservoirs and the bias are set to logic "0" by applying an OOP magnetic field of 1 kOe. All the

scale bars are 1 μm.



Extended Data Figure 9 | Propagation delay time for DW logic. a, Schematic showing the use of the propagation delay time to improve the operational reliability of logic operation in a NAND gate. The green and purple correspond to ⊙ and ⊗ magnetization, respectively. **b,** MFM images of NAND gates with different input racetrack lengths (top: $l_a = l_b$, middle: $l_a > l_b$, bottom: $l_a < l_b$, where l_a and l_b represent the racetrack length of input *a* and *b*, respectively). The bright and dark contrasts correspond to ⊙ and ⊗ magnetization, respectively. The MFM images are captured after saturation with an OOP magnetic field to set the initial magnetization direction to ⊙ in all of the reservoirs followed by application of current pulses to obtain the final states. The direction of the current flow is indicated. **c,** Schematic showing the dependence of the probability of giving a correct output as a function of propagation delay time. All the scale bars in the MFM images are 500 nm.



Extended Data Figure 10 | Hall measurement of logic operation in a NAND gate. a, Schematic including optical image of the device. Red, yellow, and purple colours in the optical image represent the regions with electrodes, the Pt cross and the NAND gate, respectively. **b,** Hall resistance as a function of pulse number and corresponding MOKE images. Left: typical Hall resistance evolution with increasing number of pulses. Right: the first 30 measurements and last 30 measurements of the 1172 repeated measurements. The Hall resistance levels for ⊙ and ⊗ output magnetizations are indicated by the red dashed lines. An OOP magnetic field is applied to set the initial state at the beginning of each measurement indicated with the red arrow. The bright and dark contrast in the gate structure in the MOKE images correspond to ⊙ and ⊗ magnetization, respectively. The boundaries of the NAND gate are indicated by red dashed lines. The current density and pulse length of the applied current pulses are 7.5×10^{11} A/m^2 and 30 ns, respectively. **c,** Operational reliability as a function of the number of current pulses. All the scale bars are 2 μm.