Current-efficient preamplifier architecture for CMRR sensitive neural recording applications

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***Abstract*—There are neural recording applications in which the amplitude of common-mode interfering signals is several orders of magnitude higher than the amplitude of the signals of interest. This challenging situation for neural amplifiers occurs, among other applications, in neural recordings of weakly electric fish or nerve activity recordings made with cuff electrodes. This paper reports an integrated neural amplifier architecture targeting in-vivo recording of local field potentials and unitary signals from the brain stem of a weakly electric fish *Gymnotus omarorum*.**

The proposed architecture offers low noise, high common-mode rejection ratio (CMRR), current-efficiency, and a high-pass frequency fixed without MOS pseudo-resistors. The main contributions of this work are the overall architecture coupled with an efficient and simple single-stage circuit for the amplifier main transconductor, and the ability of the amplifier to acquire biopotential signals from high-amplitude common-mode interference in an unshielded environment.

A fully-integrated neural preamplifier, which performs well in line with the state-of-the-art of the field while providing enhanced CMRR performance, was fabricated in a 0.5 μm CMOS process. Results from measurements show that the gain is 49.5 dB, the bandwidth ranges from 13 Hz to 9.8 kHz, the equivalent input noise is 1.88 μV_{rms}, the CMRR is 87 dB and the Noise Efficiency Factor is 2.1. In addition, in-vivo recordings of weakly electric fish neural activity performed by the proposed amplifier are introduced and favorably compared with those of a commercial laboratory instrumentation system.

***Index Terms*—Analog integrated circuits, low-power, neural amplifier, electric fish, in vivo recording, differential difference amplifier, bandpass filter, sub-threshold design, high CMRR**

I. Introduction

This work aims to support neural recording applications with low noise, current-efficency and high common-mode rejection ratio (CMRR) as main features of the recording system. One emblematic example of these applications in the neuroscience domain, is the weakly electric fish neural activity recording, where the common-mode interference produced by the discharge of the electric organ of the fish (called electric organ discharge, EOD) is a key factor [1], [2]. Another example, from the implantable devices domain is the nerve activity recorded with cuff electrodes, where the desired signal is interfered by electromyographic potentials generated by muscles near the cuff [3].

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Studies of electroreception have provided extensive knowledge about the complete sensory system. Particularly, electrophysiological recordings in weakly electric fish have contributed to the understanding of the system at different levels of organization [4]. This research has provided insights for the understanding of basic questions on brain functions [5], [6], [7], and has bio-inspired man-built autonomous systems (underwater navigation, object classification, communication, etc.) [8]. In these animals, bioelectric potentials can be recorded at: a) single cell level either intra or extracellularly, informing about cell and neural circuit signal integration; b) tissue level (local field potentials, LFP) informing about the average activity of a cell population; and c) individual level since electrosensory signals, used by the fish for object imaging and communication, are carried by a self generated electric field. For these purposes these fish evolved an electric organ as well as receptors in the skin that are capable of sensing this field.

Weakly electric fish neural recordings are a very challenging task for neural amplifiers, whether the fish is still in acute experiments or freely-moving. Firstly, the single cell signals (unitary activity) have a spike shape of very low voltage which fire simultaneously with other cells. Thus, in order to separate the activity of more than one cell recorded from the same electrode, amplifiers require a resolution in the order of microvolts and very low noise. Secondly, as previously mentioned, high CMRR is important because the electric field generated by the EOD can also be recorded in the brain. Its amplitude can be more than 1000 times larger than other extracellular signals of interest, so most of the time the EOD behaves as an extra artifact besides the classical ones observed in electrophysiological recordings (powerline and fluorescent lamps ac fields, electrode polarization, etc). Thirdly, to separate different types of LFPs containing slow and fast components from the unitary extracellular activity originated in a single cell, it is necessary to use precise and tuneable bandpass filtering. Finally, freely-moving fish recordings require a small size and weight acquisition system as well as ultra-low-power operation to further reduce size and weight, so that smaller batteries can be used and a reasonable autonomy can be achieved.

This work proposes, experimentally characterizes and in-vivo validates, a novel architecture for neural amplifiers, featuring low noise, high CMRR and current-efficiency.

II. Architecture

Harrison et al. in [9] present a neural amplifier architecture that in the last decade has become a very important refer-

ence, widely applied [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Its high-pass characteristic, which requires high valued resistors, is defined by a MOS-bipolar pseudo-resistor. The value of this nonlinear element is difficult to model and control, and can also suffer from drift [12], [20]. Therefore, although high-pass frequencies less than 0.1 Hz can be reached, this can only be done with low accuracy. A workaround on this problem is to modify the pseudo-resistor arrangement so that the equivalent resistance can be controlled through the gate voltage of the MOS transistors that operate in weak inversion [21]. This allows for an off- or on-chip tuning of the high-pass frequency. However, even if the accuracy issue is solved, a second drawback remains. This drawback is the intrinsically low CMRR, which is limited by the matching of the capacitors that set the amplifier gain (we elaborate on this point in Section II-D). Then, while acceptable values of CMRR (60 dB) are obtained, it is not possible to guarantee the values required by our application (greater than 80 dB). Other architectures, which have not had as much impact as [9], have been proposed over the years. An important subset of these, uses a differential difference amplifier (DDA) [22] as input stage [23], [24], [25], [26], while others are based on different approaches [27], [28], [29].

A DDA is composed of an operational transconductance amplifier (OTA) with two differential inputs that are added. One architecture [23] for implementing an instrumentation amplifier by means of a DDA is shown in Fig. 1. It uses one differential input for the signal to be amplified, and the other differential input for the feedback that fixes the gain (feedback factor β) and the high-pass characteristic (inverting low-pass filter). This architecture, as discussed in Section II-D, is intrinsically suitable for high CMRR, and the gain and bandpass cut-off frequencies are fixed by means of parameters that are, respectively, very accurate (i.e. ratios of transconductances) or can be easily and automatically tuned (i.e. ratios of transconductance over capacitances) [30], achieving high-accuracy without jeopardizing power consumption [31]. However, a straightforward implementation of a DDA adds an important amount of noise and consumption (because of the two OTAs at the input).

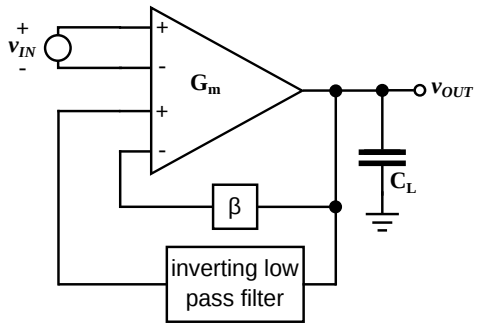

Fig. 1. Block diagram of an instrumentation amplifier based on a differential difference amplifier [22], [23].

A. Proposed solution

Our solution aims to overcome the drawbacks presented by [9] and standard DDAs in order to obtain a neural amplifier with high CMRR, low input noise and current-efficiency. Our starting point is a variant of the architecture proposed in [26] shown in Fig. 2. This architecture proposes a DDA input stage composed of two symmetrical OTAs shown as Gm1[1] and Gm2, and a feedback factor β, where the transconductance of Gm1 (G_{m1}) is higher than the transconductance of Gm2 (G_{m2}). If a standard DDA is used ($G_{m1} = G_{m2}$), the noise of Gm2 contributes to the input as much as the noise of Gm1. By making $G_{m1} > G_{m2}$, the noise contribution of Gm2 can be made negligible. A possible drawback of this architecture arises from the reduction of the current provided by Gm2 to the summing node with respect to the current provided by Gm1. This reduction decreases the range of dc currents at the Gm1 output that the feedback through Gm2 can compensate. When this compensation is not possible the circuit loses its high-pass characteristic. This was solved by fixing the high-pass frequency of the amplifier (and compensating the aforementioned dc component) through a local feedback at the output of Gm1, which is discussed in the next section. The summing block is obtained just connecting the two OTAs outputs and thus adding their output currents. β is set to 1.

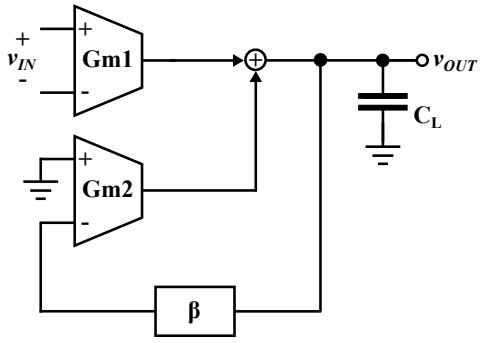

Fig. 2. Block diagram of the architecture proposed in [26].

Fig. 3 shows the novel architecture proposed in this paper. An efficient and simple single-stage circuit for the preamplifier main transconductor (Gm1) is one of the contributions of this work. Gm1 core is formed by M1, M2, M3 and M4. The M5-M8 block jointly with Gmf and C_F, implement the output feedback loop that establishes the high-pass characteristic and blocks the dc input. Gm2 and Gmf are symmetrical OTAs whose respective transconductances are G_{m2} and G_{mf} (see Fig. 3). $g_{m2} = K_{G_{m2}} G_{m2}$, where $K_{G_{m2}}$ is the copy factor of the current mirrors of Gm2, as indicated in Fig. 3, and g_{m2} is the transconductance of input transistors of Gm2. In the same way we will introduce $K_{G_{mf}}$ such that $g_{mf} = K_{G_{mf}} G_{mf}$ and g_{mf} is the transconductance of the input transistors of Gmf. We use symmetrical OTAs because it is a simple architecture,

[1]OTA notation: Gmi refers to the block, G_{mi} (italic) is the transconductance of the block and g_{mi} (italic lowercase) is the transistor transconductance.

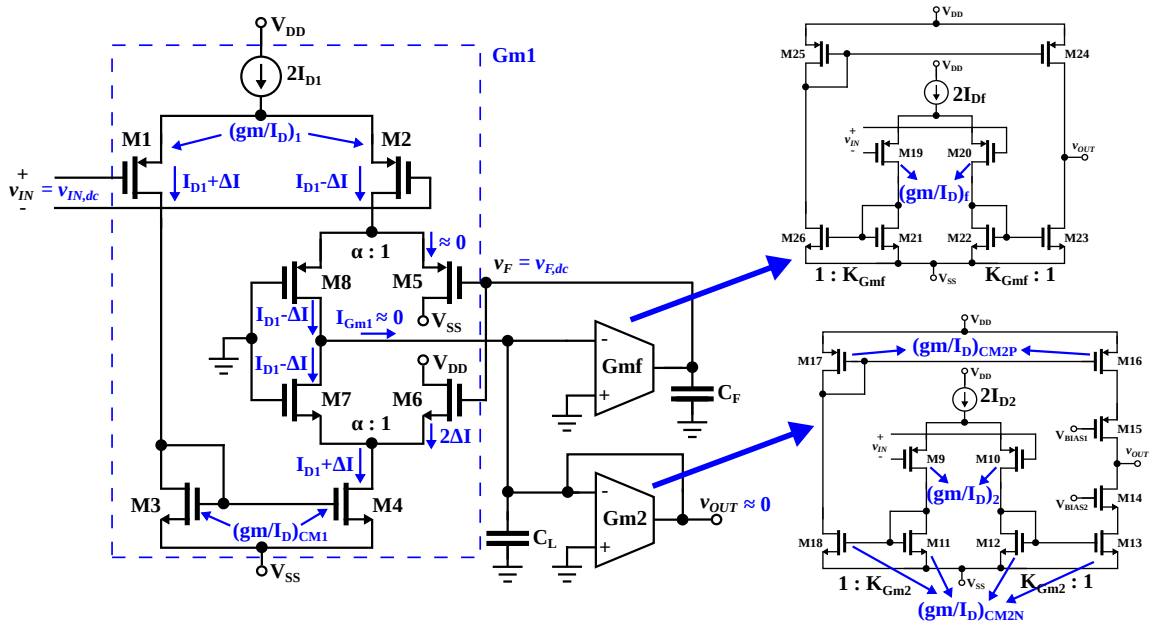

Fig. 3. Block diagram of the proposed architecture. M1-M4 are the Gm1 core. High pass characteristic is fixed through M5-M8, Gmf and C_F (the steady state condition of the input dc blocking mechanism is highlighted). Gm2 and Gmf are implemented with symmetrical OTAs.

but other alternatives could be considered. However, a single-stage circuit, like the one used in Gm1, is not suitable to accommodate the required input and output ranges of Gm2 and Gmf. Furthermore, the saving on power consumption due to the use of a single-stage circuit in these blocks has little impact.

B. Transfer function

Gm1 is an OTA with a differential input (v_{IN}) and a single ended input (v_F). This single ended input is used in the local feedback loop at the output for dc blocking. In small-signal operation it can be useful to interpret M7-M6 and M8-M5 as asymmetrical differential pairs where α defines the degree of asymmetry (see Fig. 3) $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m5}$, where g_{m5}, g_{m6}, g_{m7} and g_{m8} are the transconductance of M5, M6, M7 and M8 respectively. As will become clear in Section II-C, an $\alpha \gg 1$ is adopted, which implies that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$. Therefore, the transfer function of Gm1 is as follows (see Fig. 3):

$$i_{Gm1} \cong G_{m1} v_{IN} + (g_{m5} + g_{m6}) v_F \tag{1}$$

where G_{m1} is the Gm1 transconductance ($G_{m1} = g_{m1}$ where g_{m1} is the transconductance of M1 and M2).

The circuit depicted in Fig. 3 has the first-order bandpass transfer function presented in Eq. 2,

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L} s}{s^2 + \frac{G_{m2}}{C_L} s + \frac{(g_{m5}+g_{m6}) G_{mf}}{C_L C_F}} \tag{2}$$

and the low-pass frequency $f_{low-pass}$ is given by Eq. 3, the bandpass gain G by Eq. 4 and the high-pass frequency $f_{high-pass}$ by Eq. 5,

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{3}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{4}$$

$$f_{high-pass} = \frac{(g_{m5} + g_{m6})}{G_{m2}} \frac{G_{mf}}{2\pi C_F} \tag{5}$$

C. High-pass / input dc block circuit

Fig. 3 shows the schematic of Gm1. In an OTA standard structure (without M5 and M6) M7 and M8 would be ordinary cascode transistors, but in this circuit they also perform another function. Jointly with M5 and M6, which are in charge of draining the excess current caused by a dc input signal, they are the core of the input dc block or high-pass circuit.

Considering dc operation, the current by M1 and M2 is ID1. Any dc input signal $V_{IN,dc}$ will generate a current ΔI through M1 and M2 (see Fig. 3), that will be copied to the output by the current mirror formed by M3 and M4. Then, if M5 and M6 are not present, this current will flow by M7 and M8 and will exit the circuit at the output node.

The M5-M8 block, jointly with Gmf and C_F, are dedicated to establish the high-pass characteristic and to block the dc input. Indeed, the aforementioned ΔI current at the Gm1 output (I_{Gm1}) will be compensated by M5 or M6, in order to keep the output voltage v_{OUT} equal to zero, via the integrator Gmf-C_F.

For instance, when the dc input signal causes the current by M8 ($I_{D,M8} = I_{D1} - \Delta I$) to fall (or equivalently causes $I_{D,M7} = I_{D1} + \Delta I$, the current by M7, to rise), $I_{Gm1} = -2\Delta I$ will fall, then v_{OUT} will fall as well (Gm2 acts as a resistor to ground). Then Gmf will increase its output current and v_F will rise, making M5 to drain less current (or equivalently making M6 to drain more current). The equilibrium will be reached when $I_{D,M7} \approx I_{D,M8}$ and consequently when $I_{Gm1} \approx 0$. This steady state condition

(marked in blue in Fig. 3) holds in a simplified case where Gmf-C_F provides ideal integration with infinite dc gain. In a practical case the finite dc gain and offset of Gmf will result in a small remaining output dc offset. A similar reasoning can be carried out if $I_{D,M8}$ rises (or equivalently $I_{D,M7}$ falls).

It is interesting to note that any mismatch present in the transistors of Gm1, that can generate a ΔI current, will also be minimized by means of this technique.

One side-effect of this technique is that in ac operation M5 and M6 will drain signal current. Then, if a high level of dc input must be blocked, a loss of gain will be registered. An alternative to overcome this problem is to size M5-M8 in a way that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ ($\alpha \gg 1$). For this reason, α is a key parameter in the design process. On the one hand, if α = 1, the differential pair will be symmetrical, half of the gain will be lost in M5 and M6, and the circuit will be able to block higher levels of dc input signals. On the other, if α = 100 or greater, the loss of gain will be negligible, but the capacity of blocking high levels of dc input signals will be reduced (this is later quantified in Table IV).

D. CMRR

If we consider the architecture proposed by our work, we have

$$CMRR = CMRR_{OTA} \tag{6}$$

where $CMRR_{OTA}$ is the CMRR obtained by the transconductor Gm1 (which can be as high as it can be on any OTA).

In this structure, there are two factors that reduce the common mode gain [32, Section 4.3.5.3]. The first factor is the intrinsic rejection of common mode signals (low common mode gain) of a differential pair structure. The common mode gain of each branch of the OTA input stage is given by $R_L/2.r_{tail}$, where R_L is the load resistance and r_{tail} is the resistance of the "tail" current source of the differential pair. It is worth noting that r_{tail} could be designed to be high by well known techniques, like cascoding it. The second factor is the common mode attenuation due to symmetry. If the structure were perfectly symmetrical (i.e. without systematic or random mismatch), the common mode gain would be zero. When mismatch is considered, the common mode gain is

$$A_{OTA}^{CM} = \frac{R_L}{2.r_{tail}}(\epsilon_d + \epsilon_{cm}) \tag{7}$$

where ϵ_d and ϵ_{cm} are asymmetry error coefficients due to mismatch of the differential pair and current mirror respectively (in Section II-F, the reason why these coefficients are small in our architecture is discussed).

If we consider the amplifier proposed by Harrison et al. [9, Fig. 1], the CMRR can be expressed as [33]:

$$\frac{1}{CMRR} \cong \frac{1}{CMRR_{OTA}} + \frac{1}{CMRR_{mismatch}} \tag{8}$$

where $CMRR_{OTA}$ is the CMRR of the OTA and $CMRR_{mismatch}$ is the resulting CMRR due to the mismatch of the passive elements (capacitors C1 and C2, if we consider the in-band frequencies) considering the OTA has infinite CMRR ($CMRR_{OTA}$ = infinite).

From Eq. 6 and Eq. 8 it can be concluded that the CMRR of the architecture of [9] is always worse than the one obtained by our architecture. Additionally, it is usually met that $CMRR_{OTA} > CMRR_{mismatch}$, thus $CMRR_{mismatch}$ dominates Eq. 8. The reasons for this are, firstly, the OTA open loop differential gain is much larger than the closed loop one. Secondly, as will be shown next, the OTA common mode gain A_{OTA}^{CM} is lower than $A_{mismatch}^{CM}$.

Following a similar reasoning of [33] it can be seen that the worst-case of $CMRR_{mismatch}$ is:

$$CMRR_{mismatch} \cong \frac{1 + C1/C2}{2(\delta_1 + \delta_2)} \tag{9}$$

where δ_1 and δ_2 are the tolerance of C1 and C2 respectively[2], and the worst-case of the common mode gain is:

$$A_{mismatch}^{CM} \cong 2(\delta_1 + \delta_2) \tag{10}$$

The mismatch in the passive elements translates directly into a non zero common mode gain value which is in the order of the mismatch error or tolerance of the passive elements (e.g a mismatch of 1% leads to a common mode gain around -34 dB). Furthermore, since C2 must be much smaller than C1, in order to set a reasonably high closed loop gain (C1/C2), and as matching improves with size, at least matching of C2 will not be optimal. On the other hand, in a OTA structure, the common mode gain is reduced by the two factors mentioned before, and can be further reduced from the values imposed by mismatch by increasing the r_{tail}.

E. Noise

It can be proved that the thermal noise input-referred power spectral density S_{ni}^{total} for the circuit shown in Fig. 3 is:

$$S_{ni}^{total} \cong \frac{2\gamma_{si} n_N kT}{G_{m1}} \left(\frac{\gamma_{wi} n_P}{\gamma_{si} n_N} + \frac{(g_m/I_D)_{CM1}}{(g_m/I_D)_1} + \frac{I_{D2}}{I_{D1}}\Gamma \right) \tag{11}$$

where $(g_m/I_D)_1$ and $(g_m/I_D)_{CM1}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm1 (M1 and M2) and of the current mirror transistors of Gm1 (M3 and M4). $\gamma_{wi} = 2$ and $\gamma_{si} = 8/3$ are the excess noise factor in weak and strong inversion, respectively. n is the slope factor (the subscript indicates whether it is an NMOS or PMOS transistor), k is the Boltzmann constant, T is the absolute temperature, and Γ is:

$$\Gamma = \frac{(g_m/I_D)_2}{(g_m/I_D)_1} \frac{n_N}{n_P K_{G_{m2}}^2} + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}^2} + \\ + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}} + \frac{(g_m/I_D)_{CM2P}}{(g_m/I_D)_1} \frac{n_N}{n_P K_{G_{m2}}} \tag{12}$$

[2]The actual value of both capacitors of nominal value C1 are in the range $[1 - \delta_1, 1 + \delta_1].C1$, with $\delta_1 \ll 1$. We could consider δ_1 equal to the 3σ value of the distribution of C1. In an analog way, we consider that capacitors C2 have a tolerance δ_2, with $\delta_2 \ll 1$.

where $(g_m/I_D)_2$ and $(g_m/I_D)_{CM2i}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm2 (M9 and M10) and of the current mirror transistors of Gm2 (the subscript indicates whether it is an NMOS or PMOS transistor), and $K_{G_{m2}} = g_{m2}/G_{m2}$. These equations show the contribution of $K_{G_{m2}}$ in the noise reduction.

In order to reduce noise, according to Eq. 11, M1 and M2 have to be biased in weak inversion (maximum (g_m/I_D)), and M3 and M4 in strong inversion (low (g_m/I_D)). In order to further reduce noise it can be shown that the input transistors of Gm2 have to be biased in weak inversion and the Gm2 mirror transistors in strong inversion.

In order to evaluate the trade-off between power consumption and noise and guide the design decisions, the NEF (Noise Efficiency Factor) introduced by [27] is used:

$$NEF = v_{ni}\sqrt{\frac{I_{DD}}{2k\pi T U_T BW}} \tag{13}$$

where v_{ni} is the input-referred noise voltage, I_{DD} is the total supply current, BW is the bandwidth, $U_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature and q is the electron charge.

F. Design flow and design trade-offs

In this section a basic design flow for the proposed architecture, including the main design trade-offs is presented. I_{D1} is set through the power consumption specification or the noise specification (by means of the NEF). Then, G_{m1} is set aiming to maximize $(g_m/I_D)_1$ in order to minimize noise (see Section II-E) while having an acceptable size for M1 and M2. Next, by means of Eq. 4 and the gain specification, G_{m2} is fixed. Therefore, given the $f_{low-pass}$ specification, according to Eq. 3, C_L is determined.

The inversion level of the input transistors of Gm2 (related to $(g_m/I_D)_2$) has to be chosen considering the following trade-off. Firstly, $(g_m/I_D)_2$ has to be maximum in order to minimize noise (see Section II-E) and power consumption. Secondly, $(g_m/I_D)_2$ has to be minimum to maximize the linear range of the Gm2 input differential pair, which must be high enough to handle the maximum expected output amplitude (around 300 mV_{pp} in this work). On the other hand, $K_{G_{m2}}$ can be used to lower noise (the higher $K_{G_{m2}}$ the better, see Section II-E) at the cost of increasing the power consumption (the higher the value of $K_{G_{m2}}$, the higher the power consumption). Once $(g_m/I_D)_2$ and $K_{G_{m2}}$ are determined, as G_{m2} was already fixed, I_{D2} is also determined.

The inversion level of the cascode transistors of Gm1 (M7 and M8, and therefore M6 and M5) have to be chosen considering the following aspects. On one hand, in order to achieve a very low value of $f_{high-pass}$ (see Eq. 5), g_{m6} and g_{m5} have to take the lowest possible value, therefore, for a given current, M5, M6, M7, and M8 have to be biased in strong inversion. On the other hand, biasing these transistors in strong inversion may lead to a high saturation voltage V_{Dsat}. Finally, another important point in order to size these transistors is the condition shown in Section II-B: $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ where $g_{m7} \cong g_{m8}$.

Once g_{m2}, g_{m6} and g_{m5} are set, and considering that the value of C_F is bounded by the maximum value reachable within a reasonable area, and given a $f_{high-pass}$ specification, according to Eq. 5 G_{mf} is determined. The inversion level of the Gmf input transistors (defined by $(g_m/I_D)_f$) has to be selected paying attention to the following. On one hand, a very low $f_{high-pass}$ implies a very low value of G_{mf}, which in turn implies a low value of the W/L ratio of the Gmf input transistors. For this reason and for maximizing the linear range of the Gmf input differential pair, $(g_m/I_D)_f$ has to be minimum (strong inversion). On the other hand, biasing the Gmf input differential pair in strong inversion may lead to excessively long transistors, which may in turn result in very high values of the gate-source capacitance which impacts the load capacitance of Gm1 and hence the low-pass frequency. Therefore, biasing in moderate or weak inversion may be necessary. Finally, although from the point of view of power consumption, it might seem that the input transistors of Gmf should be biased in weak inversion, the contribution of the consumption of this stage to the overall consumption is negligible due to the low transconductance required. Once $(g_m/I_D)_f$ is set, I_{Df} is fixed.

Since noise contribution and power consumption of Gm2 cascode transistors are negligible, the only aspect to be considered in its design is the output swing. Then, in order to minimize the saturation voltage V_{Dsat} of these transistors, they have to be biased in weak inversion.

To determine $(g_m/I_D)_{CM1}$ (corresponding to Gm1 current mirror transistors M3 and M4) and $(g_m/I_D)_{CM2}$ (corresponding to Gm2 current mirror transistors) two elements have to be considered. Firstly, in Section II-E it was shown that from the point of view of noise reduction these transistors have to be biased in strong inversion. Secondly, low values of g_m/I_D may lead to a high value of the V_{Dsat} saturation voltage that impacts in the output swing.

Finally, M1 and M2 need to be large in order to operate in weak inversion, and hence will present very good matching and low ϵ_d error. Additionally, M3 and M4 have to operate in strong inversion with also large size (large L for small W/L), both conditions lead to low mismatch error (ϵ_{cm}). Therefore, it is possible to reduce noise and increase CMRR, at the cost of increasing the area.

The actual implementation resulting from these trade-offs is presented in the next section.

III. Implementation

A neural preamplifier based on the previously presented architecture was implemented in a 0.5 μm standard CMOS process. In order to obtain a NEF around 2, I_{D1} = 3.75 μA was taken. The Gm1 mirrors (M3 and M4) were biased in deep strong inversion taking[3] $(g_m/I_D)_{CM1}$ = 2.5 V^{-1}, which implies a V_{Dsat} = 590 mV. The transistors of the Gm1 input differential pair (M1 and M2) were biased in deep weak inversion with a $(g_m/I_D)_1$ = 27 V^{-1}. In order to assess the impact on flicker noise, taking an almost minimum M1 and M2 transistor length L_1 = 1 μm, different cases were

[3]Throughout the text g_m/I_D values are reported at room temperature.

simulated varying the M1 and M2 transistor width W_1. Table I shows schematic simulations of the noise performance for the main values of the W_1 considered. As expected, the higher W_1 the lower the contribution of the flicker noise. Finally, W_1 = 8000 μm was chosen.

A further analisys of Table I shows that it does not make a big difference, regarding noise performance, to vary the high-pass frequency between 0.1 Hz (external capacitor C_F = 10nF) and 18 Hz (fully-integrated capacitors). This happens because the thermal noise is integrated through a wide bandwidth (10 kHz) making the flicker noise generated between 0.1 Hz and 18 Hz negligible. The same behavior is reported in [9].

TABLE I
NOISE PERFORMANCE WITH L_1 = 1 μM, VARYING W_1 WITH FULLY-INTEGRATED CAPACITORS (FI) AND EXTERNAL C_F = 10NF (EXT).

W_1 (μm)	2000	4000		8000		12000
	FI	FI	Ext	FI	Ext	FI
M1/M2 area (μm^2)	2000	4000	4000	8000	8000	12000
g_{m1} (μS)	94.0	98.0	97.8	101.0	100.8	102.5
$(g_m/I_D)_1$ (V^{-1})	25.7	26.7	26.7	27.5	27.5	27.9
Gain (V/V)	288	299	295	306	306	309
v_{ni} (μV_{rms})	2.23	2.11	2.20	2.05	2.08	2.02
NEF	2.33	2.20	2.30	2.14	2.17	2.11

In order to make the loss of gain negligible, α was set to 100, assuring that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ due to $g_{m7}/100 = g_{m6}$ and $g_{m8}/100 = g_{m5}$.

We designed the amplifier for a gain of G = 50 dB, C_L = 5 pF and C_F = 47 pF. Both C_L and C_F were built as poly−poly capacitors for maximum linearity.

In order to achieve a very low high-pass frequency within a reasonable area and without an external capacitor, the lowest possible value for G_{mf} has to be taken. To have a G_{mf} around 1 nS the technique proposed in [34] that divides the current using series-parallel current mirrors was used. The current division factor implemented was $K_{G_{mf}}$ = 72.5, establishing a $f_{high-pass}$ = 18 Hz with an integrated capacitor C_F = 47 pF, and a $f_{high-pass}$ = 0.1 Hz with an external capacitor C_F = 10 nF. The same technique was used in Gm2 with a current division factor of $K_{G_{m2}}$ = 8.5 (in this case for noise reduction).

According to what was discussed in Section II-D and Section II-F, two techniques were implemented to guarantee a high CMRR. Firstly, the r_{tail} of the current source of Gm1 was increased by cascoding it. Secondly, as mentioned before, large M1, M2, M3 and M4 transistors were adopted, thus improving matching.

V_{DD} = 1.65 V and V_{SS} = −1.65 V were set. The dc gate voltage of M7 and M8 and the reference values of Gm2 and Gmf were set in $(V_{DD} + V_{SS})/2$ = 0 V. This 0 V voltage, the mid-point between the supply voltages, is hereinafter referred to as "ground", and the output is referred to this voltage. The common-mode voltage of the gates of M1 and M2 has to be higher than ground, so it was set to 0.6 V, this voltage is hereinafter referred to as "REF".

Fig. 4 shows a microphotograph of the fabricated chip. The area was not optimized. While the core of the amplifier occupies 0.335 mm^2 (including capacitors), biasing and testing circuits occupy 0.322 mm^2. The area of the biasing and testing circuits could be much reduced. The distribution of the area is as follows: A_{Gm1} = 0.219 mm^2 (65.37%), A_{Gmf} = 0.040 mm^2 (11.94%), A_{Gm2} = 0.021mm^2 (6.27%), A_{C_F} = 0.048 mm^2 (14.33%) and A_{C_L} = 0.007 mm^2 (2.09%).

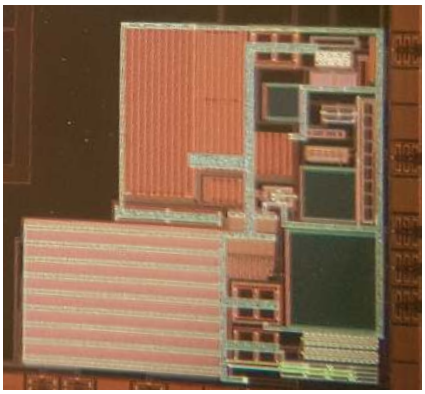

Fig. 4. Microphotograph of chip containing an amplifier with the proposed architecture.

The amplifier main parameters are presented in Table II.

TABLE II
AMPLIFIER MAIN PARAMETERS (POST-LAYOUT SIMULATIONS).

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InputPair}$	27.5 V^{-1}	9.3 V^{-1}	17.1 V^{-1}
$(g_m)_{InputPair}$	101 μS	2.7 μS	86 nS
G_m	100 μS	320 nS	1.2 nS
$(I_D)_{InputPair}$	3.67 μA	291 nA	5 nA
$(W/L)_{InputPair}$	7776/1.05	3.3/6	3/42
K_{G_m}	1.0	8.5	72.5
$(g_m/I_D)_{CM}$	2.5 V^{-1}	-	-
g_{m6}	735 nS	-	-
g_{m5}	710 nS	-	-
g_{m7}	91 μS	-	-
g_{m8}	83 μS	-	-

IV. EXPERIMENTAL RESULTS

A. Testbench results

This Section presents results of the laboratory characterization of two samples of the same chip (named IC#01 and IC#02) and post-layout simulations. The samples were randomly selected from the received prototype chips. The consistency between the results of the two samples, and the simulations including 500-runs Monte Carlo (MC) mismatch ones was deemed enough to confirm the expected performance of the chip. I_{DD} is the total current consumption of the amplifier, v_{ni} is the input-referred noise voltage, PSD corresponds to the noise power spectral density, PSRR+ is the positive power supply rejection ratio (V_{DD}), PSRR- refers to the negative power supply rejection ratio (V_{SS}), ICMR is the input common-mode range and "Output Offset" is the output dc voltage deviation from ground. To measure Gain and CMRR we used input signals of 1 mV$_{pp}$ and 100 mV$_{pp}$ respectively.

PSRR+ and PSRR- were measured by introducing a signal of 100 mV_{pp} and 50 Hz in the respective supply source. The simulations correspond to the typical value unless otherwise indicated.

Table III summarizes the main characteristics of the proposed amplifier. In general terms, expected theoretical values and simulation results agree with measured data in both chips. However, PSRR- with fully-integrated capacitors is lower than expected. This is because the integrated C_F = 47 pF was connected by mistake to V_{SS} instead of ground. The proposed architecture is very competitive with other amplifiers in the state-of-the-art as will be shown in Section IV-C.

TABLE III
EXPERIMENTAL RESULTS WITH FULLY-INTEGRATED CAPACITORS (FI) AND EXTERNAL CAPACITOR C_F = 10 NF (EXT).

	Simulation		IC#01		IC#02	
	FI	Ext	FI	Ext	FI	Ext
Gain (dB)	49.7	49.6	49.6	49.2	49.5	49.3
$f_{high-pass}$ (Hz)	17.9	0.1	13.0	0.1	12.0	0.1
$f_{low-pass}$ (kHz)	9.6	9.6	9.8	10.3	9.7	10.6
I_{DD} (μA)	8.10	8.10	8.48	8.45	8.41	8.49
v_{ni} (μV_{rms})*	1.92	1.96	1.88	1.94	2.03	2.07
NEF	2.15	2.19	2.13	2.14	2.30	2.25
Noise Int. Bandwith	3.2n-100M		0.03-25k		0.03-25k	
CMRR @ 1 kHz (dB)*	89.7	90.9	87.0	87.6	92.0	91.6
PSRR- @ 50 Hz (dB)*	35.2	68.1	35.1	63.2	35.0	67.1
PSRR+ @ 50 Hz (dB)*	73.7	82.1	74.9	72.4	76.9	86.4
Output Offset (mV)*	2.0	2.0	-1.4	-8.3	8.1	-3.0

* the simulation value corresponds to the mean value of the 500-runs MC simulation, otherwise the typical value is reported.

Fig. 5 shows the measured and simulated frequency response for two cases, fully-integrated capacitors and external C_F capacitor. Fig. 6 shows the measured and simulated CMRR for the fully-integrated capacitors version. The performance in terms of CMRR is outstanding: below 4 kHz is always greater than 80 dB, at this frequency it starts to fall, but at 10 kHz it is still greater than 70 dB. In addition, at 50 Hz the measured value is 90.3 dB, and the 500 runs MC simulation worst-case and best-case are respectively, 81.8 dB and 123.3 dB. In Fig. 7 the simulated and measured output-referred noise PSD with fully-integrated capacitors is depicted.

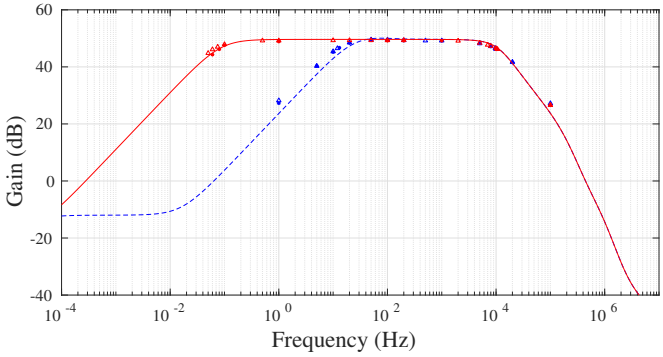

Fig. 5. Frequency response with fully-integrated capacitors (dashed line) and external capacitor C_F = 10 nF (solid line). Measurements (IC#01 = asterisks and IC#02 = triangles) and simulations (lines).

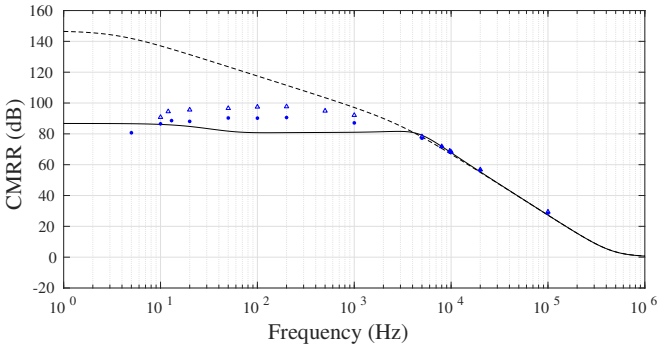

Fig. 6. Common-mode rejection ratio (CMRR) with fully-integrated capacitors. Measurements (IC#01 = asterisks and IC#02 = triangles), 500 runs MC simulation best-case iteration (dashed line), and worst-case iteration (solid line) are depicted.

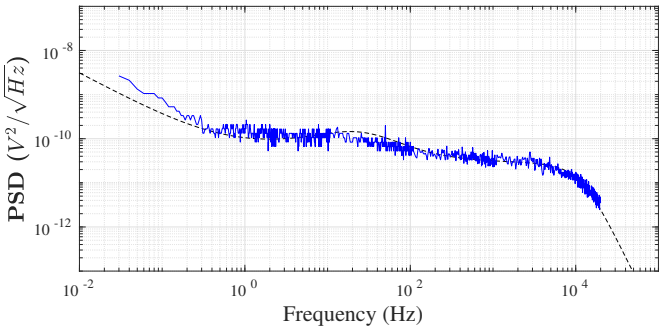

Fig. 7. Output-referred noise power PSD with fully-integrated capacitors. Measured at the output of IC#01 (solid line) and simulated (dashed line). Integration under the solid curve divided by gain G yields to an input-referred noise voltage of 1.88 μV_{rms}.

In Table IV gain measurements for different input dc voltages $V_{IN,dc}$ are presented. There it can be seen that the loss of gain is admissible for input dc voltages lower than 50 mV. In neural recordings this result is more than acceptable since the undesired input dc signals are typically in the range of 1 mV to 10 mV, and can be up to a maximum of 50 mV [35]. In addition, in many applications, small variations in the amplitude are not significant (e.g. spikes detection).

TABLE IV
VARIATION OF GAIN FOR DIFFERENT DC VOLTAGE INPUTS $V_{IN,dc}$ (MEASUREMENTS WERE PERFORMED AT 1 KHZ).

	Sim. Gain (dB)		IC#01 Gain (dB)		IC#02 Gain (dB)	
$V_{IN,dc}$	FI	Ext	FI	Ext	FI	Ext
0 mV	49.7	49.6	49.5	49.2	49.5	49.3
50 mV	41.4	41.4	41.9	40.7	40.3	40.6
100 mV	31.8	31.7	29.7	30.8	29.8	30.3

The amplifier input common-mode range ICMR is 380 mV (within a $\pm$1.65 V power supply). This value of ICMR assures a loss of gain lower than 0.5 dB and a CMRR greater than 80 dB (see Fig. 8). This ICMR is more than enough to accommodate typical common-mode signals. Fig. 8 shows that, in order to guarantee a loss of gain lower than 0.5 dB and a CMRR greater than 80 dB, the amplifier inputs need to be biased to a common-mode potential (REF) in the range from

0.32 V to 0.70 V being 0V the mid-point between the supply voltages. This can be easily implemented, as will be shown in the application example presented in Subsection IV-B (see Fig. 9).

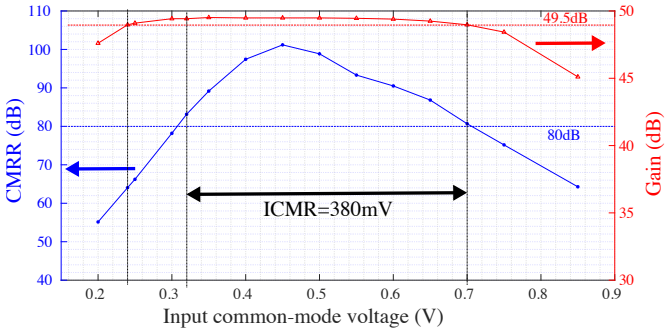

Fig. 8. Measurement of input common-mode range (ICMR) with fully-integrated capacitors. IC#01 Gain (red) and CMRR (blue) measurements for different dc input common-mode voltages (referred to ground). The figure shows that the ICMR is 380 mV (with a $\pm$1.65 V power supply). These measurements were performed at 200 Hz.

B. Weakly electric fish in-vivo recording

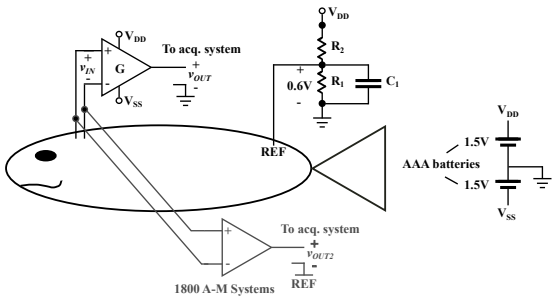

Fig. 9. In-vivo recording setup (still and freely-moving fish experiments).

Our amplifier has proved to be highly appropriate for in-vivo recording of LFPs and unitary signals from the brain stem of weakly electric fish *Gymnotus omarorum*.

Two in-vivo experiments were performed for testing our amplifier. Firstly, a freely-moving fish experiment with a pair of thin wires (60 μm diameter, insulated except at the tip), attached to the skull with dental cement, chronically-implanted at the mesencephalon (see Fig. 10). Secondly, an acute experiment with the fish still, consisted in a multitrode (Michigan type) inserted in the electrosensory lobe (one recording spot was connected to the amplifier positive input and a copper wire of 80 μm diameter insulated except at the tip was connected to the negative input).

In both experiments, the aforementioned electrodes were simultaneously connected to an unshielded custom PCB supporting our amplifier and to a standard shielded biopotential instrumentation system *Microelectrode AC Amplifier 1800* from *A-M Systems*. This amplifier features a CMRR greater than 80 dB, an input-referred noise of 3 μV_{rms} (10 Hz - 100 kHz), gain and bandwidth are programmable, and it is powered from the mains. Despite the fact that the Microelectrode AC amplifier 1800 was not designed to perform recordings in

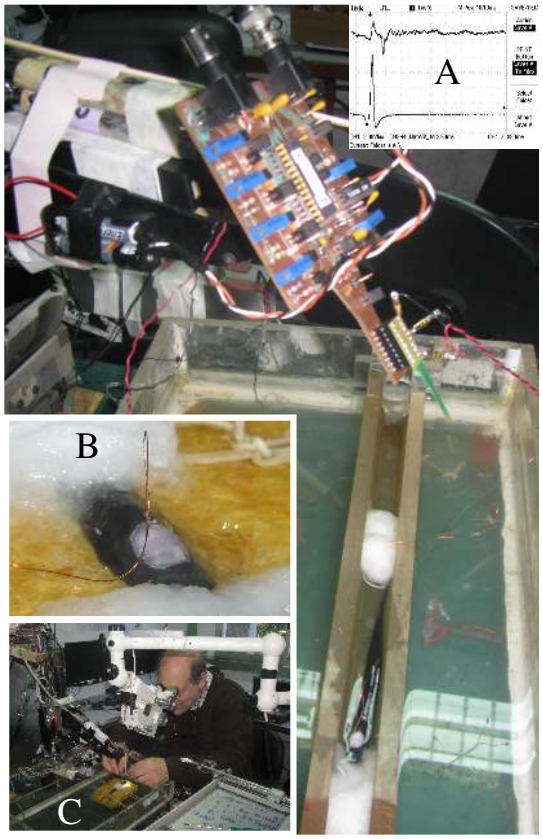

Fig. 10. In-vivo recording setup (freely-moving fish experiment). Main figure shows a fish chronically implanted at the mesencephalon with a pair of thin wires. The fish can swim in a mesh pen. Above the fish, an unshielded custom PCB supporting our integrated amplifier is shown. Inset panel A: fast field potential. Inset panel B: close up of the fish's head showing the fixation of the wires to the skull with dental cement. Inset panel C: surgical implantation.

freely-moving fish (mainly because of its size and the fact that it is powered from the mains), we were able to record simultaneously with both amplifiers, but fish movements were restricted in order to protect the animal. The output of both amplifiers were sampled through a *Datawave Technologies* acquisition system.

The experimental setup is shown in Figs. 9 and 10. A third wire placed at the dorsal muscle mass acted as a common-mode reference for both amplifiers (named REF in Fig. 9). The ground of our amplifier is referred to the fish (and to the rest of the acquisition system) by means of an auxiliary circuit formed by R_1, R_2 and C_1 (shown in Fig. 9). This circuit sets the middle point of our amplifier power supplies to a specific and configurable voltage below REF. According to what was discussed in Subsection IV-A, REF needs to be biased to a common-mode potential in the range from 0.32 V to 0.70 V being 0 V the mid-point between the supply voltages. In other words, the ground of our amplifier needs to be biased to a potential in the range from -0.32 V to -0.70 V (referred to REF). In these experiments the ground of our amplifier was set in -0.6 V from REF.

Fig. 11 shows the effect of the EOD at the output of the preamplifier, where it can be seen that the EOD is firing every 90 ms approximately. Note in this figure the perfect matching

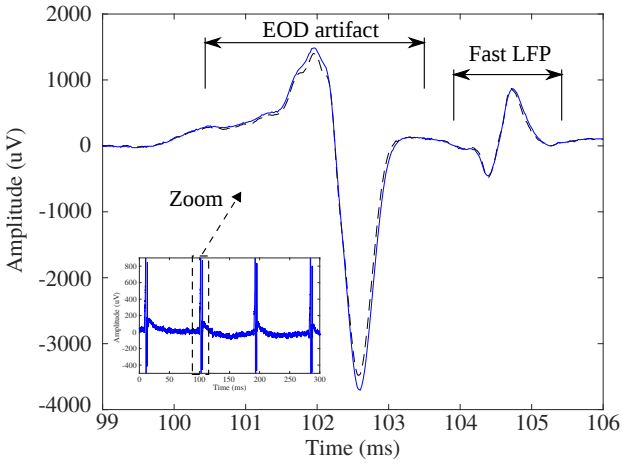

Fig. 11. In-vivo recording of a weakly electric fish *Gymnotus omarorum* (still fish experiment). Fast LFP and EOD artifact are indicated. In solid line the recording from our amplifier and in dashed line the one from the *Microelectrode AC Amplifier 1800* from *A-M Systems*. Each recorded signal is referred to the input of its corresponding amplifier (the amplitude of the output signal is divided by the amplifier gain).

of the signals recorded with our unshielded low-power amplifier (solid line) with those recorded with the shielded ac-plugged commercially available amplifier (dashed line). Fig. 11 and Fig. 10-A display in detail the EOD artifact and a short-latency fast LFP recorded in the acute and chronically implanted fish respectively. Fig. 12 shows a recording from a freely-moving experiment performed with another fish. In this case the EOD is firing every 50 ms approximately. A slow LFP can be observed, as well as the Fast LFP, the EOD artifact and unitary activity.

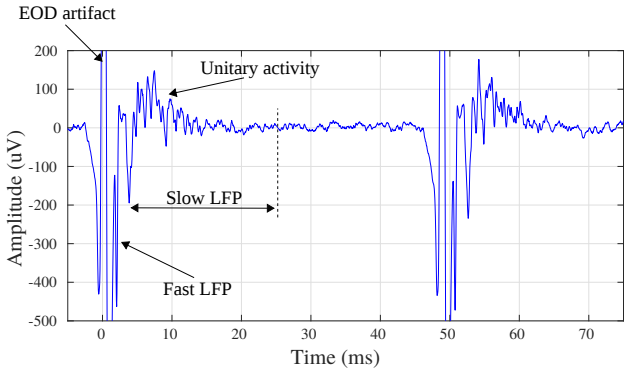

Fig. 12. *Gymnotus omarorum* in-vivo recording (freely-moving experiment).

Finally, Fig. 13 shows in-vivo neural unitary activity recordings obtained with our amplifier. The amplitude of the EOD measured at the inputs of the preamplifier was approximately 100 mV_{pp}. Therefore, in this particular experiment, we were able to accurately record 500 μV_{pp} spikes superposed to a 200 times higher EOD.

C. Comparison with previous work

Table V summarizes the main performance parameters of our preamplifier compared to state-of-the-art implementations.

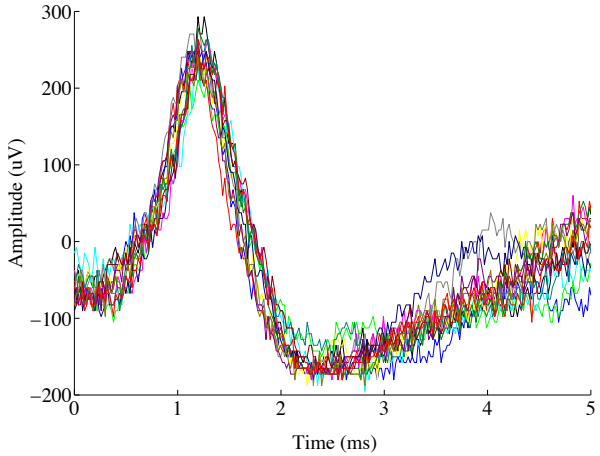

Fig. 13. Superimposed traces of a single unit repetitively active in the electrosensory lobe corresponding to the still fish experiment. Note the similarity of the time course and the large signal to noise ratio.

Over the last years remarkable research work has been done in this area. Amplifiers with outstanding CMRR results, or with good results of CMRR which specially take it into account or characterize it were selected from this rich background as well as those with reasonable CMRR performance and very good performance in NEF or input noise. The parameter "$CMRR_{worst-case}$" corresponds to a measured or simulated worst-case value. In our preamplifier we report the worst-case value at 50 Hz in a 500-runs MC simulation. In order to correctly compare input noise, PEF and NEF performance, it is important to consider the adequate noise integration bandwidth. For this reason, the measurements where the noise integration bandwidth only covers the amplifier bandwidth were marked with (*) in Table V. The actual NEF, PEF and input noise of these works, when integrated in the whole bandwidth, should be higher than the reported ones.

The power efficiency factor PEF (equal to $NEF^2 \times V_{DD}$, [36]) is considered in Table V. In battery powered systems (or powered through a linear regulator) the most relevant metric of consumption is the charge (or equivalently the current) drained from the battery. In these cases, the current-efficiency characterized by the NEF is the most appropriate figure of merit. When the amplifier is powered through a switched dc/dc converter, the power is the most relevant metric to assess consumption, since once we assume a given efficiency of the converter and battery voltage, the current consumed from the battery will be mainly determined by the power consumed by the amplifier. In this case, the power-efficiency, which can be assessed through the PEF, is the most appropriate figure of merit. Nevertheless, it must be noted that the PEF is strongly dependent on the supply voltage of the circuit, which in turn is dependent on the manufacturing process and its threshold voltage. The architecture presented here shows a similar or even a much better PEF than other circuits manufactured in similar processes, like [9], [10], [13], [17], or [28]. Another aspect directly related to the manufacturing process is the resulting area. This should be taken into account when comparing this characteristic of the design.

TABLE V
COMPARISON WITH PRIOR WORK.

	[9]	[10]	[11]	[13]	[14]	[15]	[16]	[17]	[18]	[28]	This work fully-int.	This work ext. C_F
Technology (μm)	1.5	0.5	0.13	0.35	0.35	0.18	0.18	0.35	0.065	0.35	0.5	0.5
Gain (dB)	39.5	40.8	47.5	65	40	52.0	40.0	40.8	52.1	46.0	49.5	49.2
$f_{low-pass}$ (kHz)	7.2	5.3	6.9	10.5	20	10.0	5.1	10.0	8.2	10.0	9.8	10.3
$f_{high-pass}$ (Hz)	25m	45	167	300	0.1	0.25	0.38	0.1	1.0	200	13.0	0.1
Supply current (μA)	16.0	2.7	1.6	4.3	2.0	1.6	0.8	4.3	3.3	22.4	8.5	8.5
Input noise (μV_{rms})	2.2	3.06	3.8	3.05	4.9 (*)	3.2 (*)	4.0 (*)	2.8	4.13 (*)	2.9	1.88	1.94
NEF	4.0	2.7	2.3	2.5	1.9 (*)	1.6 (*)	1.9 (*)	2.3	3.2 (*)	6.6	2.1	2.1
Noise integration bandwidth (Hz)	0.5-50k	10-98k	1-100k	0.5-50k	0.1-20k	1-10k	1-8k	0.05-200k	1-8.2k	N/A	0.03-25k	0.03-25k
$CMRR_{worst-case}$ (dB)	42	N/A	N/A	N/A	N/A	N/A	N/A	N/A	46	N/A	82	84
$CMRR_{measured}$ (dB)	83	66	83	65	90	73	60	70	80	110	87	88
THD 1% (mV_{pp})	16	7.3	3.1	N/A	N/A	N/A	9.0	3.0	0.7	>20	0.7	0.7
PSRR (dB)	85	75	70	50	80	80	70	70	78	110	74	82
Area (mm^2)	0.16	0.16	0.05	0.10	0.18	0.25	0.04	0.17	0.04	0.15	0.34	0.34
V_{DD} (V)	5.0	2.8	1.2	3.0	3.3	0.45	1.0	2.5	1.0	3.3	3.3	3.3
PEF	80	20.0	5.6	18.8	12.2 (*)	1.1 (*)	3.7 (*)	12.7	10.2 (*)	144	14.6	14.6

(*) Noise integration bandwidth only covers the amplifier bandwidth: actual PEF, NEF, and, input noise, when integrated in the whole bandwidth, should be higher than the reported ones.

Some existing works present an excellent value of CMRR (greater or equal to 90 dB), however they do not include a worst case or spread analysis that allows to assess the full CMRR performance in face of mismatches. Furthermore, these CMRR values are not achieved jointly with low NEF or low input noise. Table V shows that our work performs well in line with other state-of-the-art neural preamplifiers while providing enhanced CMRR performance. Indeed, our work is the best choice for applications that simultaneously seek low noise, high CMRR and current-efficiency.

V. CONCLUSIONS

This work presented a novel neural amplifier architecture, including silicon implementation and experimental characterization.

This architecture enables a low noise, high CMRR and current-efficient neural amplifier, with a high-pass frequency fixed without MOS pseudo-resistors.

A fully-integrated neural preamplifier, with an overall state-of-the-art performance and enhanced CMRR, was fabricated in a 0.5 μm CMOS process. Results from measurements show that the CMRR is greater than 87dB, the equivalent input noise is 1.88 μV_{rms} and the NEF is 2.1. To the best of our knowledge, this amplifier is the best option for applications that simultaneously need low noise, high CMRR and current-efficiency.

In addition, this work has presented in-vivo measurements made with the proposed architecture in a weakly electric fish (*Gymnotus omarorum*), showing the ability of the amplifier to acquire biopotential signals from high amplitude common-mode interference in an unshielded environment. Moreover, signals recorded with our unshielded low-power battery-operated amplifier perfectly match those recorded with a shielded ac-plugged commercial laboratory instrumentation system. Finally, the proposed amplifier has proved to be highly appropriate for in-vivo recordings of LFPs and unitary signals from the brain stem of a weakly electric fish.

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