Current Leads and Optimized Thermal Packaging for Superconducting Systems on Multistage Cryocoolers

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Abstract—**Packaging of a superconducting electronic system on a compact multistage cryocooler requires careful management of thermal loads from input and output leads, in order not to exceed the heat lift capacity of the various stages of the cooler. In particular, RSFQ systems typically require a large total bias current $I_b \sim 1$ A or greater. A general analysis of resistive wires shows that the tradeoff between heat flow and Joule heating yields a minimum heat load Q_{min} from optimized bias leads on a low-T stage, given by $Q_{min} \approx [0.3\ \mathrm{mW/(A-K)}]T_{hot}I_b$, where T_{hot} is the thermalization temperature of the leads on the previous (hotter) stage. This is independent of the material, number, and geometry of the leads, as long as the total lead resistance is optimized. A similar tradeoff between heat flow and signal attenuation can be applied to the optimization of high-frequency input/output lines. Superconducting leads are not subject to these limitations, and can result in further reduction in heat load. Design examples are presented for an RSFQ-based radio receiver on either a two-stage or a four-stage cooler.**

***Index Terms*—Cryocooler, cryopackaging, current leads, thermal optimization.**

I. Introduction

SUPERCONDUCTING electronic systems have typically had the appearance of laboratory experiments, with long cryoprobes immersed in a boiling bath of liquid helium, together with large numbers of wires and cables for biasing, signal input/output, and diagnostics, and racks full of custom equipment. If these systems are to move into the commercial market, they must be transformed into compact, complete turnkey systems, where the end user does not have to be familiar with cryogenics. With this in mind, the superconducting electronics industry has recently been developing systems on compact cryocoolers [1], with careful integration of electrical leads and interface electronics [2]. The present paper focuses on general strategies for optimization of the leads, subject to requirements of the circuits as well as thermal constraints of the cryocooler stages.

In particular, all-digital radio receivers [3] have been designed based on Nb integrated circuits operating at temperatures near 4.2 K. These incorporate many thousands of Josephson junctions operating as ultrafast rapid-single-flux-quantum (RSFQ) data converters [4] and logic circuits. Conventional RSFQ circuit architecture requires that most of the junctions are connected to a common ground and biased in parallel. Although the current per junction is only ~0.1 mA, the total bias current I_b for such a circuit (or combination of circuits) can easily exceed 1 A. If the electrical lead is a wire of electrical resistance R_{el}, then the Joule heating $I_b^2 R_{el}$ will contribute to the heat load on the cold stage of the cryocooler, and should be minimized. However, if R_{el} is small, then the thermal resistance $R_{th} \propto R_{el}$ (from the Wiedemann-Franz Law) will also be small, and too much heat could be conducted to the low-T stage (see Fig. 1). Clearly, there is an optimum resistance that will deliver the minimum heat load Q_{min} to the low-T stage, which takes a remarkably simple universal form [5] (derived below in Section II)

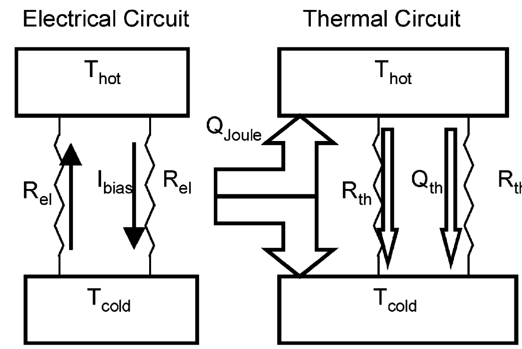

Fig. 1. Block diagram of electrical (left) and thermal (right) circuits associated with dc bias currents between two thermal stages on a cryocooler. The total heat load on the cold stage is given by (2) below.

$$Q_{\min}/I_b = V_{leads} = 2I_b R_{el} \approx 3.6 k_B T_{hot}/e \qquad (1)$$

where V_{leads} is the voltage drop (full circuit) on the leads, k_B is Boltzmann's constant, e is the electron charge, and T_{hot} is the hot temperature at which the leads are thermalized.

The result in (1) was previously derived many years ago [6] for leads to low-T_c superconducting (LTS) magnets, where $I_b \sim$ 100 A or greater, but is not widely known among the electronics community. Most LTS magnets operate in liquid He, and the heat load can be further reduced (by a factor of >40) by the use of vapor-cooled leads [7]. With recent efforts to move away from He immersion, (1) is again relevant.

Cryocoolers intended for deep cryogenic temperatures ($T_{cold} < 10$ K) invariably include at least one intermediate stage between room temperature (RT) and T_{cold}. This is particularly important for system wiring, in that it permits thermalization of current leads and other wiring from RT. This can substantially reduce the heat load on the lower-T stages, which tend to have much smaller heat-lift capabilities. Typical values of heat-lift (i.e., maximum heat load) are shown in Table I for two compact cryocooler designs, a commercial two-stage Gifford-McMahon cooler (Sumitomo SRDK-101D), and a new four-stage pulse-tube prototype currently being developed [8].

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TABLE I
TYPICAL HEAT LIFTS (mW) FOR COMPACT MULTISTAGE CRYOCOOLERS, AND MINIMUM HEAT LOADS (mW) DUE TO OPTIMIZED DC BIAS LEADS FOR $I_B = 1$ A

Stage	2-Stage		4-Stage	
Temp. [K]	Heat Lift	Heat Load	Heat Lift	Head Load
70	5000	90	5000	90
30	-	-	250	20
9	-	-	150	9
4	100	27	100	2.5

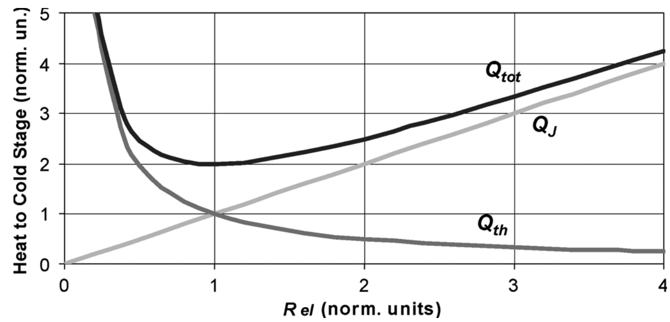

Fig. 2. Normalized plot of contributions to heat load on cold stage of cryocooler due to bias leads, showing optimum lead resistance.

Many superconducting electronic systems (such as the new digital-RF receivers) also require input and output of multiple high-frequency analog and digital signals of low amplitude. One conventional means for conveying such signals is a Cu coaxial line, for which signal attenuation is very small. However, Cu coax also conducts more heat than is desirable. Substitution of an alloy material (such as stainless steel) will reduce the heat load, but will also substantially increase the signal attenuation. So again, there is a tradeoff and optimization, although it is not quite as universal as that in (1). This will be discussed further in Section III.

A multistage cryocooler also permits one to use high-T_c superconducting (HTS) leads for $T < 80$ K. Properly designed HTS leads can carry large currents with no Joule heating and thermal load substantially less than that given by (1). In fact, high-current HTS leads designed for LTS magnets [9] have been developed and are commercially available. Unfortunately, lower-current HTS lead assemblies optimized for LTS electronic applications are not yet available. Considerations for such lead assemblies will be discussed in Section IV.

Finally, the result in (1) is not restricted to low T, but is a general consequence of optimizing thermal isolation in wiring between devices operating at different temperatures. A simple example, discussed briefly in Section IV, consists of a W filament in an incandescent light bulb. Application of (1) shows why any reasonably efficient flashlight requires at least two batteries. It is remarkable that this is a general consequence of the Wiedemann-Franz Law!

II. OPTIMIZATION OF DC BIAS LEADS

Consider the configuration indicated in Fig. 1, with a pair of bias leads between two thermal stages, labeled T_{hot} and T_{cold}. Assume for now that these leads are conventional resistive wires of resistance R_{el}, carrying a bias current I_b. Each wire generates Joule heat $Q_J = I_b^2 R_{el}$, which one can assume splits equally to the two stages. This is in addition to the usual thermal flow from the hot to the cold stage $Q_{th} = (T_{hot} - T_{cold})/R_{th}$, where R_{th} is the thermal resistance of the wire between the two stages. So the total heat load Q_{tot} on the cold stage due to the entire circuit is given by

$$Q_{tot} = 2Q_{th} + Q_J = \frac{2(T_{hot} - T_{cold})}{R_{th}} + I_b^2 R_{el}. \qquad (2)$$

Eq. (2) can now be minimized given the relation between R_{th} and R_{el}. This is based on the classic microscopic Wiedemann-Franz Law (WF) relating the thermal conductivity κ to the electrical conductivity σ. $\kappa = L\sigma T$, where $L = \pi^2 k_B^2/3e^2 = 2.45 \times 10^{-8}$ WΩ/K^2 is the Lorenz constant. WF is valid over for a wide range of metals, both pure and alloyed, over a wide range of temperatures. The major deviations from WF are in pure metals at low temperatures, but for wiring in cryogenic systems (typically Cu alloys), WF holds quite well. WF does not apply, of course, to superconductors.

By comparison with the microscopic relation, one expects a macroscopic WF relation of the form $R_{th} = R_{el}/LT^*$, where T^* is an appropriate average between T_{cold} and T_{hot}

$$T^* = \frac{R_{el}}{LR_{th}} = \frac{\int dz/\sigma A}{L \int dz/\kappa A} = \frac{\int T dz/\kappa A}{\int dz/\kappa A} \qquad (3)$$

where A is the cross-section of the wire, and z is the coordinate along the length of the wire, from cold to hot. When the Joule heating is small, the heat flowing along the line $Q = \kappa A\, dT/dz = \text{constant}$, and one can change variables in (3) from z to T using $dz = \kappa A dT/Q$, to obtain

$$T^* = \frac{\int T dT}{\int dT} = \frac{\left(T_{hot}^2 - T_{cold}^2\right)/2}{(T_{hot} - T_{cold})} = \frac{T_{hot} + T_{cold}}{2}. \qquad (4)$$

Using this macroscopic WF relation, (2) then becomes

$$Q_{tot} = L\left(T_{hot}^2 - T_{cold}^2\right)/R_{el} + I_b^2 R_{el} \qquad (5)$$

which has a minimum when the two terms are equal, as shown in Fig. 2. This corresponds to an optimum lead resistance

$$R_{el} = \frac{\sqrt{L\left(T_{hot}^2 - T_{cold}^2\right)}}{I_b} \approx \frac{\sqrt{L} \cdot T_{hot}}{I_b} = \frac{\pi}{\sqrt{3}} \frac{k_B T_{hot}}{e I_b} \qquad (6)$$

where the approximation is for the common case that $T_{cold} \ll T_{hot}$. This, in turn, gives the total voltage drop on the leads (full circuit) as

$$V_{lead} = 2 I_b R_{el} \approx 3.6 k_B T_{hot}/e \qquad (7)$$

and the total heat load on the cold stage as

$$Q_{tot} = 2 I_b^2 R_{el} = V_{lead} I_b \approx 3.6 (k_B T_{hot}/e) I_b. \qquad (8)$$

Furthermore, there is no net heat load of either sign on the hot stage; the heat flow to the cold stage is canceled by the equal and opposite Joule heat from the wire. The assumptions in this lumped-element derivation given here may seem arbitrary, but they are validated by the integro-differential equations of the full microscopic treatment [6], [7], which gives the same results without requiring assumptions.

The expressions of (7) and (8) in terms of $k_B T_{hot}/e$ could almost have been guessed by dimensional analysis. Furthermore, although the true microscopic picture involves diffusion of large numbers of electrons, the formulas seem to suggest simple transfer of energy $\sim k_B T_{hot}$ by each electron being carried by the current I_b from the hot stage to the cold stage, together with another $\sim k_B T_{hot}$ that the electron acquires from the electric field in the wire.

Consider the application of these simple formulas for a superconducting electronic system that requires a total $I_b \sim 1$ A, a typical value for a moderately complex RSFQ circuit. Then, for sample two- and four-stage cryocooler stages, optimized heat loads on each stage are shown in Table I. This assumes that the wiring from $\mathrm{RT} = 300$ K is properly thermalized on each successively lower thermal stage. Note that these heat loads are well below the heat lifts for the corresponding stages. Note also that for leads coming directly from RT to 4 K without thermalization, the optimized heat load would be 93 mW, close to the heat lift for the 4 K stage. This points out the necessity of proper thermalization, which in any case is established practice in cryogenic design.

It is clear that additional stages provide a substantial reduction in the heat load on the lowest-T stage, which tends to have the least available heat lift. Furthermore, the 4 K stage must also accept any power dissipated by the RSFQ circuits. These circuits are well known for their very small power consumption, they are typically biased at $V \sim 3$ mV, corresponding to a power ~3 mW for $I_b = 1$ A. Finally, the 4 K stage also has the most stringent temperature requirement, since it determines the operation of the RSFQ circuits. So although the two-stage cryocooler would appear sufficient for $I_b = 1$ A, the four-stage cooler has greater capacity for scaling to larger I_b for more complex superconducting systems.

Of course, the bias leads are not the only source of heat load. In particular, thermal radiation from RT ($\propto T^4$) can be quite large (~2 W or more), and must be intercepted by a heat shield thermalized on the 70 K stage. So the 5 W of heat lift on this stage does not provide quite as much margin as it might seem. In addition, high-frequency lines can also contribute significantly to the heat load, as discussed below.

The same values of Q_{min} in Table I also represent V_{leads} (in mV) and $2R_{el}$ (in mΩ) for wires between adjacent stages, since $I_b = 1$ A. The total $V_{leads} \sim 120$ mV is in addition to the voltage (~3 mV) across the RSFQ circuit itself. If R_{el} represents a single wire, then it can easily be achieved using reasonable lengths of fine Cu wire. However, more commonly (at least for prototype superconducting circuits), I_b is supplied through a number of parallel wires. For example, one might have 25 supply lines, each carrying ~40 mA, which could be independently adjusted to optimize circuit performance. Note that this does not change Q_{min} or V_{leads}, but R_{el} would increase by a factor of 25. In this case, one might use a Cu-alloy wire (e.g., phosphor bronze) for convenient wire diameters and lengths. For example, consider an alloy with resistivity $\rho \sim 10\ \mu\Omega-\mathrm{cm}$. Then for a wire 0.3 mm in diameter, $R_{el} = 14\ \mathrm{m}\Omega/\mathrm{cm}$, with optimum length L between the 30 K and 9 K stages of ~8 cm. Note that the current density J is very small, $\sim 50\ \mathrm{A/cm^2}$. This follows generally from $J\rho L = 1.8 k_B T_{hot}/e$, for typical values of L and ρ.

III. High-Frequency Input/Output Lines

Many applications of RSFQ circuits require input and output of high-speed signals. These may include weak analog microwave signals, as in a sensitive receiver, and also high-speed (GHz) low-level digital signals (~1 mV), as in the output of a digital receiver. For such signals, one must use a proper transmission line, rather than simply wires, to avoid attenuation, dispersion, and cross-talk. Generally, multiple independent lines (e.g., 50) are required. Coaxial lines with characteristic impedance $Z_0 = 50\ \Omega$ are typical. Alternatively, one may use microstrip or stripline multi-conductor assemblies. In either case, to avoid excessive heat loads, one should properly thermalize each line on each temperature stage of the cryocooler. This is particularly critical if a large number of high-speed lines are required.

The main electrical constraint for high-speed lines is not the current that they need to carry (generally small), but rather the attenuation over the full length from 4 K to 300 K. For example, if the signal amplitude is 1 mV, that corresponds for $Z_0 = 50\ \Omega$ to $I = 20\ \mu\mathrm{A}$. Even for 50 lines, that is a total of only 1 mA. But attenuation of such weak signals is a serious problem, since it adds to noise and bit errors. Attenuation A is proportional to the RF resistance R_{RF} of the transmission line, which includes the series resistance of both signal and ground conductors [10]: $A = 8.68\ \mathrm{dB}\ R_{RF}/2Z_0$, Because of skin depth effects, R_{RF} is generally much larger than the DC resistance R_{DC} of the line. For example, the skin depth δ of Cu at 1 GHz is about $2\ \mu\mathrm{m}$, and even smaller at reduced T. So only a thin conductor layer is actually carrying RF electrical current, while the entire thickness is carrying DC *thermal* current.

For example, if one can tolerate $A = 1$ dB at 1 GHz for the line segment between 300 K and 70 K, then for $Z_0 = 50\ \Omega$, $R_{RF} = 12\ \Omega$. This corresponds to $\sim 6\ \Omega$ for each of the signal and ground conductors in series, but the heat flows in parallel, corresponding to an effective parallel resistance of 3 Ω for the transmission line. R_{DC} would be even smaller, reduced by the ratio of the conductor thickness to the skin depth (d/δ). If we select a conductor with $d/\delta \sim 10$, then $R_{DC} = 0.3\ \Omega$. From Section I, this corresponds to a heat leak to the 70 K stage (assuming Joule heating is negligible) of $Q = LT^* \Delta T/R_{DC} = 3.5\ \mathrm{mW}$. If we have 50 such lines, the total heat load would be 170 mW. This may well be acceptable, but can we find a line that exhibits these properties, for reasonable lengths? One approach is to use an alloy conductor, such as stainless steel, with $\delta \sim 7$ times larger than that of Cu and negligible T-dependence. We have evaluated thin commercial all-stainless coaxial lines, as well as multi-conductor microstrip ribbons with a Cu alloy conductor. Both approaches seem feasible, although they must be carefully engineered for the specific configuration. In each case, we want to minimize the "extra" conductor thickness, not required for RF electrical conduction in the critical frequency range.

IV. Discussion and Conclusions

Superconductors violate the WF relation, since Cooper pairs carry electrical current with no loss, but cannot transport heat. HTS materials may provide possible alternatives for both DC and RF lines, from the 70 K stage down to lower T. Although we have shown that properly engineered lines are compatible with compact cryocoolers for prototype superconducting electronic systems, HTS leads may permit scaling to much larger total currents and numbers of leads. HTS leads are already available for LTS magnets with $I_b > 100$ A, but leads for $I_b < 1$ A are not. The problem is that these leads exhibit κ comparable to that in normal metallic alloys; in fact, they are typically clad in Ag(Au) alloys for stabilization. But even without such cladding, superconductors do *not* exhibit poor κ, except for $T \ll T_c$, when only Cooper pairs (and not quasiparticles) are present. For example, for YBCO in the ab conduction direction, $\kappa \sim 10\ \mathrm{W/m-K}$ at 20 K [11]. The real advantage of the superconductors is that they can carry a large current density with no Joule heating, regardless of length. Rather than an optimum $J \sim 50\ \mathrm{A/cm^2}$ as in the Cu alloy wire above, one may have $100\ \mathrm{kA/cm^2}$ for the HTS wire. For the same total current, that permits one to reduce the cross-section by a factor of 2000, which of course reduces the heat leak proportionally. However, for $I_b < 1$ A, such a small wire would not be self-supporting, and must be integrated with other wires onto a non-metallic package that is not too thermally conductive. This suggests a thin-film multi-conductor structure on a substrate.

Similar arguments may be made for application of HTS leads to RF transmission. The RF surface resistance is non-zero, but is orders of magnitude smaller than that of normal metals well into the GHz range. Here the magnetic penetration depth $\lambda \sim 0.1\ \mu\mathrm{m}$ plays the role of the RF skin depth δ. A thin-film HTS microstrip structure can carry an RF signal (up to quite large amplitudes) with negligible attenuation. Such structures are not needed for prototype development of LTS electronic circuits, but may be appropriate for future generations of complex RSFQ circuits.

This paper has focused on thermal integration of wiring for cryogenic systems, but parts of the analysis are more general. In particular, optimization of thermal isolation for a high-T electrical system is essentially the same. Consider for example a W filament in a light bulb, designed to operate at $T_{hot} = 3000$ K, provided by electrical heating. If R_{el} is too small, then too much heat will be conducted away, reducing the efficiency. If R_{el} is too large, then most of the power will go towards heating the leads rather than the filament. This is the same problem illustrated in Fig. 1, and since WF also applies to metals at high T, this yields an optimum $V_{leads} = 3.6 k_B T_{hot}/e = 0.9$ V. Most conventional flashlights have two batteries giving a source voltage of 3 V, so that most of the power goes into heating the filament. One can find small keylights that operate on a single 1.5 V battery, but most of the power is wasted in the leads, so that they are rather inefficient.

In conclusion, we have shown how the requirement of good thermal isolation in wiring of LTS electronic systems on multistage cryocoolers can be solved using some very simple and universal formulas for optimization of lead resistance, based on the Wiedemann-Franz law. For prototype RSFQ digital-RF receiver systems and compact cryocoolers, this packaging can easily be achieved using properly selected normal-metal alloy wires. If future generations of complex superconducting systems require much larger bias currents or larger numbers of RF input/output lines, HTS multi-line structures may provide a solution.

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