

Research Article **Current Mode Full-Wave Rectifier Based on a Single MZC-CDTA**

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Received 30 March 2013; Revised 14 June 2013; Accepted 15 June 2013

Academic Editor: Ali Umit Keskin

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This paper presents a current mode full-wave rectifier based on single modified Z copy current difference transconductance amplifier (MZC-CDTA) and two switches. The circuit is simple and is suitable for IC implementation. The functionality of the circuit is verified with SPICE simulation using 0.35 μ m TSMC CMOS technology parameters.

1. Introduction

The full-wave rectifiers are used in varied applications [5-8] such as signal-polarity detectors, averaging circuits, peak value detectors, clipper circuits, and amplitude-modulated signal detectors. Conventionally, full-wave rectifier is implemented using operational amplifiers which are not capable of operating at higher frequencies because of slew rate and fixed gain-bandwidth product limitations [9]. Current mode approach due to its inherent wide bandwidth which is virtually independent of closed loop gain, greater linearity, and large dynamic range [9] has generated lots of interest, and significant research efforts have been directed towards developing new active blocks based on this approach. Among these blocks, CDTA [10-12] has received considerable attention as the external resistors may be implemented by TA block of CDTA, thereby reducing/avoiding external resistors usage in the applications based on CDTA [12] and making these suitable for on-chip implementation. Additionally, due to low input impedance terminals, CDTA is free from parasitic capacitances and hence is appropriate for high frequency operation. This has resulted in development of a wide range of CDTA-based applications [1-4, 11-17].

A variety of FWR circuits using CDTA [1–4] have been reported in the literature. The CDTA-based FWR circuits presented in [1–3] use single CDTA, whereas configuration reported in [4] employs two CDTAs and a multiple output current follower. The structures [1, 2, 4] use four pn junction diodes, whereas two Schottky diodes are used in [3]. Additionally, auxiliary bias is employed in [1] and a grounded resistor is employed in [4]. In this paper, a new approach for designing a single CDTA-based current mode full-wave rectifier (FWR) configuration is presented. The proposed current mode FWR configuration uses a single CDTA called MZC-CDTA (modified Z copy CDTA) and two MOS switches. The features of the CDTA-based FWR circuits are summarized in Table 1. It may be noted that the proposed FWR uses similar a number of active elements as given in [3]; however, the use of MOS switches makes it more suitable from integration viewpoint. The functionality of the circuit is verified with SPICE simulations using $0.35 \,\mu$ m TSMC CMOS technology parameters.

2. Circuit Description

The circuit symbol of MZC-CDTA is shown in Figure 1. It is similar to ZC-CDTA except for an extra zc- port. The port relationship of the MZC-CDTA is characterized by the following matrix:

Ref. No.	Number of CDTAs	Additional active block	Number/type of passive elements	Auxiliary bias current sources
[1]	1	4 pn junction diodes	_	Yes
[2]	1	4 pn junction diodes	_	No
[3]	1	2 Schottky diodes	_	No
[4]	2	Multiple output current follower, 4 pn junction diodes	1 grounded resistor	Yes
Proposed	1	2 MOS transistors	_	No

TABLE 1: Summary of available CDTA-based FWR.

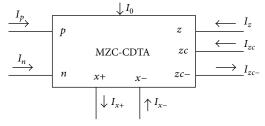


FIGURE 1: Circuit symbol of MZC-CDTA.

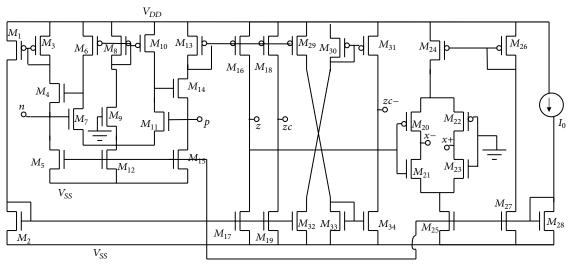


FIGURE 2: MZC-CDTA implementation.

where g_m is transconductance of the MZC-CDTA. The CMOS-based internal circuit of MZC-CDTA is depicted in Figure 2 and is based on the CDTA schematic given in [1]. The value of transconductance (g_m) is expressed as

$$g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right)_{21,23} I_0},\tag{2}$$

which can be adjusted by bias current I_0 of MZC-CDTA.

The proposed MZC-CDTA-based full-wave rectifier is shown in Figure 3. It uses a single MZC-CDTA and two MOS switches (M_{p1} and M_{n1}) connected at zc and zcports, respectively. The z port being open, its voltage would approach to V_{DD} or V_{SS} depending upon the current flowing into p terminal. Further, as x- terminal of the circuit is also

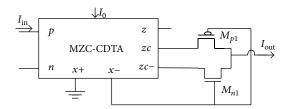


FIGURE 3: Proposed current mode rectifier.

not drawing any current, so for small current inputs, it would be saturating to supply voltage, resulting in

$$V_{x-} = V_{DD} \quad \text{for } I_{\text{in}} \le 0,$$

$$V_{x-} = V_{SS} \quad \text{for } I_{\text{in}} \ge 0.$$
(3)

At any instant, either of the two transistors M_{p1} and M_{n1} will be in ON condition as the current through zc and zc– ports is out of phase. The transistor M_{p1} will be ON for positive input currents, whereas the negative input current will bring transistor M_{n1} in ON condition thereby making I_{out} a unidirectional current.

3. Nonideal Analysis

The actual behavior of the circuit may deviate from the ideal one due to error in current transfer from p and n terminals to z, zc, and zc- terminals and also current at x+ and x- terminals. The current transfer from p and n ports to z, zc, and zc- ports may differ from unity value, and these tracking errors are represented by α_p and α_n . The inaccuracy in transconductance transfer from z to x+ and x- ports is modeled by $\beta g_m V_z$. Considering the inaccuracies outlined earlier, the output current I_{out} becomes a unidirectional current of value $\alpha_p |I_{in}|$. Depending upon the internal structure and technology used, the tracking errors α_p , α_n , and β also have first-order low-pass rolloff which affects the performance at high frequencies.

Apart from the error in the current transfer, there are parasitic impedances at p and n ports (resistances R_p and R_n) and shunt output impedances (R//C) at ports z, zc, zc-, x+, and x-. The input current is applied at p port in the proposed circuit and n port is left open, so resistances at p and n ports do not put restriction in the behavior of the circuit. The impedances at z, zc, zc-, x+, and x- ports will have an impact at higher operating frequencies.

4. Simulation Results

The functionality of the proposed current mode rectifier is validated using MZC-CDTA schematic of Figure 2. The model parameters of TSMC $0.35 \,\mu m$ CMOS process and supply voltages of $V_{DD} = -V_{SS} = 1.8$ V are used. The aspect ratios of various transistors are taken from [16], and the bias current of 60 μ A is used. The circuit of Figure 3 is excited by a 10 KHz, 20 μ A sinusoidal current signal. The time domain behaviour of voltage developed at x- port due to input current is shown in Figure 4. For positive half-cycle of the input current, a negative voltage is developed at x- port which in turn makes the transistor M_{p1} ON, whereas transistor M_{n1} remains OFF, and thus output current I_{out} is equal to input current for positive half-cycle. The negative half-cycle of the input current makes x- port voltage positive and turns transistor M_{n1} ON. The current through transistor M_{n1} is out of phase with input current, and therefore the output current would be positive. The input and output currents for the proposed circuit under sinusoidal excitation are shown in Figure 5 and conform to the theoretical predictions. The simulated ripple factor curve is plotted in Figure 6 and its value is approximately 0.5. Figure 7 shows the response of the circuit under sinusoidal excitation. The simulated total power consumption of the circuit is 14 mW.

The DC response of the proposed circuit is also studied and the transfer characteristics are shown in Figure 6. It may

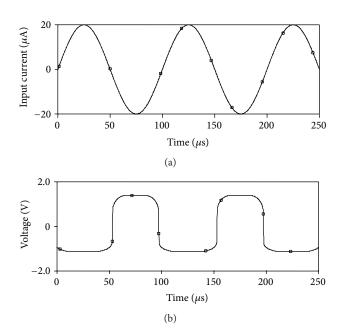


FIGURE 4: Time domain response of input current and x- port voltage.

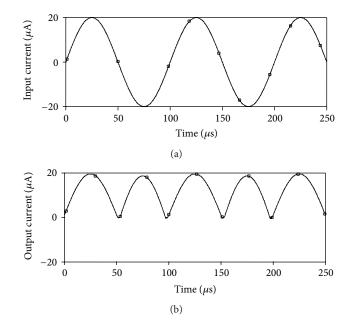


FIGURE 5: Input and output waveforms for sinusoidal excitation.

be noted that the proposed circuit behavior is linear for input currents ranging between $-300 \,\mu\text{A}$ and $+300 \,\mu\text{A}$. The positive and negative slopes of 0.967 and 0.993, respectively are observed. The deviation of slope from unity value may be attribute to CDTA nonidealities.

The proposed circuit is also tested to judge the level of harmonic distortion at the output of the signal. The %THD result is shown in Figure 9 which shows that the output distortion is around 22% for input currents up to $300 \,\mu\text{A}$.

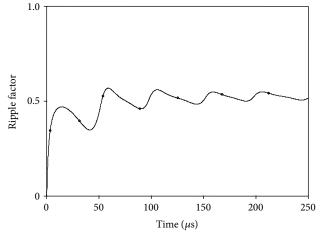


FIGURE 6: Simulated curve for ripple factor.

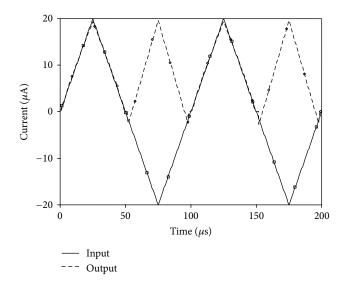


FIGURE 7: Input and output waveforms for triangular excitation.

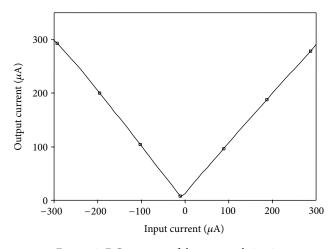


FIGURE 8: DC response of the proposed circuit.

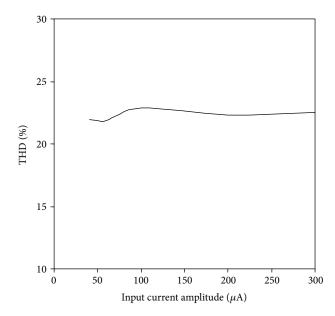


FIGURE 9: Percentage THD versus input bias current.

5. Conclusion

A single MZC-CDTA-based current mode full-wave rectifier is presented in this paper. It uses two switches. As the circuit uses only MOS transistors, it is suitable for IC implementation. SPICE simulation results using $0.35 \,\mu\text{m}$ TSMC CMOS technology parameters are given in support of the theory (see Figure 8).

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