Current mode with RMS voltage and offset control loops for a single-phase aircraft inverter suitable for parallel and 3-phase operation modes

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***Abstract*—Rms voltage regulation may be an attractive possibility for controlling power inverters. Combined with a Hall Effect sensor for current control, it keeps its parallel operation capability while increasing its noise immunity, which may lead to a reduction of the Total Harmonic Distortion (THD). Besides, as voltage regulation is designed in DC, a simple PI regulator can provide accurate voltage tracking.**

Nevertheless, this approach does not lack drawbacks. Its narrow voltage bandwidth makes transients last longer and it increases the voltage THD when feeding non-linear loads, such as rectifying stages. On the other hand, the implementation can fall into offset voltage error. Furthermore, the information of the output voltage phase is hidden for the control as well, making the synchronization of a 3-phase setup not trivial.

This paper explains the concept, design and implementation of the whole control scheme, in an on board inverter able to run in parallel and within a 3-phase setup. Special attention is paid to solve the problems foreseen at implementation level: a third analog loop accounts for the offset level is added and a digital algorithm guarantees 3-phase voltage synchronization.

I. INTRODUCTION

Aeronautic products demand special requirements of the electronics on board. Weight and size restrictions highly condition the magnetic components and, as a consequence, the output filtering. Besides, reliability issues applying to the whole system and its components are much stricte.

This paper deals with the control of a single-phase on board power inverter. The power subsystem is made up of two stages. A first DC-DC converter boosts the DC voltage of the aircraft standard bus from 28V up to 200V. In a second stage, a full-bridge DC-AC power topology generates the sine waveform required at the output terminals. A general scheme of the architecture with the application data is provided by Fig. 1. Modular operation modes in a parallel scheme and/or in a 3-phase setup are required as well.

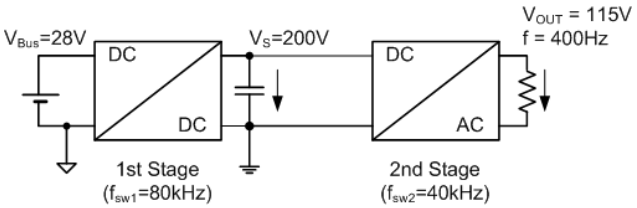


Figure 1. General scheme and data of the power architecture in this application.

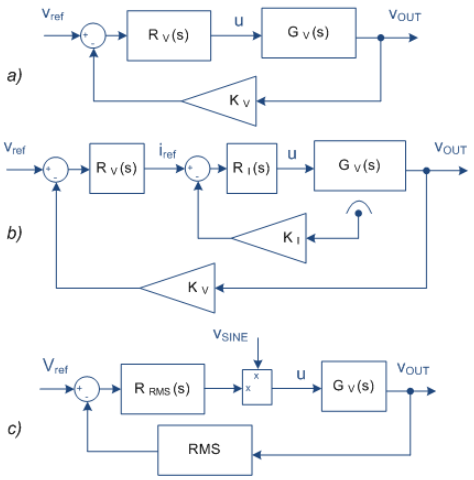


Figure 2. Block diagram representation of usual control schemes for power inverters: VMC (a), MCMC (b) and rms voltage control (c).

Several different control schemes are available for controlling DC-AC converters, summarized in Fig. 2. Classic linear approaches [1] apply just an instantaneous output Voltage Mode Control (VMC) or they combine it with a Mean Current Mode Control (MCMC). The instantaneous voltage loop within these two options may incorporate a resonance at the output frequency for enhancing such instantaneous tracking, case of the resonant regulators [2].

Other alternatives [3, 4] simply apply an rms voltage regulation. Such control loop works in DC, and the control signal for the Pulse Width Modulation (PWM) block is generated by modulating the amplitude of a constant frequency sine reference by means of the voltage compensator output signal.

The use of a current loop brings the possibility of running several converters in parallel without any extra control. Alternatively, there are other research lines for explicitly controlling the parallel operation of converters using VMC [5] for the main regulation.

II. CONCEPT OF THE CONTROL

In this control proposal, Fig. 3, the voltage loop controls the output rms voltage, v_{RMS}, by means of regulator $R_V(s)$, which modulates the amplitude of the sine current reference. Therefore, that signal, $i_{ref,AC}$, must be multiplied by a constant frequency and amplitude sine waveform, v_{SINE}. The inner current loop, regulator $R_I(s)$, controls the inductor current, i_L, generating the control signal, u, which is applied to the PWM comparators.

The rms voltage measurement is obtained by rectifying and filtering an instantaneous measurement of the output

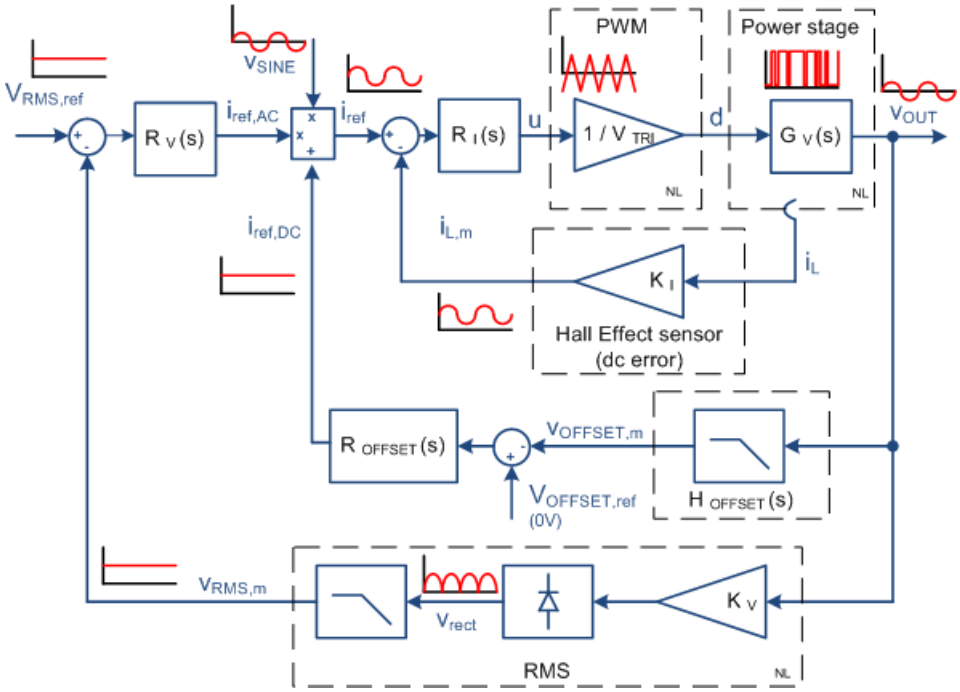


Figure 3. Block diagram of the control proposal with conceptual waveforms to distinguish DC and AC control loops.

The control scheme proposed in this paper presents an analog mean current loop whose sine current reference amplitude comes from an analog rms voltage loop [6]. Such rms voltage magnitude, combined with Hall Effect current sensing, represents the foundations of a control expected to provide low Total Harmonic Distortion (THD) due to avoiding the introduction of any instantaneous voltage measurement directly into the control. Independently from the regulation, for driving the switches at the power stage, the modulation scheme chosen is the unipolar sine PWM, since it is the modulation that brings the lowest THD for the same filter and switching frequency [7].

Following sections explain the basis and design of the control scheme proposed, analyzing advantages, limitations and application scope of the proposal. Nevertheless, the main objective is to transmit how to solve the problems that the instantaneous voltage tracking removal causes, foreseen from the conception stage and confirmed during the implementation. These drawbacks are, mainly, offset deviation appearance and voltage synchronization loss.

voltage. Such instantaneous measurement, gain K_V, comes from a differential op-amp configuration, which subtract the scaled voltage values of both output terminals. It is important to highlight that the voltage ground of the control stage is in this case the negative terminal of the input voltage -internal bus, V_S=200V-, which varies with regard to the negative output terminal at switching frequency. This might represent a noise source for an instantaneous voltage control.

Hall Effect sensors are sensitive to supply voltage asymmetries by nature. Therefore, current measurement, $i_{L,m}$, might present an offset error at its output, and be no longer gain K_I but $K_I+\Delta I$. Usually, such error gets corrected by the instantaneous outer voltage loop, which provides the needed DC value. In this proposal, this correction is impossible as long as the offset deviation is completely hidden for an rms voltage magnitude.

Accounting for offset correction, an offset loop is placed in parallel with the rms loop. By means of regulator $R_{OFFSET}(s)$, the DC reference for the current, $i_{ref,DC}$, is set, based on measurement $V_{OFFSET,m}$, which is obtained from a

low-pass filtering arrangement, $H_{OFFSET}(s)$, similar to the one in the rms measurement. Therefore, the current reference, i_{ref}, is indeed made up by the sum of signal $i_{ref,DC}$ and the product of $i_{ref,AC}$ and v_{SINE}. Commercial analog multipliers, such as AD633, actually incorporate an extra summing point, performing function x·y+z, perfect for this purpose.

III. Design Of The Control

The 3-loop control is implemented using analog regulators: op-amp differential structures with RC networks. First of all, transfer functions $G_V(s)$ (1) and $G_I(s)$ (2), are introduced. They represent dynamics from duty cycle d to generated instantaneous output voltage v_{out} and to instantaneous inductor current i_L, respectively, in a buck-derived converter [1].

$$G_V(s) = \frac{\tilde{v}_{out}}{\tilde{d}} = \frac{\frac{V_S}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (1)$$

$$G_I(s) = \frac{\tilde{i}_L}{\tilde{d}} = \frac{V_S}{L} \cdot \frac{s + \frac{1}{RC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (2)$$

A. Current Loop

The design of the current loop regulator $R_I(s)$ is done in agreement with the scheme in Fig. 4, which contains only linear elements. The design process is performed by means of classical techniques, using a PID-derived structure. Nonetheless, the proximity over the spectrum between switching frequency, f_{sw2}, and output frequency, f, involves a trade-off which must be taken into account. It is desirable to have a high gain at 400Hz for properly tracking the current reference, as well as a good attenuation at high frequency for preventing the harmonic content from becoming manifest at the output voltage. In this case, the regulator is designed to favor the attenuation at high frequency, in order not to penalize the output voltage THD, and to have a great phase margin for ensuring the system stability. Therefore, the current loop is only asked to provide a robust sine signal output, not expecting a perfect current tracking.

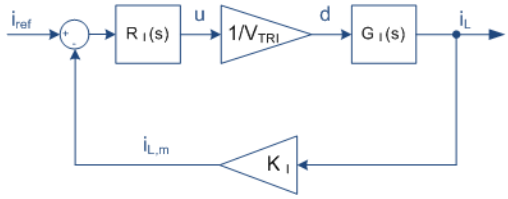


Figure 4. Current loop control scheme.

B. Rms Voltage Loop

The voltage loop is designed based on scheme of Fig. 5, which deals only with DC magnitudes. For deriving such linear scheme from the real one, Fig. 3, it becomes necessary to assume a voltage loop much slower than the current loop. Hence, a change in the amplitude current reference, $i_{ref,AC}$, is considered to get translated instantaneously into a current amplitude change and, therefore, a rms voltage change. Furthermore, if all this is seen by slow voltage regulator, signal v_{rect} -output of the rectifier- can be assumed equal to its average value. Being Z_{RC} the parallel impedance of load R and output capacitor C and keeping in mind the relationships between peak and rms values of a sine waveform and a full-wave rectified one [7], the rectifier may be substituted by gain K_{RMS} (3) and the plant to be controlled, simplified to gain G_{RMS} (4).

$$K_{RMS} = \frac{\bar{v}_{rect}}{V_{RMS}} \cong K_V \cdot \frac{2\sqrt{2}}{\pi} \quad (3)$$

$$G_{RMS}(s) = \frac{V_{RMS}}{i_{ref,AC}} \cong \frac{I_{RMS} \cdot |Z_{RC}|_{400Hz}}{I_{RMS} \cdot K_I \cdot \frac{\sqrt{2}}{v_{SINE,pk}}} \quad (4)$$

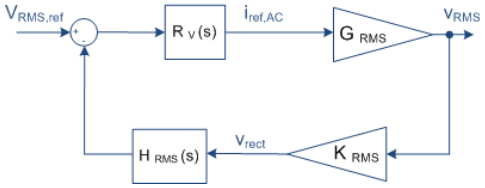


Figure 5. Rms voltage loop control scheme.

C. Offset Loop

The offset loop is designed based on scheme in Fig. 6. It only contains linear elements and its design is simple. Transfer function $G_{I,CL}(s)$ accounts for small deviations in output voltage when a small deviation in the current reference occurs. Its expression (5) is derived from the current closed loop, Fig. 4, multiplied by Z_{RC}. This loop evidently works in DC as well. It is desirable to present a low gain at output frequency in order not to interact with the other loops; otherwise it could lead to track null voltage not only for DC but for the output frequency.

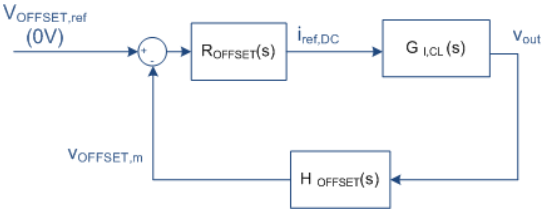


Figure 6. Offset loop control scheme.

$$G_{I,CL}(s) = \frac{\tilde{v}_{out}}{\tilde{i}_{ref}} = \frac{R_I(s) \cdot G_I(s) \cdot \frac{K_I}{V_{TRI}}}{1 + R_I(s) \cdot G_I(s) \cdot \frac{K_I}{V_{TRI}}} \cdot Z_{RC}(s) \quad (5)$$

D. Design summary and simulation results

Table I summarizes the main dynamic and stability indicators for the three analog loops reviewed and Fig. 7 shows their Bode plots, all at nominal conditions (100% of resistive load). The bandwidth of the current loop designed is about 2kHz with a 10dB gain at output frequency. This design would leave an instantaneous voltage loop almost without band to be tuned on the frequency spectrum: from 400Hz and 2kHz. Its gain at output frequency would be

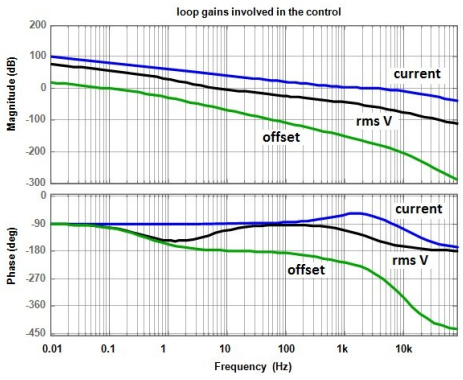


Figure 7. Open loop gains involved in the control of the inverter.

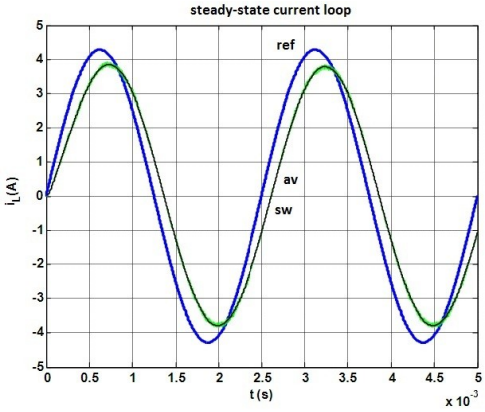


Figure 8. Current reference tracking in an averaged model and a switching one.

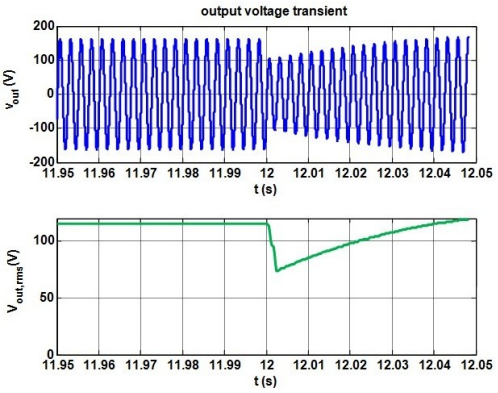


Figure 9. Voltage evolution in a load step (50% to 100%).

lower than 10dB, if not resonant control was applied. Thus, the output voltage would present a tracking error even higher than the one of Fig. 8 for the current, which would be unacceptable. Nevertheless, as long as an rms control is proposed, the voltage loop dynamics has enough spectrum to be tuned, from 400Hz down to DC, making the design easier and decoupling voltage tracking and voltage loop bandwidth. For these reasons, this control strategy might be considered for inverters with a narrow band between switching and output frequency and intended to deal with linear loads.

TABLE I. DYNAMIC INDICATORS OF THE CONTROL LOOPS

Loop	Bandwidth	Phase Margin	Gain (400Hz)	Gain (80kHz [a])
Inductor Current	2kHz	113deg	10dB	-39dB
Rms voltage	7Hz	72deg	36dB	-105dB
Offset voltage	0.1Hz	80deg	-133dB	< -200dB

a. Lowest frequency of the harmonics for a 40kHz switching unipolar sine PWM

Fig. 8 shows the current tracking of a switching model and an averaged model of the converter: both models perform exactly the same way, but falling into phase and shift error respect to the reference. In Fig. 9, the voltage transient during a step from 50% to 100% resistive load is shown, simulated over an averaged model.

IV. 3-PHASE SYNCHRONIZATION ALGORITHM

The proposed control method based on rms voltage makes the system lose the information of voltage phase, needed for properly synchronizing the three single-phase inverters involved in a 3-phase setup. If they were synchronized by shifting signal v_{SINE} -the AC current reference generator-, the three units would be synchronized at inductor current, assuming perfect tracking of the current. But, in case of an unbalanced load, this scenario would not mean voltage synchronization. An algorithm based in a Phase Locked Loop (PLL) is designed for this purpose, and implemented into a FPGA, which is already available for small tasks such as generating the sine reference v_{SINE}.

The algorithm is based on slightly changing the frequency of signal v_{SINE}, driven such variation by the phase shift error of each inverter. This way, each converter synchronizes its output voltage with its own phase reference.

Fig. 10 summarizes the synchronization process graphically:

- Reference (FPGA): a 400Hz pulse signal is generated into the 0 deg inverter, which is its sync reference, and it is sent to the 120 and 240 deg inverters. Those others shift that signal for creating their own sync reference, delayed 120 deg or 240 deg, based on its external configuration.
- Minimum shift error (HW and FPGA): shift error $\Delta\varphi$ is obtained by counting pulses into the FPGA between the sync reference and the arrival of signal ZC, which corresponds to the zero cross of the output voltage, coming from the instrumentation and control subsystem. The minimum delay is the one with minimum absolute value among $\Delta\varphi$, $2\pi-\Delta\varphi$ and $2\pi+\Delta\varphi$, as long as they all represent the same shift.
- Regulator (FPGA): based on the minimum shift error, a positive, negative or null change of frequency, Δf, is applied to the 400Hz of v_{SINE} by means of a bang-bang regulator with two levels (coarse and fine adjustment, positive or negative) and dead zone.

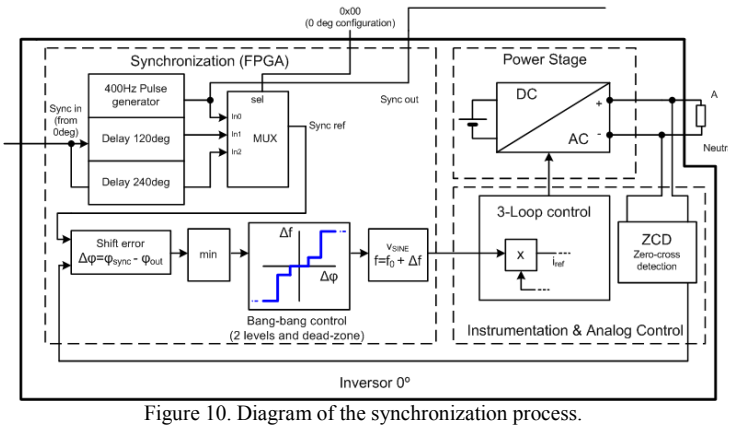


Figure 10. Diagram of the synchronization process.

This kind of regulation takes advantage from the existence of an integrator -1/s- connecting frequency change of v_{SINE} and phase shift of v_{OUT}. In other words, the control acts over a type-1 plant, which guarantees the absence of steady-state position error if the loop is stable [8]. For ensuring stability, the loop must be slower enough than the sampling of the shift, 400Hz by nature. Hence, care must be taken for ratio $\Delta f/|\Delta\varphi|$ to be short enough at every $\Delta\varphi$, in order to ensure stability.

V. Experimental Results

The following oscilloscope waveforms try to illustrate all the key points of the work presented in this paper. They were taken running the prototype of Fig. 11

Figure 11. Prototype of the power inverter.

A. Stand-alone operation mode

In Fig. 12a output offset level of about 30V can be seen without offset correction. Offset control application corrects DC level down to ±200mV, in agreement with the tolerance of the components used, Fig.12b. Maximum THD registered is 2.2%, at full load.

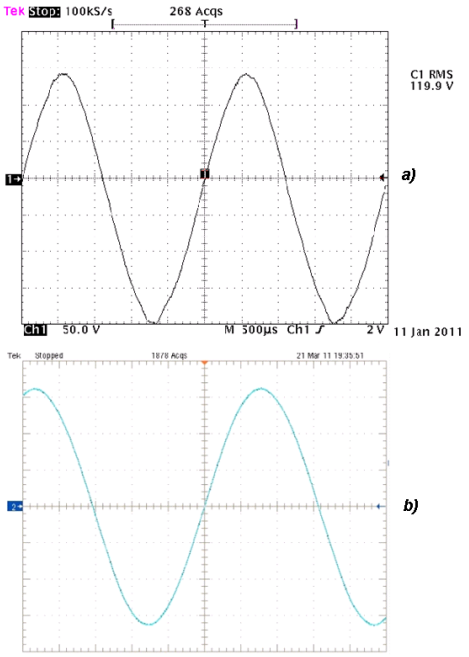


Figure 12. Output voltage without offset loop (a) and with it (b), 25% load.

Load step experiment results are given by Fig. 13: a change from 50% to 100% resistive load. The upper waveform shows the transient in output voltage, which agrees simulation of Fig. 9. The lower image represents just the current by the 50% load activated for the step.

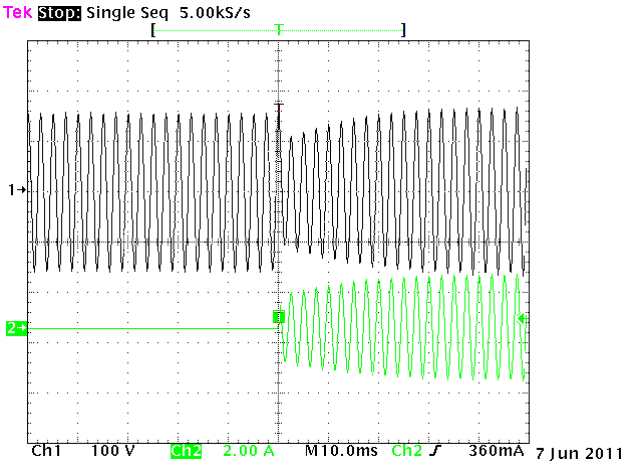


Figure 13. Output voltage transient caused by a load step (50% to 100%) and current drawn by the 50% load just activated

B. Parallel operation mode

Parallel operation of several inverters follows a Master-Slave configuration [9]. The Master keeps the whole control scheme, generating a current reference for itself and its Slaves. Into a Slave, the internal current reference is bypassed using a multiplexor which activates the Master current reference as the one to be tracked.

Fig. 14 shows the output voltage and currents for two inverters sharing a 200% load. The current breakdown is balanced among them, working at 100% each converter.

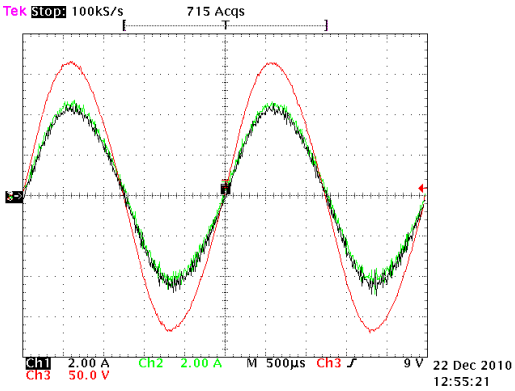


Figure 14. Output voltage and currents of two inverters in parallel sharing a resistive 200% load in total.

In Fig. 15 two inverters in parallel feed a 200% non-linear load, made up by a rectifier followed by a C filter and a resistive load. As expected, although the current balance is still good, the dynamics of the control loops involved makes impossible to deliver the proper current pulses for avoiding the output voltage distortion.

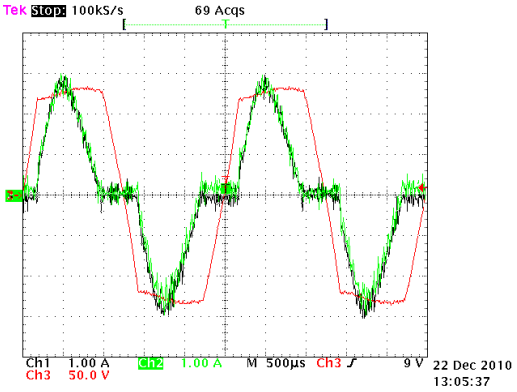
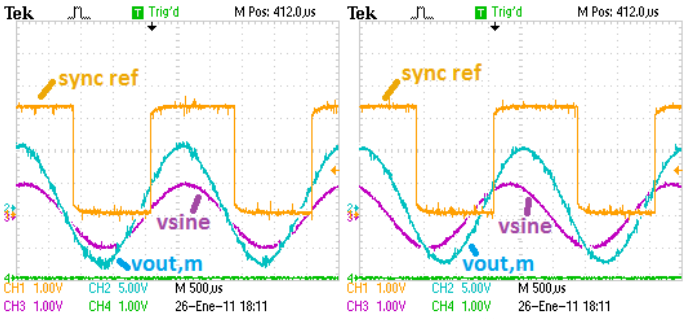


Figure 15. Output voltage and currents of two inverters in parallel feeding a rectifier with C filter and a resistive load, 200% in total.

C. *Synchronization algorithm*

Fig. 16 illustrates the performance of a single-phase inverter synchronizing with its own reference (square signal) feeding a resistive load (a) and a RL load (b). The output voltage measurement (large amplitude sine waveform) gets coupled to the reference. The algorithm makes signal v_{SINE} (small amplitude sine waveform) change its phase, thanks to a temporary change of frequency, so that the output voltage is permanently synchronized to its phase reference. Delay error between reference and output voltage is due to the hysteresis of the hardware zero-cross detector.



a) *b)*

Figure 16. Synchronization algorithm performance: converter feeding a linear RL load (a) and an R load (b).

VI. CONCLUSIONS

This paper presents the design and implementation of a control scheme for power inverters which combines rms voltage control and mean current control mode using a Hall-Effect measurement. These two design considerations are intended for enhancing the noise immunity and, along with it, improving the THD, by means of avoiding the direct introduction of any instantaneous voltage measurement from the switching stage into the control. Keeping an instantaneous current loop into the scheme simplifies the operation in parallel of several devices.

Nevertheless, the lack of any instantaneous voltage information in the control stage has several drawbacks. On one hand, the low voltage control bandwidth makes output voltage THD much higher when dealing with non-linear loads. Besides, the phase information is hidden for the voltage control and a synchronization method is required for 3-phase operation setup. In this application a PLL-based algorithm is implemented into a FPGA for this purpose.

On the other hand, from the point of view of the implementation, an offset control becomes necessary. A third analog loop which regulates the output voltage DC level is implemented for solving this issue.

The experimental results attached show the goodness of all the actions taken for successfully implementing the proposed control scheme. Firstly, the offset control loop reduces output voltage offset down to 200mV, which is in agreement with the tolerances. On the other hand, balanced operation in a 2-inverter parallel setup is shown. Furthermore, phase synchronization of one single-phase converter with a pulse reference is also demonstrated, for the 3-phase arrangement. During the tests, the maximum THD registered is 2.2% for linear full load but, as expected, dealing with non-linear loads requires taking into account much faster control schemes for not falling into high THD.

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