Current rectification in a single GaN nanowire with a well-defined *p–n* junction

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(Received 10 October 2002; accepted 7 July 2003; publisher error corrected 26 August 2003)

This letter discusses Mg incorporation in GaN nanowires with diameters ~35 nm, fabricated by vapor–liquid–solid synthesis in *p*-type nanowires. Turning on the Mg doping halfway through the synthesis produced nanowires with *p–n* junctions that showed excellent rectification properties down to 2.6 K. The nanowires are shown to possess good-quality, crystalline, hexagonal GaN inner cores surrounded by an amorphous GaN outer layer. Most wires grow such that the crystalline *c* axis is normal to the long axis of the nanowire. The temperature dependence of the current–voltage characteristics is consistent with electron tunneling through a voltage-dependent barrier. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1604190]

One of the aims of nanoscience and technology is to create low-dimensional structures with electronic and photonic properties that replicate those of conventionally fabricated systems, but to do so in ultrasmall structures created by alternative synthetic means. In this way one hopes to create circuit elements that display interesting physical properties or have utility either in their own right or as components when integrated with more conventionally fabricated systems. Hopes are bright for using nanostructures or even individual molecules as sensors,[1] ultrahigh density data storage,[2] logic gates,[3] subwavelength light guides,[4] or other light-management circuitry.[5] Recently, rectification was demonstrated in junctions formed by crossing single-walled metallic carbon nanotubes with semiconducting ones[6] in *p*-type InP nanowires crossed with an *n*-type InP nanowires[7]a and crossed *p*-type and *n*-type GaN nanowires[7]b and in ''heterojunctions'' created by crossing a *p*-type Si nanowire, with an *n*-GaN nanowire.[3,8] A *p–n* junction was reported in a single piecewise-doped silicon nanowire produced by modulation doping.[9]

In this letter we describe the fabrication of GaN nanowires with internal *p–n* junctions and the systematic investigation of their transport properties as a function of temperature, thereby opening, the possibility of single GaN nanowire transistors and other devices.

The nanowires were synthesized using vapor–liquid–solid (VLS) synthesis.[10,11] Indium nanodroplets were formed on an alumina substrate, which, together with an indium nugget and a reagent mixture consisting of metallic Ga and Ga_2O_3 powder, were placed in a crucible and distributed such that the indium was downstream and the gallium/gallium oxide mixture upstream of the alumina substrate. The reaction was carried out under flowing ammonia gas at 980 °C in a tube furnace. Similar methods were previously reported for fabricating nanowires of various materials.[7–11] Nanowires of the desired average diameter were produced by varying the reaction temperature, while the mean nanowire length was determined by the reaction time. The GaN nanowires synthesized in this way are *n* type due to the presence of nitrogen vacancies and trace oxygen impurities.[12] For *p*-type GaN nanowires, Mg atoms were incorporated into the In–Ga–N liquid through the decomposition of Mg_3N_2 placed in a separate crucible upstream of the aforementioned crucible. A similar approach for producing *p*-type GaN nanowires with similar carrier densities was recently reported.[7b]

Nanowires with *p–n* junctions were grown by initiating the process in the absence of Mg, stopping the synthesis halfway (~20 min) then introducing magnesium nitride into the furnace, and resuming the growth process. *P*-type nanowires were produced by including Mg from the outset. Field-emission scanning electron microscopy (SEM) (JEOL-6340F) images of the product show GaN nanowires with diameters narrowly distributed about an average value ~30 nm and lengths in the range 10–30 μm.

X-ray diffraction (XRD) (Scintag PAD-V) measurements unequivocally identify the GaN in the nanowires as hexagonal wurtzite with lattice parameters $a = 3.186$ Å and $c = 5.178$ Å. The only other peaks observed belong to the rhombohedral α-Al_2O_3 ($a = 4.758$ Å and $c = 12.991$ Å) substrate. High-resolution transmission electron microscopy (TEM) (JEOL-2010HR) confirms this and shows the nanowire to consist of a single-crystal core with the crystalline *c* axis aligned perpendicular to the nanowire's axis (Fig. 1) surrounded by a disordered layer that was determined by

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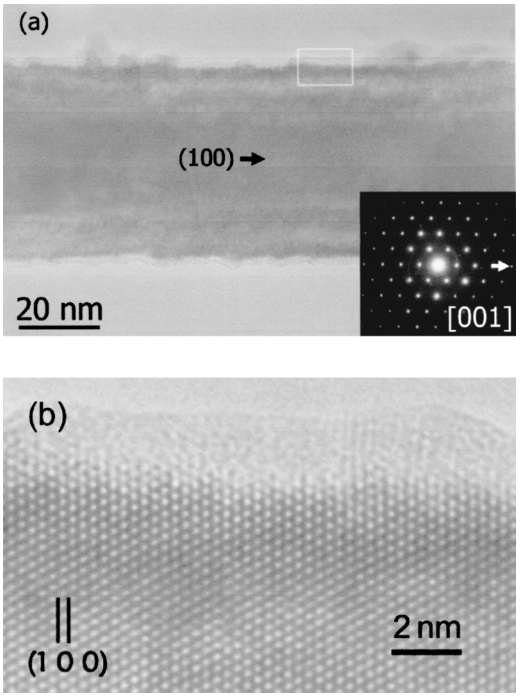

FIG. 1. High-resolution TEM images and electron diffraction pattern (inset in a) of a 30-nm-diam GaN nanowire whose growth axis corresponds to the (100) direction of single-crystal hexagonal (wurtzite) GaN. (a) Low magnification image of the nanowire's cross section. (b) The indicated portion of the nanowire enlarged to show atomic resolution.

electron energy loss spectroscopy analysis also to be GaN. (TEM measurements indicated that for GaN nanowires with average diameter ~30 nm the majority of the nanowires possess this orientation.) It is perhaps the amorphous GaN surface layer that protects the crystalline inner core of the nanowire from surface impurities that could have seriously altered its rectifying properties through extraction or injection of charge.

Samples were prepared for both SEM imaging, XRD and postfabrication for current–voltage measurements by immersing the nanowire-covered alumina disk in ultrapure methanol and sonicating for ~1 min to help detach the GaN nanowires from the surface, producing a dilute suspension of individual nanowires.

Approximately 2 ml of the nanowire suspension were placed onto the surface of 200-nm-thick oxide Si wafer and the solvent allowed to evaporate. Ti/Au (30 nm/200 nm) contacts were vapor deposited either through a suitable pattern, written using standard e-beam lithography, or through commercial copper TEM grids (12 μm wires and 113 μm openings) serving as contact masks (Fig. 2, inset). The nanowire suspension was diluted by successive trials so that several dozen nanowires were deposited randomly on the Si substrate out of a droplet approximately the size of the TEM grid. By using this procedure several pairs of pads were typically found to be connected by individual nanowires. The choice of gap size (i.e., grid-wire diameter) and nanowire length (~25 μm) ensured that nanowires connecting adjacent pads possessed their p–n junction in the gap rather than under one of the Ti/Au contacts. The locations of good candidate nanowires for $I(V)$ measurement were determined by field-emission SEM (Fig. 2), and electrical contact to the appropriate gold pads was achieved with the micromanipulated tungsten microprobes of a commercial semiconductor parametric analyzer. The same process was used to produce and characterize several p-type, n-type and p–n-type GaN nanowires.

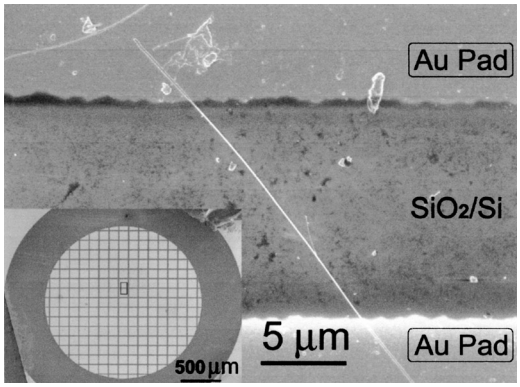

FIG. 2. SEM image showing a single GaN nanowire connecting two contact pads. The pads were deposited over the nanowires. (Inset) low-resolution SEM image of the array of Ti/Au pads fabricated by vapor deposition through a commercial TEM copper grid used as a contact mask. The area enlarged in the main image is shown as a rectangle.

Current–voltage measurements were carried out under a flowing nitrogen atmosphere. Provided a sufficiently thick layer of Ti was used under the gold contact p type and n type ~35-nm-diam GaN nanowires show almost ohmic current–voltage characteristics, implying an ohmic (rather than Schottky) metal-semiconductor junction (Fig. 3). By contrast, ~25-nm-diam GaN nanowires produced with p-n junctions (Fig. 3) showed classic rectification properties. Fitting the measured $I(V)$ to the empirical function $I \sim \exp(-eV/Nk_BT)$, produced diode ideality factors, N, in the range 5.5–6.5 for most of the nanowires investigated, over the temperature range used (the higher values generally corresponding to the lower temperatures). These numbers are larger than the near unit ideality factors characterizing commercial silicon diodes, but respectable nonetheless.

Variable temperature $I(V)$ characteristics, carried out in a Janis helium cryostat using He as a thermal exchange gas, show (Fig. 3) the small reverse bias current to be only slightly temperature dependent. However, the magnitude of the forward current at a given voltage decreases with decreasing temperature (Fig. 3) in the range investigated (2.6 to ~300 K). This behavior is consistent with tunneling through

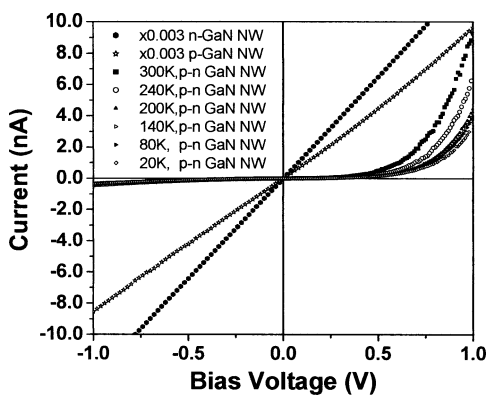

FIG. 3. Measured current–voltage characteristics of single n type, p type measured at ~300 K, and p–n GaN nanowires measured at 300, 240, 200, 140, 80, and 20 K.

a barrier out of occupied levels whose population is slightly modified by the nonzero temperature, and a potential barrier that allows increased penetration with increasing forward voltage. The essential physics can be accounted for with a simplified model that keeps the height of the barrier constant but decreases its width linearly with increasing voltage. The temperature dependence comes about from the population of low energy states on the "entry" side of the barrier according to the Fermi function, which, for temperatures near room temperature, can be approximated by a Boltzmann factor. Hence, the tunneling current, I, in this treatment will be approximately proportional to[13]

$$\int_0^W \exp(-E/k_BT)\exp(-b'L(W-E)^{1/2})dE, \tag{1}$$

where $b'=(2m)^{1/2}/\hbar$ and W is the barrier height.

We write the barrier thickness, L, as $L=L_0-\beta V$, where V is the applied voltage. When $E \ll W$ the quantity $(W-E)^{1/2}$ can be written approximately as $W^{1/2}(1-\frac{1}{2}E/W)$. With these approximations integral (1) solves to give

$$I \propto \frac{e^{\zeta V}-e^{-(W/k_BT-\zeta/2\ V-\lambda)}}{\dfrac{1}{k_BT}-\dfrac{\zeta V}{2W}-\dfrac{\lambda}{W}}, \tag{2}$$

where $b=b'W^{1/2}$, $\zeta=b\beta$, and $\lambda=bL_0/2$.

In view of the simplicity of the approach no attempt was made to fit the experimentally determined data to Eq. (2). However, temperature-dependent $I-V$ curves calculated with Eq. (2) using reasonable parameters show rather similar trends to what was observed experimentally, and the temperature dependence of the forward current measured at 1 V fit rather well by scaling Eq. (2) and adding a constant base line current (Fig. 4). The constant base line correction almost certainly arises from the fact that we approximated the Fermi function as a Boltzmann factor.

Using electron and hole mobility data derived from the conductance of the p-type and n-type GaN nanwires, we estimate the carrier densities in the p-doped and n-doped GaN nanowires to be an order of $10^{17}-10^{18}$ cm^{-3} and $10^{17}-10^{19}$ cm^{-3}, respectively, from which the depletion region of the $p-n$ GaN was in the range 35–80 nm at 1 V.

We, therefore, conclude that we have succeeded in fabricating well-defined $p-n$ junctions in ~25-nm-diam GaN nanowires by turning on a Mg source halfway through the VLS nanowire synthesis process. The nanowires show excellent rectification properties. P-doped and n-doped GaN nanowires fabricated under similar conditions invariably produce linear current–voltage curves, suggesting that the observed rectification comes from the $p-n$ junction and not from a metal-semiconductor Schottky contact junction.

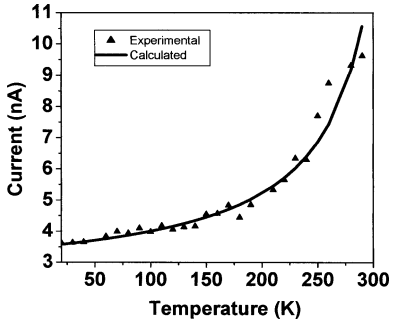

FIG. 4. (points) Current values measured as a function of temperature at a forward bias of 1 V. (line) Current vs temperature calculated using Eq. (2) and parameters: $\zeta=6.9$ V^{-1}, $W=0.13$ V, $\lambda=1$ and a scaling factor of 4.3×10^{-11} A.

The authors are deeply grateful to Professors Pierre Petroff, Shuji Nakamura, Alan Heeger, Dr. Huaiming Wang, and Ernie Caine for fruitful discussion and valuable suggestions. This work made extensive use of the MRL Central Facilities at UCSB supported by the National Science Foundation under Award No. DMR96-32716.

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