Current Recycling and SFQ Signal Transfer in Large Scale RSFQ Circuits

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***Abstract*—The practical implementation of RSFQ technology in most digital electronics application areas requires much more complexity than the presently developed circuits. There are two important issues in building large-scale RSFQ circuits: 1) the recycling of the bias currents and 2) the transfer of SFQ pulses between circuits located far apart. RSFQ circuits are well known to operate with dc current bias. Even though the dc current biasing is more forgiving than the problematic ac biasing, it can still be a big concern when the circuit size becomes large. Dramatic reduction of the total bias current can be achieved by biasing several RSFQ circuits in series, where each circuit is positioned on a separate ground plane. In this work, we have used magnetically coupled Josephson transmission lines as inputs and outputs of an isolated shift register to show the feasibility of using the concept of serial biasing in current recycling. The circuit was simulated, fabricated with Nb technology, and tested at a temperature of 4.2 K. Test results show that SFQ pulses were transferred into the shift register built on a separate ground plane, clocked through it, and sent out back to the circuit on the original ground plane. We also studied on how to transfer SFQ pulses over an extended length, an important issue in building large RSFQ circuits. We have designed the circuits to test our microstrip line and multichip module approaches. We designed, optimized, fabricated and tested the circuits. Test results show that SFQ pulses can be successfully transmitted over an extensive distance in a chip and between chips.**

***Index Terms*—Current, magnetic, microstrip, recycling.**

I. Introduction

RAPID single flux quantum (RSFQ)superconductive electronics has been recognized as a promising technology for superconducting digital applications [1]. Superconductive digital electronics uses Josephson junctions as switching elements. These devices are known to be able to switch on a picosecond time scale.

The development of new RSFQ logic circuits has been significant in recent years. A toggle flip-flop (TFF) circuit was built with this technology and operated at 770 GHz [2]. More complicated circuits have been built, including analog-to-digital converters (ADC's) [3], digital-to-analog converters [4], time-to-digital converters [5], network switches [6], etc. The performances of these circuits are superior to circuits made with other technologies because of the ultra-low power consumption and high switching speed of Josephson junctions. So far, these developments have been at the single-chip level, mostly restricted to a small section of chip area. RSFQ circuits mostly use Josephson Transmission Lines (JTL's) to transfer SFQ pulses between circuits. To extend the present RSFQ technology to large-scale circuits, we believe that the issues of transferring SFQ pulses in various geometries and reducing the amount of bias current have to be resolved. By noting that the energy contained in an SFQ pulse is less than an attojoule, it is not very surprising that a reliable SFQ pulse transfer technique has not been well established. Recently, microstrip transmission lines and multichip modules have been studied to solve this problem [7], [8].

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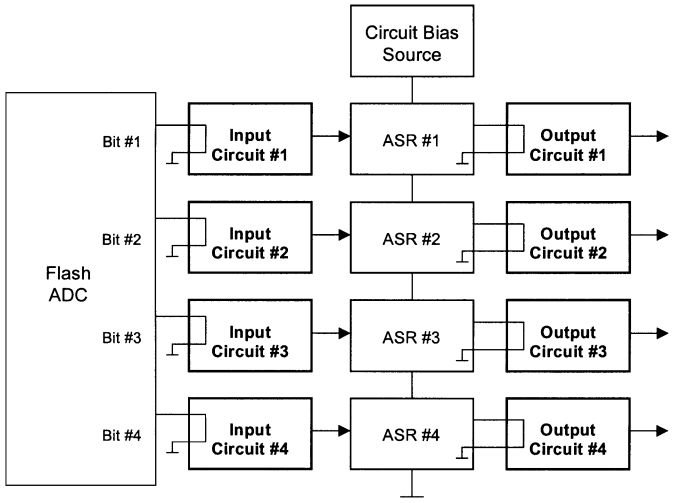

Fig. 1. Block diagram showing how the serial biasing can be used to drastically reduce the bias current in a digitizer. Each acquisition shift register (ASR) circuit is on the separate ground plane.

II. Current Recycling

The main advantage of using RSFQ circuits instead of other superconductive digital circuits is that RSFQ circuits use only dc bias. This eliminates the cross-talk problems caused by ac biasing and makes building large superconductive digital circuits easier. However, even in RSFQ circuits, total amount of dc bias current can add up to tens of amperes when the circuit size becomes large. To ease this problem we need to recycle the current by biasing the circuits serially. For example, serially biasing twenty-four cells of 512 bit shift register memory built on separate ground planes will reduce the required current from roughly 10 A to less than 500 mA, which is a large reduction.

Fig. 1 shows a block diagram for using current recycling in a 4-bit flash ADC and its acquisition shift register (ASR) memory bank. The ADC generates a data stream for each bit. Each of these data streams must be stored on chip in an ASR until the data is read out. Roughly 512 shift register cells or more are needed for the most applications of a digitizer [9]. Each of those

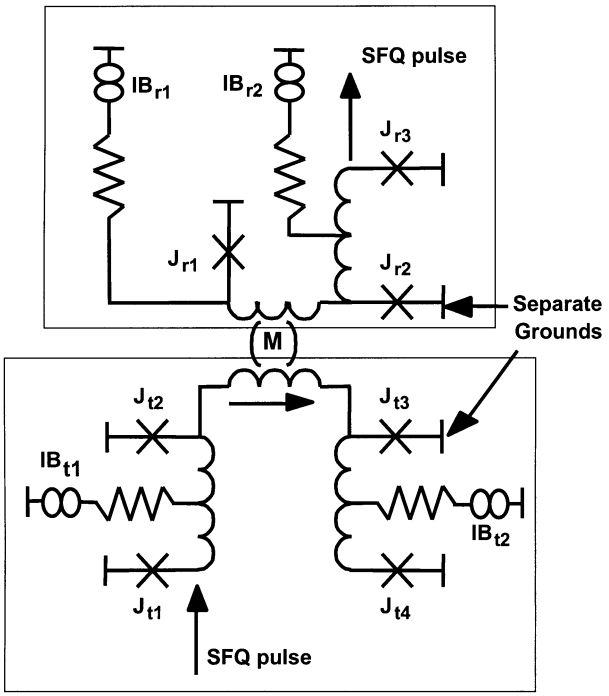

Fig. 2. Circuit schematics for the magnetically coupled SFQ pulse transfer circuit. An SFQ pulse enters from the bottom and travels through JTL's in the bottom circuit. Magnetic coupling induces an SFQ pulse on the top circuit that uses a different ground plane.

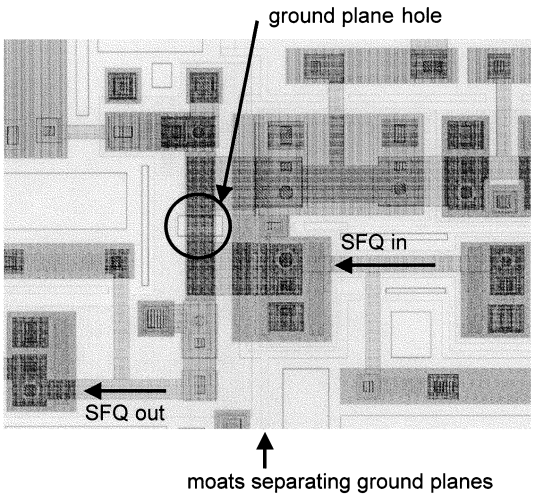

Fig. 3. Mask layout of the magnetically coupled SFQ pulse transfer circuit. A ground plane hole was used to increase the mutual inductance between the upper and the lower ground planes.

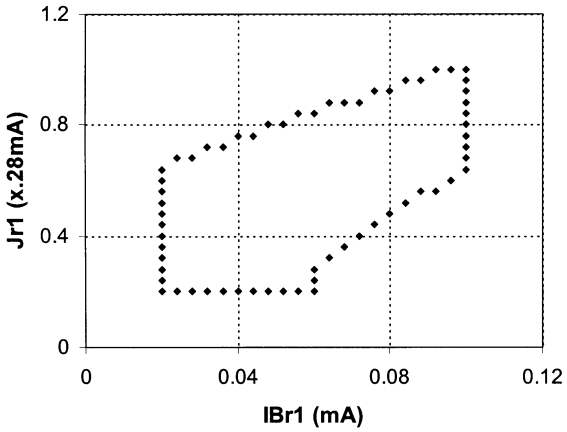

Fig. 4. Map showing the circuit margins of the critical circuit parameters, J_{r1} and IB_{r1}. Inside the marks is the region where the circuit operated correctly. Wide margins show that the circuit is robust.

shift register cells requires 0.75 mA of dc bias current, resulting in a total dc ASR bias current of approximately 3 Amperes. The design of a practical digitizer requires a drastic reduction in this bias current requirement. The solution, depicted in Fig. 1, is obtained by biasing each shift register in series with the others. Two requirements must be met to implement serially biased circuits: 1) the current drawn from each circuit must be equal, and 2) the input and output circuits must not add current to the serially biased circuits. This requires magnetically coupled inputs and outputs to avoid galvanic connections, as depicted in Fig. 1.

Fig. 2 shows the schematic of the magnetically coupled SFQ pulse transfer circuit. An inductor connecting two Josephson junctions momentarily stores a single flux quantum while an SFQ pulse propagates from one junction to another. Typically, this duration time is about 4–8 ps, depending on the circuit values. Between the times when J_{t2} and J_{t3} make voltage pulses, the magnetic flux stored in the inductor that connects J_{t2} and J_{t3} induces a current in the inductor that connects J_{r1} and J_{r2}. With proper circuit parameters, this induced current can cause a voltage pulse on J_{r1}. The flux quantum then propagates through J_{r2} and J_{r3} for further processing in the circuit on the other ground plane. In this way, an SFQ signal in one ground plane gets transferred to another ground plane [10].

Fig. 3 shows the circuit layout corresponding to the circuit schematic of Fig. 2. The bias currents for the junctions on the input side are passed to one ground plane while the ground for the junctions on the output side is isolated from the other ground by a ground plane moat. The Josephson junctions J_{t2} and J_{t3} are damped more heavily than other junctions to guarantee that minimum reflections take place at the end of the input JTL. Tight magnetic coupling is required between the pulse transmitting JTL and the pulse receiving JTL to obtain a robust circuit with excellent operational margins. For that reason, holes were opened in both the upper and the lower ground planes to increase the mutual inductance. By using Chang's formula [11], [12], the self inductance values and the mutual inductance value were calculated.

To optimize the circuit parameters of the magnetically coupled SFQ transfer circuit, we used WRspice™ and its margin analysis program. With other circuit parameters fixed, we varied two circuit parameters and mapped the correct operation region in two dimensions. By properly selecting the pairs, we obtained optimum circuit parameters with good margins. The critical circuit parameters were the junction critical current of J_{r1} and its bias current IB_{r1}. Fig. 4 shows the mapping of the correct operation boundary in two dimensions. Inside the marks is where the circuit performed correctly and outside is where the circuit made mistakes.

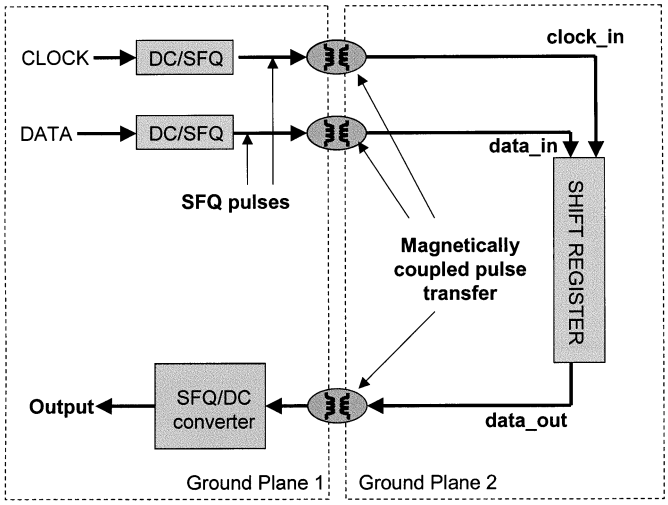

Fig. 5. Block diagram of the circuit designed to test the magnetically coupled SFQ pulse transfer circuit. Complete transmission of SFQ pulses through the circuits on separate ground planes could be tested with this circuit.

The wide operation area in Fig. 4 indicates the designed circuit is quite robust. The optimum Josephson junction critical currents were $I_{t1} = 0.39$ mA, $I_{t2} = 0.56$ mA, $I_{t3} = 0.56$ mA, $I_{t4} = 0.39$ mA, $I_{r1} = 0.2$ mA, $I_{r2} = 0.28$ mA, and $I_{r3} = 0.39$ mA. We chose the coupling constant between the coupled inductors as 0.68, which was close to the estimate from the layout in Fig. 3.

By putting two magnetically coupled SFQ transfer circuits in series, we could successfully transfer SFQ pulses in and out of an isolated region. We verified the inductance values and the junction critical currents of the magnetically coupled circuit by measuring the threshold curves of the SQUID's formed by the exact dimensions of magnetically coupled SFQ transfer circuit. Using the period of the flux lobes, we found mutual inductance values between 2.7 pH and 3.1 pH, in reasonable agreement with the designed value of 2.75 pH. The critical margins came from the IB_{r1} values that ranged between 5 and 20%.

To test the current recycling scheme, we designed a circuit whose block diagram is as shown in Fig. 5. First we separated regions by using a ground plane moat. In this way, we created two regions we refer to as ground plane 1 and ground plane 2. We used DC/SFQ converters to generate SFQ pulse trains for clock and data signals. Both clock and data pulses were transmitted from ground plane 1 region to ground plane 2 region and fed into a shift register. The output data from the shift register were sent back to the original ground plane 1 region. Readouts of the output signal were obtained by using a toggle flip-flop (TFF)-type SFQ/DC converter. We laid out the circuit and fabricated it. The circuits were fabricated by using the ten-level Nb process [13] with a junction critical current density of 2.5 kA/cm^2. The test results are as shown in Fig. 6. The first trace shows the clock input and the second the data input pattern of (11 010 001). The third trace shows the output from the SFQ/DC converter, showing that the SFQ pulses successfully moved between the regions having different ground planes. As can be seen in Fig. 6, the data were shifted through the shift register in 4 clock cycles. Since we used a TFF-type DC/SFQ converter, the output pattern shown in Fig. 6 is the results of the voltage toggles caused by SFQ pulses.

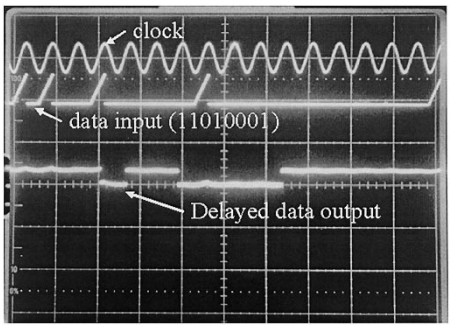

Fig. 6. Test results of the circuit to test magnetically coupled SFQ pulse transfer. The first trace shows the clock, the second the data pattern, and the third the data output toggled by SFQ pulses. 4 clock cycle delay occurred in the shift register is also shown. The scope picture was taken at 10 kHz.

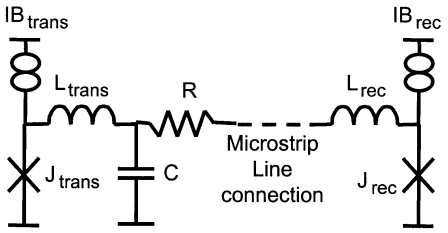

Fig. 7. Circuit diagram of the microstrip transmission line pulse transfer circuit. 1.5 ohm impedance and 1 cm length microstrip line was used in simulation where the circuit showed good operating margins.

III. Microstrip Line SFQ Pulse Transmission

To build large-scale RSFQ circuits we need to transmit SFQpulses over an extended length by using microstrip lines rather than using JTL's [7]. JTL's work very well in transmitting SFQ pulses over short lengths. However, their transmission speed is only about 10 mm/nsec, more than 10 times slower than the speed of microstrip transmission lines. Also, JTL's cannot be used when an SFQ signal has to be transmitted between chips.

To transmit SFQ pulses by a microstrip transmission line we constructed the circuit shown in Fig. 7. Shunt resistors for the junctions were chosen to give β_c of J_{trans} and J_{rec} to be about 2 and 3, respectively. The performance of the circuit was tested with WRspice™ simulation tool by watching the operating margins of IB_{trans} and IB_{rec}. Large operating margins were obtained for the junction critical currents of $I_{trans} = 0.34$ mA, $I_{rec} = 0.20$ mA. We used 1.5 ohm for the impedance of the microstrip transmission line. Operating margins of the circuit became much smaller when the impedance was raised above 2 ohm. The circuit was rather insensitive to the values of R and C when their values were in the range of within 0.2 ohm and between 0.2 pF and 1.5 pF, respectively. As can be seen in Fig. 8, the circuit had wide operating margins.

To evaluate the performance, we employed the microstrip transmission line pulse transfer circuit between a flash ADC comparator and a readout circuit. The distance between the two circuits was about 1.3 mm, corresponding to the time delay of

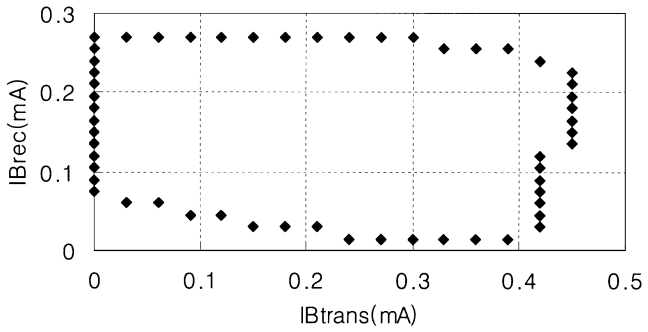

Fig. 8. Map showing the circuit margins of the critical circuit parameters, IB_{rec} and IB_{trans}. Inside the marks is the region where the circuit operated correctly. Wide margins show that the fabricated circuit may work well.

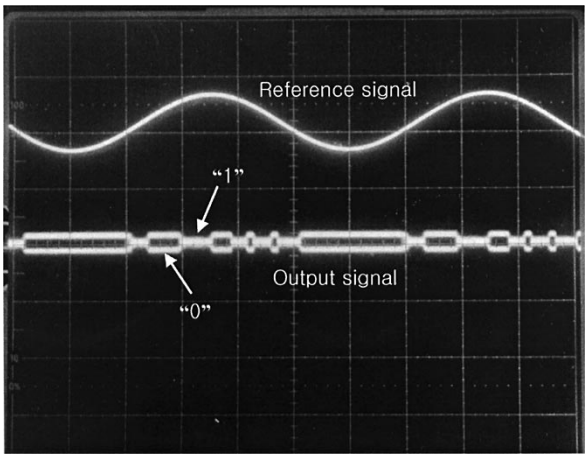

Fig. 9. 6 GHz test results of a flash ADC comparator and a TFF-type SFQ/DC converter connected by a microstrip transmission line. Correct output pattern indicates that the microstrip transmission line transmitted SFQ pulses correctly. 10 kHz beat frequency was used in the tests. 10 kHz reference signal is also shown in the first trace.

10.3 ps. Fig. 9 shows the test results at 6 GHz. We used a beat frequency test to test the circuits at multi-GHz speeds, where the input analog signal and the clock signal speeds were off by a beat frequency, which was 10 kHz in this case [14]. We used a TFF-type SFQ/DC converter for the data monitor output, considering that there was only a single stream of data flow with no clock pulses. The data stream in the beat frequency measurement was composed of a group of data "1" and a group of data "0." In the TFF-type SFQ/DC converter, there was no voltage toggle when data "0" entered the flip-flop; voltage toggled when data "1" entered. Since the data rate was much faster than the scope rate, the fast voltage toggles in the group of data "1" were displayed as an average voltage as seen in Fig. 9. The circuit worked only up to 6 GHz. This could be due to the poor comparator performance, and we expect that the microstrip transmission line will work at much higher frequencies. Further work to verify the speed limit is needed.

SFQ pulse transfer between separate chips is also one of the important issues in building large RSFQ circuits. In this case, maintaining low impedance for the chip-to-chip connection is quite difficult, so the suggested microstrip line approach may not work. Instead of SFQ pulse streams, a converted dc signal may be used for the transmission between the chips in a multichip module [15], [16].

IV. Conclusion

To build large scale RSFQ circuits, recycling of bias currents and SFQ pulse transfer between remote circuits are the important issues to solve. In this work, we demonstrated the feasibility of using the concept of serial biasing in current recycling by using magnetically coupled Josephson transmission lines. Microstrip line pulse propagation has been tested to show the successful transmission of SFQ pulses over large on-chip distances. However, converting SFQ pulses to dc signal is favored over direct transmission of SFQ pulses for inter-chip data transport.

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References

[1] D. K. Brock, E. K. Track, and J. M. Rowell, "Superconductor ICs: The 100-GHz second generation," *IEEE Spectrum*, vol. 37, pp. 40–46, December 2000.

[2] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-flip-flop operating up to 770 GHz," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3212–3215, June 1999.

[3] O. A. Mukhanov, V. K. Semenov, W. Li, T. V. Filippov, D. Gupta, A. M. Kadin, D. K. Brock, A. F. Kirichenko, Y. A. Polyakov, and I. V. Vernik, "A superconductor high-resolution ADC," *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 601–606, March 2001.

[4] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, L. A. Christian, and J. X. Przybysz, "Pulse-driven Josephson D/A converter," *IEEE Trans. Appl. Supercond.*, vol. 8, pp. 42–47, June 1998.

[5] A. F. Kirichenko, S. Sarwana, O. A. Mukhanov, I. V. Vernik, Y. Zhang, J. H. Kang, and J. M. Vogt, "RSFQ time digitizing system," *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 978–981, June 1998.

[6] S. Tahara, S. Yorozu, Y. Kameda, Y. Hashimoto, H. Numata, T. Satoh, W. Hattori, and M. Hidaka, "Superconducting digital electronics," *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 463–468, March 2001.

[7] N. Joukov, Y. Hashimoto, and V. Semenov, "Matching Josephson junctions with microstrip lines for SFQ pulses and weak signals," *IEICE Trans. Electron.*, vol. E85-C, pp. 636–640, March 2002.

[8] M. Maezawa, H. Yamamori, and A. Shoji, "Chip-to-chip communication using a single flux quantum pulse," *IEEE Trans. Appl. Supercond.*, vol. 10, pp. 1603–1605, June 2000.

[9] S. B. Kaplan, P. D. Bradley, D. K. Brock, D. Gaidarenko, D. Gupta, W. Q. Li, and S. V. Rylov, "A superconductive flash digitizer with on-chip memory," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3020–3025, June 1999.

[10] V. K. Semenov, P. N. Shevchenko, and Yu. A. Polyakov, "Digital-to-analog converter based on processing of SFQ pulses," in *Extended Abstracts of ISEC97*, vol. 2, June 1997, pp. 320–322.

[11] W. Chang, "Inductance of a superconducting strip transmission line," *J. Appl. Phys.*, vol. 50, pp. 8129–8134, 1979.

[12] W. Chang, "Measurement and calculation of Josephson junction device inductances," *J. Appl. Phys.*, vol. 52, pp. 1417–1426, 1981.

[13] HYPRES design rules can be found at Hypres web site at. [Online]. Available: www.hypres.com

[14] P. D. Bradley, "A 6-bit Josephson flash A/D converter with GHz input band width," *IEEE Trans. Appl. Supercond.*, vol. 3, pp. 2550–2557, March 1993.

[15] D. Gupta, W. Li, S. B. Kaplan, and I. V. Vernik, "High-speed interchip data transmission technology for superconducting multi-chip modules," *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 731–734, March 2001.

[16] J. H. Kang, D. Gupta, and S. B. Kaplan, "Demonstration of RSFQ digitizer on a multichip module," IEEE Trans. Appl. Supercond., September 2002, to be published.