Paper presented at EPE, Lille, France, 3 September 2013

Current Source Modular Multilevel Converter for HVDC and FACTS

Jiaqi Liang*, Alireza Nami, Frans Dijkhuizen
ABB Corporate Research
USA and Sweden
*Email: jiaqi.liang@us.abb.com

Pierluigi Tenca, Jyoti Sastry
IEEE Members

Keywords

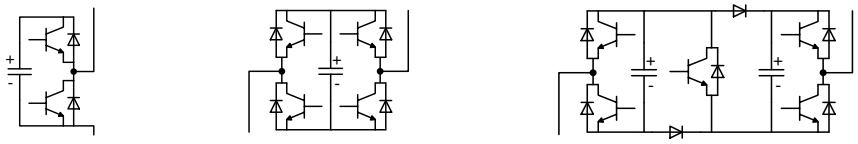
Current Source Inverter, Multilevel Converters, HVDC, FACTS.

Abstract

A current source modular multilevel converter (MMC) is proposed for high voltage AC/DC power conversion applications, such as HVDC and FACTS. Current source converters have the advantage of short-circuit fault tolerance, which is a pivotal feature for grid applications. Following the same concept as the voltage source MMC, inductor cells are connected in parallel and form a current source parallel link that can synthesize a desired current waveform. These parallel links are further connected in series to scale up in voltage. Using fully controllable reverse voltage blocking devices, the converter can provide controllable active and reactive power. Protection schemes against open-circuit failures inside the inductor cells are also proposed. Simulation results are presented to demonstrate the operation of the current source MMC and its functionality of DC fault tolerance.

Introduction

The voltage source modular multilevel converter (MMC) concept [1] [2] brings a new high voltage converter technology that is low loss, low harmonics, modular, and voltage scalable [3]. Similar to the traditional two- or three-level voltage source converters, the basic MMC topology using half-bridge capacitor cells (Fig. 1 (a)) cannot limit fault current during a DC short-circuit fault. To address this issue, using the full-bridge cells (Fig. 1 (b)) and clamped-double cells (Fig. 1 (c)) has been proposed [4]. These two types of cells can reversely insert the capacitor, and thus block the fault current. However, 50% more semiconductor devices are expected with increased converter loss. Alternatively, a low-loss hybrid DC breaker [5] may be used to safely interrupt a large short-circuit fault current. In a DC grid scenario, DC breakers can also provide line operation and regional grid protection functionalities. In any case, voltage source converters have intrinsic limitation in being DC faults tolerant.



(a) (b) (c)

Fig. 1: Capacitor cells for voltage source MMC: (a) half-bridge cell, (b) full-bridge cell, and (c) clamped-double cell.

Alternatively, properly conceived current source converters (CSCs) are inherently tolerant to DC short-circuit faults, firstly because of the dynamic nature of the inductors used, and secondly, because of the bidirectional voltage blocking capability of the switches used in most CSCs. While voltage source converters and voltage source DC grids require protection against short-circuit faults, current source DC grids require protection against open-circuit faults. Emergency current paths should be provided in the current source circuit concept (e.g. in [6]). This can be technologically easier than dissipating the energy of the magnetic field associated with a current in the voltage source DC grids.

Multilevel CSCs using fully controllable switches have the advantages of low output harmonics and controllable active and reactive power. Most of these multilevel CSC topologies are also modular by paralleling, as shown in Fig. 2 [7], [8], [9]. However, most of them require the semiconductor switches to be rated for the full AC voltage. For high voltage applications, this would require series connection of a large number of semiconductor devices, deeming these CSC topologies challenging in the aspect of voltage scaling. One way to address the CSC voltage scaling issue is to series connect single-phase inductor cells with the help of voltage-sharing capacitors, as shown in Fig. 3 [10].

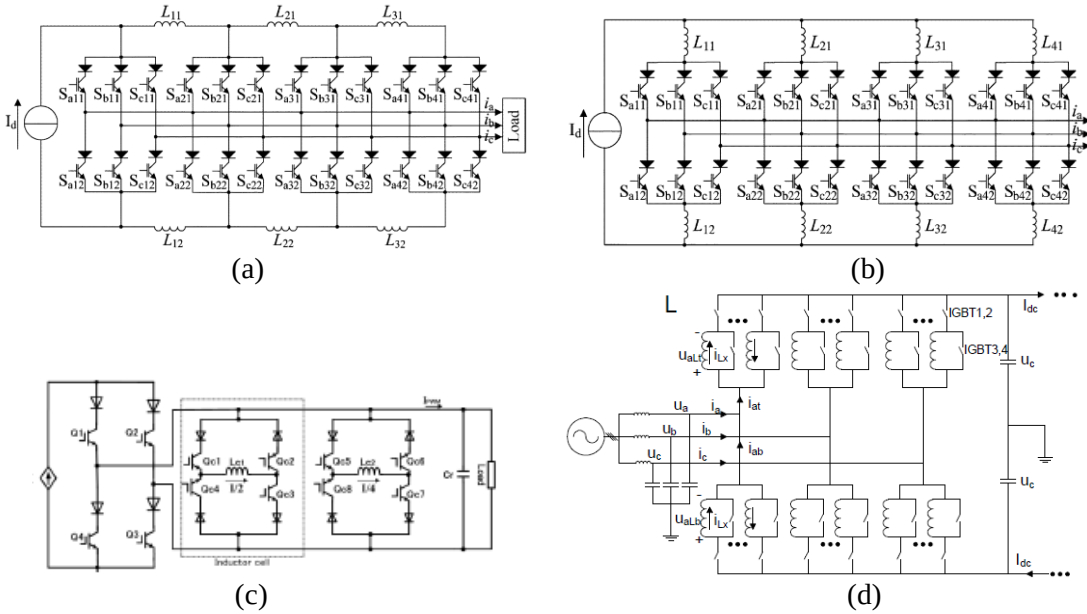


Fig. 2: Multilevel CSCs: (a) modular three-phase CSCs [7], (b) modular three-phase CSC with single-rating inductors [7], (c).single-phase CSC with full-bridge inductor-cell current shaper [8], and (d) current source MMC with half-bridge inductor cells [9].

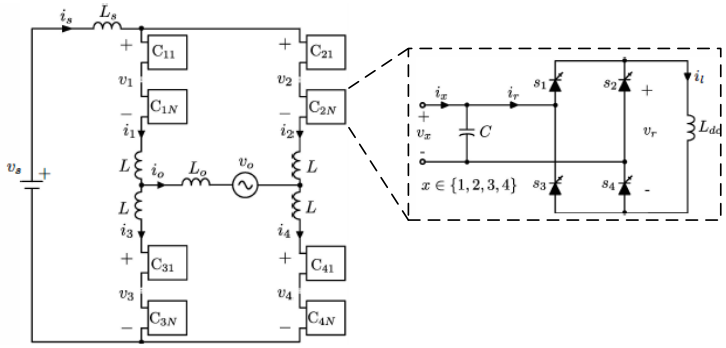


Fig. 3: Voltage scaling of a current source converter using full-bridge cells [10].

While connecting the capacitor cells in series results in a chain link, this paper presents a current source parallel link concept by connecting inductor cells in parallel. The voltage scaling method used in [10] is further generalized by series connecting single-phase current source parallel links, resulting in a current source MMC with voltage scaling capability. Simulation results are provided to demonstrate the operation of the proposed converter and its DC fault tolerance capability.

Current Source Parallel Links using Inductor Cells

Basic Current Source Inductor Cells

Two types of basic current source inductor cells, the unidirectional half-bridge cells and bidirectional full-bridge cells, are shown in Fig. 4. Other inductor cell topologies may be generated from the respective capacitor cells by employing the duality principles. Each switch element in an inductor cell

is capable of blocking bipolar voltage when open, and it is capable of conducting at least unidirectional current when closed (Fig. 4 (c)). A bidirectional current conducting switch is not strictly required but it can certainly constitute a further element of flexibility and functional improvements, should the future switching technologies materialize it. Such a reverse voltage blocking device at the present state of the art can be an IGCT, a GTO, an IGBT in series with a diode, or other semiconductor devices. Wide bandgap semiconductor devices may also be used and can down size the cell inductors with higher switching frequencies.

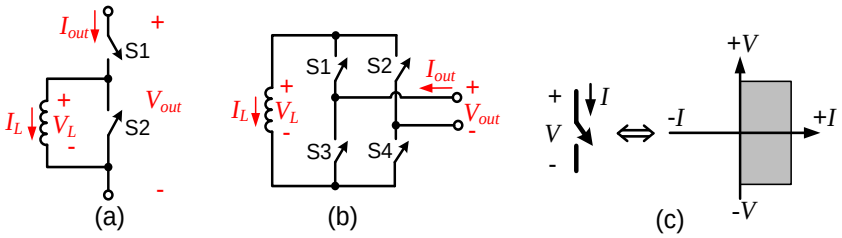


Fig. 4: Basic current source inductor cells: (a) a half-bridge cell, (b) a full-bridge cell; and (c) reverse voltage blocking switches used in these inductor cells.

Since a path must be provided to the inductor current, switches S1 and S2 in Fig. 4 cannot be off at the same time, and the same applies to switches S3 and S4. Table 1 shows the switching states and the associated output currents of a half-bridge inductor cell. When S1 is on and S2 is off, the output current is the inductor current, I_L, and the voltage across the inductor is the cell terminal voltage, V_{out}. When S1 is off and S2 is on, the inductor current is bypassed. If both S1 and S2 are on, the cell output current depends on the cell terminal voltage polarity. This is exactly dual to the half-bridge capacitor cell in a voltage source MMC. Similarly, Table 2 lists the four normal switching states and the associated output currents of a full-bridge inductor cell.

Table 1: Switching states and output current of half-bridge cells

S1	S2	I_{out}	V_L
ON	OFF	I_L	V_{out}
OFF	ON	0	0

Table 2: Switching states and output current of full-bridge cells

S1	S2	S3	S4	I_{out}	V_L
ON	OFF	OFF	ON	I_L	V_{out}
OFF	ON	ON	OFF	$-I_L$	$-V_{out}$
ON	OFF	ON	OFF	0	0
OFF	ON	OFF	ON	0	0

Inductor Cell Open-Circuit Protection

As mentioned above, one potential advantage of a CSC is the easy implementation of open-circuit protection. Dual from the voltage source shoot-through faults, where the effects of high short-circuit currents are of concern (i.e. electrodynamical forces and heating in longer time intervals), here in the current source case, the damages of concerns are those related to the stresses associated with the open-circuit high overvoltage (i.e. partial discharge or arc breakdown in insulating barriers especially towards earth). If both the switches connected to the same inductor terminal become open for any reasons, the voltages across these open switches will unavoidably rise due to lack of a current path for the inductance. Two different cell protection schemes are proposed below. Note that only half-bridge and full-bridge inductor cells are used for illustration. The proposed protection schemes may be used in other inductor cells as well.

1) Cell Protection Using Turn-On Devices

A turn-on device, e.g. a thyristor, may be added in parallel to the cell inductor to provide an emergency current path, as shown in Fig. 5. This turn-on device should be able to block bipolar voltage during normal off states. The thyristor must be turned on to circulate the inductor current in a very short time when an overvoltage is sensed, and save the cells from destruction of insulation breakdown, especially in the inductor. Such a thyristor may also be used to bypass the inductor current

in the case of overcurrent, followed by turning off switches S1 to S4. A mechanical switch, S, shown in Fig. 5, may be used to permanently disconnect the faulty cell.

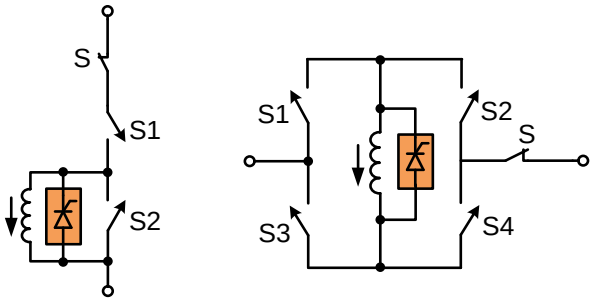


Fig. 5: Cell protection using current circulating thyristors.

2) Cell Protection Using Passive Diodes

To avoid any sensing circuit, control, and/or firing delay, Fig. 6 illustrates another protection scheme against internal open-circuit faults. A back-to-back presspack diode pair is connected in parallel with each switch element in an inductor cell. The diodes must have a lower breakdown voltage than the switch element. Such diodes can be standard rectification diodes, hence very low cost. They do not introduce any significant loss in normal operation because the back-to-back configuration cannot conduct any current other than the inverse leakage current of the reversely biased diode.

When the voltage across any of the controllable switches reaches the breakdown voltage of the presspack diode, at least one reversely biased diode fails as short circuit (a well-proven stable failure mode for presspack diodes), and provides a circulating path for the inductor current. This occurs before the breakdown voltage of the controllable switches is reached. All controllable switches thus have a well-defined protection voltage. No sensing circuit or control is required for this protection scheme, a feature that greatly decreases the risk of protection intervention failure.

It should also be noted that the presspack diodes do not need to be rated for the full current, because after their intervention, the cell will be disabled and rendered "transparent" for the rest of the circuit within few seconds. This reduces their cost further.

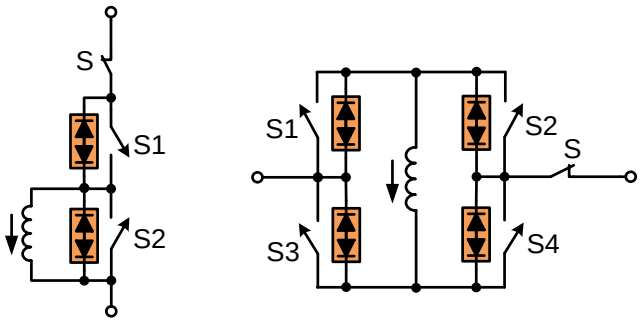


Fig. 6: Cell protection using voltage clamping diodes.

Current Source Parallel Links

A current source parallel link, dual to the voltage source chain link, is realized by connecting the inductor cells in parallel, as shown in Fig. 7. Such a parallel link may consist of the same or different inductor cells, and can synthesize a multilevel current waveform. The inductor cell current balancing can be achieved in the same way as the capacitor voltage balancing in a chain link [11]. For example in the half-bridge case, when the parallel link output current needs to be increased, the next inserted cell is the one with the highest current if V_{link} is positive, and vice versa.

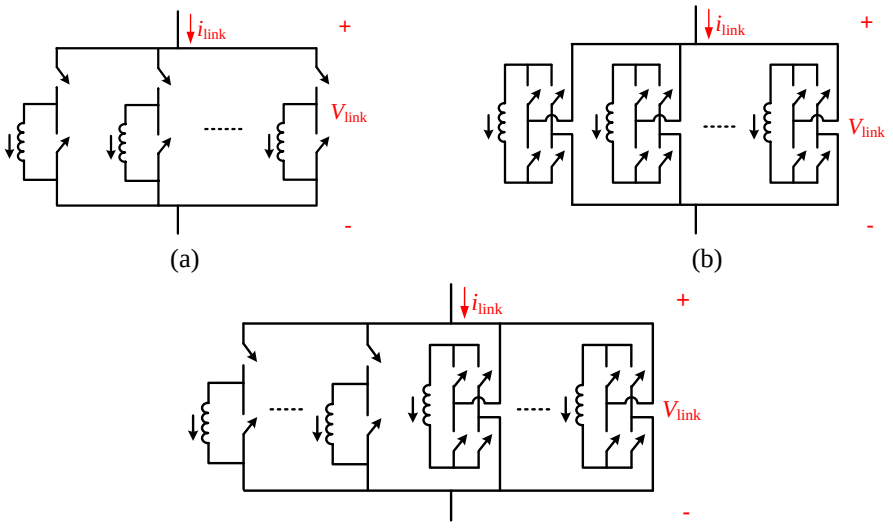


Fig. 7: Current source parallel links using: (a) half-bridge inductor cells, (b) full-bridge inductor cells, and (c) mixed inductor cells

Similar to the capacitor-cell chain links, zero average power should be guaranteed. Considering a lossless simplified case, the terminal voltage and current of the parallel link consist of only a DC and a fundamental AC component, as in

$$\begin{aligned} v_{link}(t) &= V_{link\_dc} + \sqrt{2}V_{link\_ac}\sin(\omega t) \\ i_{link}(t) &= I_{link\_dc} + \sqrt{2}I_{link\_ac}\sin(\omega t + \varphi) \end{aligned}, \tag{1}$$

where ω is the AC fundamental frequency, and φ is the load angle of the AC current.

1) Zero Average Power Constraint

The instantaneous power going into the parallel link is given by

$$\begin{aligned} P_{link}(t) &= v_{link}(t)i_{link}(t) \\ &= V_{link\_dc}I_{link\_dc} + V_{link\_ac}I_{link\_ac}\cos\varphi \\ &\quad + \sqrt{2}V_{link\_ac}I_{link\_dc}\sin(\omega t) + \sqrt{2}V_{link\_dc}I_{link\_ac}\sin(\omega t + \varphi) \\ &\quad - V_{link\_ac}I_{link\_ac}\cos(2\omega t + \varphi) \end{aligned}. \tag{2}$$

Zero average link power over one AC cycle requires

$$\bar{P}_{link} = V_{link\_dc}I_{link\_dc} + V_{link\_ac}I_{link\_ac}\cos\varphi = 0\,. \tag{3}$$

Besides the zero average link power constraint, half-bridge inductor cells, due to their unidirectional current characteristics, requires at least a bipolar terminal voltage to achieve zero average cell power. This additional requirement applies to both the half-bridge-cell and mixed-cell parallel link.

2) Instantaneous Power Interchange

The instantaneous power interchange between the parallel link and external circuit over one AC cycle is given by the last three terms in (2):

$$\Delta P_{link}(t) = A\sin(\omega t + B) - V_{link\_ac} I_{link\_ac} \cos(2\omega t + \varphi)$$
$$\text{where} \quad A = \sqrt{2V_{link\_ac}^2 I_{link\_dc}^2 + 2V_{link\_dc}^2 I_{link\_ac}^2 - 4V_{link\_dc}^2 I_{link\_dc}^2}$$
$$B = \tan^{-1}\left(\frac{V_{link\_dc} I_{link\_ac} \sin\varphi}{C}\right) + \begin{cases} 0 & if \ C \geq 0 \\ \pi & if \ C < 0 \end{cases} \quad , \tag{4}$$
$$C = V_{link\_ac} I_{link\_dc} + V_{link\_dc} I_{link\_ac} \cos\varphi$$

Integrating this instantaneous power interchange gives the stored energy variation in a parallel link (i.e. a major cause of the inductor current ripples):

$$\Delta E_{link}(t) = -\frac{A}{\omega}\cos(\omega t + B) - \frac{V_{link\_ac} I_{link\_ac}}{2\omega}\sin(2\omega t + \varphi)$$
$$E_{link}(t) = E_0 + \Delta E_{link}(t), \ \text{with} \ E_0 = \frac{N}{2} L I_L^2 \quad , \tag{5}$$

where E_0 is the initial/average stored link energy (assuming N identical cells each with current I_L). The maximum stored energy variation is evaluated for a specific half-bridge case below.

For a parallel link with half-bridge cells, the relationship between the AC and DC components is assumed to be

$$\sqrt{2} I_{link\_ac} = m I_{link\_dc} = \frac{m}{2} N I_L$$
$$V_{link\_dc} = -\frac{m}{2}\cos\varphi \sqrt{2} V_{link\_ac} \tag{6}$$

where m is a modulation index between 0 and 1, the max parallel link current = NI_L, min link current = 0, and the zero power constraint (3) is fulfilled.

Assuming E_0 = V_{link_ac} * I_{link_ac} * 0.05s, 1 pu DC current and 1 pu AC voltage, from (3) to (6), the maximum percentage peak-to-peak energy variation is shown in Fig. 8. When the modulation index is high (m>=0.8), the maximum inductor energy variation happens during pure reactive power operation (φ = +/− 90°). When the modulation index is low, the maximum inductor energy variation happens during pure active power operation (φ = 0 or 180°). It is observed that the parallel link energy variation increases as the modulation index decreases, thus it is desired to reduce the DC current amplitude (if possible), when a low AC current is to be generated.

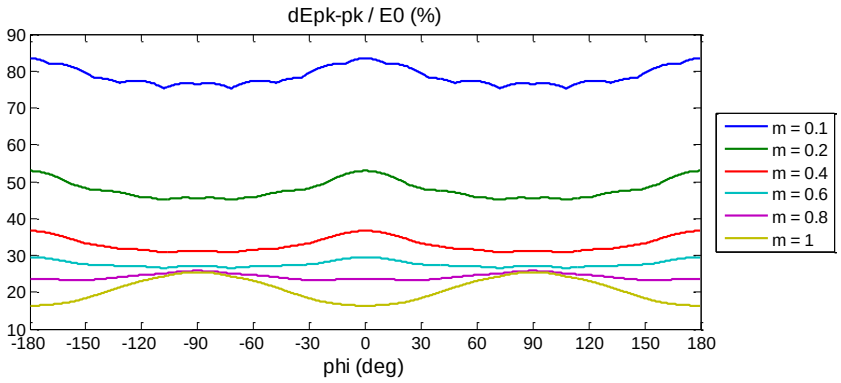


Fig. 8: Stored energy variation of half-bridge-cell parallel links (different load angles and modulation indexes)

Current Source Modular Multilevel Converters

This section introduces a voltage scalable current source MMC by series connection of current source parallel links.

Series Connection of Current Source Parallel Links

The series connection of current source parallel links is dual to the parallel connection of voltage source chain links, as shown in Fig. 9. A capacitor is connected in parallel to each parallel link. These capacitors are essential and may serve three major functions:

- Voltage sharing. Because each capacitor has a defined voltage, they can ensure the steady-state and dynamic voltage sharing between the series-connected current source parallel links.
- Providing current paths. Because the instantaneous currents among the series-connected parallel links and between these parallel links and external circuits can never be guaranteed identical (due to non-identical cell currents, delays, etc.), capacitors are required to absorb any current difference between two series connected current source elements.
- Current filtering. These capacitors may be further rated to absorb the current harmonics generated from the parallel links. Note that the parallel links generate a multilevel current waveform, which does not demand large filters.

Some damping circuits may also be required to avoid resonance between these capacitors and external circuit inductance.

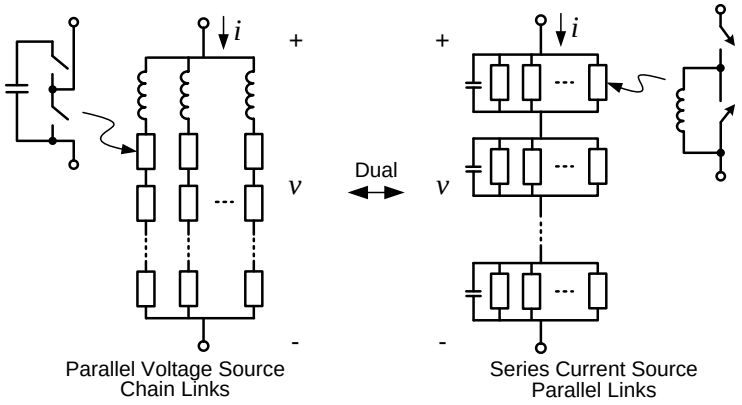


Fig. 9: Series structure of current source parallel links (right).

The parallel capacitor voltage should typically have both DC and AC components, which can be actively controlled through the current source parallel links to ensure dynamic voltage sharing. The DC component of the capacitor voltage may be regulated by controlling the DC component of the parallel link current. The AC component of the capacitor voltage may be regulated by controlling the phase angle of the AC component of the parallel link current.

Current Source MMC Topology

Using the series-connected current source parallel links as a phase arm, Fig. 10 shows a current source MMC topology using half-bridge inductor cells. For a three-phase system, if each parallel link has *m* identical inductor cells and each arm has *n* series connected parallel links, then the ideal voltage and current relationships are given by

$$\begin{aligned} v_{link1} &= \frac{1}{n} v_{ap} = \frac{1}{n}(v_{dp} - v_a) \\ i_{link1} &= i_{ap} - i_{cap1} = \frac{1}{3} i_{dc} + \frac{1}{2} i_a - \frac{1}{n} C \frac{dv_{ap}}{dt} \end{aligned}, \tag{7}$$

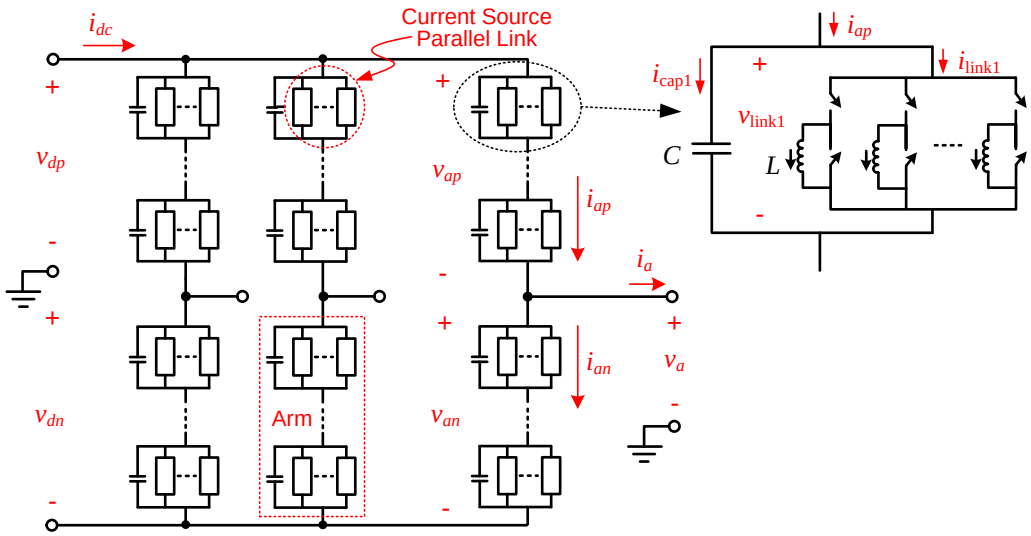


Fig. 10: Hierarchical structure of a current source MMC.

Control Principles

The control principles of this current source MMC are similar to those for a voltage source MMC [11] [12], [13]. In general, the outer P/Q control loop generates arm current references, which are then adjusted to balance energy between arms and balance voltage between series-connected parallel links. The resulting current references are then directly synthesized by the inductor cells in each parallel link, with proper cell-balancing selection scheme. Detailed dynamic analysis and control investigation are still needed in the future.

Simulation Studies

A current source MMC using half-bridge inductor cells is simulated to demonstrate the converter operation and DC fault current limiting capability. Each arm has 3 series-connected parallel links, and each link has 6 parallel-connected half-bridge cells. Table 3 lists the major parameters for the simulation model. The total stored magnetic energy in the cells is around 0.032 s * 135 MVA. Some minimum control loops are set up to allow basic operation of the converter.

Table 3: Parameters for the current source MMC simulation model

S (MVA)	I_{dc} (A)	V_{dc} (kV)	Cell I_L (A)	Cell L (H)	Link C (μF)
135	1800	± 37.5 (m=1)	200	1.99	15.28

Normal Operation

The proposed converter is first tested with normal active power ramping in invertor mode. Results are shown in Fig. 11, where active power output to the AC grid is ramped up from 0.5 pu to 1 pu at unity power factor (power measurements are passed through a 0.01 s low-pass filter). As the active power goes up, the DC side voltage increases, and the DC current remains at 1 pu.

The right plot in Fig. 11 shows more detailed voltage and current waveforms of a parallel link in phase A positive arm. The output current from the parallel link is a 7-level current waveform. The arm current has some higher order harmonics, which are a net effect of switching from other arms. The capacitor provides a path for any current difference between the arm current and the parallel link current. Some fundamental reactive current also flows through the capacitor, which provides a small amount of VAr. The voltage across the parallel link is kept at 1/3 of the arm voltage, and the cells are balanced by a proper selection scheme.

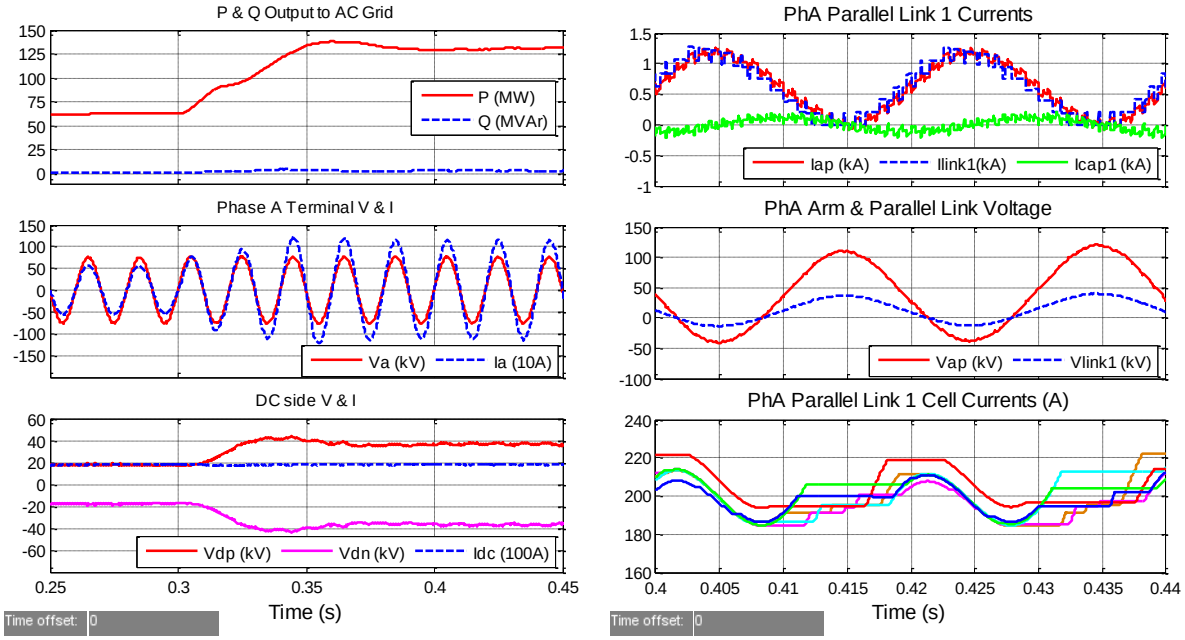


Fig. 11: Active power ramping of current source MMC.

DC Fault

A fault is tested here to show the DC fault tolerance capability of the proposed current source MMC. The converter is initially running at inverter mode outputting 120 MW and 40 MVAr. A DC short-circuit fault is applied at the converter DC terminal at 0.4 s. Results are shown in Fig. 12 and Fig. 13. At the instant of the fault, the link capacitors discharge to the new voltage level, but because this capacitor is very small, the discharging current drops to zero in less than 300 μs. The link capacitors still share the arm voltages during the fault transient because they are in series. The current through the parallel link remains almost unchanged due to the large cell inductance. The AC grid voltage is undisturbed. After the initial transient, the active power commend is reduced to zero and the converter continues to supply reactive power. Note that the DC current cannot be dropped to zero (kept at 1 pu here), because the arms consist of only unidirectional half-bridge cells. Any fault isolation operations must provide an alternative DC current path for the current source converter.

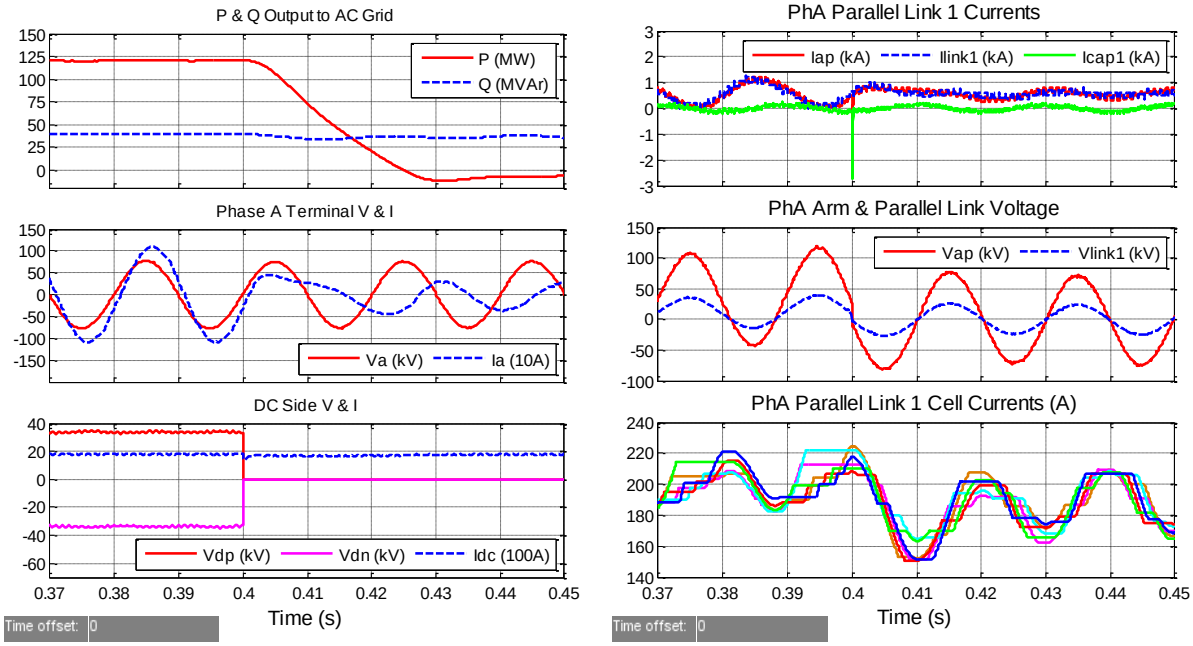


Fig. 12: Current source MMC during DC fault.

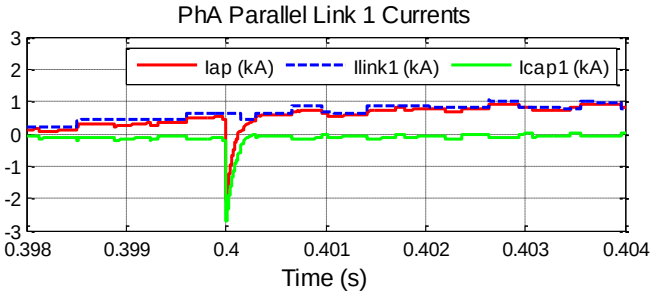


Fig. 13: Parallel link capacitor discharge at the instant of DC fault.

Conclusion

A current source modular multilevel converter topology is proposed in this paper, together with two inductor cell protection schemes, a current source parallel link concept, and series connection of current source parallel links. From the preliminary simulation studies, the proposed converter shows low output current harmonics, independent P/Q control capability, and more importantly DC fault blocking capability. More detailed analytical analysis on the converter dynamics and control design are still needed in future investigations.

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. 2003 IEEE Power Tech Conf.*, Bologna, Italy, June 2003.

[2] S. Allebrod, R. Hamerski, R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proc. IEEE Power Electronics Specialists Conference*, pp. 174-179, Rhodes, Greece, June, 15-19, 2008.

[3] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters" in *Proc. CIGRE Session 2010*, pp. B4–110, Paris, France, Aug. 22-27, 2010.

[4] R. Marquardt, " Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. 8th Int'l Conf. Power Electronics and ECCE Asia (ICPE & ECCE)*, pp.1425-1431, Jeju, South Korea, May 30-June 3, 2011.

[5] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker," ABB Grid Systems Technical Paper, Nov. 2012.

[6] P, Tenca and T. A. Lipo, "A decentralized protection scheme for converters utilizing a DC-link inductor," in *Proc. 2005 IEEE Industrial Electronics Society Annual Conf (IECON)*, Raleigh, NC, USA, Nov. 2005.

[7] Z. Bai and Z. Zhang, "Confirmation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electronics*, vol. 23, no. 5, pp. 2260-2267, Sept. 2008.

[8] T. Noguchi and S. Suroso, "Review of novel multilevel current-source inverters with H-bridge and common-emitter based topologies," in *Proc. 2010 IEEE Energy Conversion Congress and Exposition (ECCE*), Atlanta, GA, USA, Sept. 2010.

[9] Y. Zhang, T. Tang, L. Chen, F. Guo, and J. Li, "A novel voltage-source converter topology suitable for interface of renewable sources," in *Proc. Int'l Conf. Electrical Machines and Systems (ICEMS 2009)*, Tokyo, Japan, Nov. 15-18, 2009

[10] Marcelo A. Perez, Ricardo Lizana, Camilo Azocar, Jose Rodriguez, Bin Wu, "Modular multilevel cascaded converter based on current source H-Bridges cells, " in *Proc. 2012 IEEE Industrial Electronics Society Annual Conf (IECON)*, Montreal, QC, Canada, Oct. 2012.

[11] E. Solas, G. Abad, J. A. Barrena, A. Cárcar, and S. Aurtenetxea, "Modulation of Modular Multilevel Converter for HVDC application," in *Proc. 14th Int'l Power Electronics and Motion Control Conf. (EPE/PEMC 2010)*, Ohrid, Republic of Macedonia, Sept. 6-8, 2010.

[12] A. Antonopoulos, L. Angquist, and Hans-Peter Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th European Conf. Power Electronics and Applications (EPE'09)*, Barcelona, Spain, Sept. 8-10, 2009.

[13] L. Harnefors, S. Norrga, A. Antonopoulos, and H.-P. Nee, "Dynamic modeling of modular multilevel converters," in *Proc. 14th European Conf. Power Electronics and Applications (EPE'11)*, Birmingham, UK, Aug. 30-Sept. 1, 2011.