Review

Cyril R.A. John Chelliah* and Rajesh Swaminathan*

Current trends in changing the channel in MOSFETs by III–V semiconducting nanostructures

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Abstract: The quest for high device density in advanced technology nodes makes strain engineering increasingly difficult in the last few decades. The mechanical strain and performance gain has also started to diminish due to aggressive transistor pitch scaling. In order to continue Moore's law of scaling, it is necessary to find an effective way to enhance carrier transport in scaled dimensions. In this regard, the use of alternative nanomaterials that have superior transport properties for metal-oxide-semiconductor field-effect transistor (MOSFET) channel would be advantageous. Because of the extraordinary electron transport properties of certain III–V compound semiconductors, III–Vs are considered a promising candidate as a channel material for future channel metal-oxide-semiconductor transistors and complementary metal-oxide-semiconductor devices. In this review, the importance of the III–V semiconductor nanostructured channel in MOSFET is highlighted with a proposed III–V GaN nanostructured channel (thickness of 10 nm); Al_2O_3 dielectric gate oxide based MOSFET is reported with a very low threshold voltage of 0.1 V and faster switching of the device.

Keywords: III–V; channel; GaN channel; MOSFET; nanostructures; TCAD.

1 Introduction

The density of the device and its high switching speed and excellent power efficiency are the outcomes of the scaling of dimensions and voltages in complementary metal-oxide-semiconductor (CMOS) technology. Moore's law [1], generally known by areal scaling factor of 2 approximately every 18 months, has been ruling the microelectronics industry for the past decades. Moore's law also has many other performance and economic virtues which has resulted in increased power density approaching unsustainable levels. In this regard, power density is recognized as a key constraint for the continuation of Moore's law, which would threaten to halt the microelectronics revolution [2, 3]. To address this issue, computation must be performed in a more energy-efficient manner in which the performance gain of integrated circuits (ICs) is no longer relying on increased power density.

The power density in ICs is reduced by minimizing the supply voltage, V_{DD}. The subthreshold regime and the gate overdrive regime are the two regimes in the span of supply voltage, which are separated by the threshold voltage, V_{TH}. This is illustrated in the typical metal-oxide-semiconductor field-effect transistor (MOSFET) current transfer characteristics in Figure 1A.

By reducing the subthreshold component, V_{TH}, or the gate overdrive component, V_{DD}-V_{TH}, V_{DD} reduction can be realized. However, because of the non-scalability of the rate of change of current with gate voltage, defined as the "subthreshold swing" measured in decades of current change per volt that is imposed by the limit of thermionic emission, there is little room for V_{TH} reduction for logic MOSFETs. In fact, V_{TH} is expected to remain constant or increase slightly for transistors with smaller dimensions because short channel effects (SCEs) such as increase of subthreshold swing, S, and drain-induced-barrier lower, DIBL, and increased threshold voltage variation will require higher V_{TH} to achieve a given I_{OFF} target. This is illustrated in Figure 1B which shows the prediction of V_{DD} and V_{TH} from the International Technology Roadmap of Semiconductors (ITRS) [4, 5].

It indicates that the supply voltage V_{DD} needs to decrease from 0.8 V to 0.6 V from the 21 nm node to the 6.3 nm node in the next 8 years, while the saturation threshold voltage, $V_{T,SAT}$, of the n-channel type MOSFETs has to increase from 0.21 V to 0.24 V. The consequence of this is reduction of the gate overdrive, V_{DD}-V_{TH}, which will eventually compromise the drive current in the ON-state.

*Corresponding authors: Cyril R.A. John Chelliah and Rajesh Swaminathan, Nanoelectronics Laboratory, Centre for Research in Nanotechnology, Department of Nanoscience and Technology, Karunya University, Coimbatore 641114, India,
e-mail: cyrilrobinson@karunya.edu.in (C.R.A. John Chelliah); drsrajesh@karunya.edu (R. Swaminathan). http://orcid.org/0000-0003-4210-7474 (C.R.A. John Chelliah)

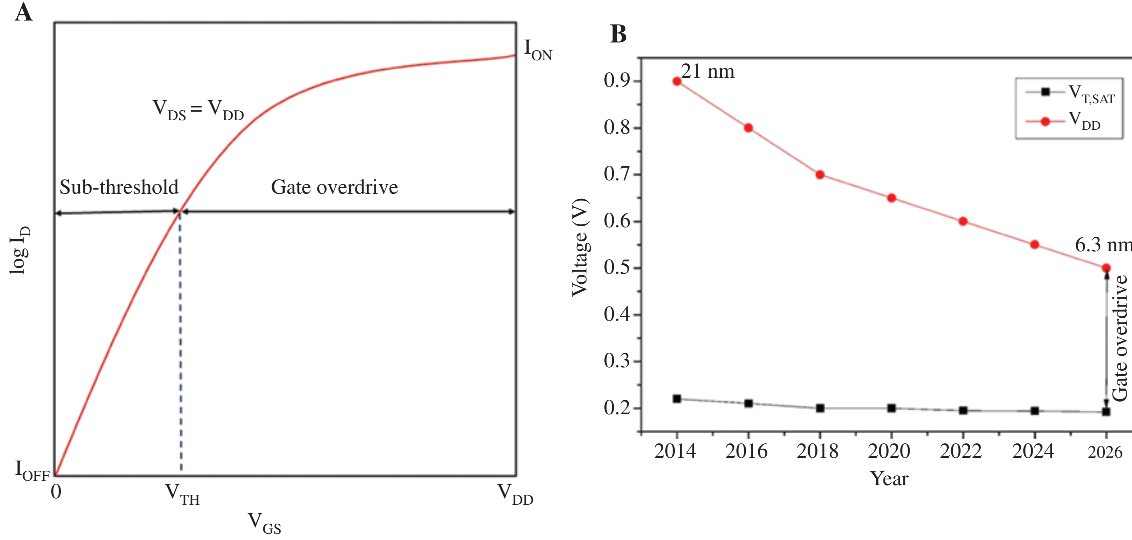

Figure 1: (A) Characteristic curve of MOSFET I_D-V_{GS}. (B) ITRS specification for supply voltage (V_{DD}) and nMOS saturated threshold voltage ($V_{T,SAT}$) scaling with respect to the upcoming devices. $V_{T,SAT}$ is the threshold voltage at $V_{DS} = V_{DD}$ [4, 5].

Furthermore, the aggressive pitch size scaling deteriorates the series resistance [6–8]. The contribution of the extrinsic parasitic components to the total ON-resistance will keep increasing and further degrade the drive current. To compensate the drive current loss, transport-enhanced channel transistors have been proposed and are currently used or explored for modern CMOS logic devices.

The drive current, I_{ON}, for modern deeply scaled transistors, can be described by equation (1):

$$I_{ON} = v_{inj} \cdot Q_{inv} \approx v_{inj} \cdot C_{inv} \cdot (V_{GS} - V_{TH}), \tag{1}$$

V_{GS}–V_{TH} is the gate overdrive and $C_{inv} \cdot (V_{GS} - V_{TH})$ gives the inversion layer charge at the virtual source. For a given gate capacitance and gate overdrive, the drive current is proportional to the source injection velocity, v_{inj} [9]. The source injection velocity is a parameter that governs carrier transport in field-effect transistors. Its physical meaning is illustrated in Figure 2, which depicts a typical MOSFET biased in strong inversion in saturation. The conduction band potential from source to drain is illustrated. The virtual source is located at the top of the barrier, $x = x_o$ [8–10]. It portrays the injection velocity of electron on top of the potential barrier where the virtual source is located.

For a given material system, the maximum possible value for v_{inj} is determined by the unidirectional thermal velocity v_θ toward the channel for carriers at $x = x_o$. This case is referred to as ballistic transport. In a modern logic transistor whose channel length is close to or smaller than the mean free path, the transistor operates near the ballistic transport limit. For conventional n-type MOSFETs, due to the relatively heavy effective mass of electron and low thermal velocity in relaxed silicon, v_{inj} saturates around 1×10^7 cm/s [8–10].

An effective way to break this bound is through transport-enhanced channel engineering. The most well-known technology of this type is strained silicon, which was adopted in manufacturing since early 2000s [11–13]. The electron and hole velocity enhancement through strained silicon is limited by the available methods to couple increased amount of uniaxial strain into the channel [12]. A lot of researches have been directed to introduce higher strain in the silicon channel. For instance, in the multiple-stressor scheme, Si:C stressors in the source and drain and SiGe stressors beneath the channel are introduced to enhance the uniaxial tensile strain in the n-type silicon channel [13]. Such technology can bring up the source injection velocity in n-type MOSFETs to about 1.6×10^7 cm/s [12, 14].

Despite the great success of strained-silicon technology in the last decade, the quest for high device density in advanced technology nodes makes strain engineering increasingly difficult. The mechanical strain and performance gain has started to diminish due to aggressive transistor pitch scaling. To continue Moore's law of scaling, it is imperative to find an effective way to enhance carrier transport in scaled dimensions. In this regard, the use of alternative materials that have superior transport properties for MOSFET channel would be advantageous. Because of the extraordinary electron transport properties of certain III–V compound semiconductors, III–Vs are considered a promising candidate as an n-type channel material for future CMOS logic [15].

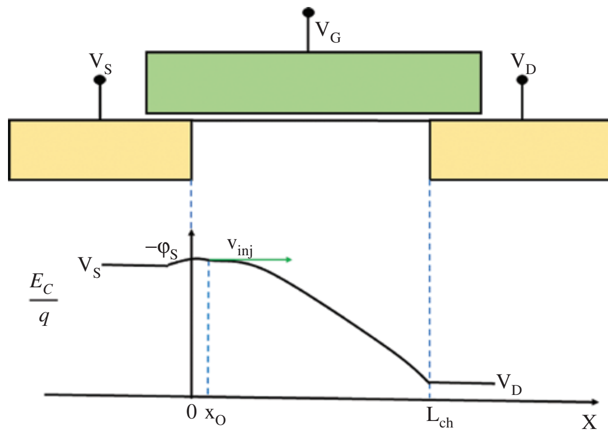

Figure 2: Simplified schematic of a MOSFET and the potential profile along the channel from source to drain when the device is on [9].

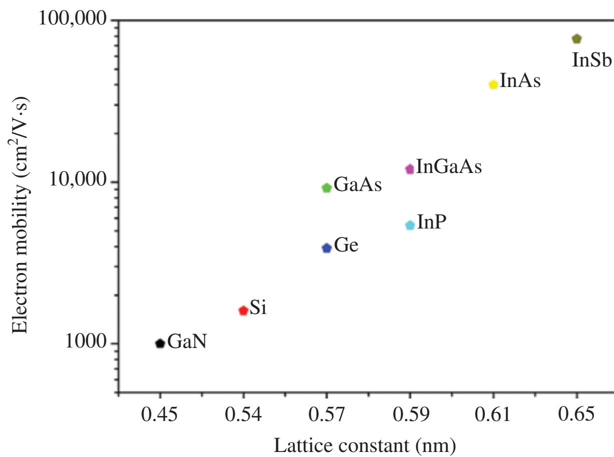

Figure 3: The highest electron mobility at room temperature in inversion layers and quantum wells for various semiconductors is shown as a function of actual semiconductor lattice constant [15].

Mobility is an important metric to evaluate the transport properties of a material system in the drift-diffusion limit. However, mobility is also closely related to the ballistic velocity in the ballistic transport limit through the effective mass [16]. When the increase in mobility is purely due to the decrease in the effective mass, ballistic velocity exhibits a power law dependence on mobility, $v_\theta \propto \mu^{1/2}$. The mobility of many III–V compound semiconductors is far greater than that of silicon.

Figure 3 shows the highest room-temperature mobility of electrons in inversion layers and quantum wells as a function of the actual lattice constant for several semiconductors of interest [15]. The highest electron mobility of 32,000 $cm^2/V\cdot s$ can be found in InSb and unstrained InAs. However, it is difficult to grow InSb and unstrained InAs on pseudomorphic substrates and build device prototypes due to large lattice mismatch to commonly available substrates such as GaAs and InP. On the other hand, reasonably thick strained InAs and $In_xGa_{1-x}As$ can be grown on a lattice-mismatched pseudomorphic InP substrate. The InAs composition x can vary from 0.53 to 1. Biaxial compressive strain of 3.1% results when InAs is grown on InP. In this case, the mobility of InAs is greater than 18,000 $cm^2/V\cdot s$.

2 Evolution of III–V CMOS FETs

2.1 Overview of III–V FETs

A brief overview of the indium gallium arsenide (InGaAs) field-effective transistor (FET) is given here. Two main architectures of InGaAs FETs are Schottky-gate high-electron-mobility transistors (HEMT) and insulated-gate MOSFET. Both of them were invented in the early 1980s. Figure 4 graphs the record transconductance, gm, as a representative metric to evaluate these two device technologies. Here, InGaAs refers to any composition of the ternary from pure GaAs to pure InAs. HEMTs made persistent progress immediately after their first demonstration in 1980. Since then, they have been delivering the highest transconductance and cut-off frequency in the family of III–V FETs [18], and have also been turned into a very successful transistor technology.

On the contrary, the InGaAs MOSFETs were evolving very slowly in the 1980s and 1990s. This was until mid-2000s when a rapid performance improvement started to happen because the prospect of III–V CMOS started to attract tremendous research interest around the world.

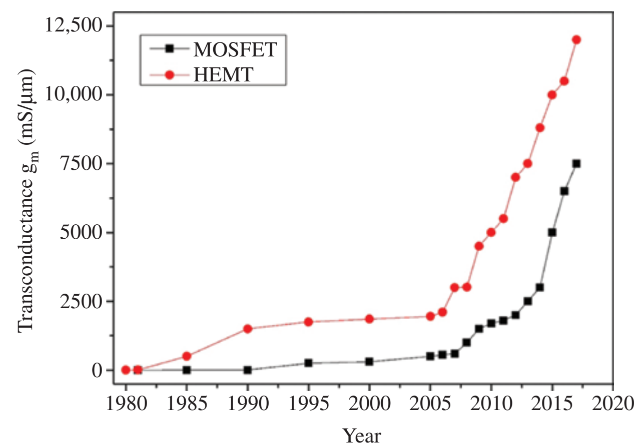

Figure 4: Record transconductance for InGaAs HEMT and MOSFET since their invention [17].

III–V CMOS research greatly accelerated the device innovation of InGaAs MOSFETs. MOSFETs have demonstrated their potential and exceeded the transconductance performance of HEMT in 2014. This record InGaAs MOSFET device, among a few others, was developed in the course of this review work.

Since the mid-2000s, a variety of III–V FET architectures were invented and investigated, including HEMT and MOSFET. They were used for the study of CMOS-relevant process integration and device physics.

2.2 III–V HEMT as a CMOS logic device

HEMT is a popular III–V device architecture for several unique electronic applications including millimeter wave and power amplifiers [19]. Owing to its similar operating principle as the MOSFET and the maturity and simplicity of its process, HEMT has also been used as the platform for device physics study for transistors with III–V CMOS channels. Those devices indeed have generated profound new understandings. As shown in Figure 5, HEMTs with the III–V channel can deliver at least 2 times v_{inj} compared to strained silicon at reduced drain voltages [15]. Increased InAs composition in $In_xGa_{1-x}As$ leads to v_{inj} enhancement. These results are evidence to support the superior electron transport properties of this material system and showcase the advantage for future high-performance and low-power CMOS applications.

The 35-year research on HEMTs has reached a mature fabrication process and device architecture that feats the transport advantage of the III–V channel for high-frequency applications. Accordingly, the process and structure of HEMTs has continued relatively unchanged over the years. The configuration which is not suitable for the CMOS applications is discussed below. The first problem is associated with the gate leakage. In high-density circuit, the gate leakage density should be bound below 1 A/cm². "Schottky gate" technology uses HEMT devices in which the gate metal is directly placed on top of a wide bandgap semiconductor or barrier (InAlAs). Due to the small band offsets, carriers can easily tunnel across the barrier if it is thin. In this case, the gate leakage can easily exceed 100 A/cm² in the ON-state [20–24]. The gate leakage limits how thin the barrier can be scaled. This compromises the SCE control when the lateral dimensions of the device are scaled down. Secondly, the removal of the n-dope semiconductor above the channel in the gate region is called "gate recess". Typical gate recess is done by selective wet etch, which results in an appreciable lateral extent and an "underlap" device architecture. This is in contrast to the modern CMOS "overlap" architecture in which the n+ region is slightly overlapped with the gate. The underlap region limits the device footprint and increases series resistance. Thirdly, since footprint is not a major concern for HEMT, typical fabrication of the gate and source/drain usually uses two separate masks. This violates the self-alignment principle required for the fabrication of front-end logic transistors. A long access region must be reserved for the lithography alignment tolerance, directly leading to a large source-to-drain spacing, approximately 2 µm. And also, HEMTs use Au-containing alloy to form the gate, source, and drain electrodes, while the pattern definition uses lift-off processes which result in the violation of CMOS compatibility in both materials and process.

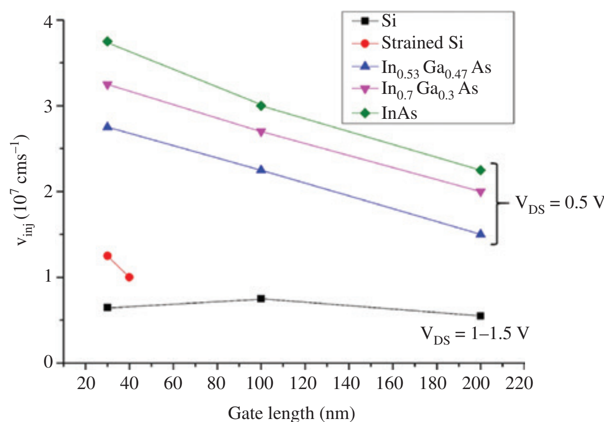

Figure 5: Source injection velocity for InAs HEMTs and silicon or strained-silicon FETs as a function of gate length [17].

2.3 Issues faced by III–V MOSFET

In this section, some of the important issues faced by III–V MOSFETs in logic applications are discussed in brief. Unlike the fruitful technologies like silicon MOSFETs and III–V HEMTs, there has only been very limited research effort on III–V MOSFETs before the mid-2000s, and those research efforts were rather failure attempts. This was mainly due to the lack of a stable oxide on III–V for gate insulator. High-quality gate stack is the heart of a MOSFET. This challenge must be first addressed before the potential of III–V for CMOS application can be realized. Recent advancements in atomic layer deposition and pulsed laser deposition (PLD) have provided the critical enabling technology to address this challenge [25, 26]. Since the gate insulator is a deposited material, the oxide/III–V interface quality is a serious concern which directly affects current drive and SCE immunity in scaled

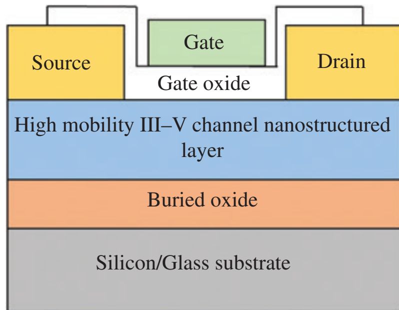

Figure 6: Cross-sectional schematic of a planar logic III–V MOSFET.

transistors. Pitch dimension is a requirement imposed by the high-density logic applications. The gate pitch of modern silicon MOSFET is well below 100 nm, within which there are three functional regions: one gate, one silicide contact, and two spacers. In the III–V terminology, they are equivalent to the gate, the ohmic contacts – source and drain, and the active regions such as high-mobility III–V based nanostructured channel layer as illustrated in Figure 6.

The lengths of those functional regions must be measured precisely and in a self-aligned manner. For CMOS-compatibility and manufacturability, neither lift-off nor Au is allowed for the CMOS front-end process. Nanoscale contact technology on III–V transistor has to be developed.

In addition to the process requirements, the III–V contact must also be able to deliver low film resistivity and low contact resistivity as required by future CMOS devices [27]. Due to those constraints, the source and drain contacts for III–V MOSFET remain a great challenge. The integration of III–V MOSFETs onto a silicon substrate is also an imperative but very challenging topic. As shown in Figure 6, the large lattice mismatch between the III–V channel semiconductors and silicon prevents direct pseudomorphic growth. An effective approach for co-integration is still to be developed.

3 Literature survey

3.1 Replacing Si channel with III–V

The article by Stevenson [28] sparks an idea about changing the channel in transistors. In his article "changing the channel" briefly explained that the transistor is not shrinking the way it used to. Moreover, he mentioned that the best ones we have today are a patchwork of fixes and kludges: speed-boosting materials that push or pull on the silicon center, exotic insulators added to stanch leaks, and a new geometry that pops things out of the plane of the chip and into the third dimension. Now, to keep Moore's law going, chipmakers are eyeing another monumental change in transistor architecture. He also added that in this era, researchers are taking aim at the current-carrying channels at the very heart of the device, replacing the silicon there with germanium and compound semiconductors known as III–Vs. If all goes well, these materials could usher in a new generation of speedier, less power-hungry transistors, allowing for denser, faster, cooler-running chips [28].

del Alamo [17] reported that ICs based on InGaAs field effect transistors are currently in wide use in the radio frequency (RF) front-ends of smart phones and other mobile platforms, wireless local area networks (LANs), high data rate fiber-optic links, and many defense and space communication systems. InGaAs ICs are also under intense research for new millimeter-wave applications such as collision avoidance radar and gigabit wireless local area networks. InGaAs FET scaling has nearly reached the end of the road, and further progress to propel this technology to the terahertz regime will require significant device innovations. Separately, as Si CMOS faces mounting difficulties to maintain its historical density scaling path, InGaAs-channel MOSFETs have recently emerged as a credible alternative for mainstream logic technology capable of scaling to the 10 nm node and below. To get to this point, fundamental technical problems had to be solved, though there are still many challenges to be addressed before the first non-Si CMOS technology becomes a reality. The intense research that this exciting prospect is generating is also reinvigorating the prospects of InGaAs FETs to become the first true terahertz electronics technology. This paper reviews progress and challenges of InGaAs-based FET technology for terahertz and CMOS [17].

Gu et al. [29] reported that high-performance InGaAs gate-all-around (GAA) nanowire (NW) MOSFETs with channel length (L_{ch}) down to 20 nm are fabricated by integrating a higher k $LaAlO_3$-based gate-stack with an equivalent oxide thickness (EOT) of 1.2 nm. It is found that inserting an ultrathin (0.5 nm) Al_2O_3 interfacial layer between the higher k $LaAlO_3$ and InGaAs can significantly improve the interface quality and reduce device variation. As a result, a record low subthreshold swing of 63 mV/dec is demonstrated at sub-80-nm L_{ch} for the first time, making InGaAs GAA NW devices a strong candidate for future low-power transistors [29].

Persson et al. [30] presented dc and RF characterization as well as modeling of vertical InAs NW MOSFETs with $L_G = 200$ nm and Al_2O_3/HfO_2 high-κ dielectric. Measurements at $V_{DS} = 0.5$ V show that high transconductance ($gm = 1.37$ mS/μm), high drive current ($I_{DS} = 1.34$ mA/μm),

and low ON-resistance (R_{ON} = 287 Ω μm) can be realized using vertical InAs NWs on Si substrates. By measuring the 1/f-noise, the gate area normalized gate voltage noise spectral density, SVG · LG · WG, is determined to be lowered by one order of magnitude compared with similar devices with a high-κ film consisting of HfO_2 only. In addition, with a virtual source model we are able to determine the intrinsic transport properties. These devices (LG = 200 nm) show a high injection velocity ($v_{inj} = 1.7 \times 10^7$ cm/s) with a performance degradation for array FETs predominantly due to an increase in series resistance [30].

Li et al. [31] reported the reliability performance of $InxGa_{1-x}As$ n-MOSFETs with Al_2O_3 gate dielectric; under positive-bias temperature instability stress is investigated. The following new phenomena are demonstrated: (1) There are high densities of fast interface traps Nit and slow oxide border traps N_{SOX} near the interface between InGaAs and Al_2O_3. The border traps are more fragile under stress, and therefore, the stress mainly induces border traps. (2) The stress-induced border traps consist of permanent acceptor traps and recoverable donor traps. Acceptor trap energy density ΔD_{SOX}Acceptor(E) is mainly distributed above the conduction band edge E_c of InGaAs with a tail extending to the midgap, whereas donor trap energy density ΔD_{SOX}Donor(E) has a large distribution inside the InGaAs energy gap with a tail extending to the conduction band. (3) Flicker noise variation after stress and its correlation to the acceptor and donor trap generation and recovery are demonstrated. (4) The recoverable donor traps induce the subthreshold slope and off-current degradation in the stress phase and recover in the recovery phase and also induce continuous degradation of on-current in the recovery phase. The permanent acceptor traps induce the transconductance and on-current degradation. The long-term device lifetime is mainly determined by the generation rate of the acceptor traps. (5) Comprehensive comparison between the Si and InGaAs MOSFETs' degradation behaviors under bias temperature instability stress is presented. The physical recovery of donor oxide traps in dielectric in InGaAs/Al_2O_3 has never been observed in a Si MOS structure, deserving special attention and further investigation [31].

Svensson et al. [32] reported that III–V semiconductors have attractive transport properties suitable for low-power, high-speed CMOS implementation, but major challenges related to co-integration of III–V n- and p-type MOSFETs on low-cost Si substrates have so far hindered their use for large-scale logic circuits. By using a novel approach to grow both InAs and InAs/GaSb vertical NWs of equal length simultaneously in one single growth step, we here demonstrate n- and p-type III–V MOSFETs monolithically integrated on a Si substrate with high I_{on}/I_{off} ratios using a dual channel, single gate-stack design processed simultaneously for both types of transistors. In addition, we demonstrate fundamental CMOS logic gates, such as inverters and NAND gates, which illustrate the viability of our approach for large-scale III–V MOSFET circuits on Si [32].

Mohd Razip Wee et al. [33] reported that a multi-gate n-type $In_{0.53}Ga_{0.47}As$ MOSFET is fabricated using gate-first self-aligned method and air-bridge technology. The devices with different gate lengths were fabricated with the Al_2O_3 oxide layer with a thickness of 8 nm. In this letter, impact of gate length variation on device parameter such as threshold voltage, high and low voltage transconductance, subthreshold swing, and off current are investigated at room temperature. Scaling the gate length revealed good enhancement in all investigated parameters, but the negative shift in threshold voltage was observed for shorter gate lengths. The high drain current of 1.13 A/mm and maximum extrinsic transconductance of 678 mS/mm with a field effect mobility of 364 cm^2/Vs are achieved for the gate length and width of 0.2 mm and 30 mm, respectively. The source/drain overlap length for the device is approximately extracted about 51 nm with the leakage current in the order of 10^{-8} A. The results of RF measurement for cut-off and maximum oscillation frequency for devices with different gate lengths are compared [33].

Conrad et al. [34] reported that further Si CMOS scaling requires development of high-mobility channel materials and advanced device structures to improve the electrostatic control. He demonstrates the fabrication of GAA InGaAs MOSFETs with highly scaled atomic-layer-deposited gate dielectrics. InGaAs, with its high electron mobility, allows higher drive currents and other on-state performance compared to silicon. The GAA structure provides superior electrostatic control of the MOSFET channel with outstanding off-state performance. A subthreshold slope of 72 mV/dec, electron mobility of 764 $cm^2/V \cdot s$, and an on-current of 1.59 mA/μm are demonstrated, for example. Variability studies on on-state and off-state performances caused by the number of NW channels are also presented [34].

Mehrotra et al. [35] reported that as MOSFETs channel lengths (Lg) are scaled to lengths shorter than Lg < 8 nm, source-drain (S-D) tunneling starts to become a major performance-limiting factor. In this scenario, a heavier transport mass can be used to limit S-D tunneling. Taking InAs and Si as examples, it is shown that different heavier transport masses can be engineered using strain and crystal-orientation engineering. Full-band extended device atomistic quantum transport simulations are performed for NW MOSFETs at Lg < 8 nm in both ballistic and incoherent scattering regimes. In conclusion, a heavier transport

mass can indeed be advantageous in improving ON-state currents in ultrascaled NW MOSFETs [35].

Yuan et al. [36] reported the formation and electrical properties of Ni-GaSb alloys by direct reaction of Ni with GaSb. It is found that several properties of Ni-antimonide alloys, including low thermal budget processing (300°C), low Schottky barrier height for holes (~0.1 eV), low sheet resistance of Ni-InGaSb (53 Ω/square), and low specific contact resistivity (7.6×10^{-7} Ω cm^2), show good progress toward antimonide-based metal S-D p-channel MOSFETs. Devices with a self-aligned metal S-D were demonstrated, in which heterostructure design is adopted to further improve the performance, e.g. ON/OFF ratio, subthreshold swing (140 mV/decade), and high effective-field hole mobility of ~510 cm^2/Vs at sheet charge density of 2×10^{12} cm^{-2} [36].

Chang et al. [37] demonstrated that compressively strained GaSb devices outperform relaxed Ge in terms of ballistic current. According to the simulations, as effective oxide thickness scales down to 0.5 nm, both the group IV and III–V p-channel devices can be assumed to operate in the classical capacitance limits, where the I_D-V_G characteristics are basically governed by the transport effective mass. As a consequence, I_{ON} enhancement is owing to the reduced transport effective mass whether it results from alternative materials, optimized transport directions, and strain effects.

3.2 III–V MOS devices reports

Table 1 below presents the observed information from various literature regarding III–V MOS devices. Koveshnikov et al. [38] demonstrated the first time the electrical properties of III–V based MOS capacitors made on 250 nm thick MBE GaAs with ultra-thin *in situ* grown Si interface passivation layer and *ex situ* deposited HfO_2

Table 1: Literature reported on III–V MOS devices.

References	III–V MOS device configuration used	Observed details
[38]	TaN/HfO_2/GaAs/Si	– Demonstrated the first time the electrical properties of III–V based MOS capacitors made on 250 nm thick MBE GaAs with ultra-thin *in situ* grown Si interface passivation layer and *ex situ* deposited HfO_2 gate oxide and TaN gate – Provide good capacitance-voltage characteristics with equivalent oxide thickness (EOT) of 2.1 nm
[39, 40]	Au/Al_2O_3/InGaAs/InP substrate	– It is suitable for digital applications because it is normally off at zero bias – Turning it on at a positive gate bias provides a drain current of 1.05 A/mm. This drain current is far higher than GaAs PHEMTs and InP HEMTs, and comparable to GaN HEMTs grown on SiC
[41]	InGaAs/BOX – SiO_2/Si	– In the 22 nm technology node and beyond, where III–V MOSFETs are expected to be introduced, SOI-based ultrathin body structures or nano-wire structures are mandatory for suppressing SCEs
[42]	HfO_2/Al_2O_3/GeO_2/Ge	– Gate stack and channel engineering for improving the channel mobility and the MOS interface properties with emphasis on thin EOT and ultrathin body, which are mandatory in the future nodes
[17]	Mo/HfO_2/InP/InGaAs channel/2DEG/InAlAs/InP	– The performance of these devices was seen to improve as more InAs was introduced in the channel
[36]	W/Al_2O_3/InGaSb/AlGaSb Ni-GaSb as source and drain	– Low thermal budget processing (300°C) – Low Schottky barrier height for holes (~0.1 eV) – Low sheet resistance of Ni-InGaSb (53 Ω/square) – Low specific contact resistivity $(7.6\times10)^{-7}$ Ω cm^2 improves the performance, e.g. ON/OFF ratio – Subthreshold swing (140 mV/decade) – High effective-field hole mobility of ~510 cm^2/Vs at sheet charge density of 2×10^{12} cm^{-2}
[43]	Mo/HfO_2InP/InGaAs/InAs/InAlAs	– To reduce the operating voltage as transistor density increases but the power density budget remains unchanged in Si – Recent demonstrations of self-aligned planar and VNW-MOSFETs give credibility to the use of III–Vs (InGaAs) in sub-10 nm CMOS nodes
[37]	GaSb and InSb as channel	– I_{ON} enhancement due to the reduced transport effective mass whether it results from alternative materials, optimized transport directions, and strain effects – Simulated ballistic currents across the group IV and III–V-based UTB devices indicate that Ge, GaSb, and InSb pMOSFETs provide relatively better performance than that of Si, GaAs, and InAs

gate oxide and TaN gate. It provides good capacitance-voltage characteristics with EOT of 2.1 nm. In 2008, Ye [39, 40] demonstrated a III–V based device using InGaAs as the channel on the InP substrate with Al_2O_3 as the gate dielectric. This device is reported to be suitable for digital applications because it is normally off at zero bias and provides more drain current compared with GaAs based PHEMT and InP based HEMT [39, 40]. In the 22 nm technology node and beyond, where III–V MOSFETs are expected to be introduced, SOI-based ultrathin body structures or nanowire structures are mandatory for suppressing SCEs. It is suggested by Takagi et al. [41] in his findings with InGaAs/BOX-SiO_2/Si. Later, he suggested while working with HfO_2/Al_2O_3/GeO_2/Ge device in 2012 that gate stack and channel engineering is essential for improving the channel mobility and the MOS interface properties with emphasis on thin EOT, and ultrathin body are mandatory in the future nodes [42]. del Alamo [17] reported that the performance of Mo/HfO_2/InP/InGaAs channel/2DEG/InAlAs/InP based devices was seen to improve as more InAs was introduced in the channel [17]. Yuan et al. [36] demonstrated a device with W/Al_2O_3/InGaSb/AlGaSb in which Ni-GaSb is the source and drain. The device provided the following merits: low thermal budget processing (300°C), low Schottky barrier height for holes (~0.1 eV), low sheet resistance of Ni-InGaSb (53 Ω/square), low specific contact resistivity (7.6×10^{-7} Ω cm^2), improved performance, e.g. ON/OFF ratio, subthreshold swing (140 mV/decade), and high effective-field hole mobility of ~510 cm^2/Vs at sheet charge density of 2×10^{12} cm^{-2} [36]. del Alamo et al. [43] demonstrated that the configuration prior to the configuration provided Mo/HfO_2/InP/InGaAs/InAs/InAlAs and suggested that self-aligned planar and VNW-MOSFETs give credibility to the use of III–Vs (InGaAs) in sub-10 nm CMOS nodes [43].

3.3 III–V nanostructured channel based devices reports

Table 2 below presents the observed information from various literature regarding III–V nanostructured channel based devices. In 2011, Nilsson et al. [44] introduced the III–V InSb NW as a channel. Due to low bandgap of InSb, I_{OFF} of the device is high and resulted in ambipolar current-voltage characteristics. Along with the findings, a region of Coulomb blockade oscillation is also found above the threshold voltage of 0 V, which is very interesting to work with such nanostructures for the researchers [44]. Forbes et al. [45] implemented GaAs/InAs quantum dot (QD)/GaAs/GaP/GaAs substrate, and the results due to the QDs on substrate

Table 2: Literature reported on III–V nanostructured channels (quantum dots/nanorods/nanotubes/nanowires) based devices.

References	III–V Nanostructured channel device configuration used	Observed details
[44]	Ti/Au/HfO_2/InSb nanowire/SiO_2/Si substrate	– Due to low bandgap of InSb, I_{OFF} of the device is high – Ambipolar characteristics – QD devices have been characterized at T = 4.2 K – A region of Coulomb blockade oscillation is found above the theshold voltage of 0 V
[45]	GaAs/InAs QD/GaAs/GaP/GaAs substrate	– Substrate orientation on QD enhanced solar cell investigated
[46]	Pt/Al_2O_3/7 nm InGaSb/AlGaSb/GaAs substrate	– Electron/hole mobility >4000/900 cm^2/Vs achieved in this single channel material – Challenge identified: contact resistance – Improved with TiO_2 at interfacial layer
[47]	n-GaAs/n-$Al_{0.4}Ga_{0.6}As$ cladding layer/InAs-GaAs QD layers/p-$Al_{0.4}Ga_{0.6}As$ cladding layer/p+-GaAs bonding layer/p+-Si substrate	– Promising for use in high-density photonic integrated circuits for their low lasing threshold current density and high temperature stability
[48]	Bottom Gate FET : InAs, InP and InSb QDs realized Al Source and drain contacts/III–V QD/gate dielectric/SiO_2/Si gate	– QD films used in FETs surpass the mobilities for low current applications such as photodetectors or photovoltaic cells
[49]	Sample A: 30 nm GaAs/50 nm n-GaAs/300 nm GaAs/350 µm S-I GaAs substrate Sample B: 30 nm GaAs/2.4 nm monolayers InAs QDs/50 nm n-GaAs/300 nm GaAs/350 µm S-I GaAs substrate	– The transistor with InAs QD layer revealed higher responsivity values corresponding to GaAs – High speed operation for long wavelength detection at room temperature for photodetector application

orientation enhanced the investigation with the solar cell application. Tanabe et al. [46] worked with a 7 nm ultrathin InGaSb channel device. The configuration of the device from the top to bottom includes Pt/Al_2O_3/InGaSb/AlGaSb/GaAs substrate. Electron/hole mobility of >4000/900 cm^2/Vs was achieved in this single channel material. He identified a challenge with the contact resistance which was improved with an interfacial TiO_2 layer [46]. Then, he worked with n-GaAs/n-$Al_{0.4}Ga_{0.6}As$ cladding layer/InAs-GaAs QD layers/p-$Al_{0.4}Ga_{0.6}As$ cladding layer/p+-GaAs bonding layer/p+-Si substrate. It is promising for use in high-density photonic ICs for their low lasing threshold current density and high-temperature stability [47]. Hetsch et al. [48] suggested in his article that QD Films used in FETs surpass the mobilities for low current applications such as photodetectors or photovoltaic cells. He worked with bottom-gated FET. InAs, InP, and InSb QDs were realized in the place of channel. The device configuration consists of Al S-D contacts sandwiched with the III–V QD/gate dielectric/SiO_2/Si gate [48]. Later in 2015, Chen et al. [49] worked with two different configurations. One configuration was 30 nm GaAs/50 nm n-GaAs/300 nm GaAs/350 μm S-I GaAs substrate, and the other configuration was 30 nm GaAs/2.4 nm monolayers InAs QDs/50 nm n-GaAs/300 nm GaAs/350 μm S-I GaAs substrate. It was found out that the transistor with InAs QD layer revealed higher responsivity values corresponding to GaAs. High-speed operation for long wavelength detection at room temperature is used for photodetector application [49].

4 Summary and future scope

In summary, we have highlighted that III–V semiconductor nanostructures and quantum structures such as nanocrystals (QD), nanorods, nanotubes, and nanospheres will replace the present Si, strained Si, and conventional III–V semiconductor channels. The proposed structure of the III–V QD (replaced with nanorods,

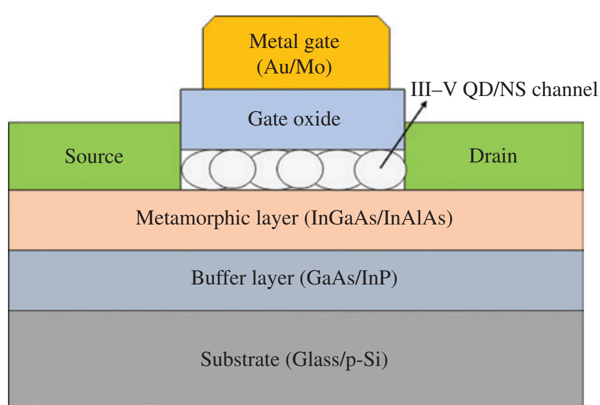

Figure 7: Proposed schematic of III–V QD or nanostructured (NS) channel based MOSFET.

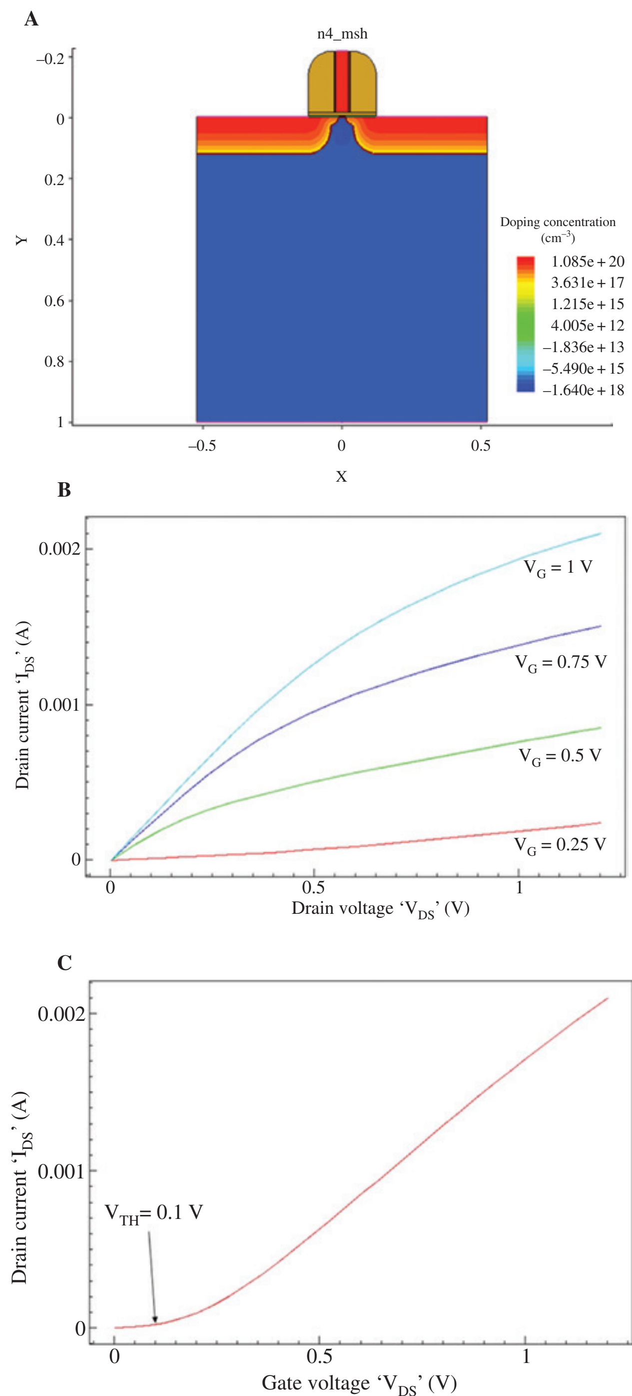

Figure 8: (A) III–V GaN nanostructure (10 nm thickness) channel/Al_2O_3 as gate dielectric oxide-based transistor (TCAD simulation). (B) Drain characteristics of the proposed device – III–V GaN/Al_2O_3 FET. (C) Output/transfer characteristics of the proposed device – III–V GaN/Al_2O_3 FET (threshold voltage = 0.1 V).

nanotubes, nanospheres, nanocore-shell dendrimers, or any nanostructures) semiconductor channel MOSFET is shown in Figure 7.

Starting with the substrate, a buffer layer is deposited using physical vapor deposition method. Then a metamorphic layer is deposited above the deposited buffer layer. A buffer or metamorphic layer is optional. A thin III–V QD semiconductor layer as channel of the device is deposited using any advanced technologies of physical deposition methods. A region for source and drain terminal is saved. Gate oxide Al_2O_3 or ZrO_2 is then deposited above the QD layer using sophisticated PLD method. A metal gate material is sputtered above to form the gate terminal. The fabricated device will then be characterized for further studies.

A nanostructure III–V GaN channel and Al_2O_3 based MOSFET is proposed here as shown in Figure 8A. This device consists of Si substrate, III–V GaN channel, and a gate dielectric Al_2O_3. The simulation through technology computer aided design was performed, and the current voltage drain characteristics are shown in Figure 8B and the transfer characteristics are shown in Figure 8C.

From the simulated device, it is estimated that the threshold voltage of the device is 0.1 V, which is very low compared to conventional channel devices. This is expected to be lesser in the quantum structured or nanostructured channel devices as referred with various literature reports. Hence, as a future scope, the III–V semiconductor channel will be a better replacement for the high-mobility, low power consuming, and faster switching applications.

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Bionotes

Cyril R.A. John Chelliah
Nanoelectronics Laboratory, Centre for Research in Nanotechnology, Department of Nanoscience and Technology, Karunya University, Coimbatore 641114, India
cyrilrobinson@karunya.edu.in

Cyril Robinson Azariah John Chelliah is a research student in the Department of Nanoscience and Technology, Karunya University, Coimbatore, India. His research interest includes CMOS VLSI design, thin film devices and nanoelectronics.

Rajesh Swaminathan
Nanoelectronics Laboratory, Centre for Research in Nanotechnology, Department of Nanoscience and Technology, Karunya University, Coimbatore 641114, India
drsrajesh@karunya.edu

Rajesh Swaminathan is a professor and program coordinator in the Department of Nanoscience and Technology, Karunya University, Coimbatore, India. His research interest includes solar cell, thin film physics and nanoelectronics devices.