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CUTWIDTH OF THE DE BRUIJN GRAPH (*)

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Abstract. – *We prove optimal upper bound on the cutwidth of the general de Bruijn graph. Our upper bound is essentially based on a new relation between the cutwidth and the area of the VLSI layout of a graph. The relation is interesting itself as it generalizes the known relation between the area and the bisection width of graphs of bounded degrees and holds for arbitrary graphs.*

Résumé. – *Nous donnons une majoration optimale de la largeur de coupe du graphe de De Bruijn. Notre majoration est essentiellement basée sur une nouvelle relation entre la largeur de coupe d'un graphe et la surface nécessaire à son implantation V.L.S.I. Cette relation est intéressante en elle-même car elle généralise à des graphes de degré quelconque une relation déjà connue entre la surface nécessaire et la bissection-arête des graphes ayant un degré borné.*

1. INTRODUCTION

The cutwidth is a fundamental parameter of graphs which plays an important role in the VLSI design [7]. Informally, the cutwidth problem is to find a linear layout of vertices of a graph so that the maximum number of cuts of a line separating consecutive vertices with edges is minimized. The problem is *NP*-complete in general but solvable in polynomial time for trees [11]. Very little is known on the exact or even approximate values of cutwidths of specific graphs, *see e.g.* [2, 6, 8]. Barth *et al.* [1] proved that cutwidths of the *n*-dimensional shuffle-exchange and the binary de Bruijn graphs are of order $\Theta(2^n/n)$.

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The aim of this note is to extend their result for general de Bruijn graphs. More precisely, we show that the cutwidth of the k -ary n -dimensional de Bruijn graph is $\Theta(k^{n+1}/n)$. Our upper bound is essentially based on a new relation between the cutwidth and the area of the VLSI layout of a graph. The relation is interesting itself as it generalizes the known relation between the area and the bisection width of graphs of bounded degrees and holds for arbitrary graphs.

The cutwidth is a special case of the congestion. From reasons which will be clear later, we define the cutwidth through the congestion.

Let $G_1 = (V_1, E_1)$ and $G_2 = (V_2, E_2)$ be graphs such that $|V_1| \leq |V_2|$. An embedding of G_1 in G_2 is a couple of mappings (ϕ, ψ) satisfying

$$\phi : V_1 \rightarrow V_2 \text{ is an injection, } \psi : E_1 \rightarrow \{\text{set of all paths in } G_2\},$$

such that if $uv \in E_1$ then $\psi(uv)$ is a path between $\phi(u)$ and $\phi(v)$. Define the congestion of an edge $e \in E_2$ under ϕ, ψ as

$$cg_e(G_1, G_2, \phi, \psi) = |\{f \in E_1 : e \in \psi(f)\}|$$

and the congestion of G_1 in G_2 as

$$cg(G_1, G_2) = \min_{(\phi, \psi)} \max_{e \in E_2} \{cg_e(G_1, G_2, \phi, \psi)\}.$$

Let P_n be an n -vertex path. Define the cutwidth of $G = (V, E)$, $|V| = n$ as

$$cw(G) = cg(G, P_n).$$

We will use also an equivalent definition of the cutwidth. Let $\phi : V \rightarrow \{1, 2, \dots, n\}$ be a 1-1 labeling of vertices of G . Define

$$cw(G, \phi) = \max_i \{|\{uv \in E : \phi(u) \leq i < \phi(v)\}|\}.$$

Then

$$cw(G) = \min_{\phi} \{cw(G, \phi)\}.$$

A related concept is the bisection width of the graph G , denoted by $bw(G)$, and defined as

$$bw(G) = \min_{\phi} \{ |\{ uv \in E : \phi(u) \leq \left\lfloor \frac{n}{2} \right\rfloor < \phi(v) \}| \}.$$

The k -ary n -dimensional de Bruijn digraph $B(k, n)$ consists of k^n vertices. Each vertex corresponds to a string $u_{n-1} u_{n-2} \dots u_1 u_0$ over the alphabet $\{0, 1, 2, \dots, k-1\}$. There is a directed edge from a vertex u to a vertex v iff v can be obtained from u by a left shift followed by inserting a letter on the freed place. As the orientation of edges does not influence the cutwidth, from now on we consider the de Bruijn graph obtained from the de Bruijn digraph by omitting orientations. Note that the resulting graph has loops and multiply edges.

Let $deg(v)$ denote the degree of a vertex v in G and $\Delta(G) = \max_v \{ deg(v) \}$.

We use the standard model for laying out VLSI circuits [9, 10]. The circuit is viewed as a graph G in which vertices correspond to processing elements and edges to wires. The graph is then embedded in a two-dimensional grid with unit spacing between horizontal and vertical tracks subject to the following assumptions:

(i) Vertices of degree less than or equal to 4 are mapped in the nodes of the mesh. Vertices of degrees $deg(v) > 4$ are embedded in a square of side d tracks in the mesh. Let us assume the square sides coincide with some tracks in the mesh. Vertices can not overlap each other.

(ii) Edges are routed along grid lines with the restriction that no two edges overlap except possibly when crossing perpendicular to each other or when bending. Also, an edge can not be routed over a node it does not connect. The area of two dimensional layout of G is defined as the product of the number of vertical tracks and the number of horizontal tracks that contain a node or a wire segment of the graph. The area of G is denoted by $A(G)$.

2. UPPER BOUND

Our upper bound is based on a new relation between the area of the VLSI layout of a graph and the cutwidth of the graph. Thompson [9] proved that if $\Delta(G) \leq 4$ then

$$A(G) = \Omega(bw^2(G)).$$

The same result for arbitrary graphs without a proof is mentioned in [4]. Another extension of the Thompson's result for bounded degree graphs is in [3]. We extend the Thompson's result to the following:

LEMMA 2.1: *For an arbitrary graph G*

$$A(G) = \Omega(cw^2(G))$$

Proof: First we give a short proof for the case $\Delta(G) \leq 4$. Consider the layout with the minimal area $A(G)$. Let w and h be the number of the used vertical and horizontal tracks, respectively. Wlog assume $w \geq h$. Then

$$A(G) = wh \geq h^2. \quad (1)$$

We can view the layout as an embedding of the graph G into an $h \times m$ mesh M with unit congestion. Further, it is easy to embed the mesh M into the wh -vertex path P with a cutwidth $h + 1$. Now we use an observation that $cg(G_1, G_3) \leq cg(G_1, G_2) cg(G_2, G_3)$ with $G_1 = G$, $G_2 = M$, $G_3 = P$. We get $cw(G) \leq cg(G, P) \leq h + 1$. Combining this with (1) we prove the claim.

Now consider an arbitrary graph G on n vertices laid out in the mesh. From now on we will not distinguish between vertices and edges of G and their images in the mesh. Introduce the coordinate system with the origin in the intersection of the left most vertical and the bottom most horizontal used tracks and axes parallel to tracks. For each vertex v of $deg(v) > 4$, omit the upper, lower and right side of the corresponding square of side $deg(v)$. It is easy to connect the edges attached to the removed sides with the left side so that the congestion remains 1. In this way we obtain a new layout, in which each vertex of degree $deg(v) > 4$ is mapped to a vertical straight line segment of length $deg(v) - 1$.

If $deg(v) > 4$ then define the y -coordinate of v as the y -coordinate of the lower end of the segment corresponding to v . Sort vertices of G lexicographically according to their coordinates (x, y) . Label the vertices of G by $1, 2, \dots, n$ according to the lexicographic order. Let ϕ denote this labeling. Then

$$cw(G) \leq \max_i \{ |\{ uv \in E : \phi(u) \leq i < \phi(v) \}| \}. \quad (2)$$

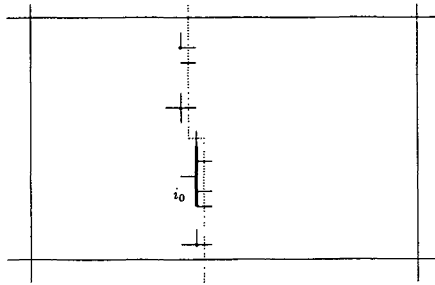


Figure 1. - Separating first i_0 vertices.

Let the maximum be attained at some $i = i_0$, *i.e.*

$$\begin{aligned} \max_i \{ |\{ uv \in E : \phi(u) \leq i < \phi(v) \}| \} \\ = |\{ uv \in E : \phi(u) \leq i_0 < \phi(v) \}|. \end{aligned} \tag{3}$$

It is easy to see that there exists a vertical line L , possibly with one jog of unit length, which divides the layout into two parts s.t. one of them contains exactly vertices with labels $1, 2, \dots, i_0$. See Figure 1 (line L is dotted).

Let $c(L)$ denote the number of edges of G crossed by L . By the definition of the cutwidth we have

$$c(L) = |\{ uv \in E : \phi(u) \leq i_0 \leq \phi(v) \}|. \tag{4}$$

Finally, we bound $c(L)$ from above in terms of h . The “zig-zag” line L crosses at most $h + 1$ edges of the mesh. Clearly, $c(L)$ equals the sum of congestions of the crossed mesh edges which can not be greater than $h + 1$, because the congestion of the crossed mesh edge is not greater than 1. Consider a set of vertices $\{v_1, v_2, \dots, v_k\}$ satisfying: they lie to the left from L , $deg(v_j) > 4$ and the distance of the vertex v_j from L is smaller than $deg(v_j) - 1$, for $j = 1, 2, \dots, k$. It holds that $\sum_{j=1}^k deg(v_j) \leq h$.

Otherwise some vertices would overlap in the original layout - contradiction to the assumption (i) of the model. Hence

$$c(L) \leq 2h + 1. \tag{5}$$

Combining (1)-(5) we get the claimed result. \square

THEOREM 2.1: *The cutwidth of the k -ary n -dimensional de Bruijn graph satisfies*

$$cw(B(k, n)) = \Theta\left(\frac{k^{n+1}}{n}\right).$$

Proof: Kleitman *et al.* [5] constructed a layout of the shuffle-exchange graph with area $O(2^{2n}/n^2)$. Brebner [4] used the Kleitman's *et al.* construction to lay out $B(k, n)$ in area $O(k^{2n+2}/n^2)$. Note that Brebner uses slightly different model of VLSI layout, namely a vertex of degree d is mapped into a square of side $d/4$ in the mesh. Scaling his layout by the factor 4 in both dimension we get a layout compatible with our model. These upper bounds together with Lemma 2.1 imply the upper bound on cutwidth. Brebner showed a lower bound for the bisection width of $B(k, n)$ of order $\Omega(k^{n+1}/n)$ which is also a lower bound for the cutwidth. \square

REFERENCES

1. D. BARTH, F. PELLEGRINI, A. RASPAUD, and J. ROMAN, On bandwidth, cutwidth and quotient graphs, *RAIRO Informatique, Théorique et Applications*, to appear.
2. A. BEL HALA, Congestion optimale du plongement de l'hypercube $H(n)$ dans la chaîne $P(2^n)$, *RAIRO Informatique, Théorique et Applications*, 1993, 27, pp. 1-17.
3. G. BILARDI and F. PREPARATA, Area-time lower bound techniques with application to sorting, *Algorithmica*, 1986, 1, pp. 65-91.
4. G. BREBNER, Relating routing graphs and two-dimensional grids, in: Proc. *VLSI: Algorithms and Architectures*, North Holland, 1985.
5. D. KLEITMAN, F. T. LEIGHTON, M. LEPLEY and G. L. MILLER, New layouts for the shuffle-exchange graph, in: Proc. *13th Annual ACM Symposium on Theory of Computing*, ACM Press, 1981, pp. 278-292.
6. T. LENGAUER, Upper and lower bounds for the min-cut linear arrangements problem on trees, *SIAM J. Algebraic and Discrete Methods*, 1982, 3, pp. 99-113.
7. A. D. LOPEZ and H. F. S. LAW, A dense gate matrix layout method for MOS VLSI, *IEEE Trans. Electron. Devices*, 1980, 27, pp. 1671-1675.
8. K. NAKANO, Linear layout of generalized hypercubes, in: Proc. 19th Intl. Workshop on Graph-Theoretic Concepts in Computer Science, *Lecture Notes in Computer Science 790*, Springer Verlag, Berlin, 1994, pp. 364-375.
9. C. D. THOMPSON, Area-time complexity for VLSI, in: Proc. *11th Annual ACM Symposium on Theory of Computing*, 1979, pp. 81-88.
10. J. D. ULLMAN, *Computational Aspects of VLSI*, Computer Science Press, Rockville, 1984.
11. M. YANNAKAKIS, A polynomial algorithm for the Min Cut Linear Arrangement of trees, *J. ACM*, 1985, 32, pp. 950-988.