Cycling Endurance of NOR Flash EEPROM Cells Under CHISEL Programming Operation—Impact of Technological Parameters and Scaling

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***Abstract*—The impact of technological parameter (channel doping, source/drain junction depth) variation and channel length scaling on the reliability of NOR Flash EEPROM cells under channel initiated secondary electron (CHISEL) programming is studied. The best technology for CHISEL operation has been identified by using a number of performance metrics (cycling endurance of program/erase time, program/disturb margin) and scaling studies were done on this technology. It is explicitly shown that from a reliability perspective, bitcell optimization for CHISEL operation is quite different from that for channel hot electron (CHE) operation. Properly optimized bitcells show reliable CHISEL programming for floating gate length down to 0.2 μm.**

***Index Terms*—Band-to-band tunneling, channel hot electron (CHE), channel initiated secondary electron (CHISEL), device scaling, drain disturb, Flash EEPROMs, hot carriers.**

I. INTRODUCTION

CHANNEL INITIATED secondary electron (CHISEL) injection is an excellent programming mechanism for NOR Flash EEPROMs [1]–[5]. It relies on impact ionization feedback, is activated by the application of a negative substrate bias (V_B) and provides high-energy electrons that get injected into the floating-gate (FG) over a spatially broad area in the channel [1]–[9], as schematically shown in Fig. 1. Compared to channel hot electron (CHE) injection [10], CHISEL injection provides lower voltage and lower power operation for equivalent programming time (T_P) and faster T_P under equivalent programming power. CHISEL injection also offers self-convergent programming leading to excellent threshold voltage (V_T) control and a unique recovery procedure for over-erased cells [1]–[5], [9], [11], [12] not available under conventional CHE programming [13].

From the reliability perspective, CHISEL programming has shown good programmed and erased V_T endurance up to 10^5 program/erase (P/E) cycles [14], [15]. P/E cycling and data retention (after cycling) results obtained from large 32-Mbit arrays showed tight V_T control and over 10 years of charge retention [14]. It has been clearly demonstrated that CHISEL programming is free from anomalous bit failure through increased disturbs, window closure, or charge loss.

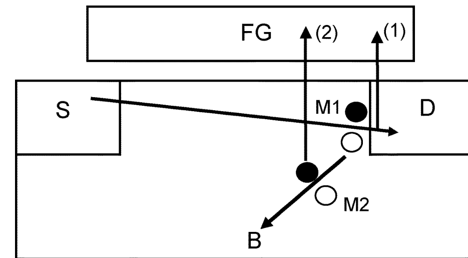

Fig. 1. CHISEL injection mechanism (schematic). Channel electrons, heated by lateral electric field create primary electron-hole pairs by impact ionization (M1). Primary holes flow to the substrate and in the presence of high transverse electric field (due to negative substrate bias) create secondary electron-hole pairs by impact ionization (M2). The secondary electrons move toward the interface and those having energy greater than 3.1 eV get injected into the FG.

From the cell scaling perspective, a few earlier reports indicated degradation in CHISEL programming efficiency for deeply scaled cells [16], [17]. However, it has been recently demonstrated, albeit on pre-cycled cells, that it is possible to maintain excellent CHISEL programming efficiency for cells having FG length (L_{FG}) down to 0.2 μm with proper adjustment of technological parameters [18]. However, to the best of our knowledge, the impact of technological parameters and cell scaling on cycling endurance has not been reported so far for CHISEL programming operation.

This scope of paper is two fold. First, the best cell design for reliable CHISEL operation is identified from a number of technology parameter options (variation in channel doping and junction depth and option of halo doping). Cycling induced degradation in T_P, erase time (T_E), P/E V_T (V_{TP} and V_{TE}) and program/disturb (P/D) margin were used as metrics for cell selection. It is shown that halo doping is not a good option since those cells suffer from severe degradation of T_E and P/D margin after cycling. On the other hand, nonhalo cells with shallow junction depth suffer from degradation in P/D margin. The best tradeoff between T_P and P/D margin was obtained for nonhalo cells with higher channel doping but somewhat deeper junction. It is also explicitly shown that the best cell design for reliable CHISEL operation is quite different from that under CHE operation. Second, the impact of L_{FG} scaling on the cycling endurance of the above reliability metrics was studied for the optimized cell. For the present choice of technological parameters, reliable CHISEL programming operation is achieved for cells having L_{FG} down to 0.2 μm.

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TABLE I
DEVICES USED IN THIS STUDY. V_T (V_{CG} FOR $I_D/V_D = 5\ \mu A/0.8$ V) AND V_{BD} (V_D FOR $I_D = 1\ \mu A$, $V_{CG} = 0$) MEASURED ON IDENTICAL FG-CG SHORTED FETS

Device	Channel Implant	Junction Depth	Halo	Natural V_T (V)	Junction V_{BD} (V)
LL	Low	Low	No	2.11	7.2
HH	High	High	No	2.21	7.3
HL	High	Low	No	2.37	7.0
Halo	Very low	Very high	Yes	2.43	6.6

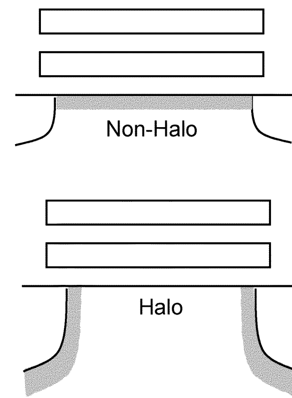

Fig. 2. Schematic representation of the two type of Flash cells used in the study. Nonhalo cells have moderate to high channel doping, shallower S/D junction and no halo implant. Halo cells have lower channel doping, deeper S/D junction and heavy halo implant.

II. EXPERIMENTAL

The devices used in this work were fabricated using a state-of-the-art 0.18-μm triple well process featuring advanced modules such as shallow trench isolation and self-aligned source/drain (S/D) contacts leading to cell area of about 0.45 μm^2. Measurements were performed on isolated, fully scaled bitcells having finished L_{FG} of 0.32 through 0.2 μm, width (W) of 0.3-μm, tunnel oxide (T_{OX}), and oxide–nitride–oxide interpoly dielectric thickness of 12 and 20 nm, respectively, and gate coupling of about 0.55. Four different types of cells (LL, HH, HL, and Halo) were fabricated to study the impact of changes in technological parameters on CHISEL program and disturb performance, before and after P/E cycling. Their doping schemes, junction depth, natural V_T, and junction breakdown voltage (V_{BD}) are mentioned in Table I.

This paper focuses on CHISEL programming, which was performed using $V_B = -2$ V (source grounded). For comparison, CHE programming was performed for select cases using $V_B = 0$ V. The cells were erased using uniform channel erase with source, drain and substrate grounded. V_T was defined as the control gate bias (V_{CG}) required to obtain 5-μA drain current (I_D) at 0.8-V drain bias (V_D). Programmed and erased levels are defined as $V_{TP} = 5.4$ V and $V_{TE} = 1.9$ V, respectively. Drain disturb [19] measurements were performed at identical V_D and V_B as programming, but with zero V_{CG} to simulate an unselected *WL*. Drain disturb is studied for both the charge gain (erased cell) and charge loss (programmed cell) modes. Disturb time T_D is defined as time for a V_T change of 0.1 V during disturb transients. P/E cycling was done under fixed T_P and T_E as the initial cell.

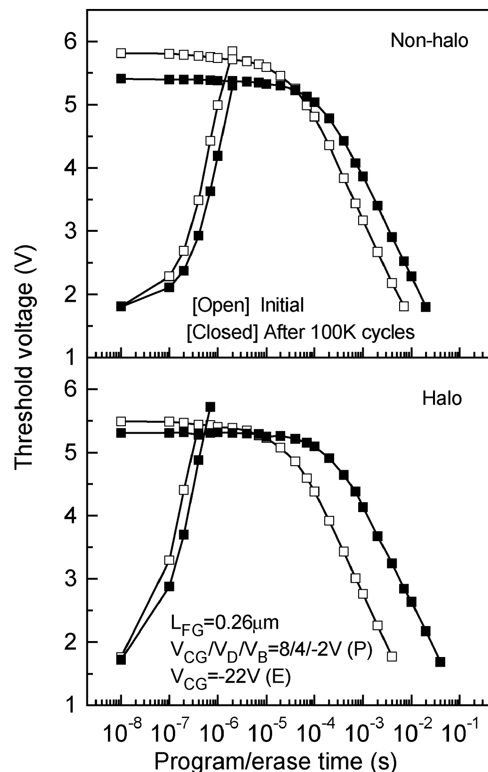

Fig. 3. P/E transients measured under equivalent bias on nonhalo (LL) and halo cells before and after 100 K P/E cycles.

III. RESULTS AND DISCUSSION

A. Comparison Between Halo and Nonhalo Cells

Fig. 2 shows the schematic representation of the halo and nonhalo cells used in the study. Nonhalo cells have lower channel doping, a shallower S/D junction and no halo implant. Halo cells have lower channel doping, a deeper S/D junction anda heavy halo implant. Fig. 3 shows CHISEL program and erase transients for halo and nonhalo (LL) $L_{FG} = 0.26$ μm cells before and after 100 K P/E cycles under identical bias. Initial T_P and T_E are slightly lower for the halo cell. It can be clearly seen that the degradation of programming transients (and T_P) after cycling is comparable (and negligible) for both technologies. Note that such negligible cycling induced degradation of programming transients is a standard feature of CHISEL programming operation [14], [15]. However, the halo device shows higher degradation in erase time compared to the nonhalo device.

Fig. 4 shows the P/E cycling induced degradation of programmed and erased V_T for halo and nonhalo (LL) $L_{FG} = 0.26$ μm cells under identical bias as in Fig. 3. Identical bias condition was chosen for comparison, as there exists different combination of V_{CG} and V_D to get the same T_P [18]. V_{TP} degradation is always insignificant for both the cells while the halo cell shows higher V_{TE} degradation, consistent with T_P and T_E degradation shown in Fig. 3. It is well known that the electron

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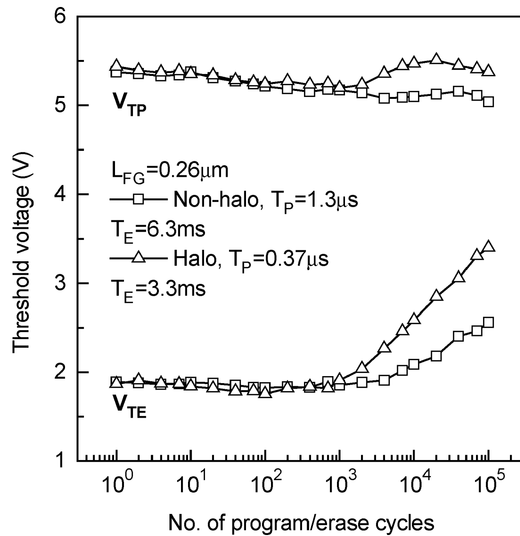

Fig. 4. Cycling endurance of program and erase V_T measured under equivalent bias (as in Fig. 3) on nonhalo (LL) and halo cells.

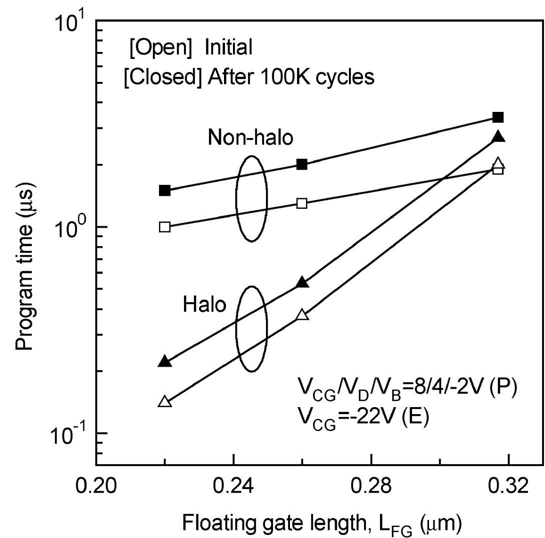

Fig. 5. Program time (T_P) as a function of FG length $(L_{\rm FG})$ measured under equivalent bias on nonhalo (LL) and halo cells before and after 100 K P/E cycles.

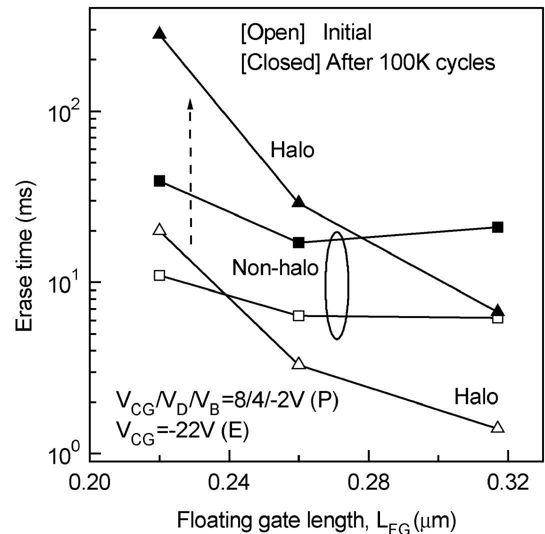

Fig. 6. Erase time (T_E) as a function of FG length $(L_{\rm FG})$ measured under equivalent bias on nonhalo (LL) and halo cells before and after 100 K P/E cycles.

energy distribution (EED) high-energy tail under CHISEL operation is always populated due to secondary impact ionization [1]–[9]. Hence, electrons that constitute the gate current (I_G) during programming can easily overcome the increased injection barrier caused by cycling induced negative bulk and interfacial charges and results in negligible T_P degradation [14], [15]. It is also well known that CHISEL injection takes place over a broader area (toward the channel) and the resultant broader area of defect generation affects electron-ejection during erase and degrades T_E (compared to CHE operation) [15]. Higher T_E degradation for halo cells indicates higher (or wider) defect generation in the channel for such cells during cycling under CHISEL programming operation.

Figs. 5 and 6, respectively, show program and erase time before and after 100 K P/E cycles as a function of FG length for halo and nonhalo (LL) cells. Program and erase were done at fixed biases for all $L_{\rm FG}$ values. The halo cells shows much better T_P scaling and comparable T_P degradation after cycling compared to the nonhalo cells. The faster programming clearly indicates higher hot electron generation for halo cells under identical bias (expected because of higher doping around the junction). The halo cells also show better initial T_E. However, they suffer from severe T_E degradation after cycling (specially at smaller $L_{\rm FG}$) compared to the nonhalo cells. This is expected since a wider defect generation area is likely to degrade a significant part of the channel for smaller $L_{\rm FG}$ halo cells and therefore cause higher degradation in T_E after cycling.

Fig. 7 shows the drain disturb time before and after 100 K P/E cycles as a function of FG length for halo and nonhalo (LL) cells, under both charge gain and loss disturb modes. It has been previously identified that unlike CHE operation, CHISEL operation shows both charge gain and loss disturb that originates from band-to-band tunneling (BTBT) [19]. BTBT generated electrons (holes) get heated by the junction field and get attracted toward the FG by positive FG charge in erased state (by negative FG charge during erase state) and cause charge gain (charge loss) disturb. Note that increased disturb implies lower T_D and vice-versa. It can be clearly seen that charge gain disturb increases but charge loss disturb decreases after P/E cycling. Such opposite cycling induced degradation of charge gain and loss disturb under CHISEL operation has already been observed and explained [20], [21]. The cycling induced degradation in T_D is higher for halo cells compared to the nonhalo cells, which is consistent with higher defect generation for the former device. The drastic increase in charge gain disturb after cycling specially at smaller $L_{\rm FG}$ for halo cells (resulting in a P/D margin of $\sim 10^4$ at $L_{\rm FG} = 0.21\ \mu$m) is a very severe concern.

The above results show that halo cells, despite showing quite promising T_P scaling, fare badly after cycling due to severe degradation in T_E and P/D margin. This forces us to abort the halo cells and find out the best among the nonhalo technologies, which is done in the next section.

B. Optimization of Nonhalo Cells

All the nonhalo technologies (LL, HH and HL, L = low, H = high, the letters correspond to channel doping and junction

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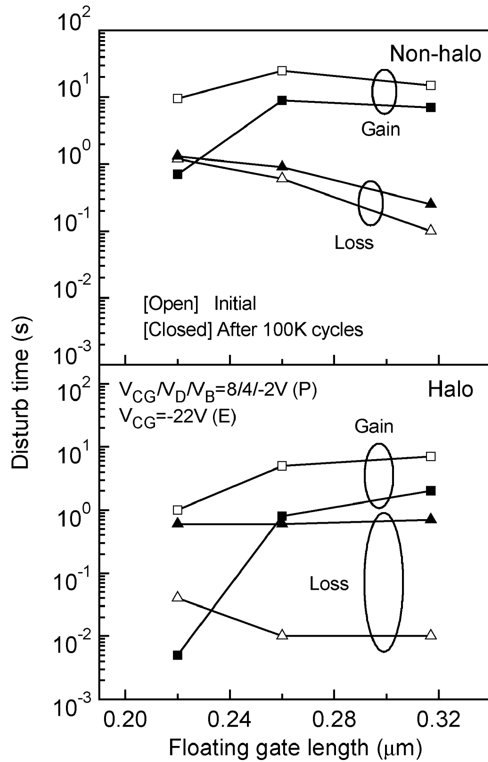

Fig. 7. Disturb time (T_D) as a function of FG length (L_{FG}) measured under equivalent bias on nonhalo (LL) and halo cells before and after 100 K P/E cycles.

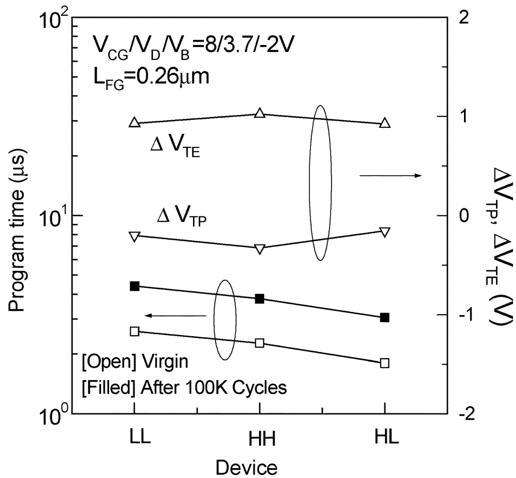

Fig. 8. Impact of technology parameters on cycling endurance of program time and programmed and erased V_T for nonhalo cells under CHISEL operation.

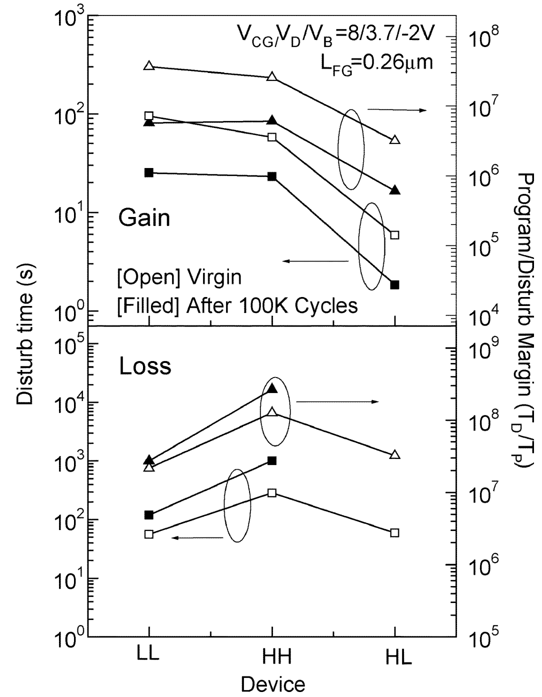

Fig. 9. Impact of technology parameters on the cycling endurance of disturb time and program/disturb margin for nonhalo cells under CHISEL operation.

depth, respectively) were compared under identical program and erase biases.

Fig. 8 shows the programming time before and after 100 K P/E cycles and corresponding degradation in programmed and erased V_T ($\Delta V_{\rm TP}$ and $\Delta V_{\rm TE}$) for different nonhalo technologies under CHISEL operation. Note that initial T_P reduces from LL to HL cells because of increasing transverse field under identical programming bias [18]. However, the cycling induced degradation in T_P, $V_{\rm TP}$ and $V_{\rm TE}$ (and T_E, not shown) are insensitive to changes in technological parameters. Similar T_P and $V_{\rm TP}$ degradation does not necessarily suggest identical cycling induced degradation across different technologies. This is because the high-energy secondary electrons can easily overcome any moderate differences in injection barrier (caused by moderate differences in cycling induced degradation) across different technologies. However, similar $V_{\rm TE}$ degradation (note that erase is by Fowler–Nordheim electron ejection) suggests similar cycling induced degradation during CHISEL operation across various technologies.

Fig. 9 shows the disturb time and P/D margin before and after 100 K P/E cycles for different nonhalo technologies under CHISEL operation. The device HL did not show detectable charge loss after P/E cycling within the measurement timescale. Charge loss disturb is always less compared to the charge gain disturb for all technologies. Furthermore, charge gain disturb increases while charge loss disturb decreases after P/E cycling. The P/D margin is therefore an important concern only for the charge gain mode. It can be seen from the figure that both LL and HH cells show comparable P/D margin while that for HL cells are lower both before and after 100 K cycles. Since CHISEL drain disturb originates from BTBT, HL cells with highest transverse field results in lowest T_D (which also showed fastest T_P during programming). However, T_D degradation is similar after P/E cycling for all technologies. This is expected since cycling induced degradation has been found to be similar across different technologies.

By comparing the degradation in T_P and P/D margin after cycling under CHISEL operation, the best technology is identified to be HH. This technology is chosen for studying CHISEL $L_{\rm FG}$ scaling in the next section.

Note that CHISEL mechanism is substantially different from the conventional CHE process. It is therefore expected that the best-optimized technology for CHISEL operation need not be the same for CHE operation and vice-versa. Fig. 10 shows the

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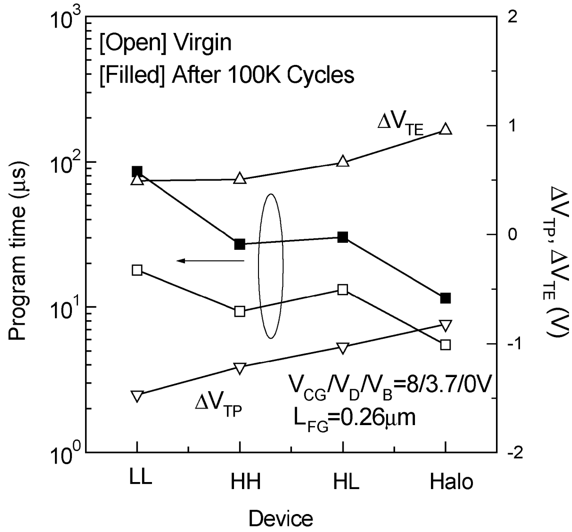

Fig. 10. Impact of technology parameters on cycling endurance of program time and programmed and erased V_T for nonhalo cells under CHE operation ($V_B = 0$ V).

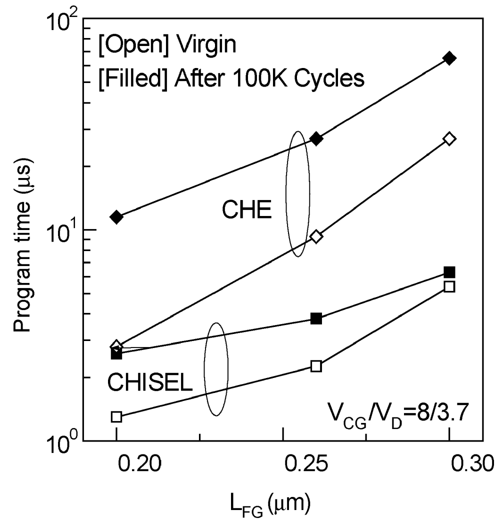

Fig. 12. Impact of L_{FG} scaling on the cycling endurance of program time for nonhalo HH cells under CHISEL and CHE operation.

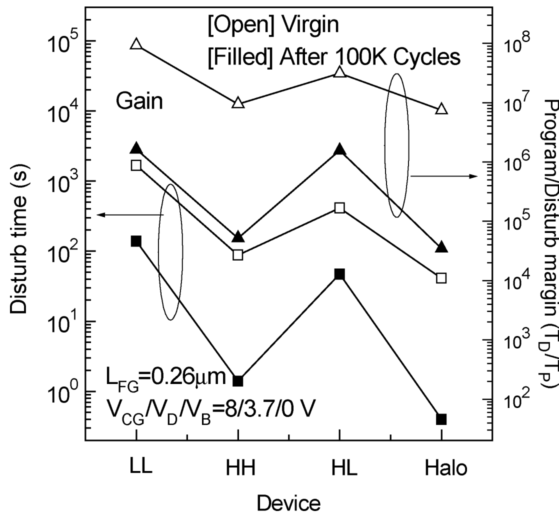

Fig. 11. Impact of technology parameters on the cycling endurance of disturb time and program/disturb margin for nonhalo cells under CHE operation.

programming time before and after 100 K P/E cycles and corresponding degradation in programmed and erased V_T for all nonhalo and halo technologies under CHE operation. The programming was done at identical V_{CG} and V_D. It is important to note that unlike CHISEL operation there is a wide variation in degradation across different technologies under CHE operation. Halo cells show fastest initial T_P and lowest T_P and V_{TP} degradation but highest V_{TE} degradation after cycling. On the other extreme, nonhalo LL cells show worst initial T_P and highest T_P and V_{TP} degradation but lowest V_{TE} degradation after cycling. The degradation of HH and HL cells fall between these two extremes.

Fig. 11 shows the impact of technology parameters on charge gain drain disturb and P/D margin before and after 100 K P/E cycles under CHE operation. Note that CHE shows charge loss disturb at much higher V_D values than used in this work [19]. Contrary to CHISEL operation, cells with lower junction depth show lower initial and degraded T_D and correspondingly higher P/D margin. Unlike CHISEL operation, the HL technology fares best (among the available choices explored in the present work) in terms of T_P and P/D margin degradation under CHE operation. This clearly shows that the Flash memory cell optimization should be treated differently for CHE and CHISEL operation.

C. Effect of Scaling

In the previous section, it has been identified that HH nonhalo technology shows the most reliable CHISEL operation. In this section the scaling performance of this technology is explored. The program and erase biases were held fixed as L_{FG} is varied, which yields faster T_P at smaller L_{FG}. Comparison under identical T_P (by suitably adjusting V_{CG} and V_D) is beyond the scope of the present paper. Furthermore, studying the scalability of the best optimized CHE cell is also beyond the scope of the present paper.

Fig. 12 shows the programming time before and after P/E cycles as a function of FG length under CHISEL operation. For comparison, the cycling induced T_P degradation under CHE operation is also shown. Note that T_P degradation after 100 K cycles increases as L_{FG} is reduced. This is expected since at constant V_D smaller L_{FG} cells are expected to degrade by a large amount, despite lower T_P during cycling. However, the degradation under CHISEL operation is much smaller than that under CHE operation. It has been shown before [22] that CHISEL operation results in a highly populated EED high-energy tail even at shorter L_{FG}. These highly energetic CHISEL electrons can easily overcome the increased energy barrier caused by trapping of electrons during cycling. This is reflected in lower degradation of T_P as shown.

Fig. 13 shows charge gain and loss drain disturb and corresponding P/D margin as a function of FG length before/after P/E cycling under CHISEL operation. Charge loss disturb decreases at smaller L_{FG} (increase in drain coupling makes FG voltage less negative and reduces BTBT). As mentioned before, charge loss disturb also decreases after cycling. The corresponding P/D margin is improved and therefore is not an issue during CHISEL cell scaling. Charge gain disturb is less sensitive to L_{FG} before cycling under CHISEL operation [19]. However, it increases and hence P/D margin reduces after cycling as L_{FG} is scaled.

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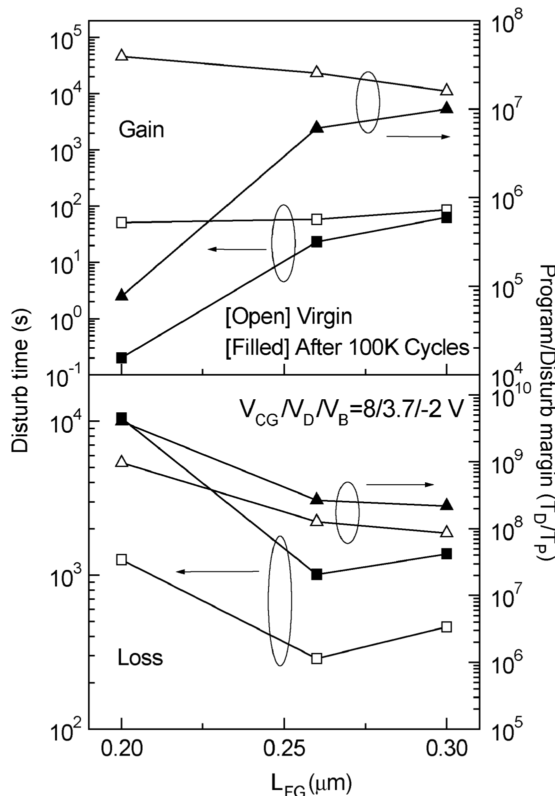

Fig. 13. Impact of L_{FG} scaling on the cycling endurance of disturb time and program/disturb margin for nonhalo HH cells under CHISEL operation.

This is due to higher cycling induced degradation (since V_D is kept constant) at lower L_{FG}. Therefore charge gain disturb poses some concern for L_{FG} scaling during CHISEL operation.

For the present HH technology optimized for $L_{\mathrm{FG}} = 0.26\ \mu$m, a $L_{\mathrm{FG}} = 0.2\ \mu$m cell shows $T_P = 2.6\ \mu$s and P/D margin greater than 5×10^4 after 100 K P/E cycles under CHISEL operation at $V_D = 3.7$ V.

IV. CONCLUSION

To summarize, we have studied the impact of variation in technological parameters (channel doping, S/D junction depth) and channel length scaling on the reliability of NOR Flash EEPROM cells under CHISEL programming operation. Cycling induced degradation of P/E time and program/disturb margin were used as performance metric. It has been shown that halo doped cells, despite showing excellent initial performance are not reliable after cycling. Nonhalo cells with high channel doping and somewhat high S/D junction depth has been found to be most suitable for reliable CHISEL operation. It has been also shown that bitcell optimization for reliable CHISEL operation is quite different from that for CHE operation. Under present condition, the best-optimized nonhalo cells show reliable CHISEL programming for FG length down to 0.2 μm. These results prove that CHISEL programming can be reliably used in deeply scaled NOR Flash EEPROM cells.

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