CYCLONE: Automated Design and Layout of RF LC-Oscillators

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Abstract

This paper presents an automated, layout-aware RF LC-oscillator design tool, called CYCLONE that delivers an accurate and optimal LC-oscillator design, from specification to layout. The tool combines the accuracy of device-level simulation and finite element analysis with the optimisation power of simulated annealing algorithms and is verified with experimental results.

1. Introduction

A major challenge in the design of future single-chip RF transceivers is the integration of the Voltage Controlled Oscillator (VCO) that generates the Local Oscillator (LO) carrier signal. The most important specifications of a VCO are low phase noise, low power and high frequency operation. Passive LC-oscillators tend to be the best choice for integration of high-performance VCOs on silicon substrates. The schematics of the most common RF LC-VCOs, the single differential topology (a) and the double differential topology (b), are given in Figure 1.

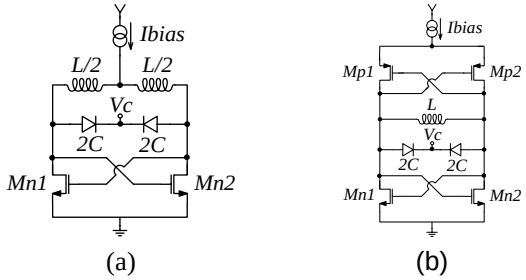

Figure 1: Common RF LC-VCO topologies

In the past years much knowledge has been gathered on RF oscillators [1,2,3]. However, no methodology exists that reuses the empirical IP built up by RF design engineers, to come to an automated design flow. Because the integrated inductor is the most critical part of a LC-oscillator, it is crucial to determine the inductor parasitic losses accurately. Since the best VCO performance is obtained using balanced octagonal coils [2], formula-based approaches [4,5] cannot be used to calculate an accurate parameter set for the used inductor. In particular, the inductor's series resistance cannot be predicted accurately enough by an analytical formula.

In this paper a specification driven layout-aware RF LC-oscillator design tool, called CYCLONE, is presented. It automatically performs finite element simulations and optimisation of RF coils, combined with VCO circuit sizing to yield an optimal and accurate RF LC-oscillator design. Finally, the layout is generated based on the circuit sizes taking into account all layout parasitics. Experimental results are given at the end of the paper.

2. Electro-magnetical (EM) tools

Both the phase noise performance and the power consumption of RF LC-VCOs are mainly determined by the quality of the integrated inductor. For full integration, planar spiral inductors are the best solution. The quality factor of this type of inductors is limited by several parasitic effects, of which the metal resistance and substrate losses are the most important. While the DC series resistance of the metal can be calculated in a straightforward manner, this is not the case for the extra resistances due to substrate spread resistance and eddy currents.

The major drawback of analytical approaches, as [5,6], is that the expression for the inductor's series resistance is only a first order approximation. The influence of eddy currents in the metal lines and in the substrate [2] are not taken into account. These effects become very important at frequencies higher than 1 GHz, especially on conductive CMOS substrates [7]. Therefore, good phase noise predictions are hard to make based on this analytical model and a full electromagnetic simulation is needed to accurately predict all parasitic effects.

In CYCLONE, two electromagnetic (EM) simulator tools are used. For technologies with low substrate resistance (< 5 Ωcm), the finite-element simulator Magnet© [8] is used. To speed up the simulation, the axi-symmetric properties of circular coils are exploited. Only a two-dimensional simulation of a cross-section has to be made to obtain full three-dimensional information [2]. For high resistive substrates (≥ 5 Ωcm), the simulator FastHenry [9] is implemented. FastHenry is a three-dimensional inductance extraction program that computes the frequency-dependent self and mutual inductance and resistance between conductors. FastHenry is optimised for the simulation of planar conductors on planar ground planes, taking into account the effective inductor geometry, including the connecting leads.

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3. Systematic Design Methodology

The performance driven top-down design methodology has been accepted as the de facto standard for systematically designing analogue building blocks in academia [10]. This methodology defines two phases in the design. During the top-down phase the blocks are sized. After the completion of this sizing task, the layouts of all basic blocks are generated and assembled bottom-up. Intermediate verification steps guarantee a successful design process.

In the area of RF design, only parts of synthesis systems have been reported up till now. In [11] RF front-ends have been analysed and optimally designed at the system level. In [12], the sizing of LC oscillators has been implemented using Geometric Programming (GP), but the method uses simple analytical formulas and no link is provided with layout. In this paper, the link to layout is fully implemented and accurate EM simulations are used.

The automated design flow implemented in the CYCLONE tool is shown in figure 2. The flow is user-interactive and consists of:

1. Technology Selection: a *Custom Technology File* is loaded. Physical and electrical properties of the used technology, e.g. metal, substrate and oxide thickness, polysilicon sheet resistance, etc. are defined in this file.
2. Topology selection. Figure 1 (a) or (b) can be selected. Other topologies can be implemented quite easily in the open framework when required by designers.
3. Specification input. Typical values are given in table 1.

Oscillation Frequency *(F_c)*	3.6 GHz
Power Supply	2 V
Phase Noise *@Fc + 600kHz*	< - 115 dBc *(DCS1800)*
Power usage	Minimal
Tuning range	25%

Table 1 Typical specifications for a VCO for RF-applications

4. Optimisation start-up. The EM-simulator is selected automatically by the tool, depending on the substrate resistance. A first-order model for current, G_M and capacitances of the gain cell, is derived from a single simulation per transistor type in the gain cell. The output buffer of the VCO is sized, so its exact parasitic capacitance can be added to the LC-tank. The Layout Tool generates the leaf cells for the gain and diode cells using the minimum distances from the *Technology Layout File* and user-defined settings in the *Design Configuration File*. The sizes of the leaf cells are passed to the Optimisation Startup.
5. The Optimisation Loop is then executed and returns a sized VCO-circuit, a sub-circuit of the segmented coil and a substrate sub-circuit.
6. In the last phase, the layout generator composes the different devices, starting from the previously generated leaf cells and the size information from the optimisation. It returns the skill-code or GDSII-files of the VCO core cells.

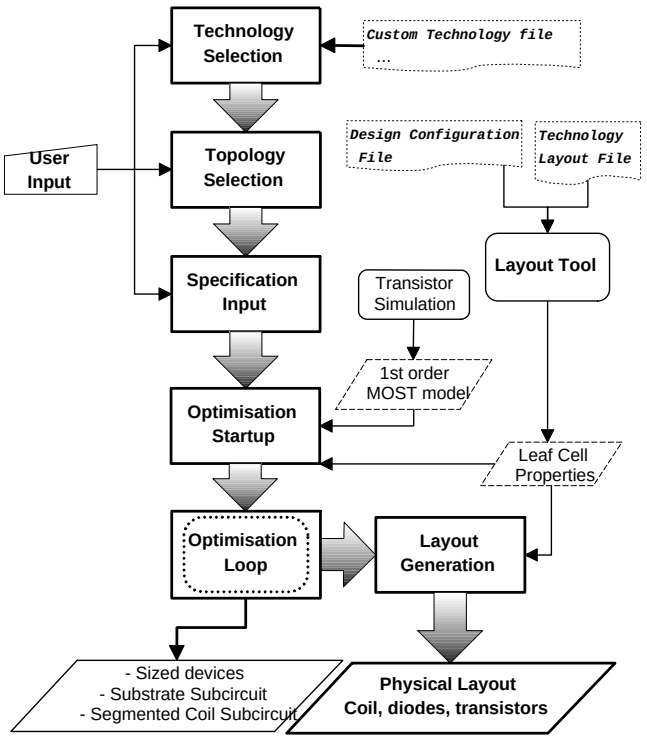

Figure 2 Flowchart of the CYCLONE tool

4. Optimal sizing of the complete VCO circuit

In figure 3 the interaction between the different calculation steps in the optimisation loop is schematically presented. A double arrow is used to represent an interface with an external program.

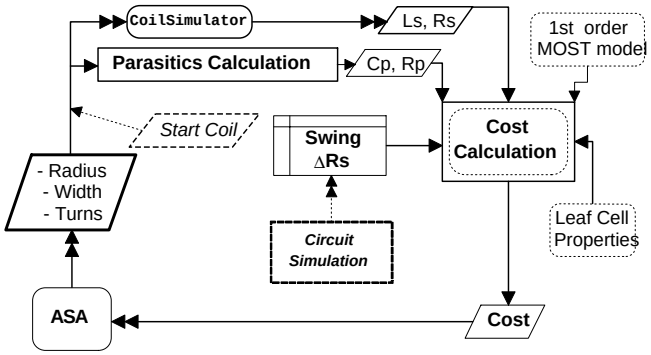

Figure 3 Interaction in the optimisation loop

The optimisation loop is initialised using a random or user-defined *Start Coil*, characterised by its independent topological parameters *Radius*, *(number of) Turns* and *(metal) Width*. These parameters are converted into the electrical parameters *Ls, Rs, Cp* and *Rp* using two parallel processes. *Ls* and *Rs* are the coil inductance and its total series resistance; *Cp* is the combined capacitance of the coil and substrate and *Rp* the parallel resistance to ground. The two parallel processes consist of a *Coilsimulator* that calculates *Ls* and *Rs* and a *Parasitics Calculation* that calculates *Cp* and *Rp* analytically from the three-element coil model of figure 4. Herein, *Cox* is the physical coil-to-substrate capacitance, *Rsub* and *Csub* are the substrate resistance and the substrate parallel capacitance.

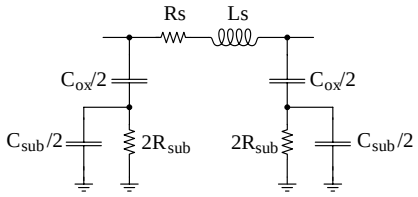

Figure 4 Lumped coil model

From the four electrical parameters, one *Cost* is calculated that serves as input of the optimiser (ASA [13]). The output of the optimiser is then a new set of independent topological parameters.

The *Cost Calculation* takes three elements into account in a weighted fashion: phase noise, power and tuning range. For all gain cell-related calculations, the first-order model is used.

- Phase noise and power depend directly on the value of R_{eff}. This effective tank resistance consists of two terms:

$$Reff = Rs + \Delta Rs \quad (1)$$

where

$$\Delta Rs = Rdiodes + Rgate \quad (2)$$

is the additional resistance in the LC-tank caused by the implemented diodes and the transistor gates of the gain cell. Since this resistance depends on the needed number of diode leaf cells and gain leaf cells, a 2-step iteration is used to get estimation on the value for ΔRs. The *Leaf Cell Properties* are needed in this iteration to calculate the diode and gate resistance.

- The power is given by:

$$P = V_{dd} . I_{bias} \propto G_M . V_{dd} \quad (3)$$

where G_M of the gain stage has to fulfil the Barkhausen oscillation criterion which, including a start-up *Safety*-margin, is given by :

$$G_M = Safety . \frac{R_{eff}}{(\omega_\circ Ls)^2} \quad (4)$$

The phase noise is then given by:

$$dV^2_{out}\{\Delta\omega\} = kT \cdot R_{eff} \cdot [1+F] \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \left(\frac{1}{swing^2/2}\right) \quad (5)$$

where $dV^2_{out}\{\Delta\omega\}$ is the single-sideband spectral noise density at an offset $\Delta\omega$ from the oscillation frequency ω_0, F is the excess noise of the oscillator's amplifier, *swing* is the differential oscillation amplitude and R_{eff} is given by (1). The s*wing* can be an estimated value provided by the user, or resulting from a transient simulation of the circuit. Likewise, the value of ΔRs can be extracted from ac circuit simulation instead of analytically calculated. If required by the user, these simulations are done before each cost calculation.

- The last element of the cost function, the tuning range, is given by (6), where C_{diode} is the diode (varactor) capacitance:

$$Tuning \propto \sqrt{C_{diode} . (\omega^2 . Ls / 2)} \quad (6)$$

5. Layout Generation of the complete VCO

In analogue layout systems the following procedure has been adopted: module generation, module placement and routing. Procedural module generators are widely accepted in industrial environments. These module generators are implemented in a technology independent way. Academic analogue place and route tools [14] have also been proposed.

From the schematics (shown in figure 1) it could be assumed that a VCO circuit contains standard CMOS devices, except for the integrated inductors. In reality, only the current source is implemented as a standard device. The other devices are grouped in RF-optimised layout structures (balanced diode pair, balanced MOST pair,…). For the designed VCOs this results in 4 out of 5 layout structures being optimised for RF.

5.1 Module generator technology

The three module generators required for the layout automation have been implemented in our in-house layout framework [14]. The coil device generator accepts as input the following parameters: the coil radius, the wire width and the number of turns. It supports an unlimited number of metal layers, and reads the *Technology Layout File*, thus ensuring technology independence.

Whereas the coil is a concentric device, the varactor and MOS cross-coupled pair are block repetitive. Therefore, a new type of device generator has been implemented: a template-based procedural generator based on block stretching. Three components have been joined to create this new type of device generator:

1. The stretch box and stretch command. As shown in figure 5, the stretch box *selects* the polygons (and stretch boxes) to be modified in the layout whereas the stretch command *moves*, *cuts* or *copies* the set selected by the stretch box. If the stretch box has a height equal to the manufacturing grid of the technology, this combined operation is equivalent to stretching of the geometry.

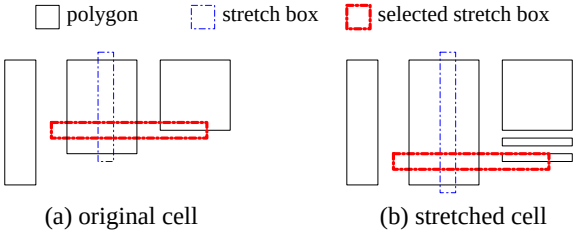

Figure 5 Example of a stretch operation on a cell.

2. Symbolic layers. These are needed to ensure technology independence. A symbolic layer is for instance a contact area between polysilicon and metal1. A box drawn on the symbolic layer is replaced by a structure containing polysilicon, metal1 and the maximal allowed number of contacts, as derived from the *Technology Layout File*.
3. Device Templates. Based on a template and arithmetic expressions, the stretch commands are executed by the layout generation program, resulting in a completed layout of the device.

5.2 Module Placement & Routing

Based on a floorplan the placement and routing of the VCO circuit can be done with the LAYLA tool [14]. The relative placement of the floorplan is enforced during placement by extra constraints. An example of a layout that has been generated is given in figure 6, clearly showing the different devices generated by the tool. It takes only 5 minutes of CPU time to generate this layout on a HP9000/785 workstation.

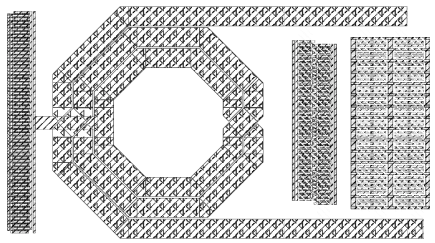

Figure 6 Automatically generated layout of the VCO core

6. Design Example – Experimental results

As an example, a comparison is made between two different technologies. In the top of table 2 the main technology features are compared. In both technologies, a VCO with the design specifications of table 1 was generated using CYCLONE. The leads were assumed to be 20 μm, and the used topology was the one given in figure 1(a), using an nMOST-only gain cell.

	Technology	
Parameter	Low resistive sub CMOS 0.35μm	High resistive sub BiCMOS 0.65μm
Substrate resist.	0.015 Ω.cm	7.98 Ω.cm
Available/used metal layers	5 / 3 top layers	3 / 3
Ls	1.26 nH	2.3 nH
Rs	6.5 Ω	5.2 Ω
Rad, W, Turns	109 μm, 40 μm, 2	141 μm, 5 μm, 2
Power	32 mW	8.2 mW

Table 2 Comparison of high vs. low resistive substrate

Technology		CMOS 0.35μm, low resistive substrate	
Vdd	1.8 V	**Ibias (core)**	11 mA
Vdiode	**Oscillation Frequency**		**Error**
[V]	Simulation (Hspice)	Measurements	[%]
1.8	3.192 GHz	3.330 GHz	4.1
1.6	3.143 GHz	3.276 GHz	4.1
1.2	2.990 GHz	3.127 GHz	4.4
0.8	2.841 GHz	2.905 GHz	2.2

Table 3 Comparison between measurements and simulation

After 700 iterations, the results shown in table 2 were obtained. As could be expected, the VCO in the technology with a high resistive substrate consumes less power than the VCO with identical specifications in the low resistive substrate technology. From this, one can conclude that a high resistive substrate is certainly favourable for analogue RF design.

To show the reliability of the used models in the tool, a comparison between measurements and circuit simulation is shown in table 3. The error between simulation and measurement is smaller than 5%, making the tool very useable for first-time right optimal design of RF VCOs.

7. Conclusions

In this paper a specification driven, layout-aware design tool for RF LC-oscillators, called CYCLONE, was presented. Two commonly used VCO topologies were implemented. The layout generating capabilities of the tool were demonstrated in an example. Finally, the design experiments show the usability of the tool for a wide range of technologies and the reliability of the implemented models and subcircuits.

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