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Damage free integration of ultralow-k dielectrics by template replacement approach

L. Zhang,[1,2] J.-F. de Marneffe,[1] N. Heylen,[1] G. Murdoch,[1] Z. Tokei,[1] J. Boemmels,[1] S. De Gendt,[1,2] and M. R. Baklanov[1]
[1]*IMEC, Kapeldreef 75, 3001 Heverlee, Belgium*
[2]*Department of Chemistry, Katholieke Universiteit Leuven, 3000 Leuven, Belgium*

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Cu/low-k integration by conventional damascene approach is becoming increasingly difficult as critical dimensions scale down. An alternative integration scheme is studied based on the replacement of a sacrificial template by ultralow-k dielectric. A metal structure is first formed by patterning a template material. After template removal, a k = 2.31 spin-on type of porous low-k dielectric is deposited onto the patterned metal lines. The chemical and electrical properties of spin-on dielectrics are studied on blanket wafers, indicating that during hard bake, most porogen is removed within few minutes, but 120 min are required to achieve the lowest k-value. The effective dielectric constant of the gap-fill low-k is investigated on a 45 nm ½ pitch Meander-Fork structure, leading to k_{eff} below 2.4. The proposed approach solves the two major challenges in conventional Cu/low-k damascene integration approach: low-k plasma damage and metal penetration during barrier deposition on porous materials. © *2015 AIP Publishing LLC*.
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The need for continuous increase in device performance drives dimensional scaling, materials changes, and the search for new integration sequences. With critical dimensions continuously decreasing, the interconnect delay becomes an increasing limitation of the overall signal propagation delay. In order to reduce this resistance-capacitance (RC) signal delay in multilevel interconnect structures, Copper with lower resistivity and low-k materials with dielectric constants lower than 4.2 was introduced to replace the traditional Aluminum/SiO_2 interconnects. Unlike Al, Cu etch with VLSI-compatible dry etch process is impossible, as copper does not form volatile products at process temperatures accepted by etch tool manufacturers. Therefore, the dielectric layer must be deposited and patterned first before the metallization, i.e., damascene technology.[1]

Porous organosilicate glass (p-OSG) materials with low dielectric constant have been introduced as inter-metal dielectrics.[2] In the past few years, continuous k value reduction was enabled by increasing the open porosity and pore size. However, a larger porosity degrades the most important material properties, such as the mechanical properties (stiffness and hardness) and dielectric reliability. A key challenge of p-OSGs is their weak compatibility to conventional interconnect processing, especially to plasma etching[3] and barrier deposition.[4] Plasma induced damage (PID) is mainly due to the penetration of etch radicals, photons, and residues into the interconnected pores, which results in the modification of the low-k's structure and composition deep into the bulk. The loss of organic groups turns the pores' sidewalls hydrophilic and subsequent moisture adsorption degrades the dielectric properties and reliability.[5] Likewise, the penetration of metal-based species during the physical- or chemical-vapor deposition of the metal diffusion barrier causes issues of barrier continuity, leakage, and effective dielectric constant. The increasing pore size also requires thicker barriers, which have such high resistivity that when using Cu to form narrow lines target line resistance cannot be achieved. As a result, damascene technology meets huge challenges in advanced technology nodes and k-value scaling for inter-metal dielectrics is far below expectations. According to recent editions of the ITRS, low-k materials with dielectric constants still as high as k = 2.5 were expected to be integrated in 2012.[6] Recently, the Post Porosity Plasma Protection (P4)[7,8] was proposed as a solution to enable low damage integration of advanced porous low-k. This approach modifies the interconnect processing flow by introducing at an early stage an extrinsic sacrificial filler which suppresses the porosity of the low-k film. This temporary pore filling allows protection during the plasma etching and subsequent metallization steps. However, our previous study showed non-negligible low-k degradation even with polymers filling the pores due to high diffusivity F radicals and vacuum ultraviolet photons.[9] Until now, the P4 approach requires further optimization, and other options for damage-free low-k patterning still need to be explored.

Given the increasing difficulty of integrating advanced porous low-k, it makes sense to reconsider the subtractive approach, where the metal structure is defined first, followed by dielectric deposition. In spite of many research efforts in developing new Cu etch chemistries and plasma conditions, there has been limited success in providing a satisfactory morphological profile.[10,11] The present work investigates an alternative integration approach which essentially relies on the replacement of a sacrificial template by spin-on ultralow-k dielectric after metallization, rendering Cu etch unnecessary. Fig. 1 shows a simplified single damascene Cu/low-k integration flow using this so-called "Template Replacement Approach." Trench/via is formed first by conventional Litho-Etch patterning of a sacrificial material. After metallization, including barrier deposition, Cu plating and CMP, the

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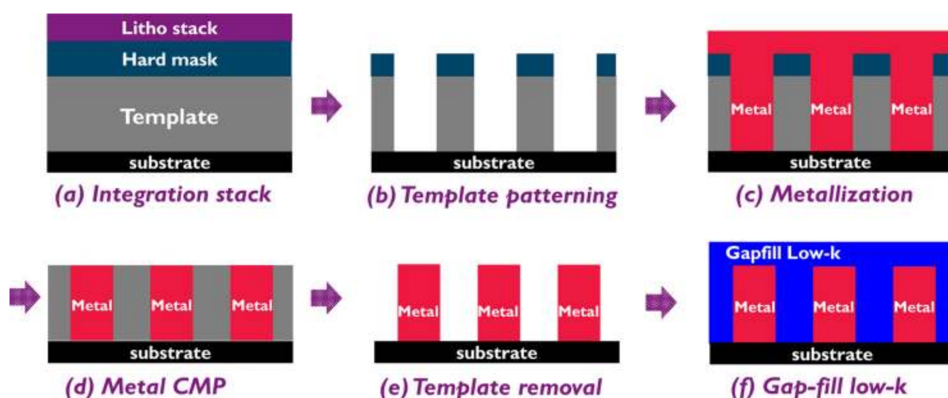

FIG. 1. Schematic shows single damascene Cu/low-k interconnect process flow with gap-fill low-k.

sacrificial template is removed. In this way, well-shaped Cu trench or via can be fabricated without reactive ion etching of Cu. Finally, a porous low-k dielectric is deposited by spin coating followed by hard bake, so as to encapsulate the metal gap structure. In this paper, the processing steps needed for forming a narrow (90 nm pitch) single damascene structure are presented and studied. The material properties of spin-on low-k are revealed by chemical and electrical analysis on blanket films. The effective dielectric constant of gap-fill low-k is studied based on capacitance measurement and 2-Dimension simulation.

The definition of the metal structure is realized by patterning a sacrificial template film instead of porous organosilicate. Template material selection is thus of crucial importance in order to get the specified feature dimensions and morphologies. It must be compatible with plasma patterning at small dimensions and high aspect ratio structures, sustain the thermal budget required by metallization steps, and resist the Cu CMP process. The template material used in the present work is a hydrogenated amorphous carbon (a-C:H) layer deposited at 400 °C by chemical-vapor deposition. It consists of both sp^2 and sp^3 bonded carbon atoms, with hydrogen terminations.[12] High thermal stability and mechanical strength offer good compatibility with hard mask deposition, barrier deposition, and CMP. With TiN as hard mask, excellent etch selectivity and line roughness were obtained by N_2/H_2 based CCP gas discharges. Compared with porous low-k etched with a conventional damascene process, the surface roughness after template etch (RMS $\sim$ 0.4 nm) is greatly improved. This is essential to get a continuous thin metal barrier. Fig. 2(a) shows high aspect ratio template lines at 90 nm pitch.

Using a conventional metallization process, including metal diffusion barrier physical-vapor deposition (3 nm TaN/Ta), Cu plating and Cu CMP, the metal structure is formed. Afterwards, the sacrificial layer must be stripped away completely without Cu damage. As per the sacrificial material, the template should be removed afterwards without extra damage to metallization structure. As counterexamples, Silica has an excellent compatibility with the metallization process, however, it cannot be removed by fluorine free treatments. With either wet or plasma processes, Fluorine introduces severe corrosion to the Cu and the Cu barrier. A He/H_2 based remote plasma was used to strip the a-C:H template in between Cu lines. Fig. 2(c) shows water contact angle (WCA) measured on blanket a-C:H films ashed by He/H_2 based remote plasma. WCA increases with longer ashing time, indicating a lowered surface energy. This is caused by carbon atoms on sp^2 sites reacting with hydrogen radicals, and forming less polarized sp^3 bonds. Further hydrogenation breaks the C-C bonds and leads to volatile CH_4 by-products. The use of a remote plasma is motivated by the absence of any energetic ions or reactive species (F, Cl, or O), and hence it causes no physical sputtering or chemical corrosion to the metal. It is also isotropic and therefore compatible with dual-damascene structures. 55 nm metal lines (Cu and barrier) at 90 nm pitch were obtained after Cu CMP. Top-down SEM measurement showed no CD change after template removal, confirming the absence of strong morphological damage to the metal. Finally, high aspect ratio Cu lines were formed with continuous thin TaN/Ta barrier coated on sidewall, as shown in Fig. 2(b).

Porous low-k dielectrics are normally prepared through co-deposition of precursors containing a silica-like matrix and an organic porogen, by either Chemical Vapor Deposition (CVD) or spin-coating.[2] Afterwards, the porogen

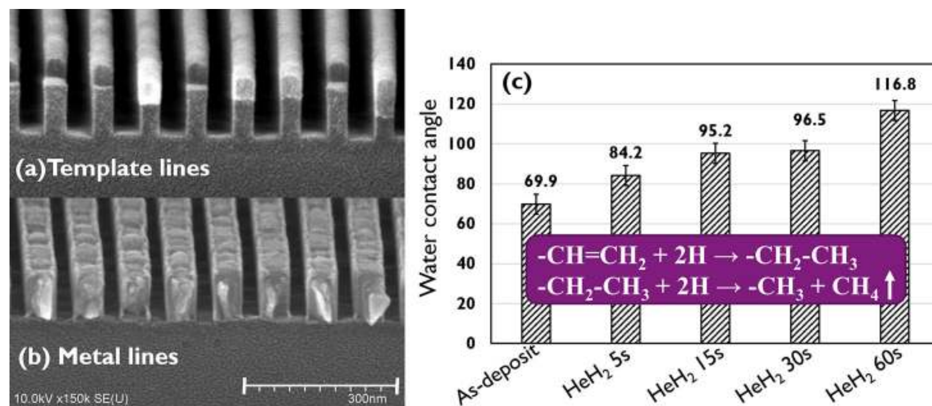

FIG. 2. (a) SEM cross section for patterned template trenches, TiN hardmask in still in place. (b) SEM cross section for patterned metal lines after template removal. (c) Water contact angle of a-C:H thin films ashed by He/H_2 remote plasma. At 250 °C, ashing rate on blanket surface is 0.81 nm/s.

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is baked out to form a highly interconnected mesoporous structure, and hence a low dielectric constant is achieved. In this work, a Liquid Phase Self-Assembly (LPSA) low-k dielectric was tested as candidate for gapfilling low-k. The main advantage of LPSA over PECVD low-k dielectrics is the ability to separately engineer pore size and open porosity using a variety of templates.[13] Study of material properties was first performed on a flat wafer with bare Si as substrate. After soft bake, FTIR shows a large amount of porogen peaks in the range of 3000–2800 cm^{-1} and 1200–1100 cm^{-1}. A high level of moisture is also observed in the range 3500–3200 cm^{-1}, which is due to polar silanol groups from the precursor. The open porosity is almost 0, and the measured k value is as high as 6.9. A 400 °C hard bake burns out the porogen and increases the open porosity. Simultaneously, thermally induced self-hydrophobization contributes to less moisture uptake. Both factors lead to a sharp decrease of the effective dielectric constant after a short time thermal cure. After 30 min of hard bake, the blanket k-value extracted with the MIS structure is already below 2.5. Longer time thermal bake removes further porogen residue and lowest k value of 2.31 is achieved after 120 min hard bake.

The LPSA precursor was applied to patterned wafers for low-k gap filling, with 400 °C hard bake as porogen removal. The addition of surfactant in the solution enables a good wettability along the gap surface (Cu or TaN). The cross-section SEM in Fig. 4(b) shows that the trench is filled with low-k without void formation. Dielectric properties are highly related to the efficiency of the template removal process.[14] However, those analysis techniques on blanket wafers do not have a lateral resolution for a 90 nm pitch structure. In the present work, we make use of electrical characterization method on patterned wafers, in order to qualify the effective k-value after integration. The capacitance of a Meander-Fork (Meander length of 2 cm) structure was measured at 100 kHz with a Hewlett-Packard semiconductor parameter analyzer HP4156 system. Fig. 4(c) shows the evolution of the normalized capacitance during the gapfill low-k process. After a-C:H stripping, the metal lines show a very low capacitance. After spin-coating of the low-k solution and soft bake, the capacitance increases sharply, corresponding to the presence of a dense composite of both the matrix and porogen precursor. The hard bake at 400 °C was applied to burn out porogen from gap-fill low-k precursor. As shown in Fig. 4(c), after a short bake time of a few minutes, the capacitance value is significantly lowered, indicating the decomposition of most of the porogen. With a longer anneal of up to one hour, there is a further slight decrease in capacitance, indicating further removal of porogen residues. It is notable that, comparing Figs. 3(b) and 4(c), the effective dielectric constants extracted from both gap-fill patterned wafers and from blanket wafers show similar values. By annealing, the efficiency of porogen removal in narrow lines is the same as on blanket wafers. Although needed to achieve a lower effective dielectric constant, the long thermal cure is questionable. In current work, degraded yield on meander line resistance (open resistance) was observed. The failure mechanism by mean of Cu migration was reported, which due to Rayleigh instability[15] and Cu oxidation.[16] The loss of Cu by out-diffusion induces extensive voiding and subsequent failure in Cu meander lines. Therefore, it is necessary to make passivation[17] on metallization structure before replacement low-k. An alternative solution is to explore low temperature porogen removal approaches, e.g., H_2 remote plasma or UV irradiation.[18]

Using a Meander-Fork vehicle, the effective k value can be extracted by 2-D simulation.[19] The calculation is carried out by static field solver in order to determine the dependence of the line-to-line capacitance on the k-value of the investigated low-k material. The 2-D model is defined on the basis of scanning electron microscopy (SEM) cross sections and realistic assumptions made on the dielectric constants of the other layers in the damascene stack. Fig. 4(c) shows the resulting integrated k value at 90 nm pitch. Cu lines without low-k, i.e., with air gaps, show a k_{int} very close to 1, indicating the reliability of the method. Gap-fill low-k precursor after soft bake shows a very high k value, above 5, as it is still a dense composite material containing matrix and porogen. After a 400 °C hard bake, most of porogen is decomposed within 30 min and an effective k value equal to 2.48 is obtained.

In summary, an alternative Cu/low-k integration approach is proposed, based on the patterning of a sacrificial template, then metal filling and CMP, then subsequent replacement by a gap-fill low-k dielectric. The proposed method eliminates plasma-induced low-k damage, as well as barrier penetration issues. A spin-on type LPSA organosilicate low-k dielectric is used to fill the trenches formed between the metal lines. A fast removal of porogen by thermal bake at 400 °C is observed for both situations in narrow patterned gap and blanket surface. However, a longer cure time is still required to completely remove porogen residue. Integrated dielectric properties can be evaluated by means of effective k value simulation on a Meander-Fork integration

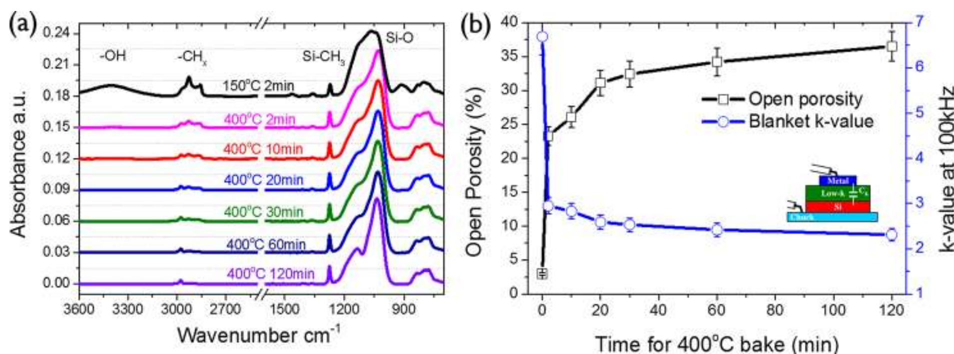

FIG. 3. Characterization of spin-on low-k films on flat Si wafer. (a) FTIR spectra showing chemical composition changes after soft bake and hard bake. (b) Open porosity measured by Ellipsometry Porosimetry[20] and k value measured with MIS structure.[21]

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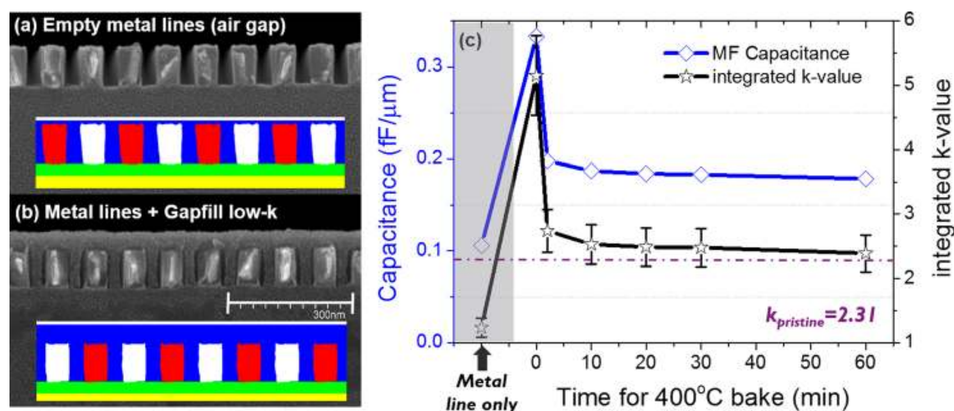

FIG. 4. (a) SEM cross section and 2-D simulation model for empty metal trench after template removal. (b) SEM cross section and 2D simulation model for metal trench with gap-filled porous low-k, thermal cure time is 60 min. (c) Evolution of capacitance and simulated effective dielectric constant during low-k gap filling and hard bake. Capacitance is measured on Fork-Meander-Fork integration structure with 90 nm pitch. Spin-coated low-k precursors receive a soft bake at 150 °C for 2 min to evaporate solvent. Porogen is then burnt out by hard bake in N_2 at 400 °C for 2–60 min.

vehicle. By annealing for 60 min, an effective k-value 2.39 is obtained on a 35 nm gap structure, which corresponds to integrated $\Delta k < 0.1$ compared with fully cured pristine material on blanket wafer.

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