

## Dataflow modeling of real-time memory controllers

***Citation for published version (APA):***

Li, Y., Moreira, O., Akesson, K. B., & Goossens, K. G. W. (2015). *Dataflow modeling of real-time memory controllers*. Poster session presented at ICT.OPEN 2015, Amersfoort, Netherlands.

***Document status and date:***

Published: 01/01/2015

***Document Version:***

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

***Please check the document version of this publication:***

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

***General rights***

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

[www.tue.nl/taverne](http://www.tue.nl/taverne)

***Take down policy***

If you believe that this document breaches copyright please contact us at:

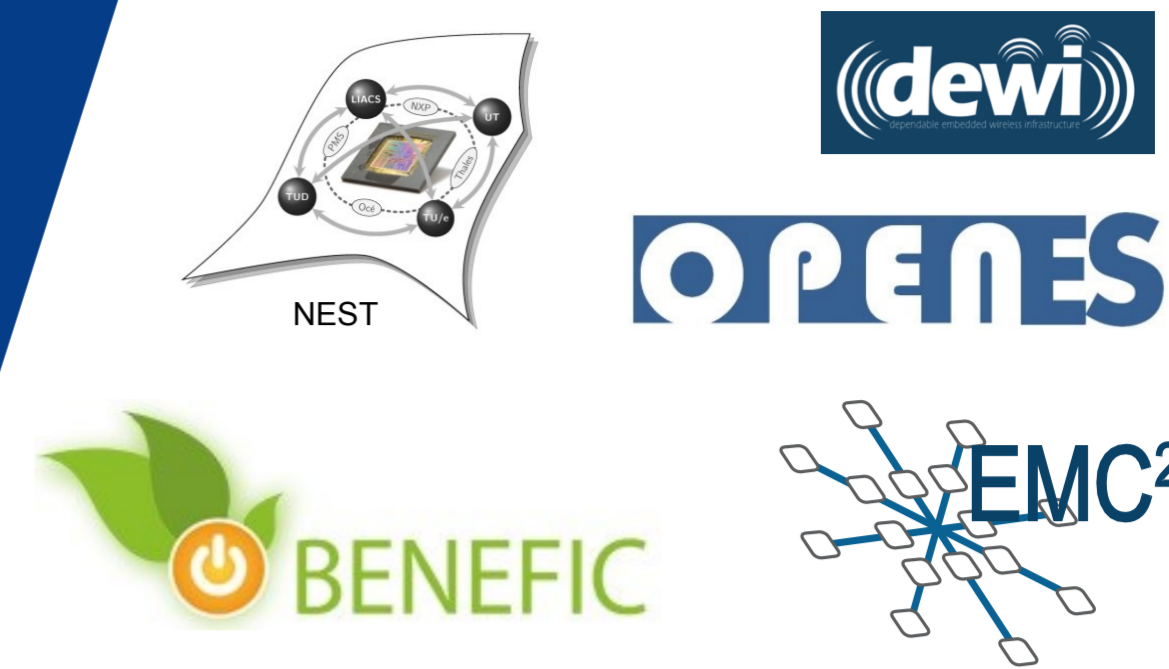
[openaccess@tue.nl](mailto:openaccess@tue.nl)

providing details and we will investigate your claim.



# Dataflow Modeling of Real-Time Memory Controllers

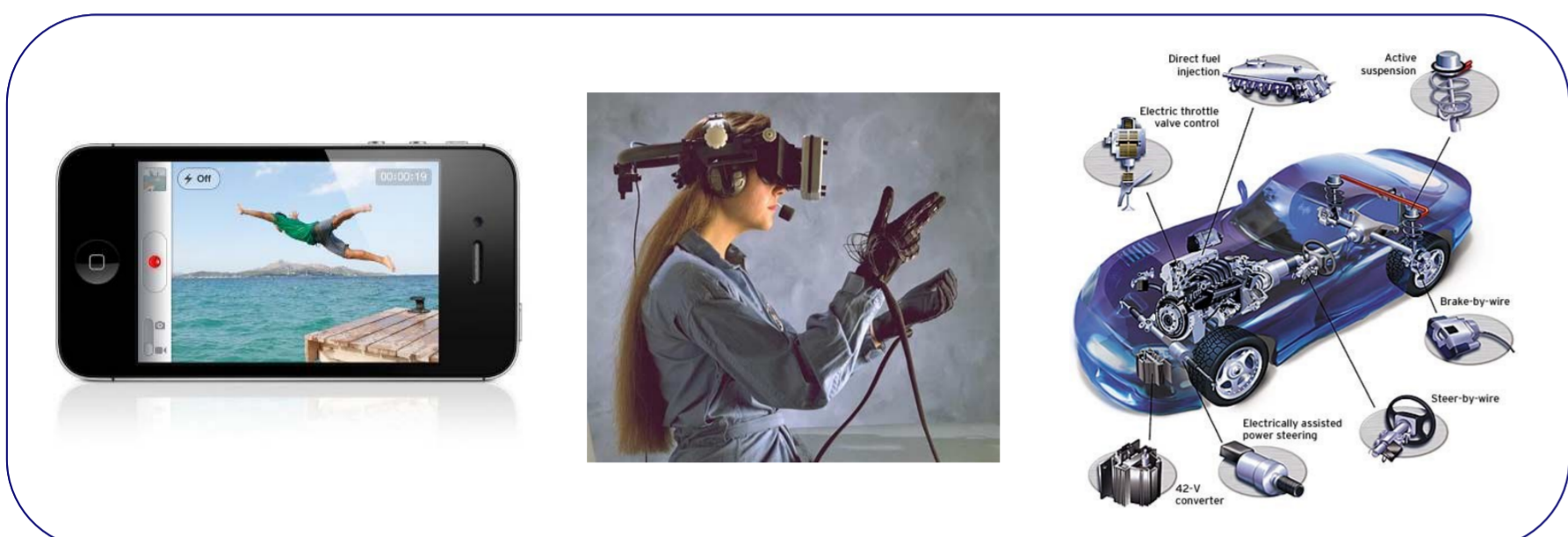
Yonghui Li, Orlando Moreira, Benny Akesson, and Kees Goossens



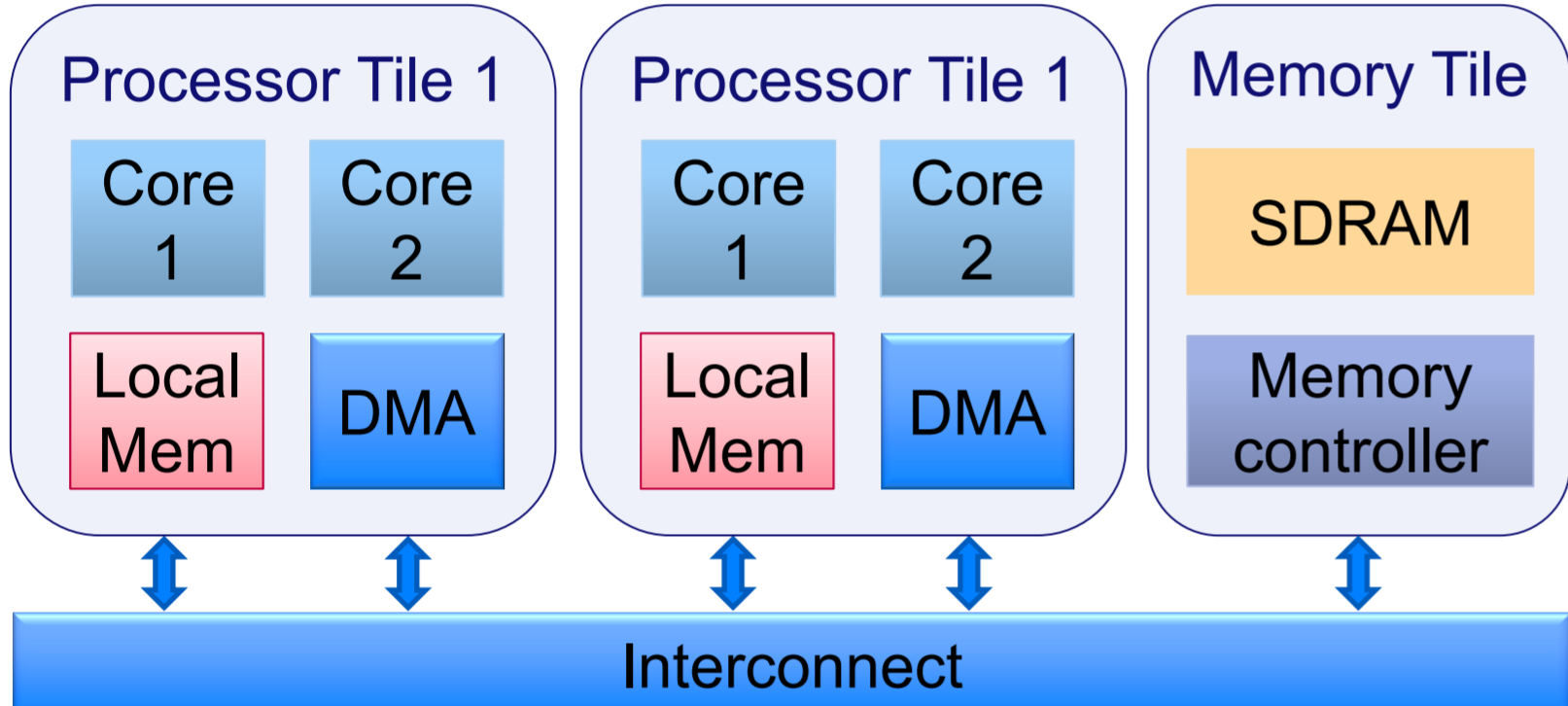
## 1. Real-Time Applications & Multicore Systems

Various applications on modern multicore systems

- Some of them have real-time requirements, which are caused by the interaction with physical world
- Others are non-real-time, but must be responsive



Real-Time Applications    Non-Real-Time Applications



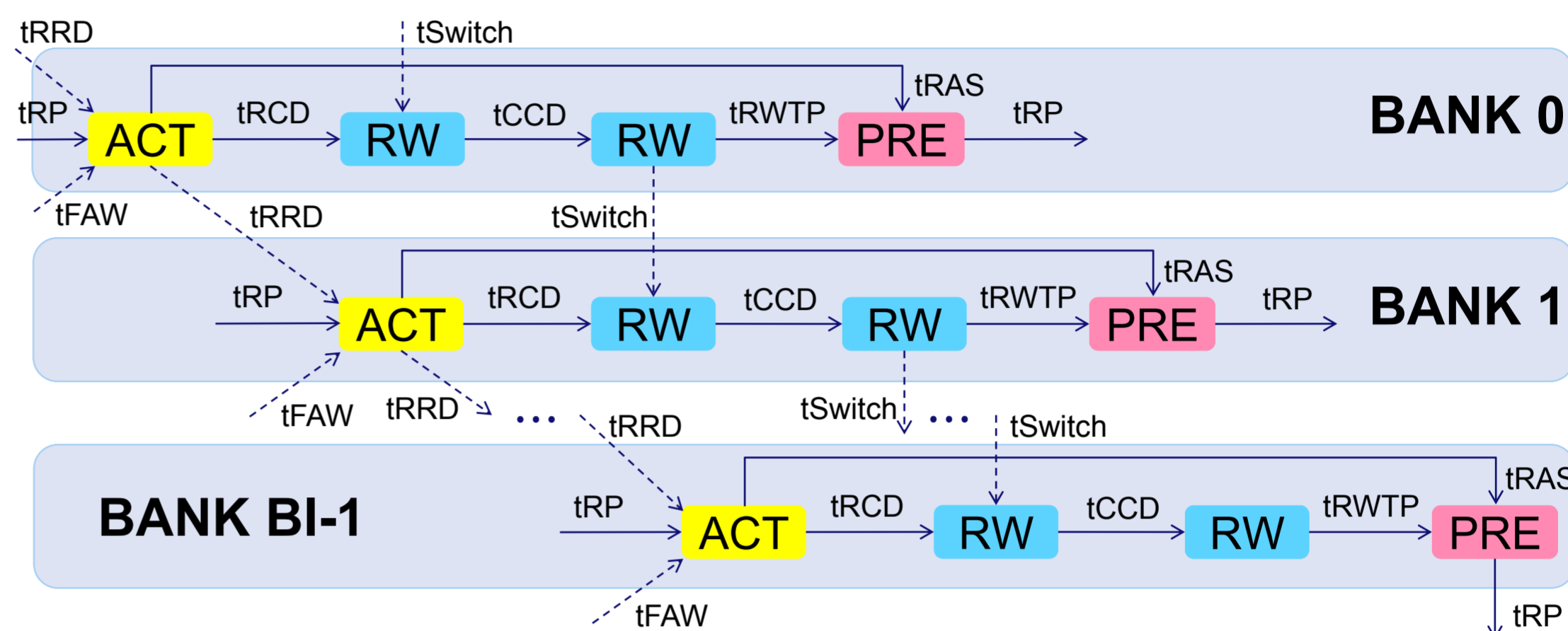
Multicore real-time system

- Has to guarantee the performance for real-time applications, even though resources are shared.
- The SDRAM is one of the most commonly shared resource, and the WCET of memory transactions is critical for designing a real-time system.

## 4. Command Scheduling Dependencies

Scheduling dependencies are caused by

- JEDEC timing constraints (constants) between commands
- Scheduling algorithm.

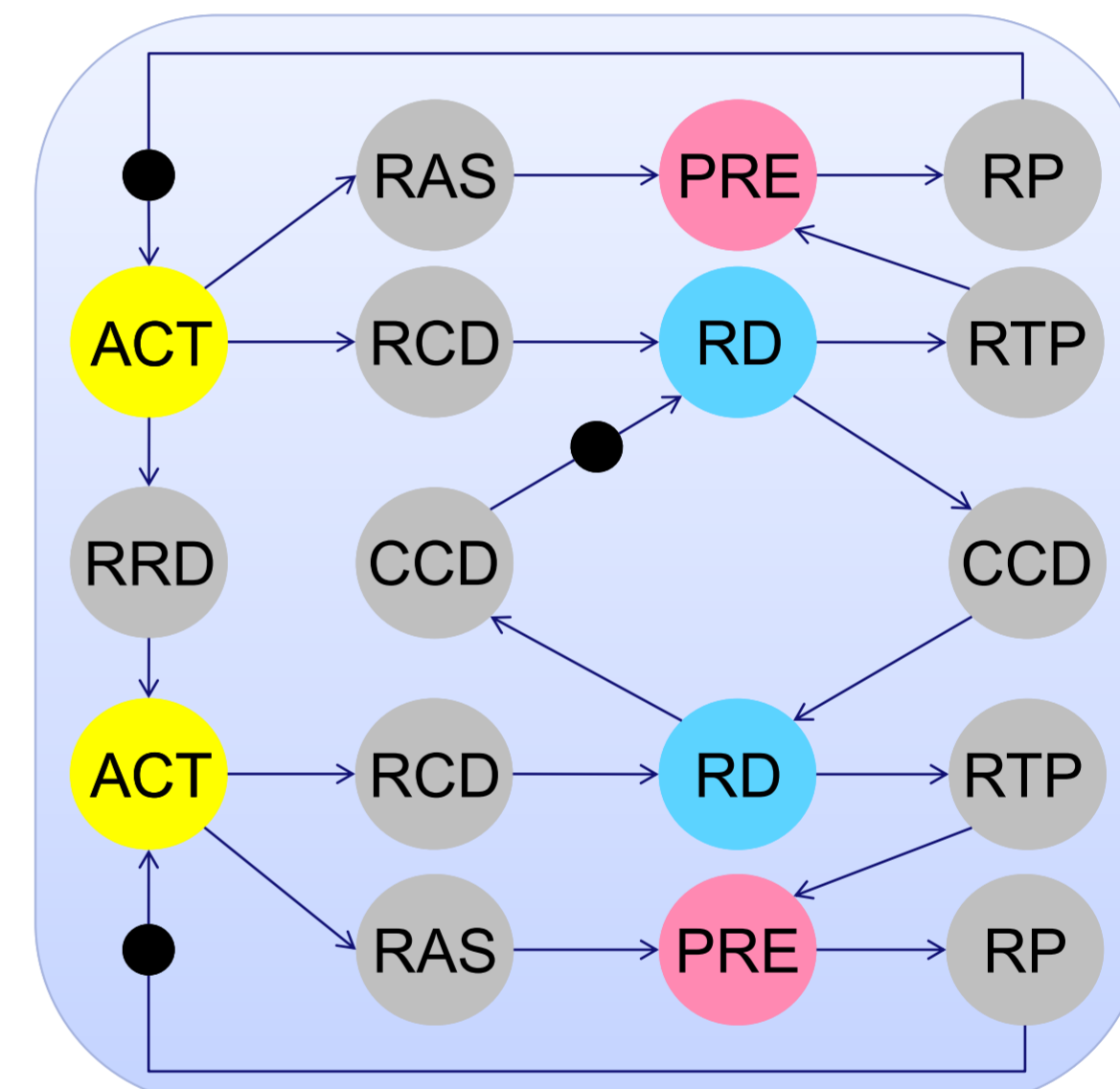


## 5. Dataflow Modeling of Scheduling Dependencies

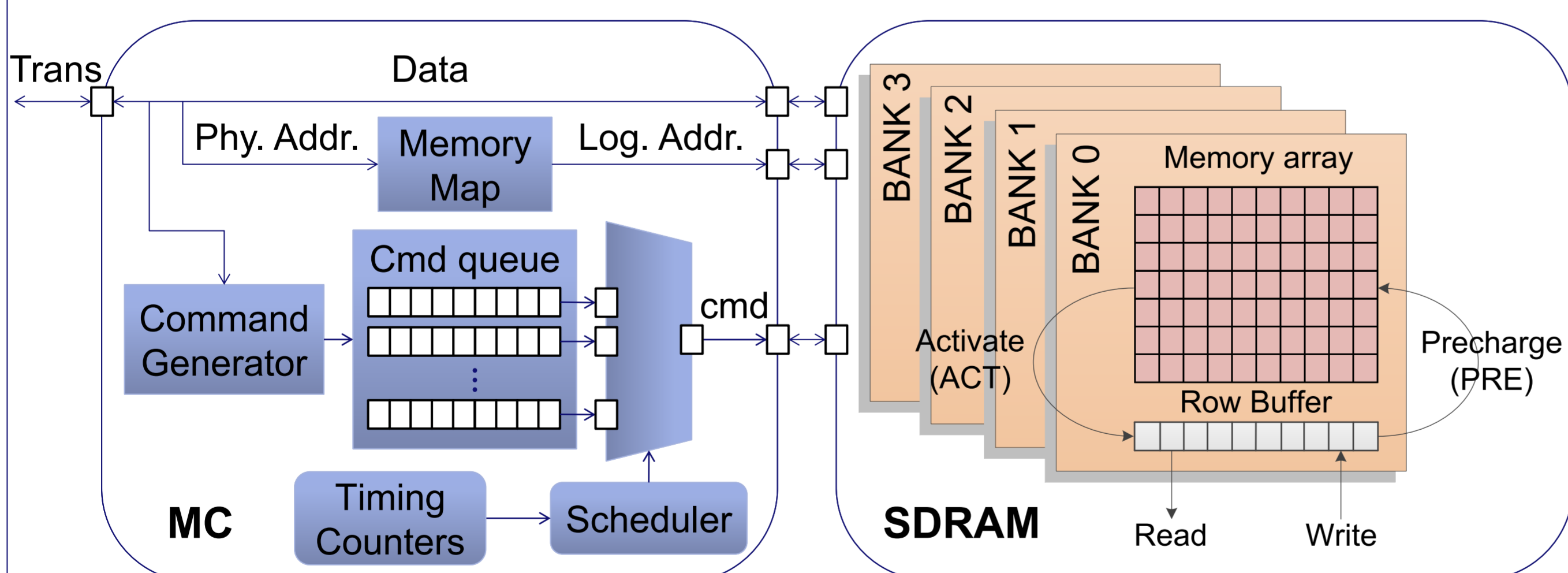
Memory command Scheduling is described by dataflow model

- Commands are captured by actors
- Timing constraints are molded by delay actors
- Scheduling dependencies are depicted by the edges between actors

Single rate dataflow Graph for a Read Transaction

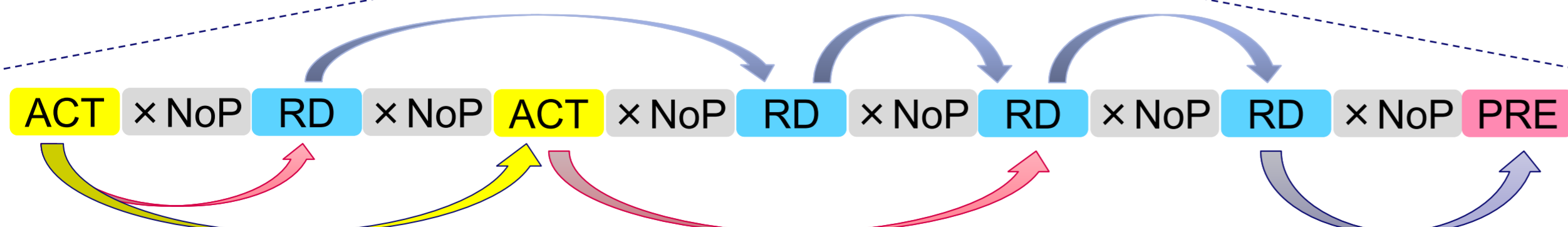


## 2. SDRAM & Memory Controller (MC)



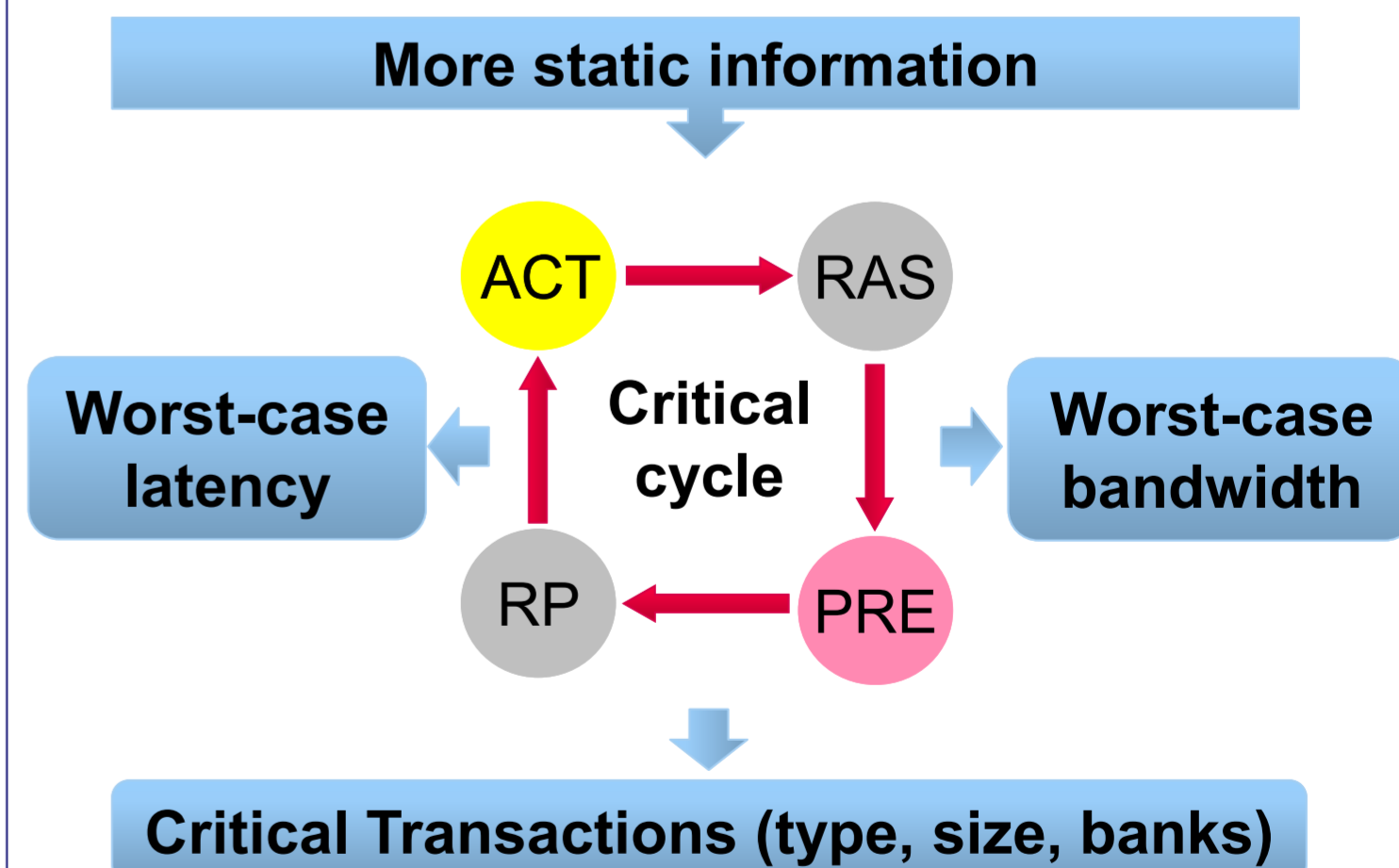
## 3. From Transaction to Commands

E.g., a read transaction



A transaction is translated into a sequence of commands that are scheduled subject to the SDRAM timing constraints, which cause the dependencies between commands.

## 6. Worst-case analysis



## 7. Contact



Name: Yonghui Li  
Email: yonghui.li@tue.nl



## Reference

[1] Yonghui Li, Benny Akesson, and Kees Goossens. *Dynamic Command Scheduling for Real-Time Memory Controllers*. In Proc. ECRTS 2014.